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TUA 6041-2

Low Power 3-Band Digital TV / Portable Tuner IC with Digital Alignment

LIGHTNING

Communication Solutions

Never stop thinking

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Low Power 3-Band Digital TV / Portable Tuner IC with Digital Alignment

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TUA 6041-2 'LIGHTNING'

Revision History:	**2006-12-19**	**Data Sheet, Revision 3.1**
Previous Version:	2006-09-12	Preliminary Specification, Revision 3.0

Page	Subjects (major changes since last revision)
9 - 11, 28, 30 - 41	L-Band application added. Operating range and AC/DC Characteristics extended for L-Band.
31 - 41	Table Footnote added with description for impedance measurement.

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horst.klein@infineon.com

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1 Product Info

General Description

The **TUA 6041-2** integrates the mixer-oscillator, AGC amplifier, digitally programmable phase lock loop (PLL) and a digital alignment feature so that traditional air coils can be replaced by SMD coils. This makes the **TUA 6041-2** an ideal product for applications where size and low power consumption are required design key factors. Typical applications include TV's, VCR's, Set Top Boxes (STB) and also a range of portable products.

Features

General

- Suitable for PAL, NTSC, SECAM, DVB, DMB, DAB, ISDB-T and ATSC
- High band covers frequency range for L-Band up to 1.5 GHz
- Supply voltage range from 3 to 5.5 V
- Combined small - wide AGC detection
- AGC + AGC buffer output
- Low phase noise
- Full ESD protection
- Qualified according to JEDEC for consumer applications

Mixer/Oscillator

- Three band tuner
- Unbalanced highohmic LOW band input
- Balanced lowohmic MID band input
- Balanced lowohmic HIGH band input
- Two pin oscillators for LOW/MID band
- Four pin oscillator for HIGH band

IF-Amplifier

- 4 IF pins to connect a 2 pole bandpass
- Symmetrical SAW driver
- Fully balanced IF AGC amplifier

PLL

- I^2C / three wire combi bus
- 4 independent I^2C addresses
- High voltage VCO tuning output
- Two PMOS ports
- One voltage referred port
- Internal LOW/MID/HIGH band switch
- Xtal oscillator, range from 4 to 16 MHz
- Xtal buffer output with programmable level and output divider
- Clock generator for DC/DC converter with programmable high and low time

Digital alignment

- Three DACs for digital alignment, control range up to 5 volt

Power management

- Bus controlled stand by mode

Application

- The IC is suitable for PAL, NTSC, SECAM, DVB-C, DVB-T, DVB-H, DMB-T, DAB, ISDB-T, ATSC and L-Band tuners.

Ordering Information

Type	Ordering Code	Package
TUA 6041-2	SP000250163	PG-VQFN-48

2 Product Description

The **TUA 6041-2** integrates the mixer-oscillator, variable AGC output amplifier, digitally programmable phase lock loop (PLL) not requiring an external high voltage buffer and a digital alignment feature. Furthermore, the **TUA 6041-2** integrates a buffered RF AGC, programmable clock signals for an external DC-DC up converter along with open drain DAC outputs used for automatic digital alignment.

The integrated mixer oscillator function comprises of three balanced mixers. The first mixer has an unbalanced high impedance input while the other two have balance low impedance inputs. The tuner also has firstly, 2-pin asymmetric oscillators for both Low and Mid bands and secondly a 4-pin symmetrical oscillator for High band operations including a band selector switch.

The output signal from the mixer is amplified via a SAW filter driver followed by variable gain amplifier stage in order to achieve a constant output level used for A/D conversion. All functions can be programmed with up to four different IC addresses. Also, the PLL connected to a 4-16 MHz reference crystal which is buffered on-chip, allows the setting of the tuner oscillator with a minimum step size of 20 kHz. A Lock flag will be set once the PLL is locked and communicated via the I2C/3-Wire bus.

The complete control setting of the IC is done by a microprocessor via the I2C/3-Wire bus. The device also has three output ports of which P2 can be configured as a programmable output voltage port.

2.1 Features

2.1.1 General

- Supply voltage range 3 to 5.5 V.
- Suitable for PAL, NTSC, SECAM, DVB-T/H/C, DAB, ISDB-T, ATSC and L-Band.
- Wideband and Narrow AGC detectors for tuner RF AGC
  - 5 programmable take-over points
  - 2 programmable time constants.
- Low phase noise.
- Full ESD protection.

2.1.2 Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band.
- Low impedance mixer input (common base) for MID band.
- Low impedance mixer input (common base) for HIGH band.
- 2 pin oscillator for LOW band.
- 2 pin oscillator for MID band.
- 4 pin oscillator for HIGH band.
- Oscillator for HIGH band divided by 3 available for MID band mixer.

2.1.3 SAW Filter Driver

- Symmetrical IF preamplifier with low output impedance able to drive a compensated SAW filter (500 Ω//40 pF).

2.1.4 IF AGC Amplifier

- Symmetrical variable gain IF output amplifier with low noise, high linearity, high dynamic range.

2.1.5 PLL

- 4 independent I^2C addresses, or 3-Wire bus mode.
- I^2C bus protocol compatible with 3.3 V and 5V micro-controllers up to 400 kHz.
- High voltage VCO tuning output.
- 3 PNP ports, one of them realized as programmable voltage output.
- 1 clock output for external DC/DC upconversion to generate the tuning supply voltage, may be used as NPN port.
- Stand-by programmable for functional blocks allows customized ramping.
- Internal LOW/MID/HIGH band switch.
- Lock-in flag.
- 4 to 16 MHz crystal oscillator with programmable output buffer.
- programmable reference divider ratios.
- 4 charge pump currents, programmable in 15 steps.

2.1.6 DAC outputs

- Open drain outputs, load resistors to Vcc, 5V or tuning supply voltage.
- Overvoltage protection for operation from tuning supply voltage.

2.1.7 IF switch and Loop through for tuner alignment

- 2 programmable switches to bypass the bandpass/SAW filter to facilitate the tuner pre-stage alignment.

2.2 Application

- The IC is suitable for PAL, NTSC, SECAM, DVB-T/H/C, DAB, ISDB-T, ATSC and L-Band tuners.
- The integrated RF AGC control has wide band detectors at the mixer inputs and a narrowband detector at the saw filter driver output.

2.2.1 Recommended band limits in MHz

Table 1 ATSC tuners

	RF input		Oscillator	
Band	**min.**	**max.**	**min.**	**max.**
LOW	55.25	157.25	101	203
MID	163.25	451.25	201	479
HIGH	457.25	861.25	503	907

Table 2 DVB-T and analog tuners

	RF input		Oscillator	
Band	**min.**	**max.**	**min.**	**max.**
LOW	48.25	154.25	87.15	193.15
MID	161.25	439.25	200.15	478.15
HIGH	447.25	863.25	486.15	902.15

Table 3 ISDB-T tuners

	RF input		Oscillator	
Band	**min.**	**max.**	**min.**	**max.**
LOW	93	167	150	224
MID	173	467	230	524
HIGH	473	767	530	824

Note: Tuning margin of 3 MHz not included.

3 Functional Description

3.1 Pin Configuration

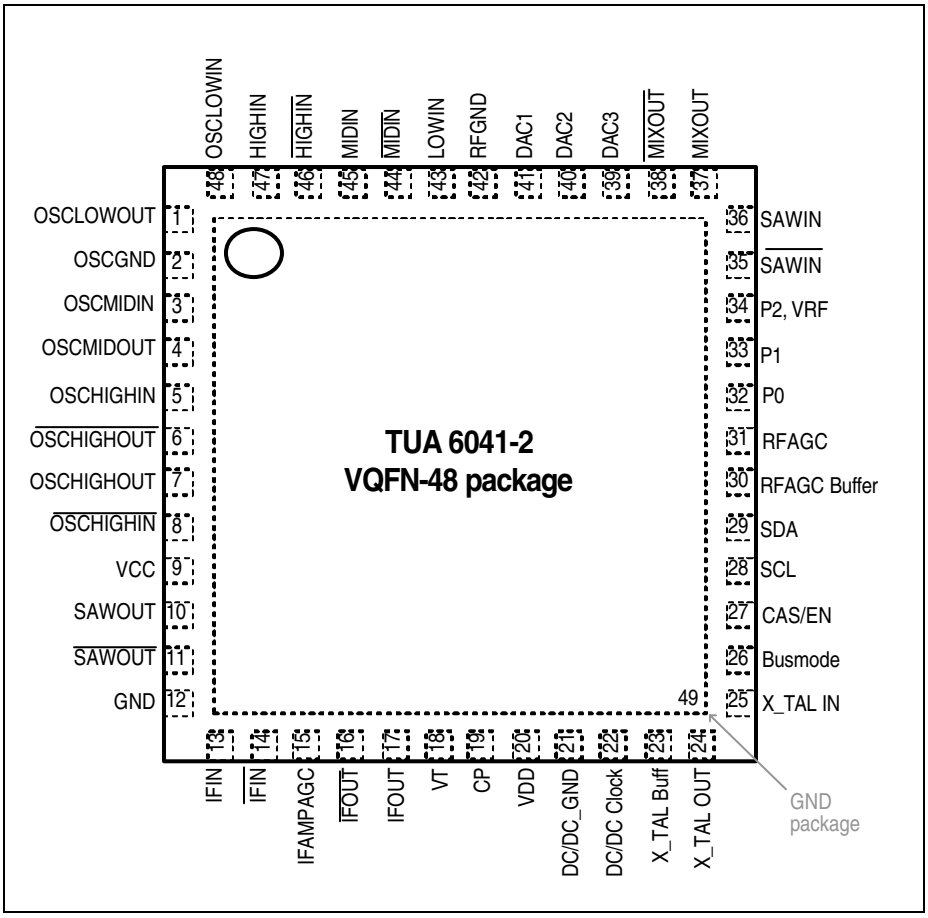
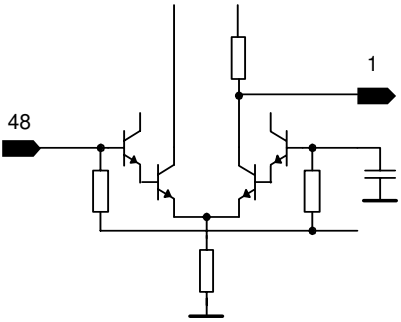
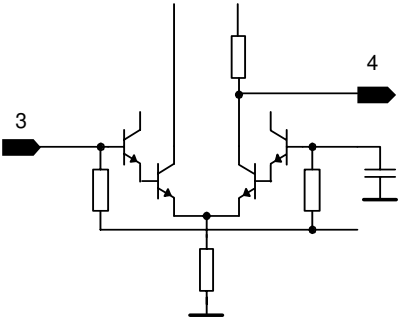
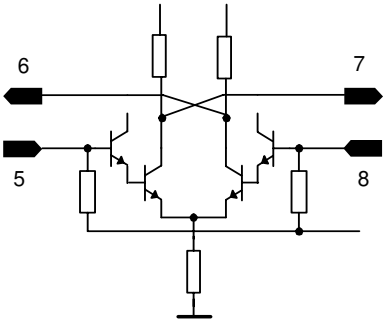
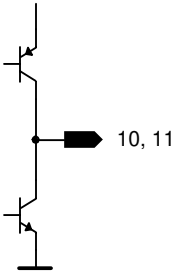
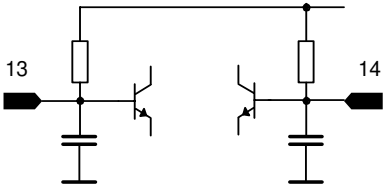


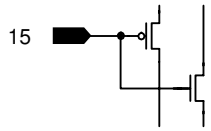
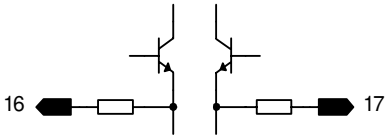
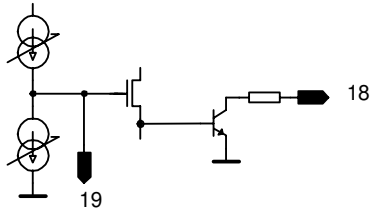
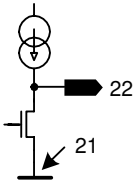
Figure 1 Pin Configuration TUA 6041-2 in VQFN-48 Package

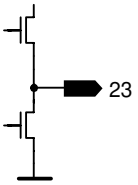
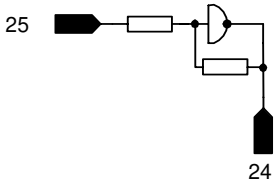
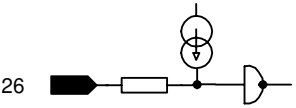
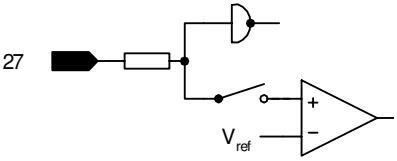
3.2 Pin Definition and Functions

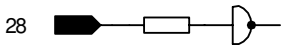
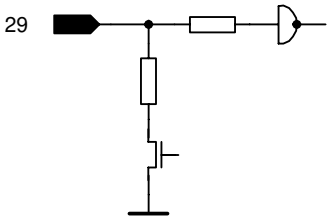
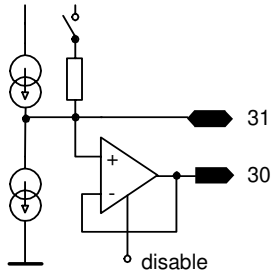
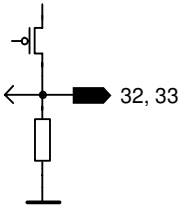
- Pin Definition and Functions

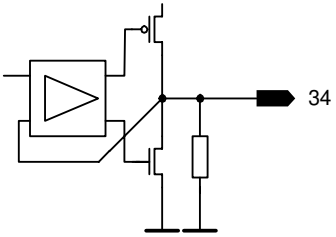
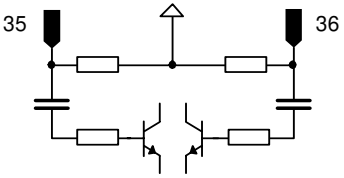
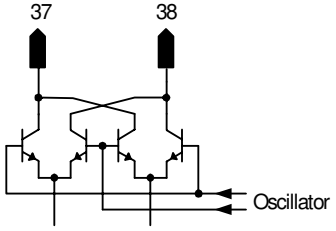
Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
48	OSCLOWIN		2.3 V		
1	OSCLOWOUT		1.8 V		
2	OSCGND	Oscillator ground	0.0 V	0.0 V	0.0 V
3	OSCMIDIN			2.3 V	
4	OSCMIDOUT			1.8 V	

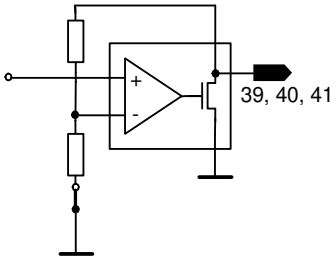
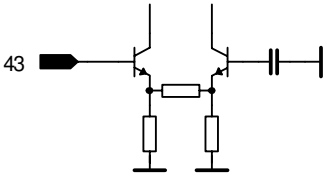
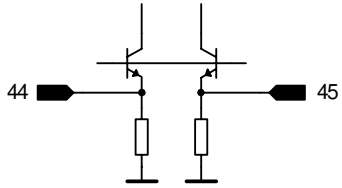
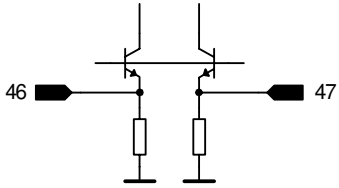
Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
5	OSCHIGHIN				2.3 V
6	OSCHIGOUT				2.25 V
7	OSCHIGOUT				2.25 V
8	OSCHIGHIN				2.3 V
9	VCC	Supply voltage	3.3 V	3.3 V	3.3 V
10	SAWOUT		1.65 V	1.65 V	1.65 V
11	SAWOUT		1.65 V	1.65 V	1.65 V
12	GND		0.0 V	0.0 V	0.0 V
13	IFIN		2.64 V	2.64 V	2.64 V
14	IFIN		2.64 V	2.64 V	2.64 V

Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
15	IFAMPAGC		n.a.	n.a.	n.a.
16	IFOUT		1.6 V	1.6 V	1.6 V
17	IFOUT		1.6 V	1.6 V	1.6 V
18	VT		VT	VT	VT
19	CP		1.7 V	1.7 V	1.7 V
20	VDD	Supply voltage	3.3 V	3.3 V	3.3 V
21	DC/DC_GND		0.0 V	0.0 V	0.0 V
22	DC/DC Clock		n.a.	n.a.	n.a.

Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
23	XTAL Buffer				
24	XTAL Out		0.9 V	0.9 V	0.9 V
25	XTAL In		0.9 V	0.9 V	0.9 V
26	Busmode		n.a.	n.a.	n.a.
27	CAS/EN		n.a.	n.a.	n.a.

Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
28	SCL		n.a.	n.a.	n.a.
29	SDA		n.a.	n.a.	n.a.
30	RFAGC Buffer		3.2 V	3.2 V	3.2 V
31	RFAGC		3.2 V	3.2 V	3.2 V
32	P0		0 V or V_{CC}-V_{CE}	0 V or V_{CC}-V_{CE}	0 V or V_{CC}-V_{CE}
33	P1		0 V or V_{CC}-V_{CE}	0 V or V_{CC}-V_{CE}	0 V or V_{CC}-V_{CE}

Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
34	P2, VRF		VRF	VRF	VRF
35	SAWIN		V_{CC}	V_{CC}	V_{CC}
36	SAWIN		V_{CC}	V_{CC}	V_{CC}
37	MIXOUT		V_{CC}	V_{CC}	V_{CC}
38	MIXOUT		V_{CC}	V_{CC}	V_{CC}

Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
39	DAC3		V_{DAC3}	V_{DAC3}	V_{DAC3}
40	DAC2		V_{DAC2}	V_{DAC2}	V_{DAC2}
41	DAC1		V_{DAC1}	V_{DAC1}	V_{DAC1}
42	RFGND	IF ground	0.0 V	0.0 V	0.0 V
43	LOWIN		2		
44	MIDIN			1	
45	MIDIN			1	
46	HIGHIN				1
47	HIGHIN				1
49	GND package	Exposed pad ground (Die pad)	0.0 V	0.0 V	0.0 V

3.3 Functional Block Diagram

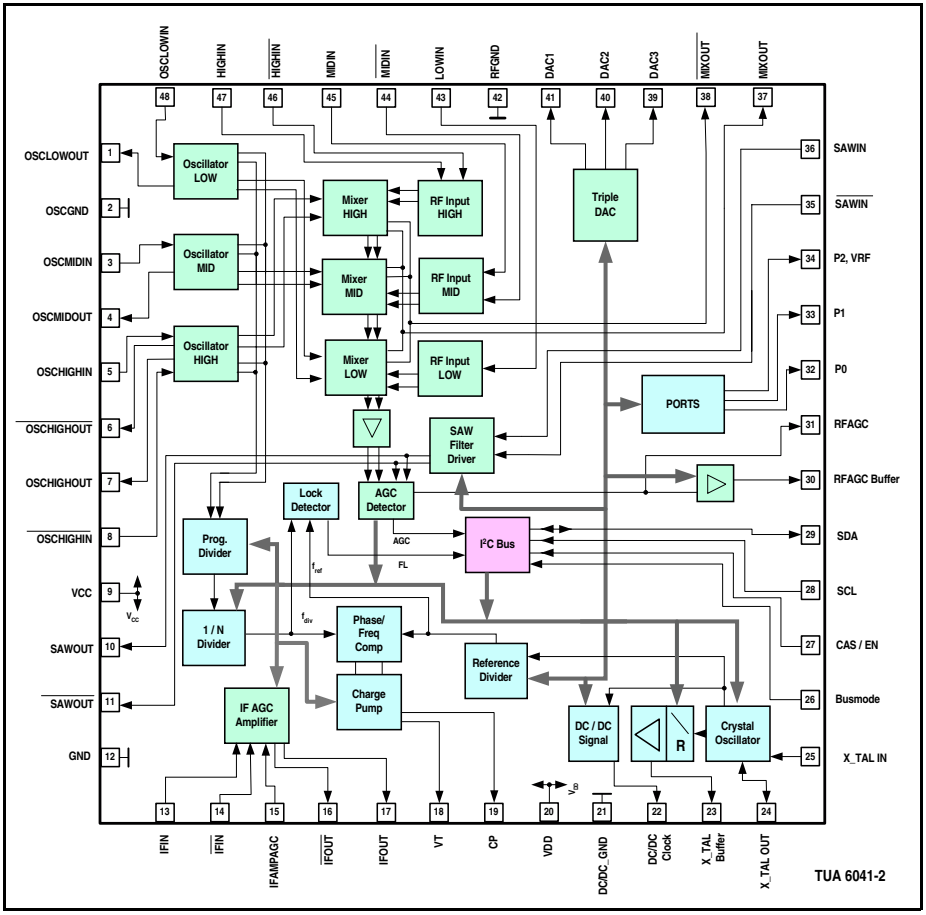


Figure 2 Functional Block Diagram TUA 6041-2 in VQFN-48 package

3.4 Circuit Description

3.4.1 Mixer-Oscillator-block, SAW filter driver

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, a reference voltage, and a band switch.

Filters between tuner input and IC separate the TV frequency signals into three bands. The band switching in the tuner front-end is done by using three PNP port outputs. In the selected band, the signal passes through a tuner input stage with a MOSFET amplifier, a double-tuned bandpass filter and is finally fed to the mixer input of the IC. The impedance of the mixer at LOW band has high ohmic, while MID or HIGH band has a low ohmic input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency.

The IF is filtered by means of an external SAW filter (Surface Acoustic Waves filter) in between the 2 mixer output pins and the 2 input pins of the following SAW filter driver. The SAW filter driver has a low output impedance to drive the SAW filter directly.

3.4.2 RF AGC

The RF AGC stage combines a wide band and a narrow band detection. The wide band detector (WB) detects the input signal directly at the RF input for each band. The narrow band detector (NB) detects the level of the SAW filter driver output signal. If both detected levels are below the RF AGC take-over points, a external capacity will be charged with the source current of 300 nA or 9 µA (release current). If one of the detected levels is above the RF AGC take-over points, the external capacity will be discharged with the sink current of 100 µA (attack current). The integrated current generates an AGC voltage for gain control of the tuners input transistors. The AGC take-over and the time constant are selectable by the I^2C bus as shown in **Table 17 "Subaddress 03H, AGC Control and IF Signal Processing Control" on Page 53**.

An integrated RF AGC buffer allows to monitor the AGC voltage without any influence on the tuner gain control. This buffer can be disabled as shown in **Table 16 "Subaddress 02H, Reference Divider R and Crystal Oscillator Control" on Page 51**

3.4.3 IF AGC amplifier

Coming out of the SAW filter the IF signal is sent through a VGA (Variable Gain Amplifier) which will set the differential IF output signal to the desired level (preferably 1 Vpp). The gain of the VGA is determined by the DC-voltage at pin IFAMPAGC

3.4.4 PLL block, XTAL oscillator

The VCO frequency f_{OSC} is stabilized by a digital CMOS PLL (Phase Locked Loop, Frequency Synthesizer). The oscillator signal is internally DC-coupled as a differential signal to the programmable divider input. The signal subsequently passes through a programmable divider (N) and then the divided VCO signal:

$$f_{div} = \frac{f_{OSC}}{N}, (N = 240 \ldots 65535)$$

is compared in a digital frequency/phase detector (PD, frequency detector) with a programmable reference frequency:

$$f_{ref} = \frac{f_{XTAL}}{R}, (R = 2 \ldots 1023)$$

which is derived from a quartz reference f_{XTAL} divided by a programmable reference divider (R).

The phase detector has a linear operating range without a dead zone for very small phase deviations. A programmable ABL pulse width (Anti BackLash) works against the delay of the charge pump cell. The selectable ABL pulse width values have been implemented for test purpose only and have no performance effects.

The phase detector has two outputs (up & down) that drive two current sources of opposite polarity as charge pump (CP). If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source (I_{source}) pulses for the duration of the phase difference. In the reverse case the negative current source (I_{sink}) pulses. If the two signals are in phase (PLL is locked), the integrated charge pump current is approximately zero. In case of active closed loop control the charge pump provides programmable output current drive capability to optimize the loop requirements. The charge pump currents are programmable from 0 to 1.125 mA in steps of 75 µA.

The PLL contains an integrated lock detector. A lock-in flag is set when the loop is locked. It can be read by the processor via the common I^2C/3-Wire bus.

The crystal oscillator (XTAL) is an unbalanced Pierce oscillator which operates in parallel resonance with quartz crystals from 4...16 MHz. By programming it's possible to pass the oscillator frequency f_{XTAL} through a divider stage to a buffered output pin or to use an external quartz clock for the reference oscillator via a switchable preamplifier for test purpose only.

3.4.5 Bus Interface

The programming of the CMOS frequency synthesizer is done via a combined serial I^2C/3-Wire bus interface. The choice of the desired bus is made by a bus mode select signal at pin BUSMODE.

In I^2C-bus mode four different chip addresses can be set by appropriate DC levels at pin CAS (Chip Address Select), while in 3-Wire mode the chip is addressed by a low active enable signal at pin EN.

The content of the bus telegram (serial data format) is controlled by software programming and assigned to the registers of the functional units according to the several sub addresses. The most significant bit (MSB) of the data protocol is shifted in first.

The clock is generated by the processor (input pin SCL/Clock), while pin SDA/Data functions as an input or an output (open drain, external pull-up resistor) depending on the direction of the data (write or read mode). Both inputs have schmitt-trigger circuits with hysteresis and furthermore a low-pass characteristic, which suppress a certain noise level on the bus lines and enhance so the noise immunity of the combi-bus.

A detailed description of the chip address organization in I^2C-mode as well as the used sub addresses of the data registers is given in **chapter 5.2 "Bus Interface" on page 42** - and the programmable I^2C/3-Wire bus data format is shown in **chapter 5.3 "Bus Data Format" on page 44**.

3.4.6 DC/DC clock output

To drive a bipolar NPN switching transistor of an external DC/DC converter directly, a programmable DC/DC clock generator is integrated. The clock frequency and the duty cycle of the DC/DC clock generator can be set over the I^2C/3-Wire bus as shown in **Table 18 "Subaddress 04H, DC-DC Converter" on Page 55**.

3.4.7 DAC

Three DACs for digital alignment with a control range up to 5 volt can be programmed in 256 steps as shown in **Table 19 "Subaddress 05H, DACs" on Page 56**. This voltage is required for a automatic alignment of the tuner prestage filters as illustrated in **Figure 4 "Tuner application block diagram" on Page 26**.

3.4.8 Power-on Reset, Stand-by Condition

While applying the supply voltage, integrated power-on reset circuits ensure a defined state after initial power-up. The required programming data will be set to default values.

When V_{CC} fall below approximately 1.2 V (typ.) the power-on resets go active and tie all write data registers to their power-on defaults (= power-down reset). While power-on reset is active no programming is possible.

The power-on flags (POFx) are set at power-on and when V_{VCCx} falls below appr. 1.2 V (typ.). They will be reset at the end of a READ operation of the status register.

By programmable stand-by control bits it's possible to reduce the current consumption of the IC up to 99%. In the full stand-by mode only bus interface is staying active and the

current consumption is reduced below 200 µA. After power-on reset only bus interface and XTAL-oscillator with bandgap are active and the current consumption is about 2.6 mA (typ.).

3.4.9 IF switch, Loop thru

For the alignment procedure of the tuner module two programmable switches are integrated to bypass the bandpass, the SAW driver and the SAW filter. The first switch called “IF switch” can switch between the mixer output signal and the bandpass output signal. The second switch called “Loop thru” can switch between the signal after the first stage of the IF AGC amplifier and the SAW filter output signal.

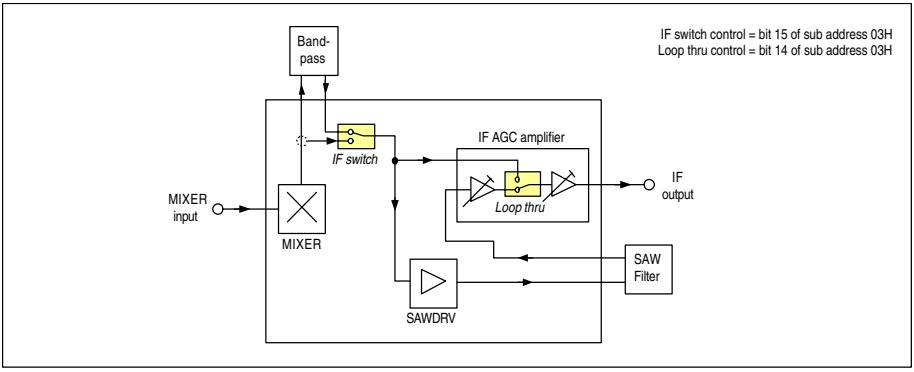


Figure 3 Functional Block Diagram of IF switch and Loop thru