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Product Information

To:

Product Name: TVL-55682D101U-LW-I-AAN

Document Issue Date: 2013/02/21

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2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by KYOCERA DISPLAY for any intellectual property claims or other problems that may result from application based on the module described herein.

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Revision	Date	Page	Old Description	New Description	Remark
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1 General Descriptions

1.1 Introduction

The TVL-55682AAN is a Color Active Matrix Thin Film Transistor (TFT) Liquid Crystal Display (LCD) module, which uses amorphous Silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT LCD has a 10.1-inch (diagonally measured) active display area with WSVGA resolution (1,024 vertical by 600 horizontal pixel array).

1.2 Features

- 10.1" TFT LCD Panel
- LED Light-bar Backlight System
- Supports WSVGA (V:1,024 lines, H:600 pixels) Resolution
- Compatible with RoHS Standard

1.3 Product Summary

Items	Specifications	Unit	Remark
Screen Diagonal	10.1	inch	
Active Area	222.72(H) x 125.28(V)	mm	
Pixels(H x V)	1,024 (x3) x 600	-	
Pixel Pitch	0.2175(H) x 0.2088(V)	mm	
Pixel Arrangement	R.G.B. Vertical Stripe	-	
Display Mode	TN Mode, Normally White	-	
White Luminance	200 (Typ.)	cd/ m^2	5 Points Average, 20mA per LED
Contrast Ratio	500 (Typ.)	-	
Response Time	8 (Typ.)	ms	
View Angle(L/R/U/D)	45/45/15/35 (Typ.)	-	
Input Voltage	+3.3 (Typ.)	V	
Power Consumption	2.4	Watt	Black Pattern
Module Weight	190 (Max.)	g	
Outline Dimension(H x V x D)	235.5(H) x 143.5(V) x 5.2(D) (Max.)	mm	
Electrical Interface (Logic)	LVDS	-	
Support Color	262 K	-	
NTSC	45 (Typ.)	%	
Optimum Viewing Direction	6 o'clock	-	
Surface Treatment	Anti-Glare	-	

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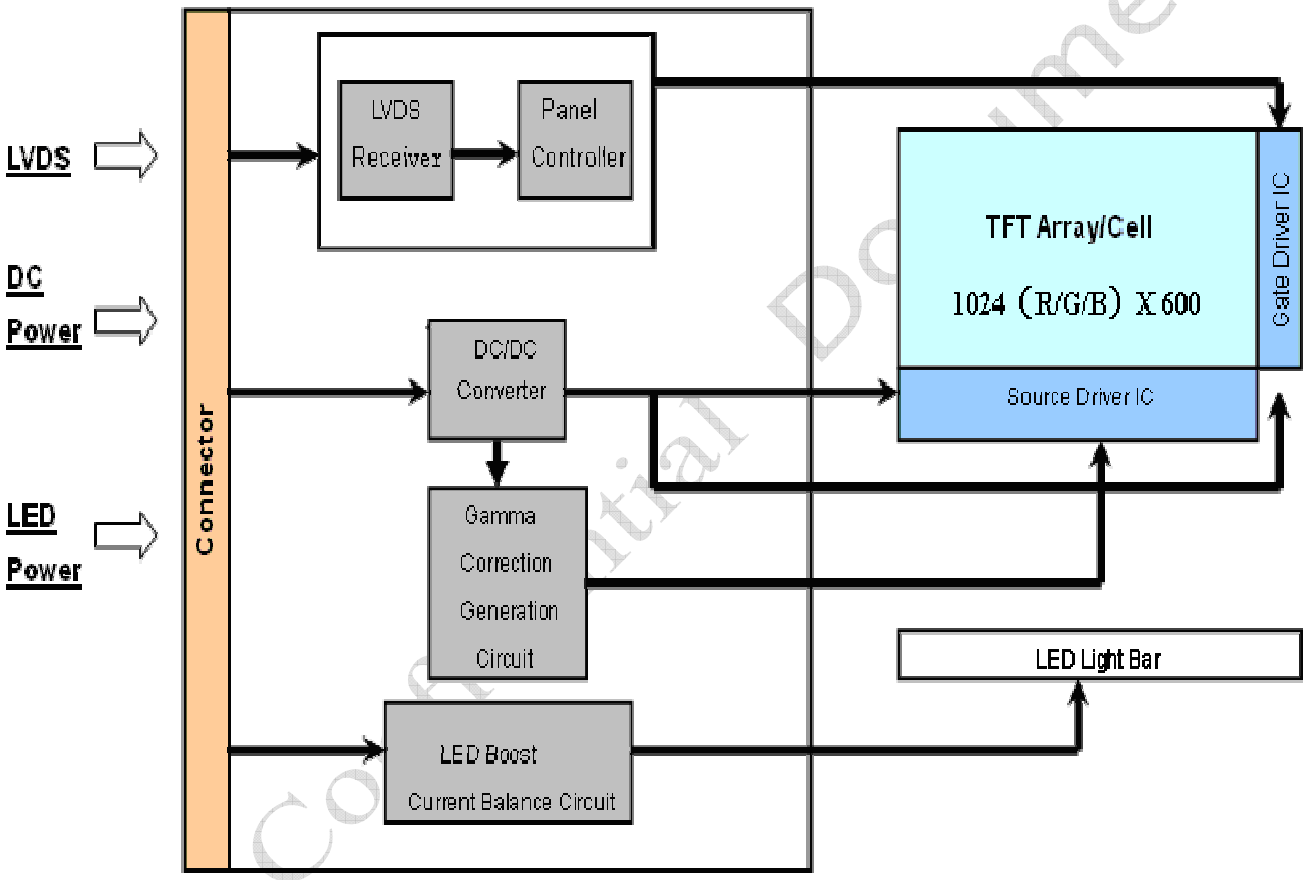
1.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module.

Figure 1 Block Diagram



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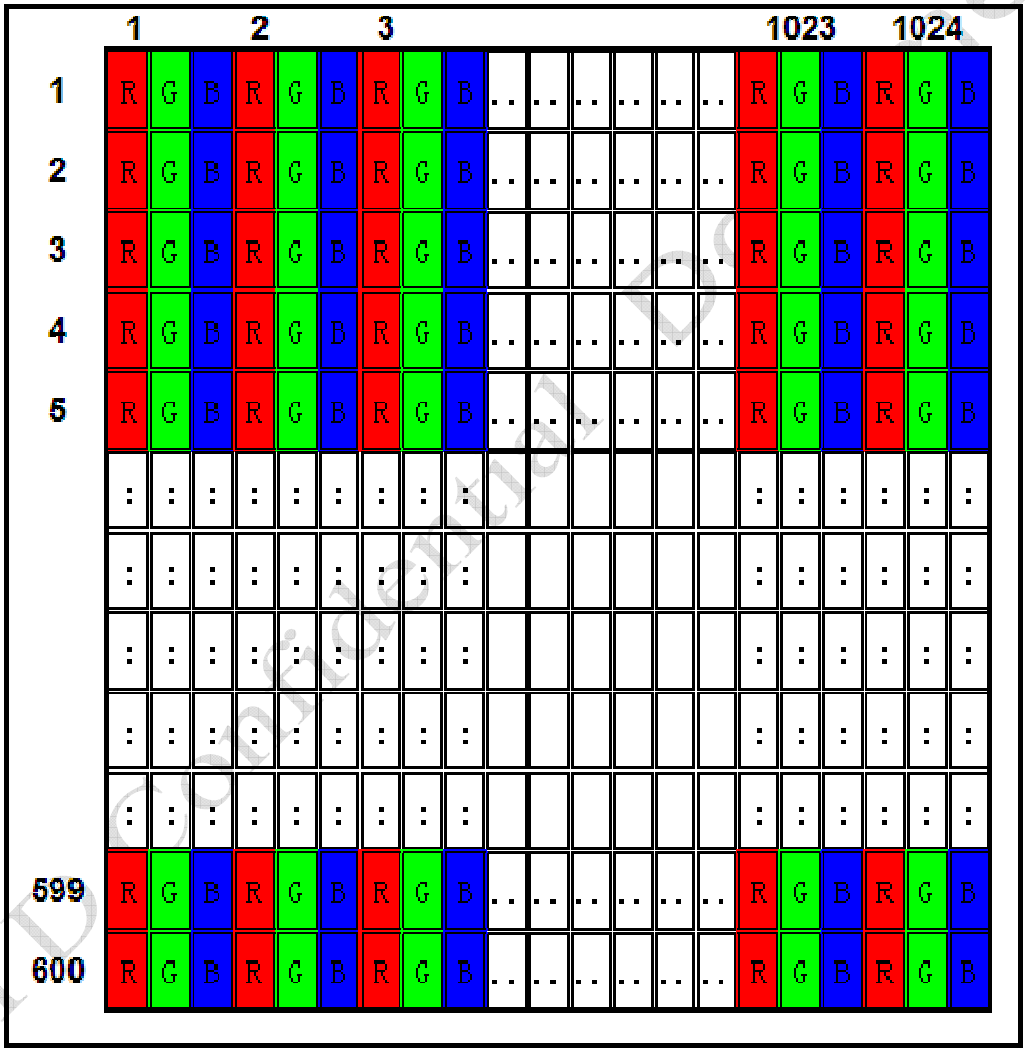
1.5 Pixel Format Image

Figure 2 shows the relationship of the input signals and LCD pixel format image.

Figure 2 Pixel Format



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2 Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1

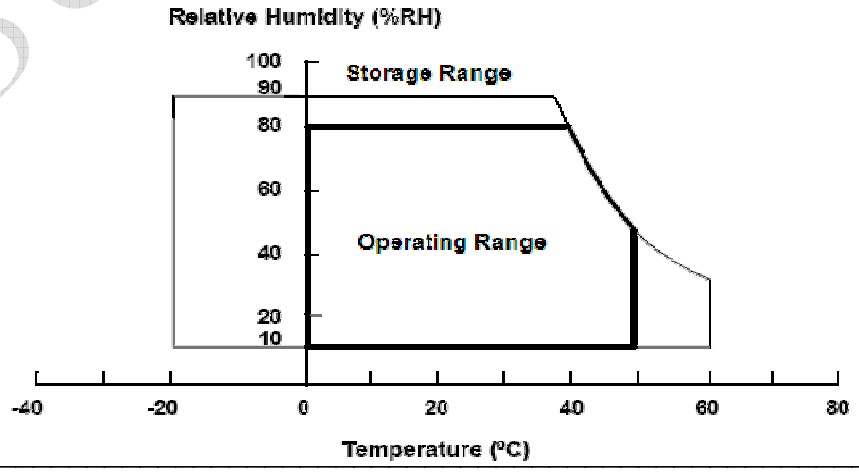
Item	Symbol	Min.	Max.	Unit	Conditions
Supply Voltage	V_{DD}	-0.3	4.0	V	-
Supply $V_{\_LED}$ Voltage	$V_{\_LED}$	5	21	V	-
Input Signal	-	-0.3	2.7	V	LVDS Signals
Operating Temperature	TOP	0	50	℃	Note(3)
Operating Humidity	HOP	10	80	%RH	Note(3)
Storage Temperature	TST	-20	60	℃	Note(3)
Storage Humidity	HST	10	90	%RH	Note(3)
Vibration	Level	-	1.5	G	30min. for X, Y, Z axis
	Bandwidth	-	10~500Hz	Hz	
Shock	Level	-	220	G	Half Sine Waveform, 2ms
LED Current	$I_{\_LED}$	-	20.5	mA	Per LED

Note

(1)Maximum Wet-Bulb should be 39℃ and No condensation.

(2)When you apply the LCD module for OA system, please make sure to keep the temperature of LCD module under 60 ℃.

(3)Storage /Operating temperature & humidity:



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3 Electrical Specification

3.1 Electrical Characteristics

Table 2 Electrical Characteristics

Symbol	Parameter		Min.	Typ.	Max.	Units	Condition
V_{DD}	Logic/LCD Drive Voltage		3	3.3	3.6	V	Note (1)
I_{DD}	VDD Current		-	160	-	mA	Black Pattern, 60Hz
P_{DD}	VDD Power		-	-	0.53	W	Black Pattern, 60Hz
Irush	Rush Current		-	-	2	A	Note (2)
$V_{DD}rp$	Allowable Logic/LCD Drive Ripple Voltage		-	-	300	mVp-p	-
$V_{\_LED}$	LED Input		5	12	21	V	-
V_F	LED Forward Voltage		2.95	3.3	3.4	V	-
I_F	LED Forward Current		19.5	20	20.5	mA	-
P_{LED}	LED Power Consumption		-	-	1.87	W	Note(3)
L_T	LED Life Time		10,000	-	-	Hours	Note(4)
V_{PWM_EN}	PWM Signal Voltage	High	2	3.3	3.6	V	-
		Low	0	-	0.5	V	
F_{PWM}	Output PWM Frequency		-	200	1K	Hz	-
$V_{\_LED\_EN}$	LED Enable Voltage	High	2	3.3	3.6	V	-
		Low	0	-	0.5	V	
PWM	PWM Duty Ratio		5	-	100	%	-

Note: (1)V_{DD} Power Dip Condition

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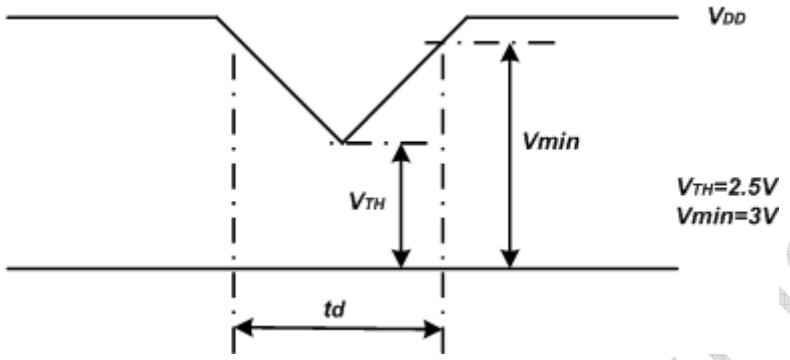
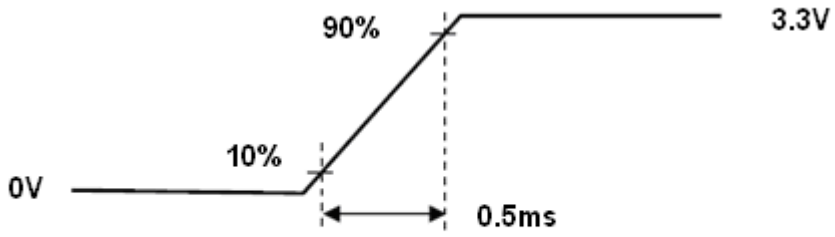
Figure 3 V_{DD} Power Dip



If $V_{TH} < V_{DD} \leqslant V_{min}$ and $t_d \leqslant 10ms$, our panel must revive automatically when the voltage returns to normal.

(2)Measure Condition

Figure 4 V_{DD} rising time



VDD rising time

(3) P_{LED} is calculation value for reference. P_{LED} =24 x V_F (Normal Distribution) x I_F (Normal Distribution) / Efficiency

(4) The lifetime of LED is defined as the time when LED packages continue to operate under the conditions at Ta = 25℃ and I_F= 20 mA (per chip) until the brightness becomes≦50% of its original value.

(5)All values are measured at condition of $V_{\_LED}$ =12V and Ta=25℃.

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3.2 Interface Connector

Table 3 Connector Name / Designation

Manufacturer	I-PEX (or equivalent)
Mating Receptacle/Part Number	20453-040T(I-PEX)

Table 4 Signal Pin Assignment

Pin #	Signal Name	Description	Remarks
1	GND	Ground	
2	V_{DD}	Power Supply 3.3V (Typ.)	
3	V_{DD}	Power Supply 3.3V (Typ.)	
4	V_{EDID}	EDID +3.3V Power	
5	NC	Not Connected(Reserve)	LCD panel self test enable
6	$CLK_{\_EDID}$	EDID Clock Input	
7	$DAT_{\_EDID}$	EDID Data Input	
8	RXin0-	−LVDS Differential Data Input(R0-R5,G0)	
9	RXin0+	+LVDS Differential Data Input(R0-R5,G0)	
10	GND	Ground	
11	RXin1-	−LVDS Differential Data Input(G1-G5,B0-B1)	
12	RXin1+	+LVDS Differential Data Input(G1-G5,B0-B1)	
13	GND	Ground	
14	RXin2-	−LVDS Differential Data Input(B2-B5,HS,VS,DE)	
15	RXin2+	+LVDS Differential Data Input(B2-B5,HS,VS,DE)	
16	GND	Ground	
17	CLKN-	−LVDS Differential Clock Input	
18	CLKN+	+LVDS Differential Clock Input	
19	NC	Not Connected(Reserve)	
20	NC	Not Connected(Reserve)	
21	NC	Not Connected(Reserve)	
22	GND	Ground-Shield	
23	NC	Not Connected(Reserve)	
24	NC	Not Connected(Reserve)	
25	GND	Ground-Shield	
26	NC	Not Connected(Reserve)	

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27	NC	Not Connected(Reserve)	
28	GND	Ground-Shield	
29	NC	Not Connected(Reserve)	
30	NC	Not Connected(Reserve)	
31	V_{LED_GND}	LED Ground	
32	V_{LED_GND}	LED Ground	
33	V_{LED_GND}	LED Ground	
34	NC	Not Connected(Reserve)	
35	V_{PWM_EN}	System PWM Logic Input Level	
36	V_{LED_EN}	LED Enable Input Level(+3.3V)	
37	NC	Not Connected(Reserve)	
38	V_{LED}	LED Power Supply 5-21V	
39	V_{LED}	LED Power Supply 5-21V	
40	V_{LED}	LED Power Supply 5-21V	

Note: All input signals shall be at low or Hi-Z state when V_{DD} is off.

3.3 LVDS Receiver

3.3.1 Signal Electrical Characteristics For LVDS Receiver

The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644) standard.

Table 5 LVDS Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold	V_{th}	-	-	+100	mV	V_{cm}=+1.2V
Differential Input Low Threshold	V_{tl}	-100	-	-	mV	V_{cm}=+1.2V
Magnitude Differential Input Voltage	$\|V_{id}\|$	100	-	600	mV	
Common Mode Voltage	V_{cm}	|Vid/2|+0.6	1.2	1.8-|Vid/2|	V	
Common Mode Voltage Offset	ΔV_{cm}	-	-	50	mV	V_{cm}=+1.2V

Note:

(1)Input signals shall be at low or Hi-Z state when V_{DD} is off.

(2)All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

(3)All values are measured at condition of V_{DD} =3.3V and Ta=25℃.

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Figure 5 Voltage Definitions

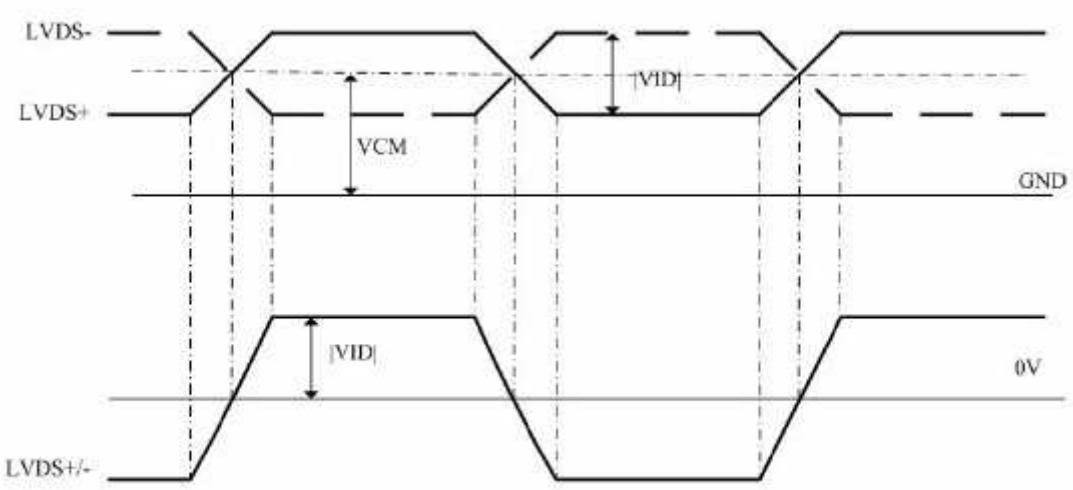


Figure 6 Measurement System

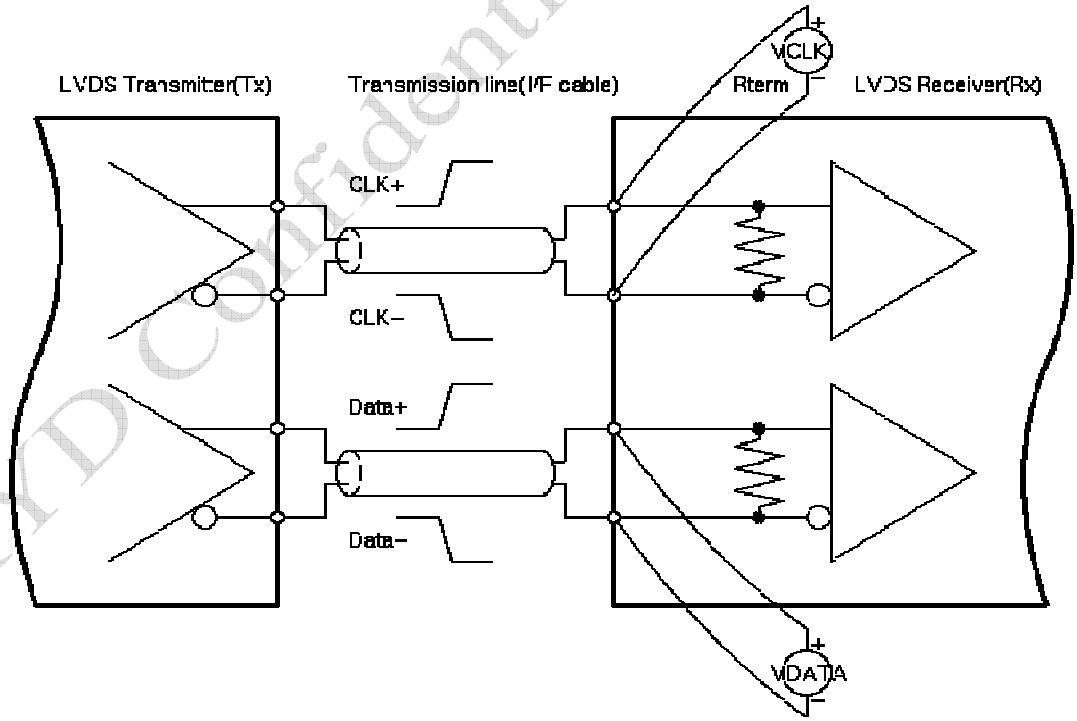
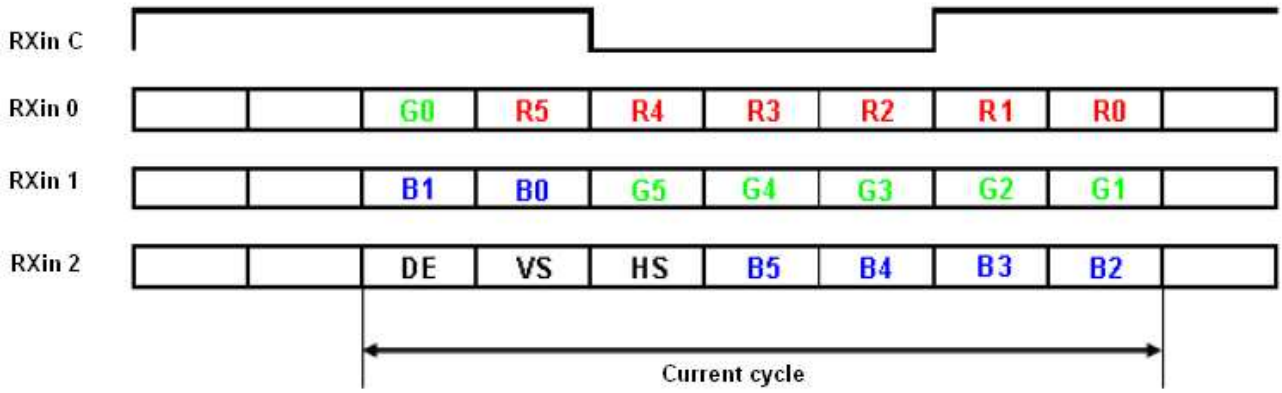


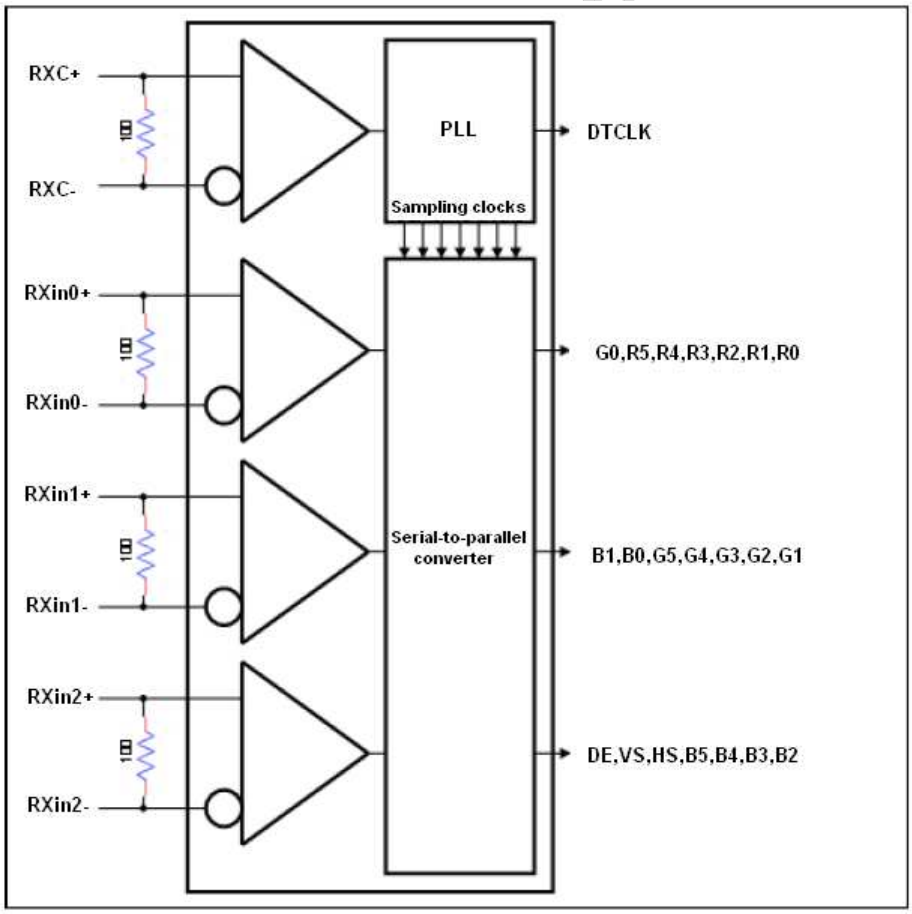
Figure 7 Data mapping



3.3.2 LVDS Receiver Internal Circuit

Figure 8 LVDS Receiver Internal Circuit shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

Figure 8 LVDS Receiver Internal Circuit

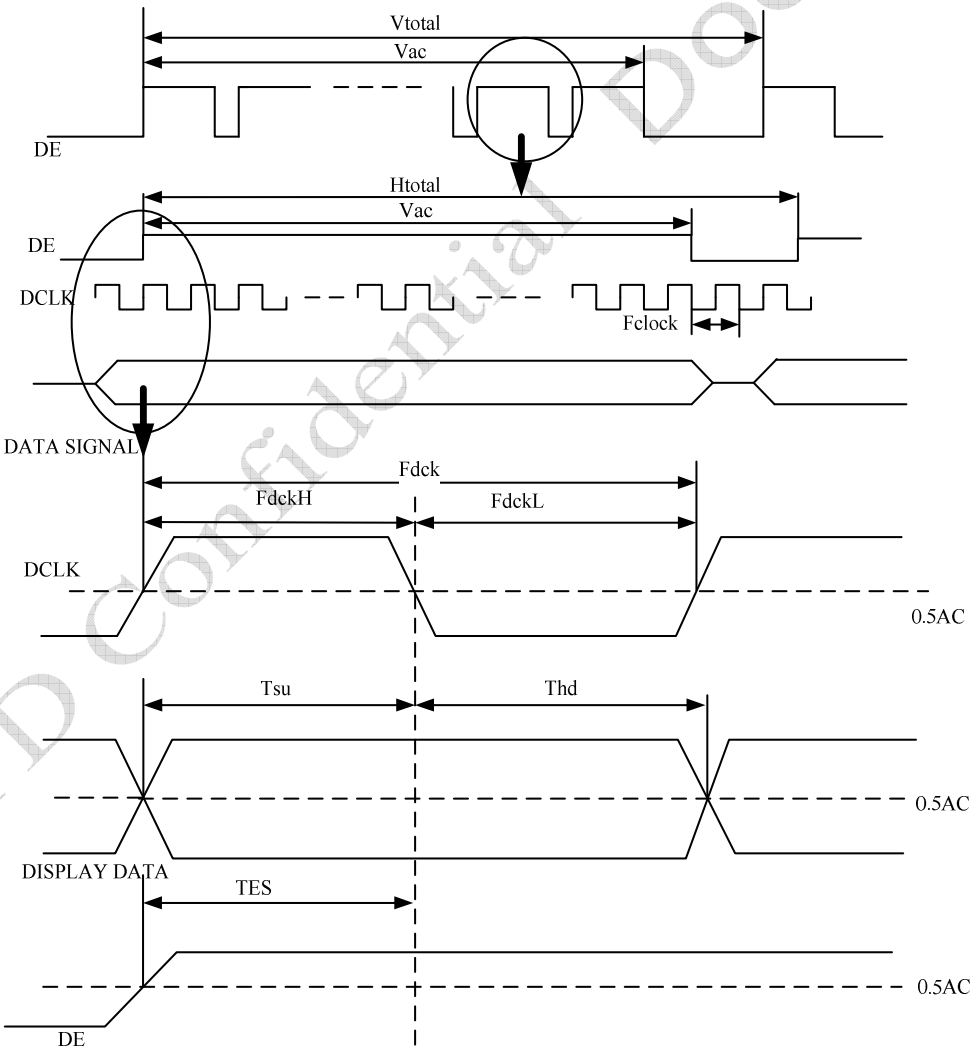


3.4 Interface Timings

Table 6 Interface Timings

Parameter	Symbol	Unit	Min.	Typ.	Max.
LVDS Clock Frequency(single)	F_{dck}	MHz	44.4	50.4	65.2
H Total Time	H_{total}	Clocks	1,320	1,344	1,362
H Active Time	H_{ac}	Clocks	1,024	1,024	1,024
V Total Time	V_{total}	Lines	612	625	638
V Active Time	V_{ac}	Lines	600	600	600
Frame Rate	V_{sync}	Hz	55	60	65

Figure 9 Timing Characteristics



Note: TES is data enable signal setup time.

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3.5 Power ON/OFF Sequence

V_{DD} power, interface signals, and lamp on/off sequence are showing on Figure 10.

Signals shall be Hi-Z state or low level when V_{DD} is off.

Figure 10

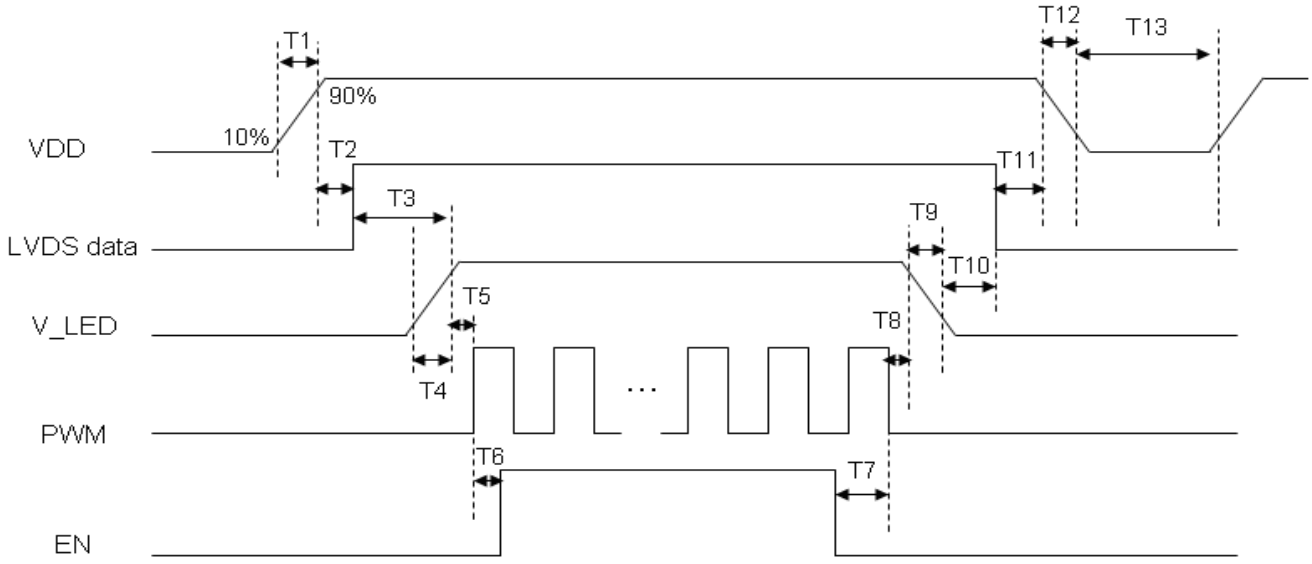

Table 7 Power Sequencing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{DD} Rising Time	T1	0.5	-	10	ms
V_{DD} Good to Signal Valid	T2	30	-	90	ms
Signal Valid to Backlight on	T3	200	-	-	ms
Backlight Power on Time	T4	0.5	-	-	ms
Backlight V_{DD} Good to System PWM on	T5	10	-	-	ms
System PWM on to Backlight Enable on	T6	10	-	-	ms
Backlight Enable off to System PWM off	T7	0	-	-	ms
System PWM off to B/L Power Disable	T8	10	-	-	ms
Backlight Power off Time	T9	-	10	30	ms
Backlight off to Signal Disable	T10	200	-	-	ms
Signal Disable to Power Down	T11	0	-	50	ms
V_{DD} Falling Time	T12	-	10	30	ms
Power off	T13	500	-	-	ms

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4 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

Table 8 Optical Characteristics

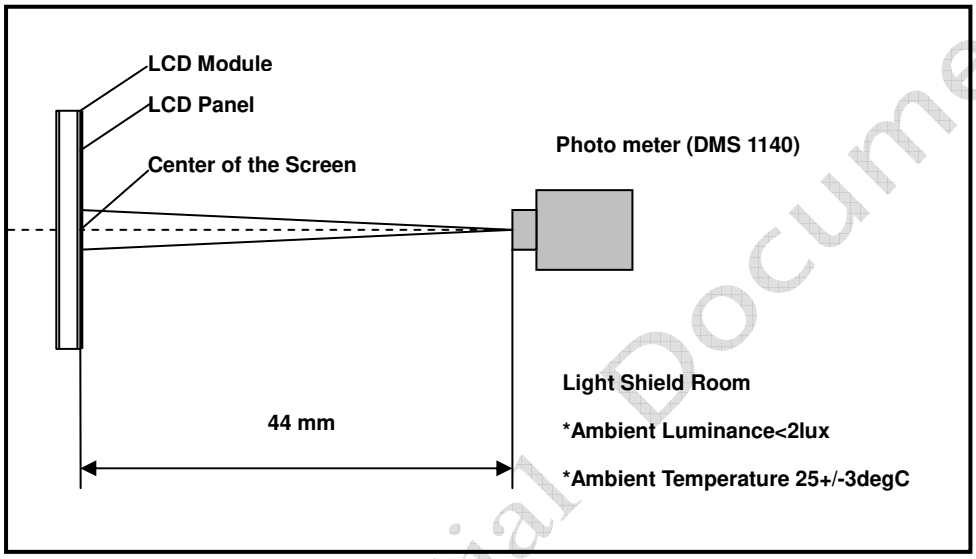
Item	Conditions		Specification				
			Min.	Typ.	Max.	Unit	Note
Viewing Angle [degrees] K=Contrast Ratio>10	Horizontal	Left	40	45	-	Deg.	(1),(2)
		Right	40	45	-	Deg.	
	Vertical	Up	10	15	-	Deg.	
		Down	30	35	-	Deg.	
Contrast Ratio	Center		400	500	-	-	(1),(3)
Response Time	Rising		-	3	-	ms	
	Falling		-	5	-	ms	
	Rising + Falling		-	8	16	ms	(1),(4)
Color Chromaticity (CIE1931)	Red x		Typ. -0.03	0.579	Typ. +0.03	-	(1)
	Red y			0.346		-	(1)
	Green x			0.336		-	(1)
	Green y			0.560		-	(1)
	Blue x			0.156		-	(1)
	Blue y			0.123		-	(1)
	White x		0.283	0.313	0.343	-	(1)
	White y		0.299	0.329	0.359	-	(1)
White Luminance [cd/m^2]	$I_{\_LED}$ =20.0mA		180	200	-	cd/m^2	(1), (5)
Luminance Uniformity [%]	$I_{\_LED}$ =20mA, 13points		62.5	-	-	-	(1), (6)
	$I_{\_LED}$ =20mA, 5points		80.0	-	-		

Note: (1)Measurement Setup

The LCD module should be stabilized at 25℃ for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the

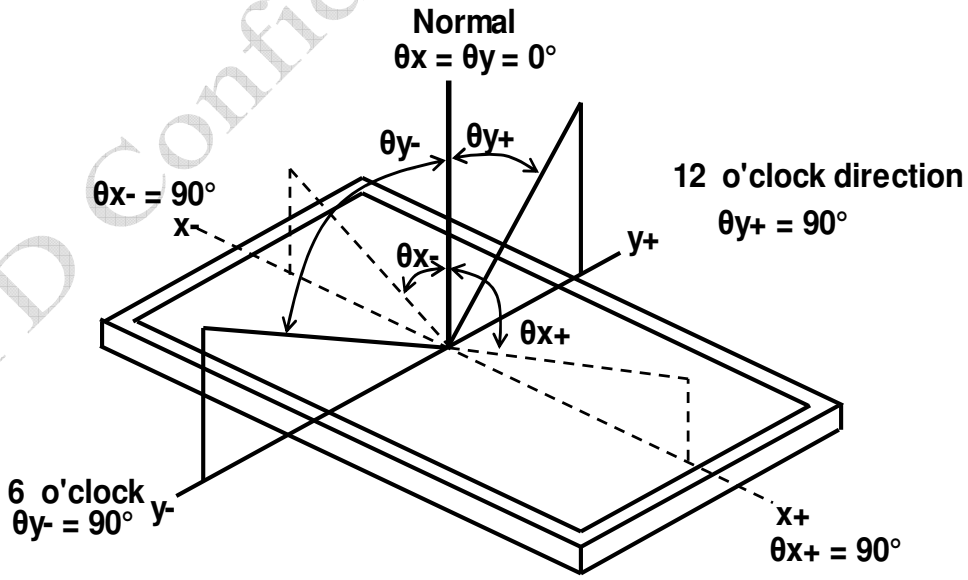
measurement should be executed after lighting backlight for 15 minutes in a windless room.

Figure 11 Measurement Setup



(2)Definition of Viewing Angle

Figure 12 Definition of Viewing Angle



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(3)Definition of Contrast Ratio (CR)

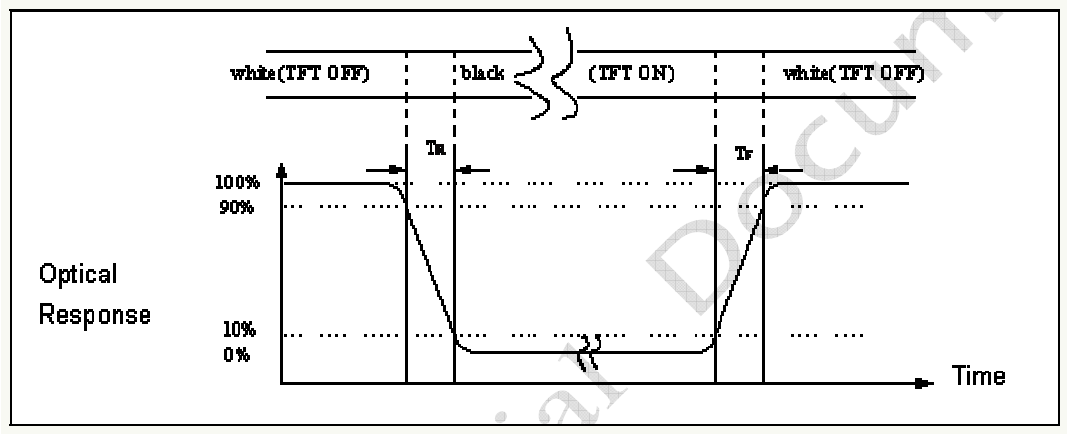
The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

(4)Definition of Response Time (T_R, T_F)

Figure 13 Definition of Response Time



(5)Definition of Luminance White

Measure the luminance of gray level 63 at 5 points(Fig.14).

Center of Luminance = Y1

Average Luminance of 5 points = $\frac{Y_1 + Y_2 + Y_3 + Y_4 + Y_5}{5}$

(6)Definition of Luminance Uniformity(Variation)

Measure the luminance of gray level 63 at 13 points.

Uniformity of 13 points = $\frac{\text{Min Luminance of Y1~Y13}}{\text{Max Luminance of Y1~Y13}}$ x 100%

Uniformity of 5 points = $\frac{\text{Min Luminance of Y1~Y5}}{\text{Max Luminance of Y1~Y5}}$ x 100%

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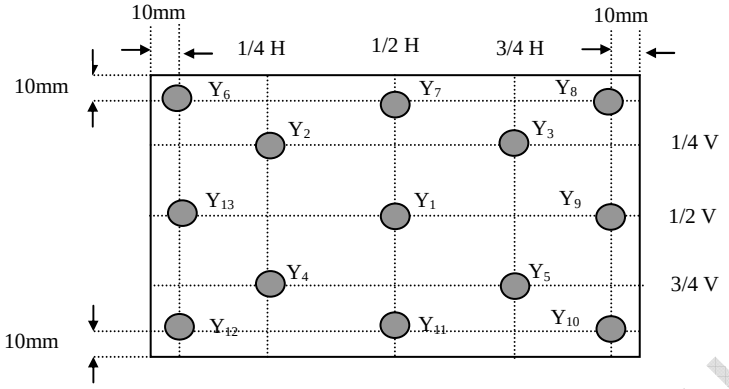
Figure 14 Measurement Locations of 13 Points



5 Mechanical Characteristics

Figure 15 Reference Outline Drawing (Front Side)

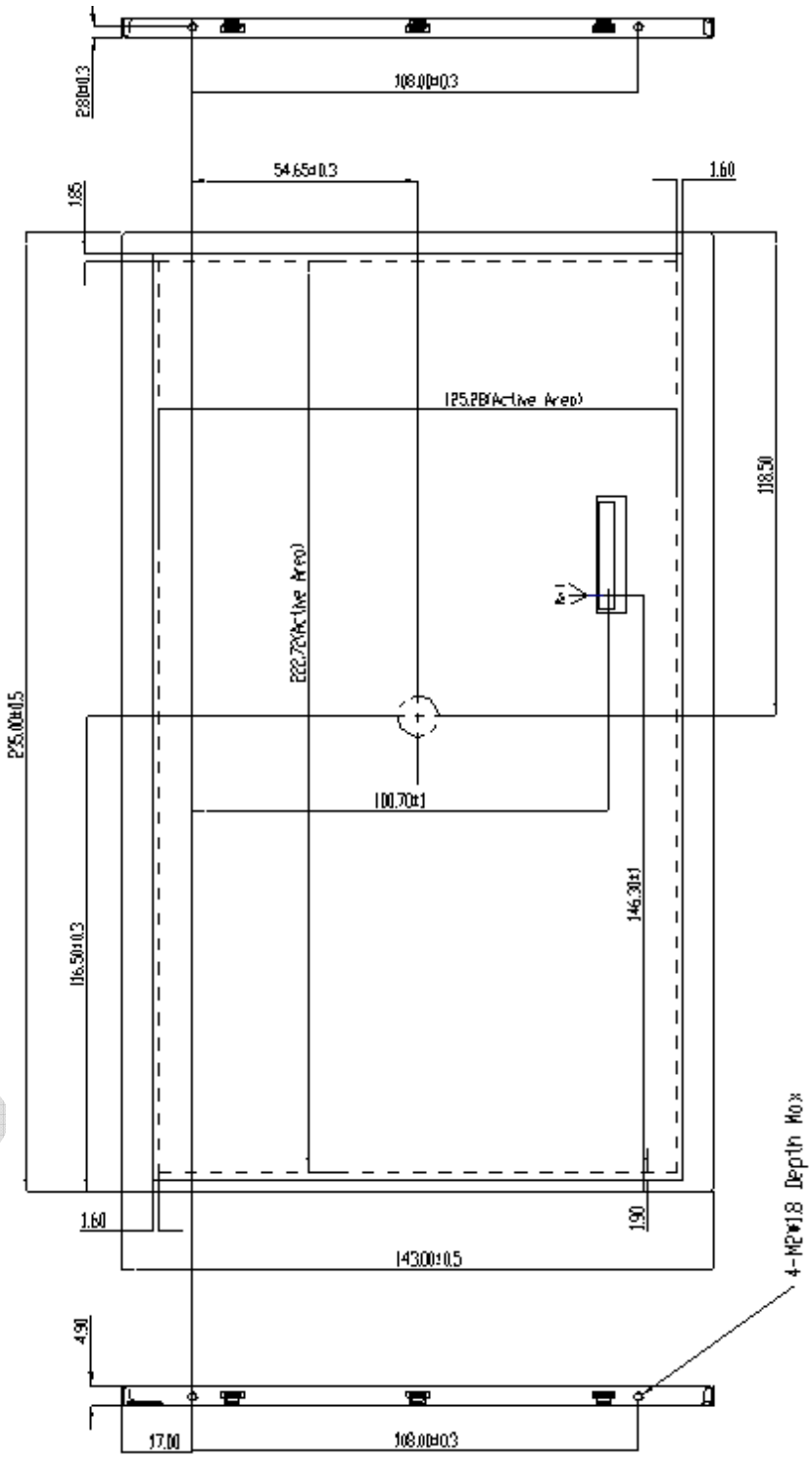
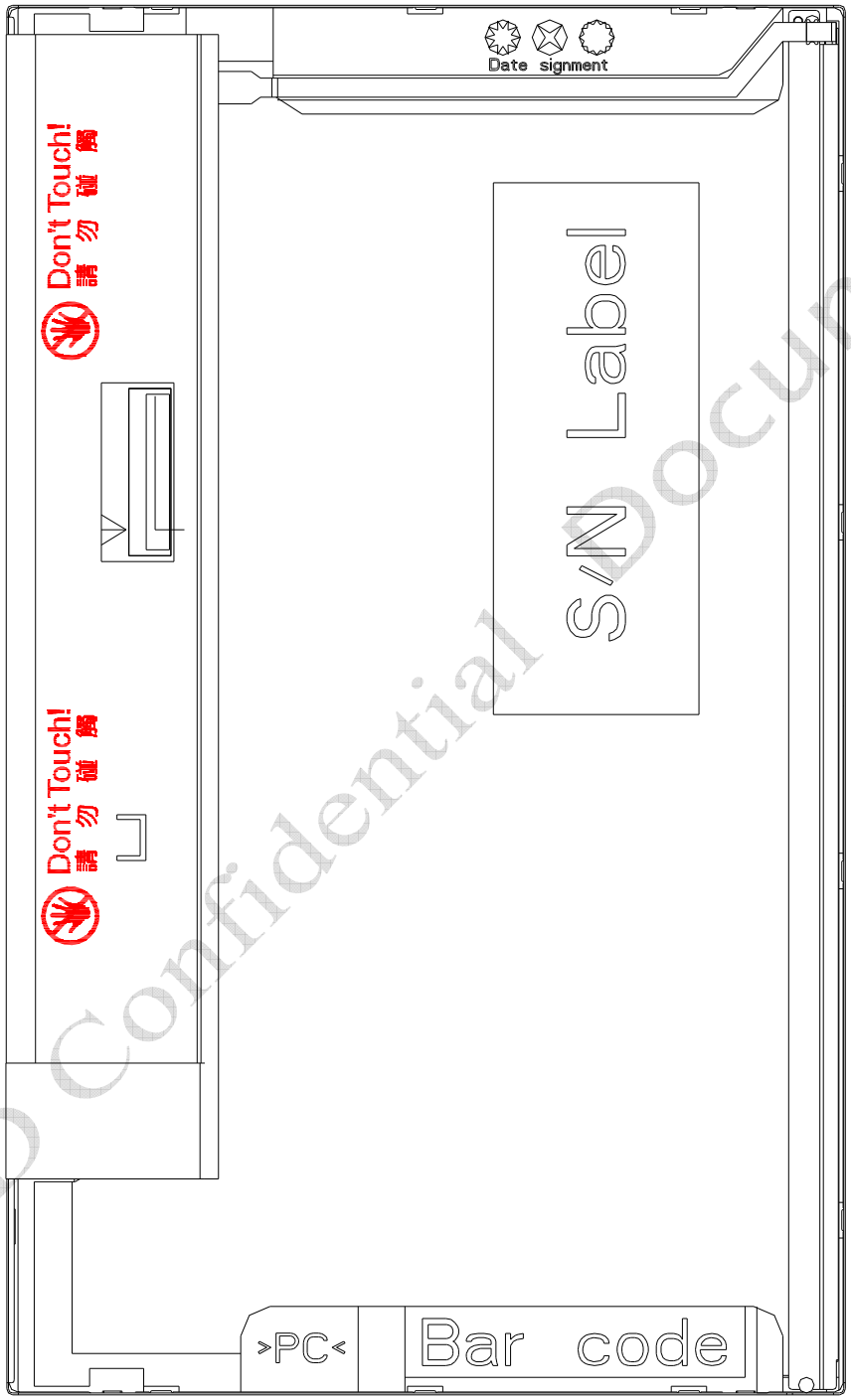


Figure 16 Reference Outline Drawing (Back Side)



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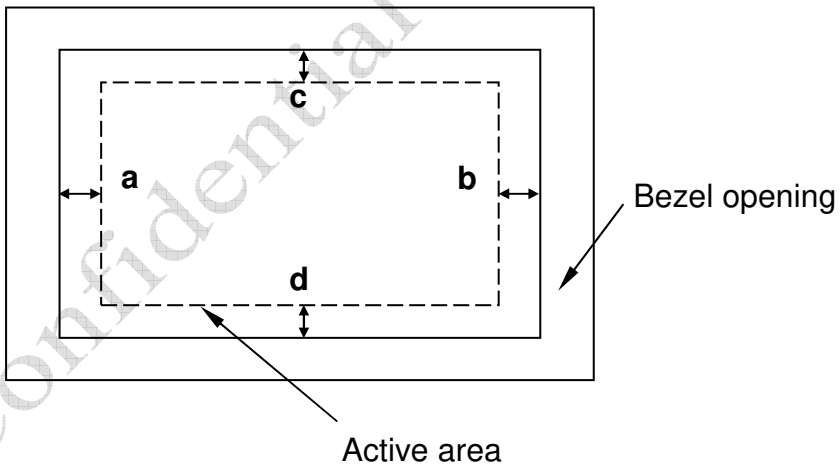
5.1 Dimension Specifications

Table 9

Item		Value	Unit
Width		235.00±0.5	mm
Height		143.00±0.5	mm
Thickness(Max.)		5.2	mm
Bezel Opening	X	226.47±0.5	mm
	Y	128.48±0.5	mm
Weight(Max.)		190	g
BM Width	| a-b | & | c-d |	≤1.0	mm



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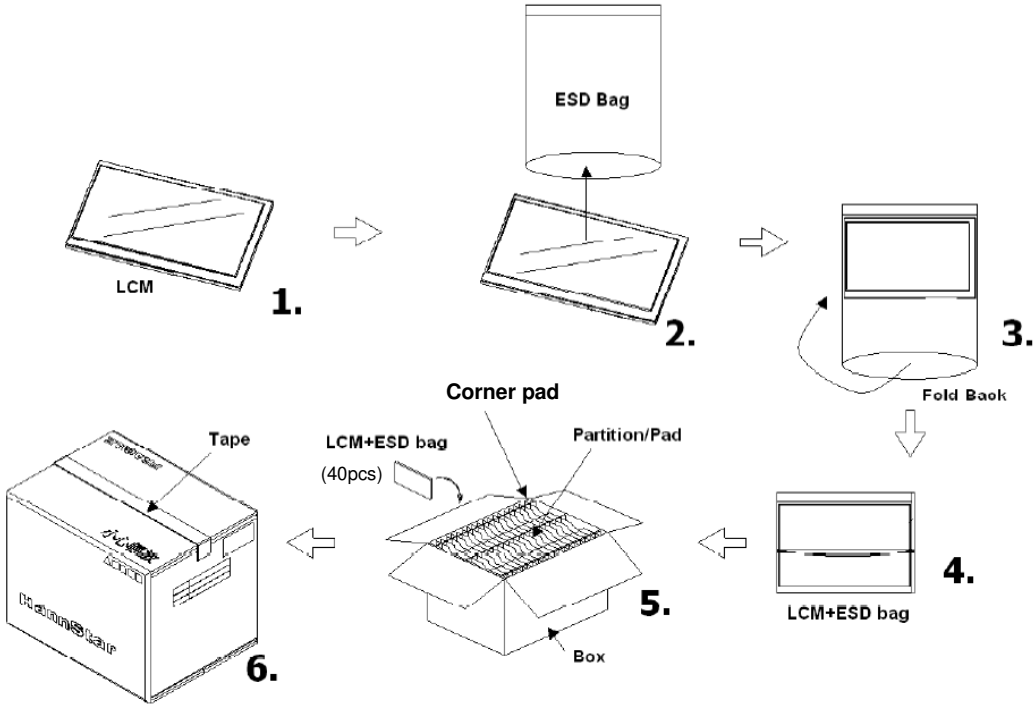
6 Package Specification



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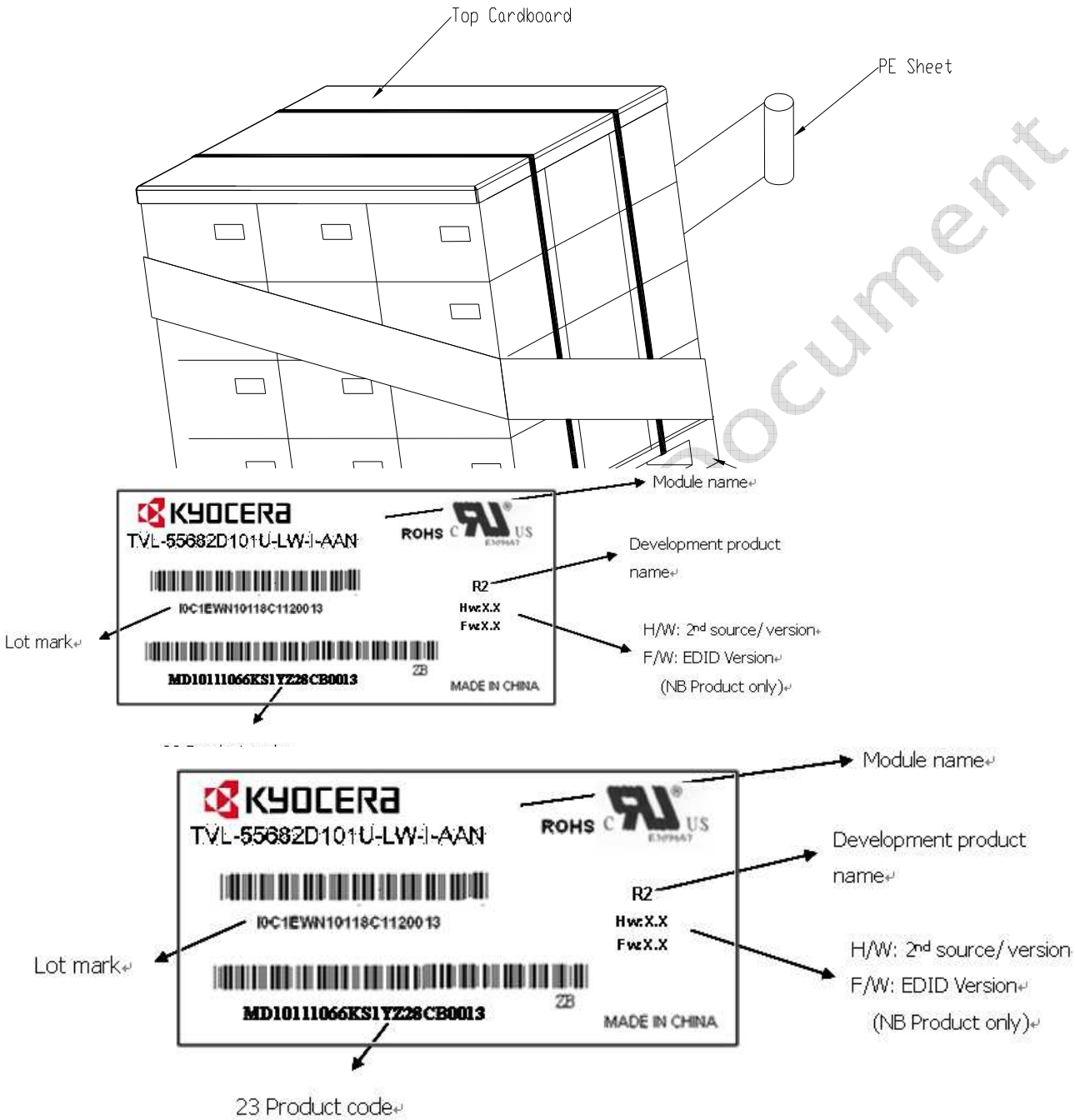

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