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Product Information

To:

Product Name: TVL-55683D116U-LW-I-AAN

Document Issue Date: 2013/02/21

Note: 1. Please contact Kyocera Display Company. before designing your product based on this product.
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by KYOCERA DISPLAY for any intellectual property claims or other problems that may result from application based on the module described herein.

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Revision	Date	Page	Old Description	New Description	Remark
00	2012/05/10	All	--	First issued	

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1.0 General Descriptions

1.1 Introduction

The TVL-55683D116U-LW-I-AAN is a color active matrix thin film transistor (TFT) TN liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT LCD has an 11.6-inch diagonally measured active display area with WXGA resolution (1366 vertical by 768 horizontal pixel array).

1.2 Features

- 11.6”WXGA TFT LCD Panel
- LED Light-bar Backlight System
- Supported WXGA (V:1,366 lines, H:768 pixels) resolution
- Compatible with RoHS Standard

1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	11.6	Inch
Active Area	256.125 (H) x 144.000(V)	mm
Pixels H x V	1,366 (x3) x 768	-
Pixel Pitch	0.1875x0.1875	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally White (TN)	-
White Luminance	220 (Typ.) 5 points average	cd/ m^2 (20mA of per LED)
Contrast Ratio	500（Typ.）	-
Response Time	8(Typ.)	ms
View Angle(L/R/U/D)	75/75/50/60(Typ.)	-
Input Voltage	+3.3 (Typ.)	V
Power Consumption	4.2 (Max.)	Watt
Module Weight	235 (Max.)	g
Outline Dimension (Max)	278.5(H) x 168.0(V) x3.7(D)	mm
Electrical Interface (Logic)	LVDS	-
Support Color	262 K	-
Color Gamut	45%(Typ)	
Optimum Viewing Direction	6 o’clock	-
Surface Treatment	Anti-Glare	-

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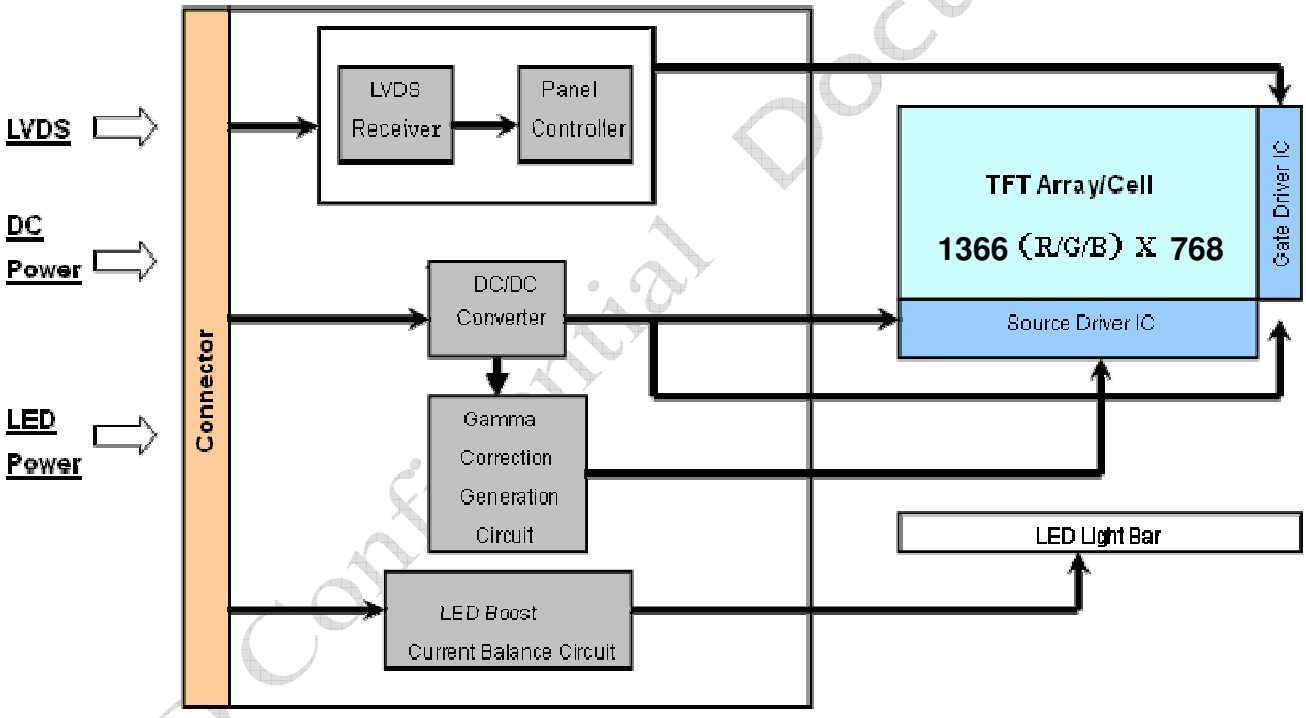
1.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module

Figure 1 Block Diagram



2.0 Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1

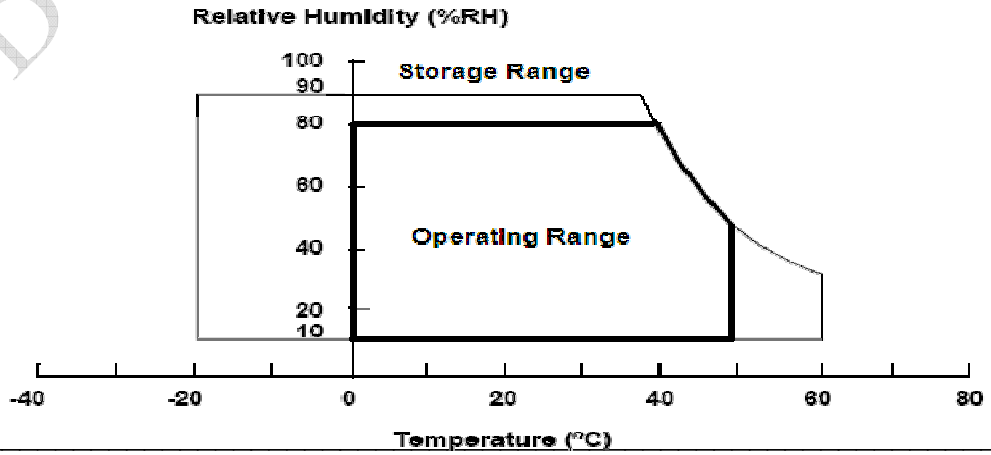
Item	Symbol	Min	Max	Unit	Conditions
Supply Voltage	VDD	-0.3	4.0	V	Typ.=3.3V
Supply V_{LED} Voltage	V_{LED}	6	21	V	
Input Signal		-0.3	2.7	V	LVDS signals
Operating Temperature	TOP	0	50	deg. C	(Note 3)
Operating Humidity	HOP	10	80	%RH	(Note 3)
Storage Temperature	TST	-20	60	deg. C	(Note 3)
Storage Humidity	HST	10	90	%RH	(Note 3)
Vibration	Level	-	1.5G	G	30min for X, Y, Z axis
	Bandwidth		10～500Hz	Hz	
Shock	Level	-	220	G	Half sine wave,2ms

Note

(1) Maximum Wet-Bulb should be 39 degree C. No condensation.

(2) When you apply the LCD module for OA system. Please make sure to keep the temperature of LCD module is less than 60℃

(3) Storage /Operating temperature



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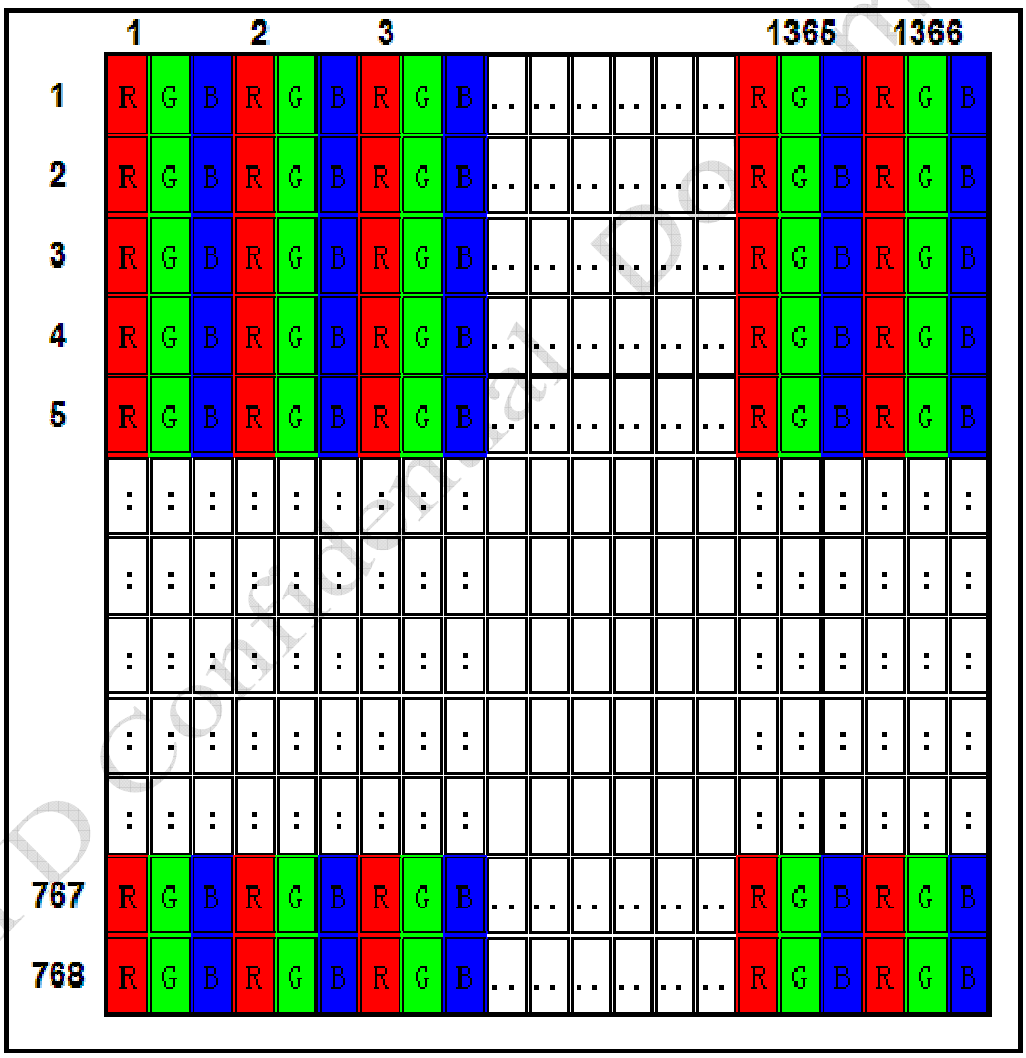
3.0 Pixel Format Image

Figure 2 shows the relationship of the input signals and LCD pixel format image.

Figure 2 Pixel Format



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4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes

Table 2 Optical Characteristics

Item	Conditions		Specification			
			Min	Typ.	Max	Note
Viewing Angle [degrees] K=Contrast Ratio>10	Horizontal	Left	70	75	-	A, B
		Right	70	75	-	
	Vertical	Up	45	50	-	
		Down	55	60	-	
Contrast ratio	Center		350	500	-	A, C
Response Time [ms]	Rising + Falling		-	8	16	A, D
Color Chromaticity (CIE1931)	Red x		Typ. -0.03	0.581	Typ. +0.03	A,
	Red y			0.343		A,
	Green x			0.334		A,
	Green y			0.570		A,
	Blue x			0.156		A,
	Blue y			0.130		A,
	White x		0.263	0.313	0.363	A,
	White y		0.279	0.329	0.379	A,
White Luminance [cd/m^2]	I-LED=20.0mA		200	220	-	5point A, E
Luminance Uniformity [%]	I-LED =20mA, 13points		60	-	-	A, F
	I-LED =20mA, 5points		80	-	-	

Note: A. Measurement Setup:

The LCD module should be stabilized at 25□ for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.

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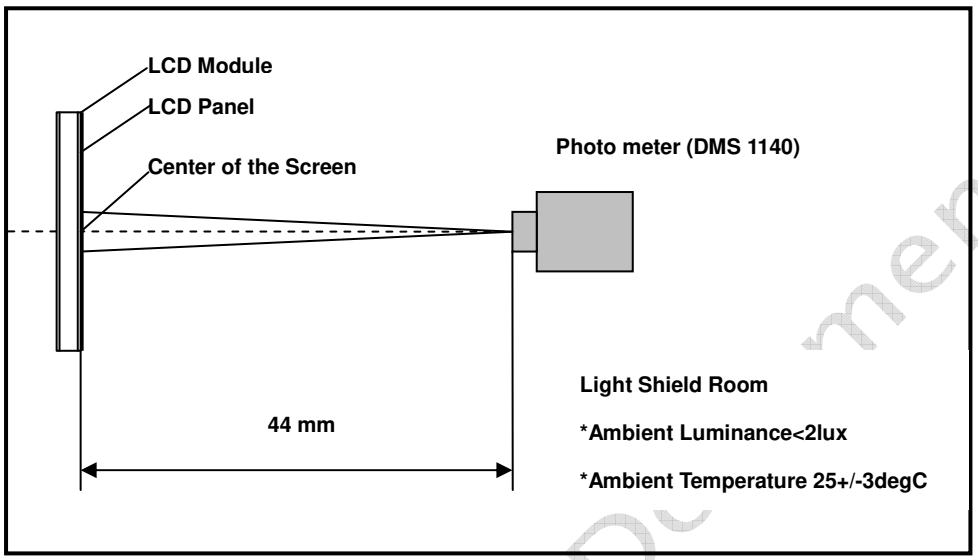
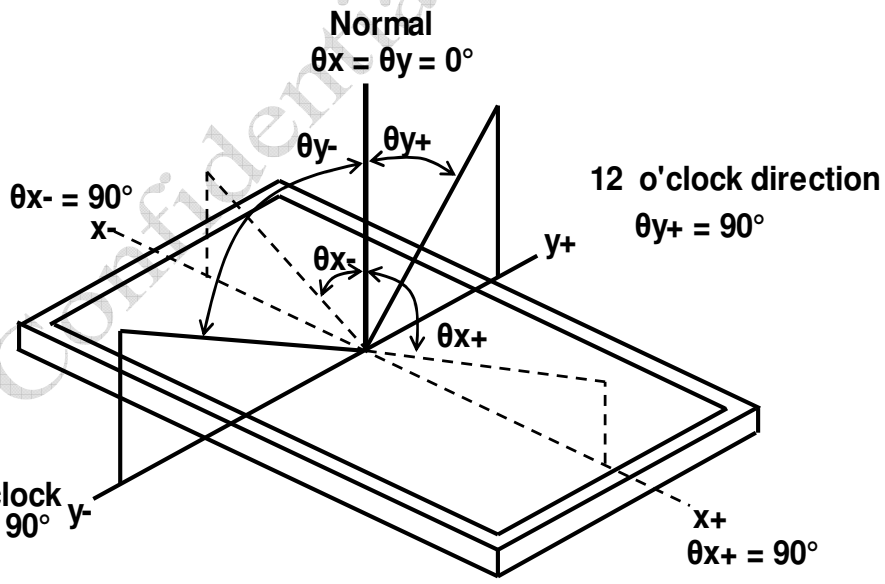
Figure 3 Measurement Setup



B. Definition of Viewing Angle

Figure 4 Definition of Viewing Angle



C. Definition of Contrast Ratio (CR)

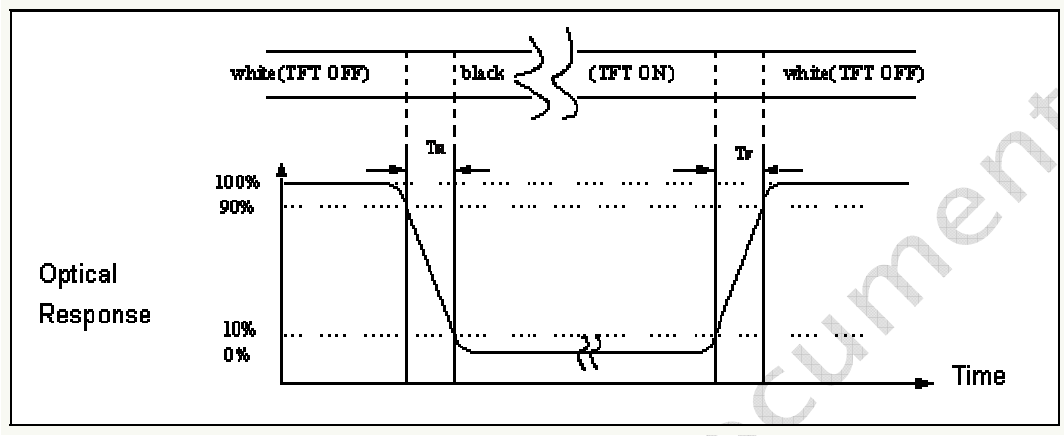
The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

D. Definition of Response Time (T_R, T_F)

Figure 5 Definition of Response Time



E. Definition of Luminance White

Measure the luminance of gray level 63 at center point and 5 points.

Center of Luminance = Y1

Average Luminance of 5 points = $\frac{Y_1 + Y_2 + Y_3 + Y_4 + Y_5}{5}$

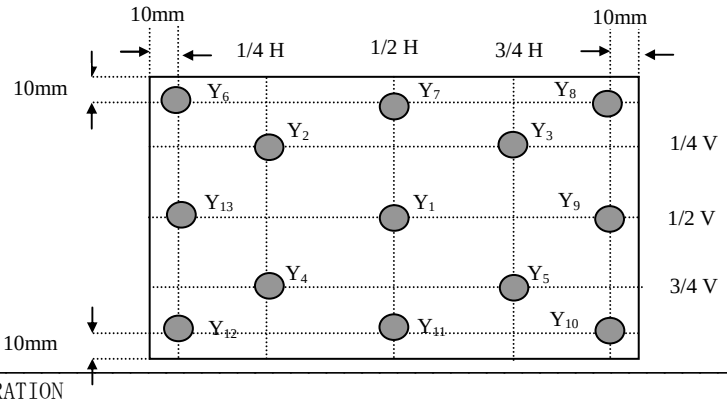
F. Definition of Luminance Uniformity(Variation)

Measure the luminance of gray level 63 at 13 points.

$$\text{Uniformity of 13 points} = \frac{\text{Min Luminance of Y1~Y13}}{\text{Max Luminance of Y1~Y13}} \times 100\%$$

$$\text{Uniformity of 5 points} = \frac{\text{Min Luminance of Y1~Y5}}{\text{Max Luminance of Y1~Y5}} \times 100\%$$

Figure 6 Measurement Locations of 13 Points



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5.0 Backlight Characteristics

5.1 Parameter Guideline of LED Backlight

Table 3 Parameter Guideline for LED Backlight

Symbol	Parameter		Min.	Typ.	Max.	Units	Condition
VLED	LED input		6	12	21	[V]	Note A
V_F	LED Forward Voltage		2.9	3.3	3.4	[V]	Ta=25
I_F	LED Forward Current			20		[mA]	Ta=25
P_{LED}	LED Power Consumption		-	-	3.0	[W]	Ta=25[deg C] Note B
LT	LED Life Time		10,000	-	-	Hours	Ta=25[deg C] Note C
VPWM_EN	PWM Signal Voltage	High	2.0	3.3	3.6	V	-
		Low	0	-	0.5	V	
FPWM	Output PWM frequency		-	200	1K	Hz	-
VLED_EN	LED enable Voltage	High	2.0	3.3	3.6		-
		Low	0	-	0.5	V	
PWM	PWM Duty ratio		5	-	100	%	-

Note A: A higher LED power supply voltage will result in better power efficiency. Keep the $V_{\_LED}$ between 12V and 21V is strongly recommended.

Note B: Calculator value for LED chip specification.

Note C: The lifetime of LED is defined as the time when LED packages continue to operate under the conditions at Ta = 25℃ and I_F= 20 mA (per chip) until the brightness becomes≦50% of its original value.

Note D: All values are measured at condition of $V_{\_LED}$ =12V、Ta=25℃ and 55%RH.

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6.0 Electrical Characteristics

6.1 Interface Connector

Table 4 Connector Name / Designation

Manufacturer	UJU (or equivalent)
Type / Part Number	IS050-L40B-C10
Mating Receptacle/Part Number	HS050-L40N-N10

Table 5 Signal Pin Assignment

Pin #	Signal Name	Description	Remarks
1	NC	Not connected	
2	VDD	Power supply	3.3V(Typ.)
3	VDD	Power supply	3.3V(Typ.)
4	VEDID	EDID Power	3.3V(Typ.)
5	NC	Not connected(Reserve)	
6	SCLK_EDID	EDID Clock Input	
7	SDAT_EDID	EDID Data Input	
8	Rin0-	−LVDS differential data input(R0-R5,G0)	
9	Rin0+	+LVDS differential data input(R0-R5,G0)	
10	GND	Ground	
11	Rin1-	−LVDS differential data input(G1-G5,B0-B1)	
12	Rin1+	+LVDS differential data input(G1-G5,B0-B1)	
13	GND	Ground	
14	Rin2-	−LVDS differential data input(B2-B5,HS,VS,DE)	
15	Rin2+	+LVDS differential data input(B2-B5,HS,VS,DE)	
16	GND	Ground	
17	RX_OCLK-	−LVDS differential clock input	
18	RX_OCLK+	+LVDS differential clock input	
19	NC	Not connected(Reserved for Color Engine)	
20	NC	Not connected	
21	NC	Not connected	
22	GND	Ground-Shield	
23	NC	Not connected	
24	NC	Not connected	
25	GND	Ground-Shield	

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26	NC	Not connected	
27	NC	Not connected	
28	GND	Ground-Shield	
29	NC	Not connected	
30	NC	Not connected	
31	VLED_GND	LED Ground	
32	VLED_GND	LED Ground	
33	VLED_GND	LED Ground	
34	NC	Not connected	
35	VPWM_EN	System PWM Logic Input Level	
36	VLED_EN	LED enable Input Level	3.3V(Typ.)
37	NC	Not connected（Reserved for DBC）	
38	VLED	LED Power Supply 6～21V	12V(Typ.)
39	VLED	LED Power Supply 6～21V	12V(Typ.)
40	VLED	LED Power Supply 6～21V	12V(Typ.)

Note: All input signals shall be low or Hi-Z state when VDD is off.

6.2 LVDS Receiver

6.2.1 Signal Electrical Characteristics for LVDS Receiver

The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644) standard.

Table 6 LVDS Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Conditions
Differential Input High Threshold	Vth	-	-	+100	mV	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100	-	-	mV	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100	-	600	mV	
Common Mode Voltage	Vcm	0.9	1.2	1.5	V	
Common Mode Voltage Offset	ΔVcm	-	-	50	mV	Vcm=+1.2V

Note:

A. Input signals shall be low or Hi-Z state when VDD is off.

B. All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

Note: All values are at VDD=3.3V, Ta=25 degree C.

Figure 7 Voltage Definitions

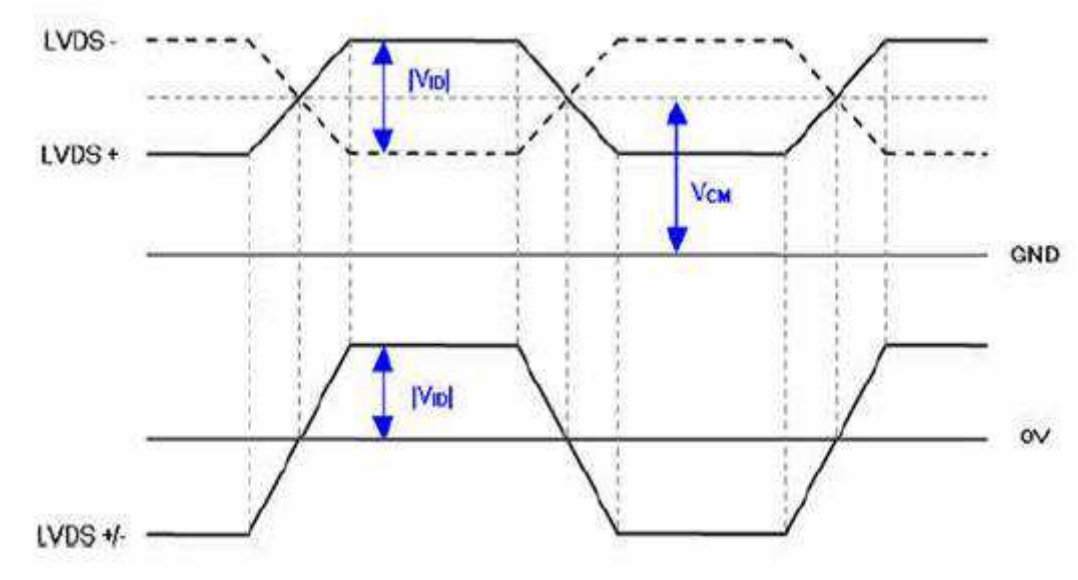


Figure 8 Measurement System

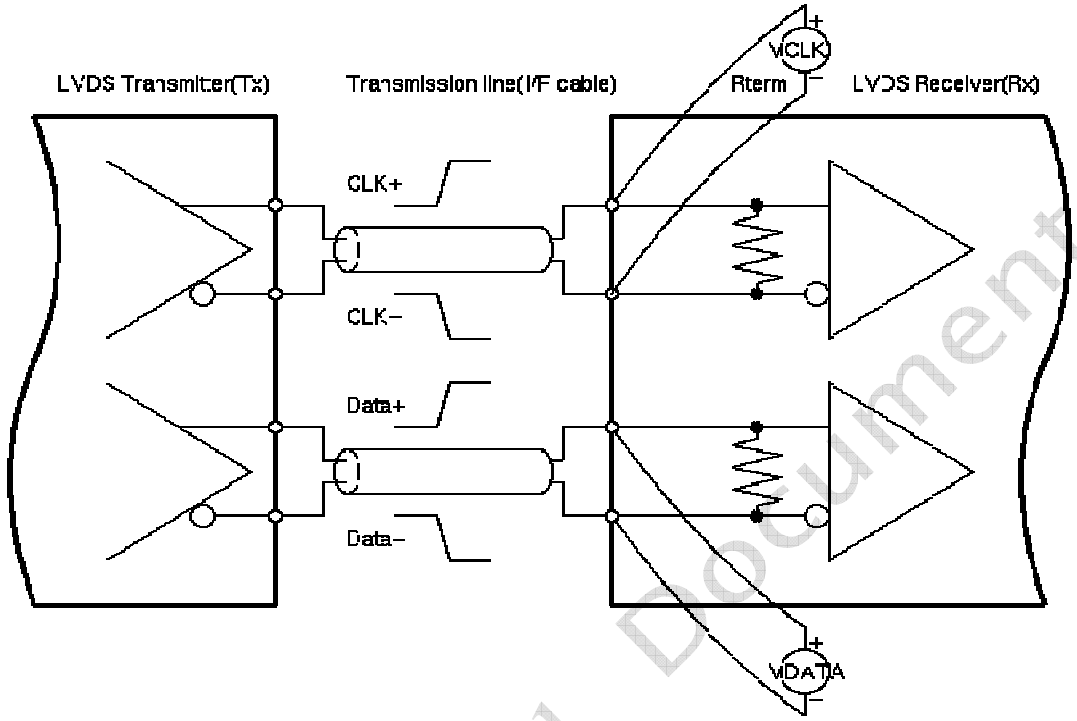
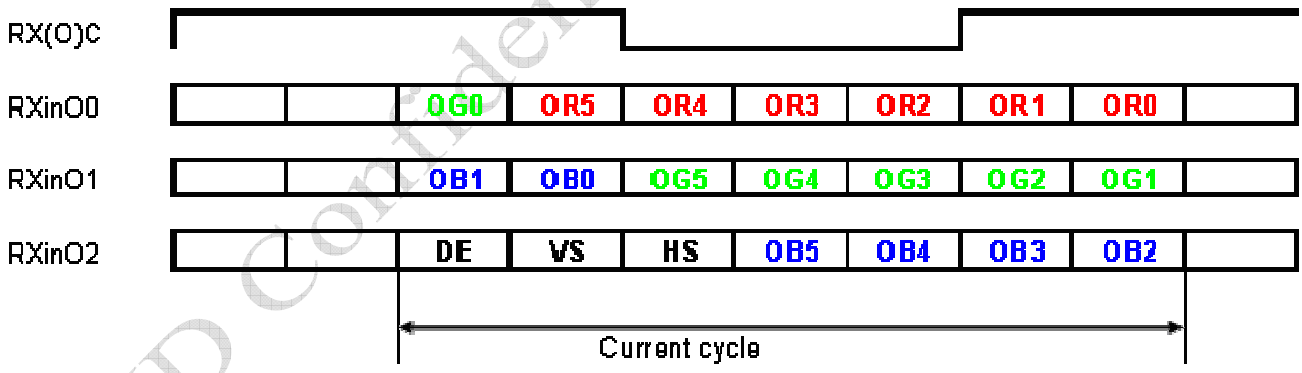


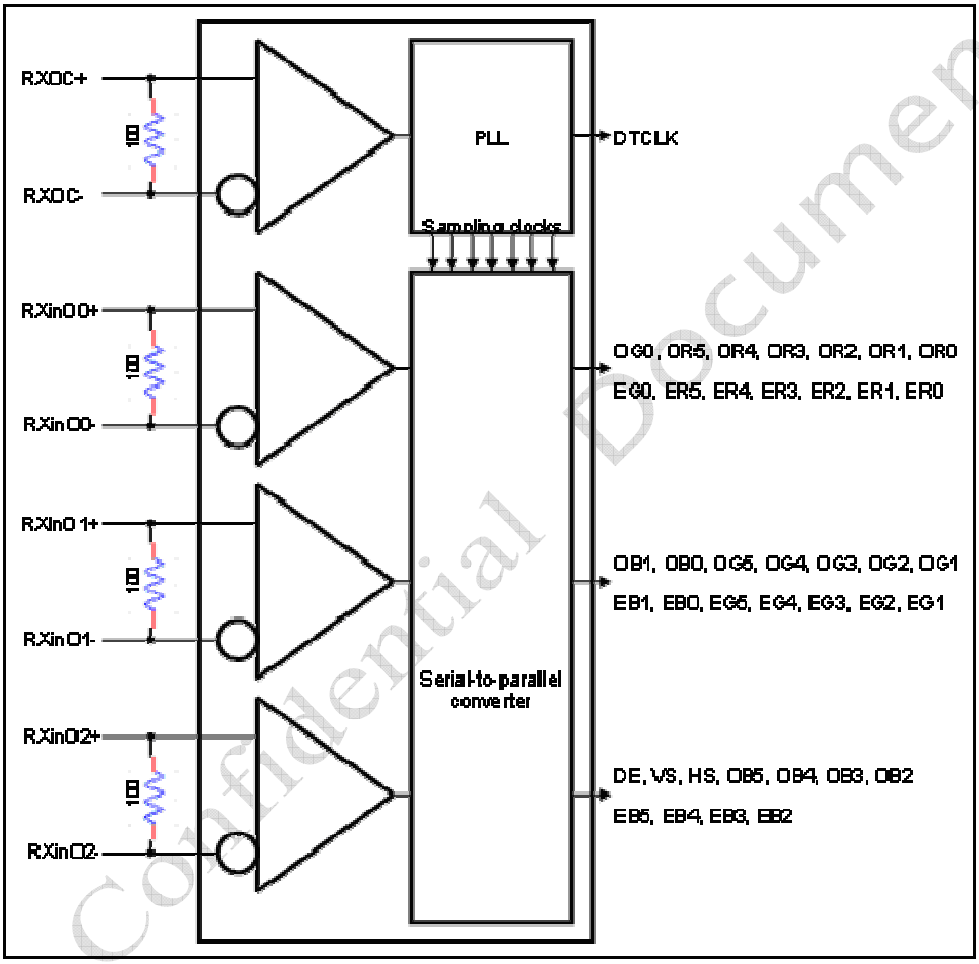
Figure 9 Data mapping



6.2.2 LVDS Receiver Internal Circuit

Figure 10 LVDS Receiver Internal Circuit shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

Figure 10 LVDS Receiver Internal Circuit



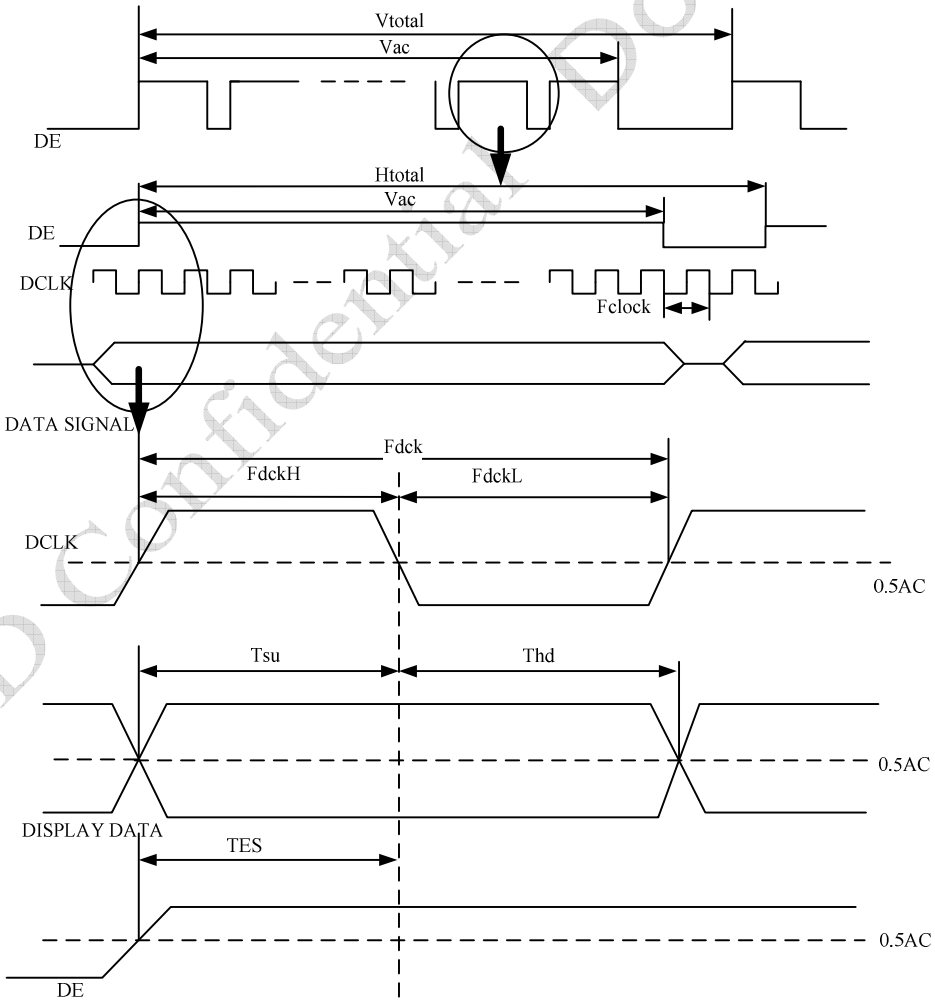
7.0 Interface Timings

7.1 Timing Characteristics

Table 7 Interface Timings

Parameter	Symbol	Unit	min	Typ.	Max
LVDS Clock Frequency(single)	F_{dck}	MHz	65.88	76.85	82.67
H Total Time	H_{total}	clocks	1520	1560	1690
H Active Time	H_{ac}	clocks	1366	1366	1366
V Total Time	V_{total}	lines	788	821	850
V Active Time	V_{ac}	lines	768	768	768
Frame Rate	V_{sync}	Hz	55	60	65

Figure 11 Timing Characteristics



Note: TES is data enable signal setup time.

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8.0 Power Consumption

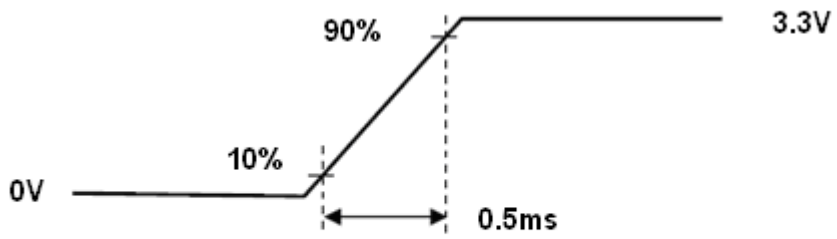
Input power specifications are as follows.

Table 8 Power Consumption

Symbol	Parameter	Min	Typ.	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[V]	-
IDD	VDD Current	-	280	340	[mA]	Black pattern, 60Hz
PDD	VDD Power	-	-	1.2	[W]	Black pattern, 60Hz
Irush	Rush Current	-	-	2	[A]	Note A
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	300	[mVp-p]	-

Note: A. Measure Condition

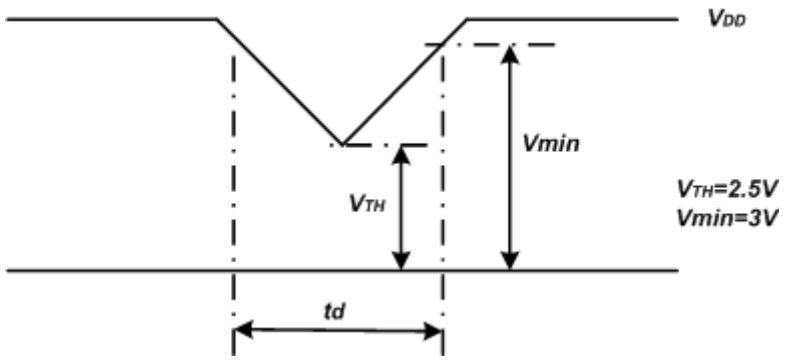
Figure 12 VDD rising time



VDD rising time

B.VDD Power Dip Condition

Figure 13 VDD Power Dip



If $V_{TH} < V_{DD} \leqslant Vmin$，then $t_d \leqslant 10ms$；when the voltage return to normal our panel must revive automatically.

9.0 Power ON/OFF Sequence

VDD power, interface signals, and lamp on/off sequence are shown in .Signals shall be Hi-Z state or low level when VDD is off.

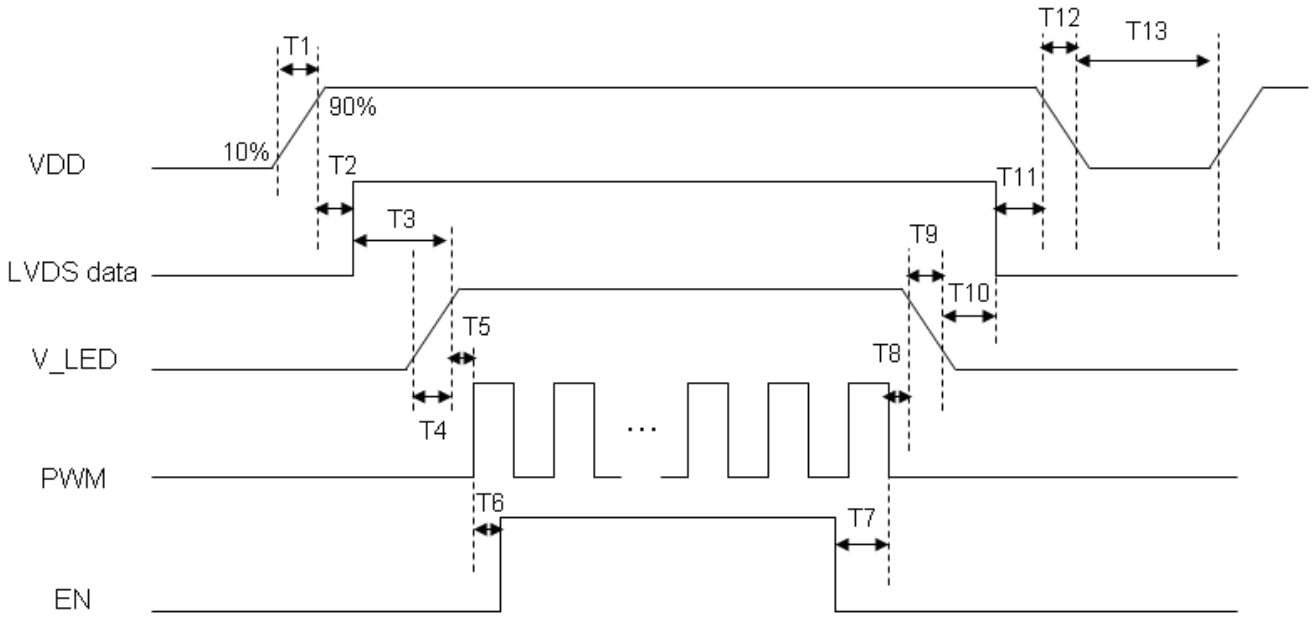


Table 9 Power Sequencing Requirements

Parameter	Symbol	Unit	min	typ	max
VDD Rise Time	T1	ms	0.5	--	10
VDD Good to Signal Valid	T2	ms	30	--	90
Signal Valid to Backlight On	T3	ms	200	--	--
Backlight Power On Time	T4	ms	0.5	--	--
Backlight VDD Good to System PWM On	T5	ms	10	--	--
System PWM ON to Backlight Enable ON	T6	ms	10	--	--
Backlight Enable Off to System PWM Off	T7	ms	0	--	--
System PWM Off to B/L Power Disable	T8	ms	10	--	--
Backlight Power Off Time	T9	ms	--	10	30
Backlight Off to Signal Disable	T10	ms	200	--	--
Signal Disable to Power Down	T11	ms	0	--	50
VDD Fall Time	T12	ms	--	10	30
Power Off	T13	ms	500	--	--

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10.0 Mechanical Characteristics

Figure 14 Reference Outline Drawing (Front Side)

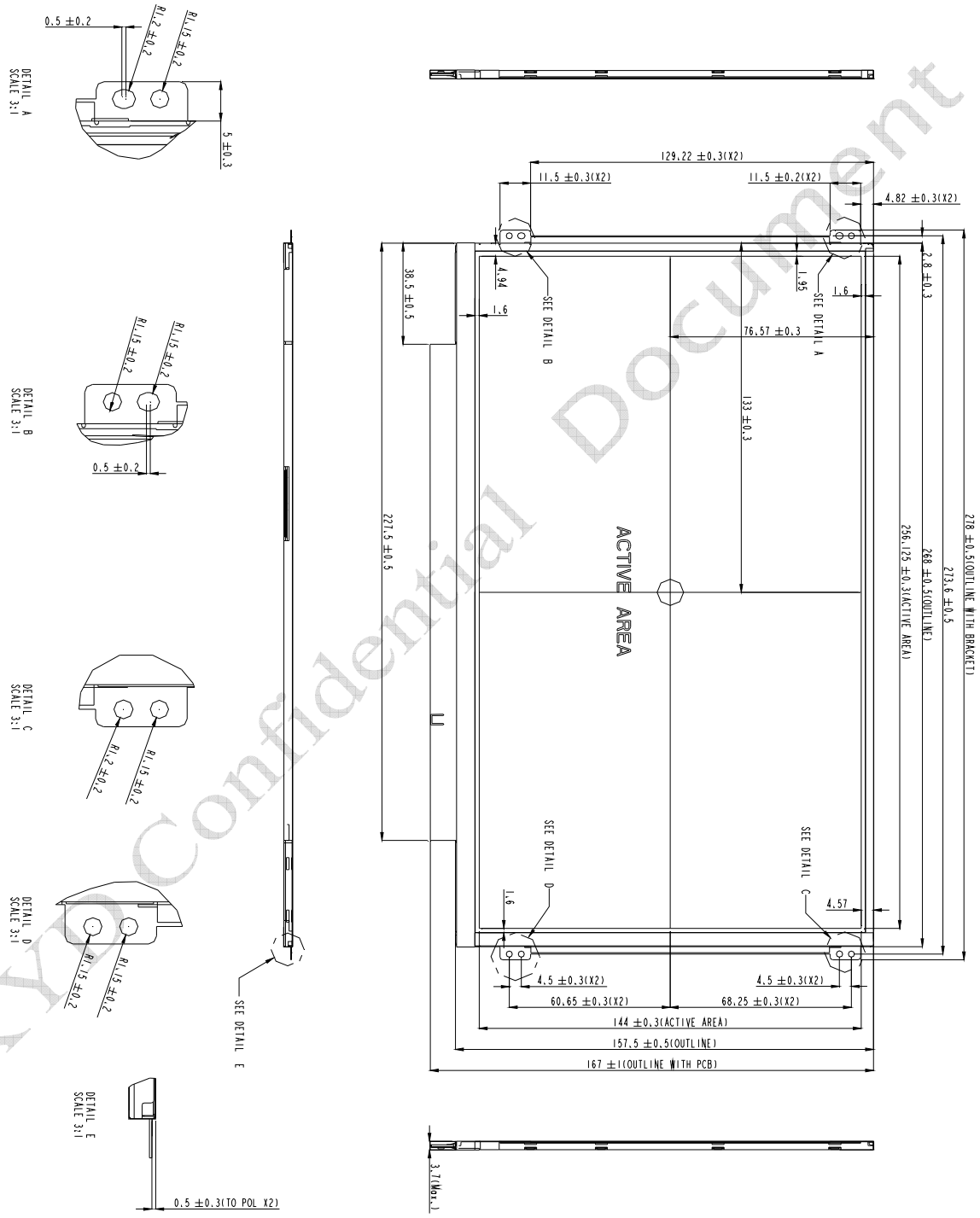
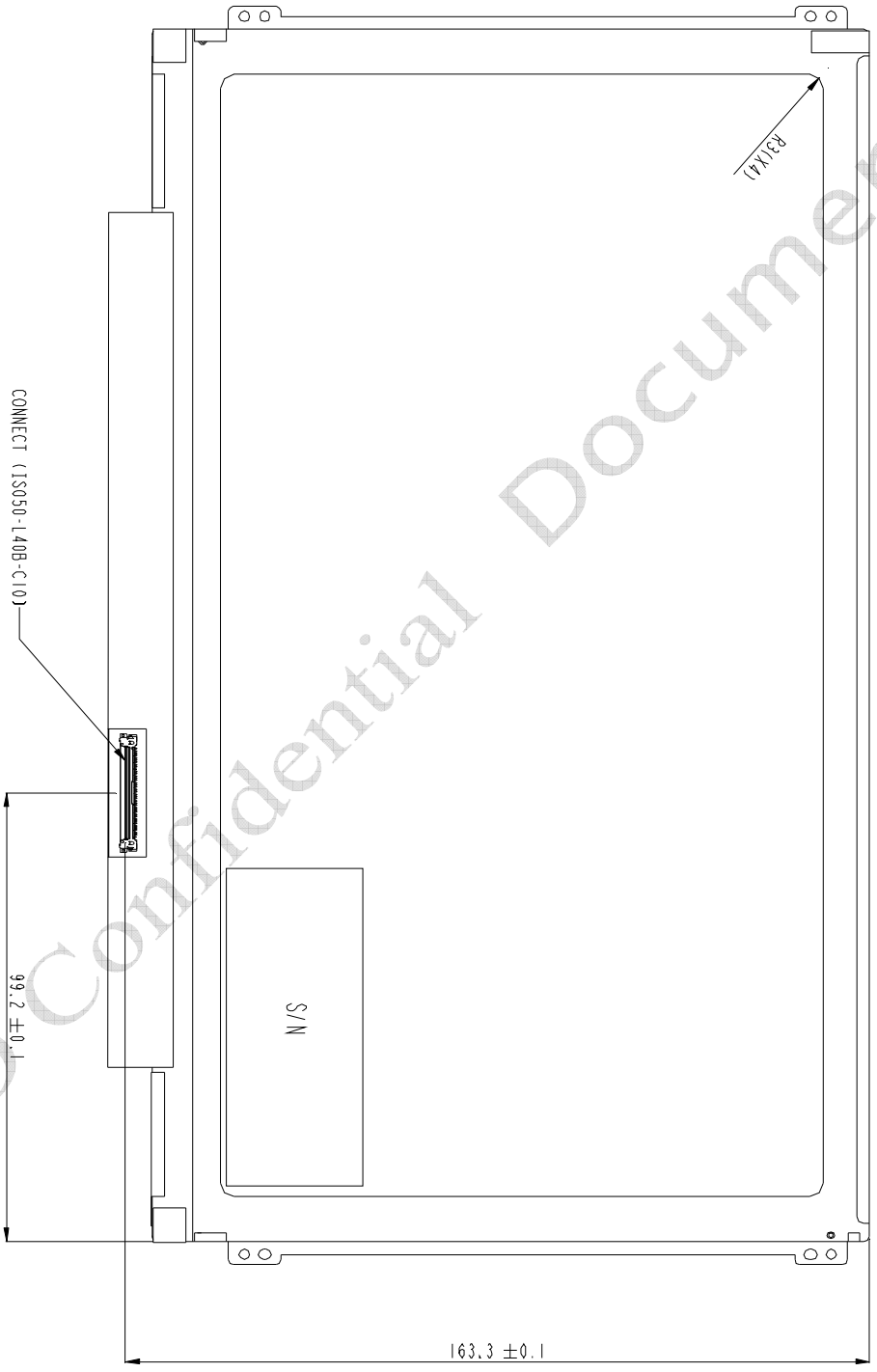


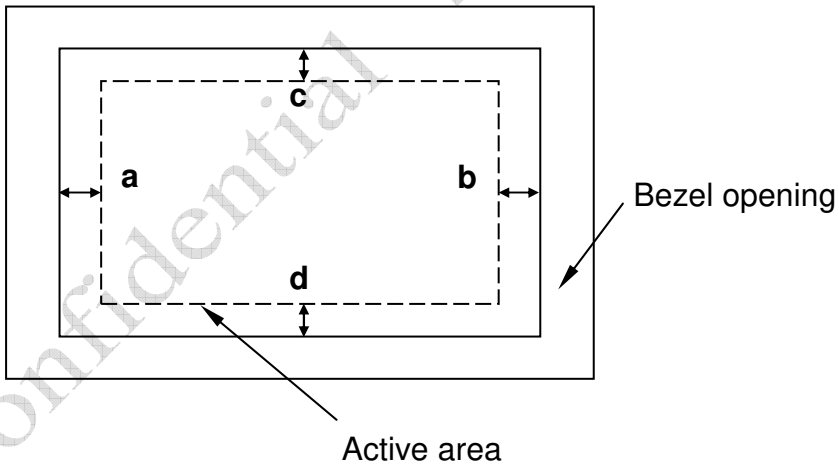
Figure15 Reference O Outline Drawing (Back Side)



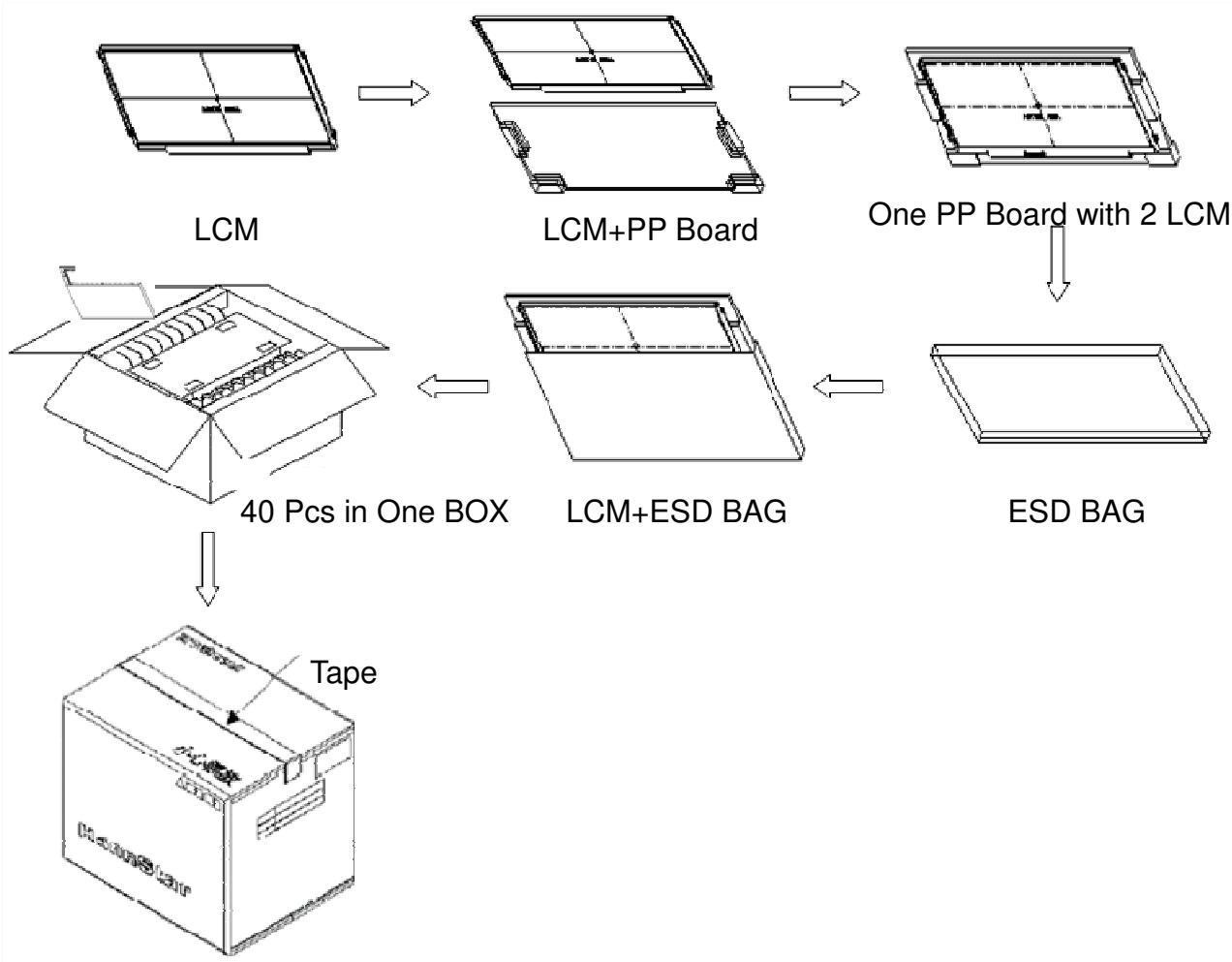
10.1 Dimension Specifications

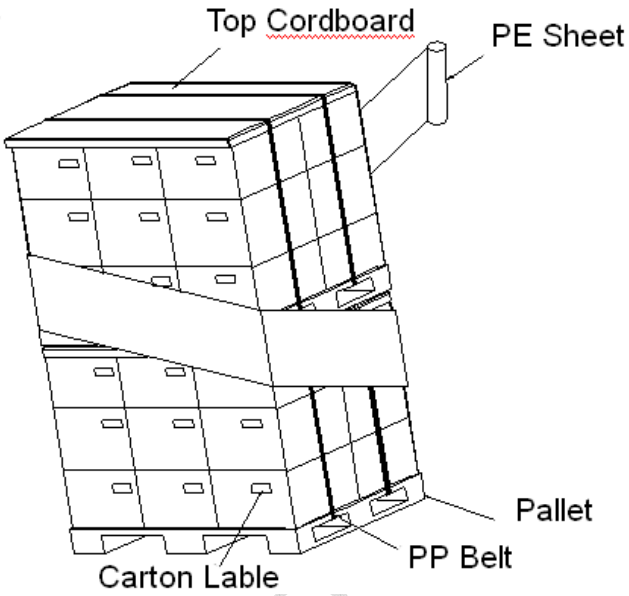
Table 10

Width [mm]		278.0±0.5
Height [mm]		167.0±1.0
Thickness [mm]		3.7 (max)
Tape Opening [mm]	X	259.675±0.3
	Y	147.200±0.3
Weight [g]		235 (max)
BM Width [mm]	| a-b | & | c-d |	≤1.0

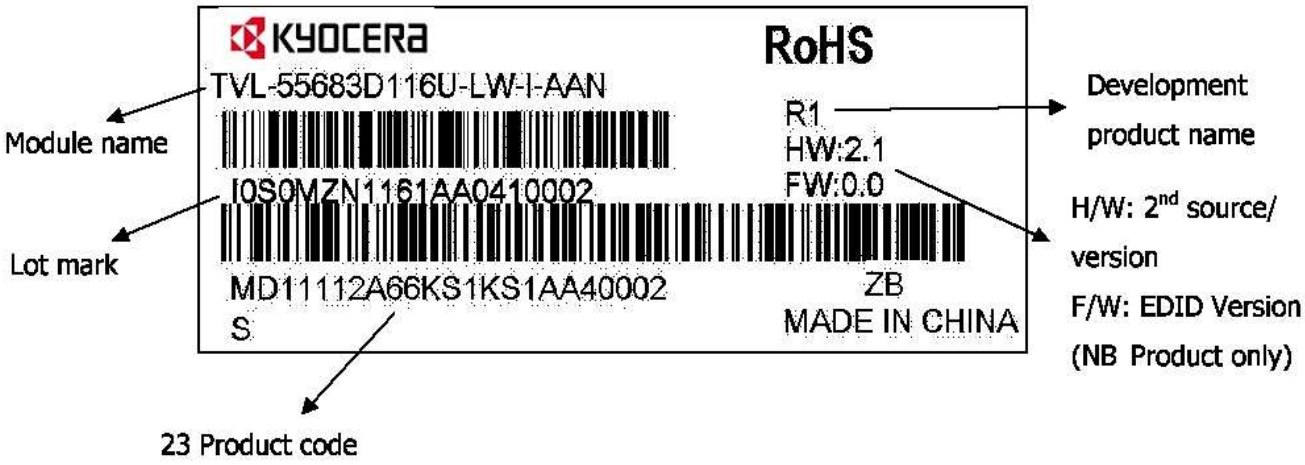


11.0 Package Specification





12.0 Lot Mark



12.1 Lot Mark

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

code 1,2,4,5,6,7,8,9,10,11,16: KYOCERA DISPLAY internal flow control code.
code 3: production location.
code 12: production year.
code 13: production month.
code 14,15: production date.