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TW2802/4 Multiple Video Decoder

For Security Applications

Preliminary Data Sheet from Techwell, Inc.

Information may change without notice

Disclaimer

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Introduction and Features

The TW280X includes four high quality NTSC/ PAL video decoders, which convert analog composite to digital component YCbCr for security application. The TW280X contains four 10-bit A/D and proprietary digital gain/clamp controllers and utilizes proprietary techniques for separating luminance & chrominance to reduce both cross-luminance and cross-chrominance artifacts. The high performance dual scalers in each channel offer two differently scaled video outputs with 54MHz ITU-R BT.656 format for security system design. Four built-in motion detectors can also increase the feature of security system.

Features

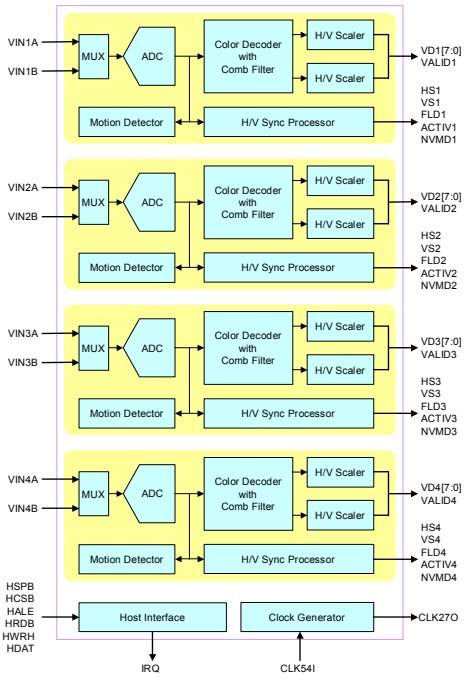
- Accepts all NTSC (M/N/4.43) / PAL (B/D/G/H/I/K/L/M/N/60) standard formats with auto detection
- Four 10-bit video CMOS analog to digital converters
- Adjust video level with proprietary automatic clamp and gain control system
- Proprietary architecture for locking to weak, noisy, or unstable signals
- High performance adaptive comb filters for all NTSC/PAL standards
- IF compensation filter for improvement of color demodulation
- PAL delay lines for correcting PAL phase errors
- Programmable hue, saturation, contrast, brightness and sharpness
- Dual high quality horizontal and vertical down scaler for each channel
- Four built-in motion detectors for security system
- Supports the standard ITU-R BT.656 / 8bit ITU-R BT.601 format
- Supports two differently scaled output mode with 54MHz ITU-R BT.656 format
- Supports a two-wire serial or parallel interface
- Low power consumption
- 128 PQFP package

Applications

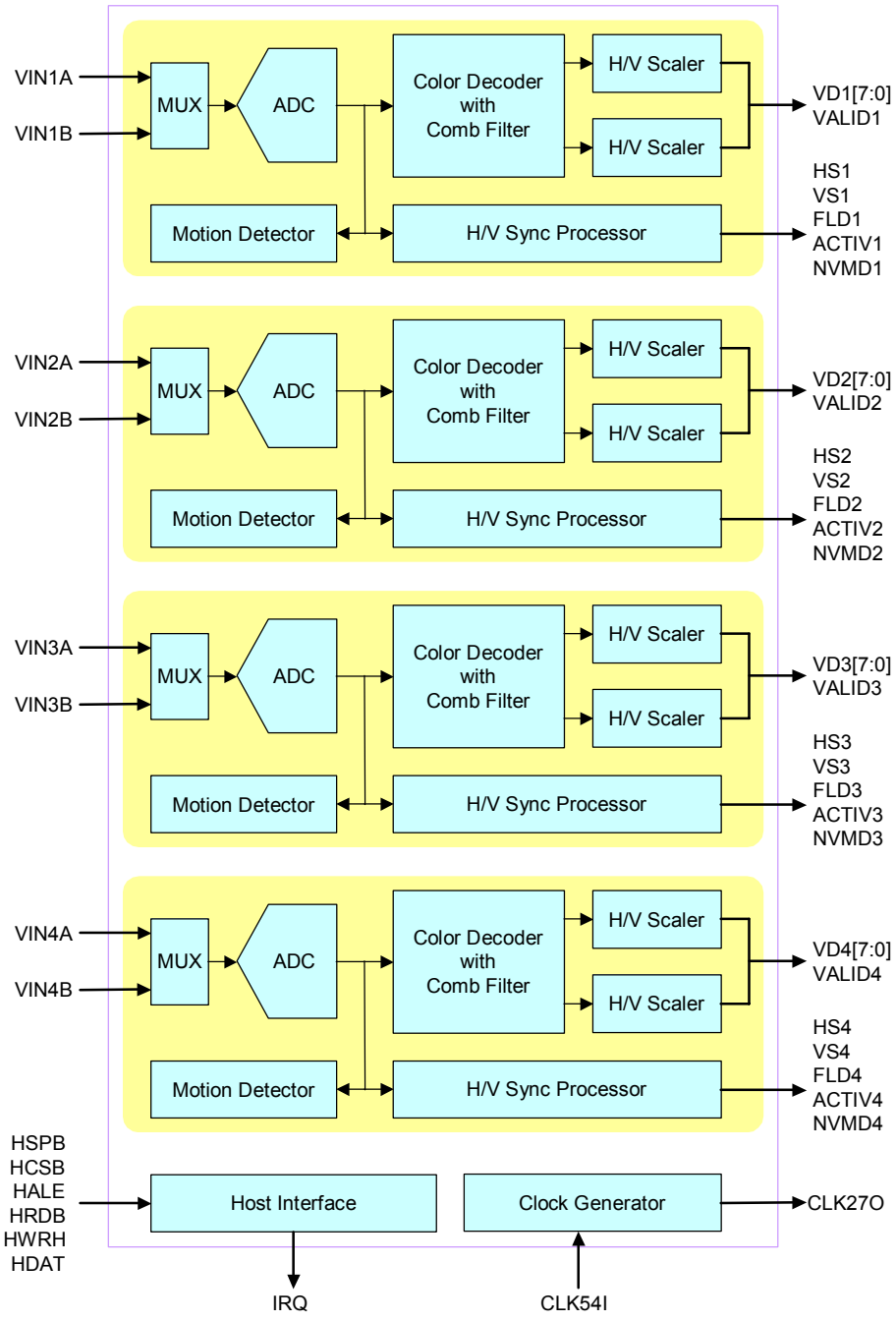
Security systems

Device Options

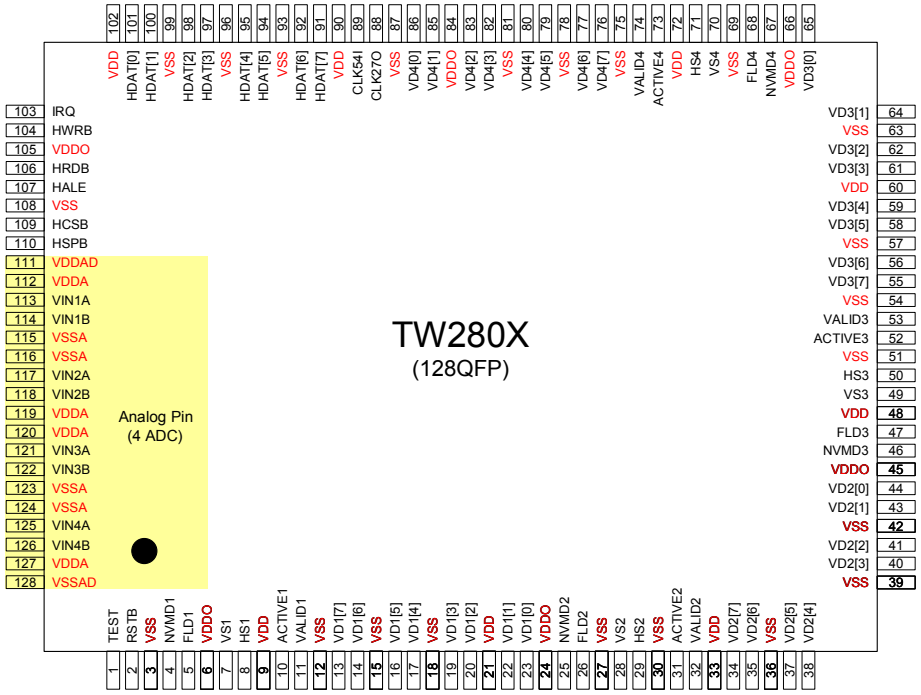
Device Name	Features
TW2802	2 Channel Video Decoder
TW2804	4 Channel Video Decoder



Block Diagram



Pin Diagram



Pin Description

Analog Interface Pins

Name	Number	Type	Description
VIN1A	113	A	Composite video input A of Channel 1. Must be connected through 2.2uF cap to input.
VIN1B	114	A	Composite video input B of Channel 1. Must be connected through 2.2uF cap to input.
VIN2A	117	A	Composite video input A of Channel 2. Must be connected through 2.2uF cap to input.
VIN2B	118	A	Composite video input B of Channel 2. Must be connected through 2.2uF cap to input.
VIN3A	121	A	Composite video input A of Channel 3. Must be connected through 2.2uF cap to input.
VIN3B	122	A	Composite video input B of Channel 3. Must be connected through 2.2uF cap to input.
VIN4A	125	A	Composite video input A of Channel 4. Must be connected through 2.2uF cap to input.
VIN4B	126	A	Composite video input B of Channel 4. Must be connected through 2.2uF cap to input.

Digital Data Interface Pins

Name	Number	Type	Description
VD1 [7:0]	13,14,16,17, 19,20,22,23	O	Dual scaled video data output for channel 1.
VD2 [7:0]	34,35,37,38, 40,41,43,44	O	Dual scaled video data output for channel 2.
VD3 [7:0] *	55,56,58,59, 61,62,64,65	O	Dual scaled video data output for channel 3.
VD4 [7:0] *	76,77,79,80, 82,83,85,86	O	Dual scaled video data output for channel 4.
VALID1	11	O	Valid data indicator for channel 1.
VALID2	32	O	Valid data indicator for channel 2.
VALID3*	53	O	Valid data indicator for channel 3.
VALID4*	74	O	Valid data indicator for channel 4.
HS1	8	O	Horizontal sync output for channel 1.
HS2	29	O	Horizontal sync output for channel 2.
HS3*	50	O	Horizontal sync output for channel 3.
HS4*	71	O	Horizontal sync output for channel 4.
VS1	7	O	Vertical sync output for channel 1.
VS2	28	O	Vertical sync output for channel 2.
VS3*	49	O	Vertical sync output for channel 3.
VS4*	70	O	Vertical sync output for channel 4.
FLD1	5	O	Even/odd field flag output for channel 1.
FLD2	26	O	Even/odd field flag output for channel 2.
FLD3*	47	O	Even/odd field flag output for channel 3.
FLD4*	68	O	Even/odd field flag output for channel 4.
ACTIVE1	10	O	Active flag output for channel 1.
ACTIVE2	31	O	Active flag output for channel 2.
ACTIVE3*	52	O	Active flag output for channel 3.
ACTIVE4*	73	O	Active flag output for channel 4.
NVMD1	4	O	Video loss or Motion detection flag for channel 1.
NVMD2	25	O	Video loss or Motion detection flag for channel 2.
NVMD3*	46	O	Video loss or Motion detection flag for channel 3.
NVMD4*	67	O	Video loss or Motion detection flag for channel 4.

Notes: * Disabled for TW2802

System Control Pins

Name	Number	Type	Description
RSTB	2	I	System reset.
CLK54I	89	I	54MHz system clock input.
CLK27O	88	O	27MHz Clock output.
TEST	1	I	Test pin. Connect to ground.
HSPB	110	I	Select Serial/Parallel host interface.
HCSB	109	I	Chip select for parallel interface. Slaver address [0] for serial interface.
HALE	107	I	Address line enable for parallel interface. Serial clock for serial interface.
HRDB	106	I	Read enable for parallel interface. Ground for serial interface.
HWRB	104	I	Write enable for parallel interface. Ground for serial interface.
HDAT [7:0]	91,92,94,95, 97,98,100,101	I/O	Data bus for parallel interface. HDAT [7] is serial data for serial interface. HDAT [6:1] is slaver address [6:1] for serial interface. HCSB is slaver address [0].
IRQ	103	O	Interrupt request by video loss and Motion detection

Power/Ground Pins

Name	Number	Type	Description
VDD	9,21,33,48,60, 72,90,102	P	Digital power for internal logic. 2.5V.
VDDO	6,24,45, 66,84,105	P	Digital power for output driver. 3.3V.
VSS	3,12,15,18, 27, 30,36,39,42,51, 54,57,63,69,75, 78,81,87,93,96, 99,108	G	Digital ground.
VDDA	112,119,120,127	P	Analog power. 2.5V.
VSSA	115,116,123,124	G	Analog ground.
VDDAD	111	P	Analog digital power. 2.5V.
VSSAD	128	G	Analog digital ground.

Functional Description

Video Input Formats

The TW280X supports all NTSC/PAL standard formats and has built-in automatic standard detection circuit. The following Table 1 shows the identified standards. Automatic standard detection can be overridden by writing the value into the IFMTMAN and IFORMAT register (0x01, 0x41, 0x81, 0xC1). Even in no-video status, the device can be forced to free-run in a particular video standard mode for fast locking by programming IFORMAT register.

Table 1 Input Video Format Supported

Format	Line/Fv (Hz)	Fh (KHz)	Fsc (MHz)
NTSC-M* NTSC-J	525/59.94	15.734	3.579545
NTSC-4.43*	525/59.94	15.734	4.43361875
NTSC-N	625/50	15.625	3.579545
PAL-BDGHI PAL-N*	625/50	15.625	4.43361875
PAL-M*	525/59.94	15.734	3.57561149
PAL-NC	625/50	15.625	3.58205625
PAL-60	525/59.94	15.734	4.43361875

Notes: * 7.5 IRE Setup

Analog-to-Digital Converter

The TW280X contains four 10-bit Analog to Digital converters that digitizes the analog video inputs. As the inputs are digitized at greater than two times that of the Nyquist sampling rate, only simple external anti-aliasing LPF are needed to prevent out-of-band frequencies. Each ADC has two analog switches that are controlled by ANA_SW (0x22, 0x62, 0xA2, 0xE2) registers. The A/D converters can also be put into power-down mode by the ADC_PWDN (0x78) registers.

Sync Processing

The sync processor of TW280X detects horizontal synchronization and vertical synchronization signals in the composite. The TW280X utilizes proprietary technology for locking to weak, noisy, or unstable signals such as those from on air signal and fast forward or backward of VCR system.

Video Level Adjustment

A patented digital gain and clamp control circuit restores the ac coupled video signal to a fixed dc level. The clamping circuit provides line-by-line restoration of the video pedestal level to a fixed dc reference voltage. In no AGC mode, the gain control circuit adjusts only the video sync gain to achieve desired sync amplitude so that the active video is bypassed regardless of the gain control. But when AGC mode is enabled, both active video and sync are adjusted by the gain control. The range of AGC is from –6dB to 18dB approximately.

Horizontal Sync Processing

The horizontal synchronization processing contains a sync separator, a PLL and the related decision logic. The horizontal sync separator detects the horizontal sync by examining low-pass filtered video input whose level is lower than a threshold. Additional logic is also used to avoid false detection on glitches. The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. In case the horizontal sync is missing, the PLL is on free running status that matches the standard raster frequency.

Vertical Sync Processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. The field status is determined at vertical synchronization time. When the location of the detected vertical sync is inline with a horizontal sync, it indicates a frame start or the odd field start. Otherwise, it indicates an even field.

Color Decoding

Decimation Filter

The digitized composite video data at 2X pixel clock rate first passes through decimation filter. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image. Fig 1 shows the characteristic of the decimation filter.

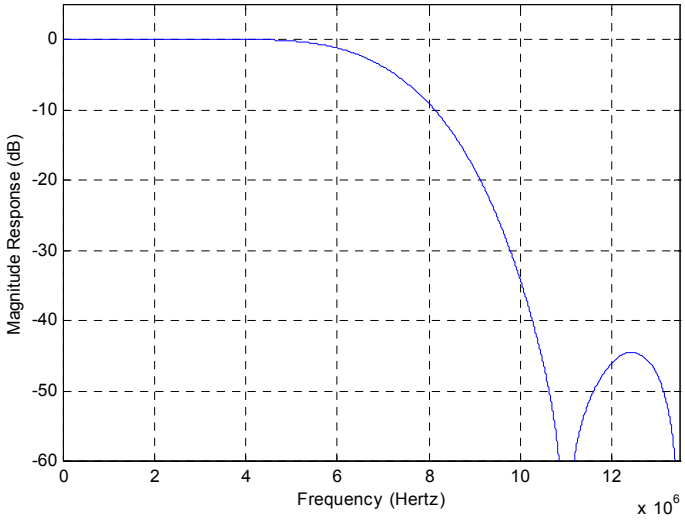


Fig 1 The Characteristic of the Decimation Filter

Y/C Separation

The adaptive comb filter is used for high quality luminance/chrominance separation from NTSC/PAL composite video signals. The comb filter improves the luminance resolution and reduces noise such as cross-luminance and cross-color. The adaptive algorithm eliminates most of errors without introducing new artifacts or noise. To accommodate some viewing preferences, additional chrominance trap filters are also available in the luminance path. Fig. 2 and Fig 3 show the frequency response of notch filter for each system NTSC and PAL.

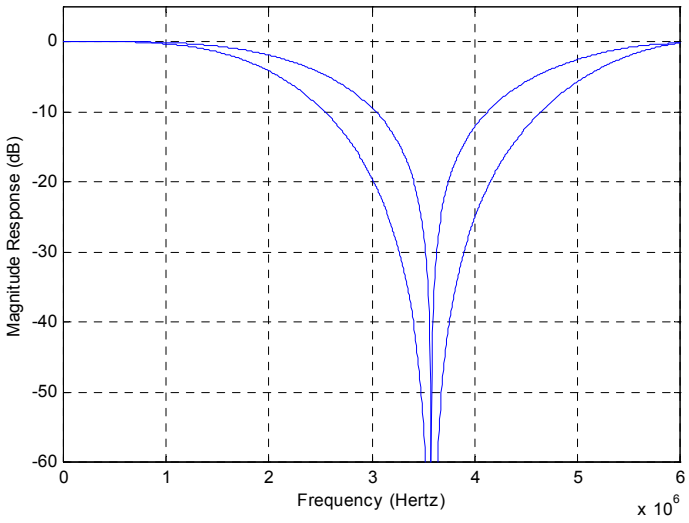


Fig. 2 The Characteristics of Luminance Notch Filter for NTSC

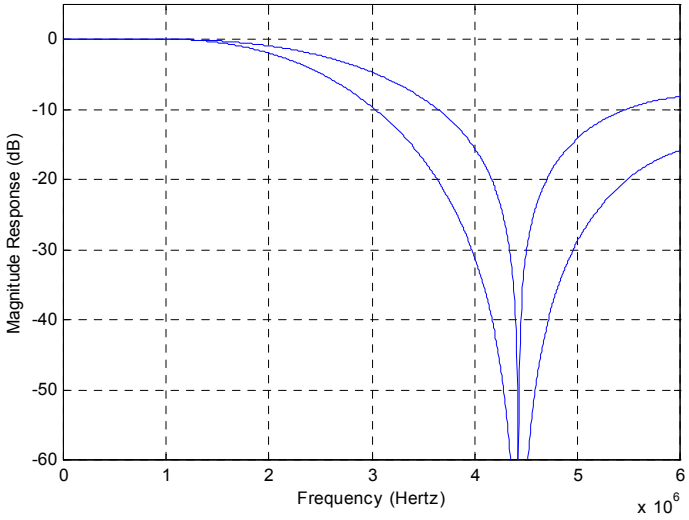


Fig 3 The Characteristics of Luminance Notch Filter for PAL

Luminance Processing

The luminance signal is separated by adaptive comb or trap filter is then fed to a peaking circuit. The peaking filter enhances the high frequency components of the luminance signal. Fig. 4 shows the characteristics of the peaking filter for four different gain modes. The picture contrast and brightness adjustment is provided through CONT (0x11, 0x51, 0x91, 0xD1) and BRT (0x12, 0x52, 0x92, 0xD2) registers. The contrast adjustment range is from approximately 0 to 200 percent, and the brightness adjustment is in the range of ±25 IRE. Moreover, a high frequency coring function is also embedded in TW280X to minimize a high frequency noise. The coring level is adjustable through the Y_H_CORE (0xF8) register.

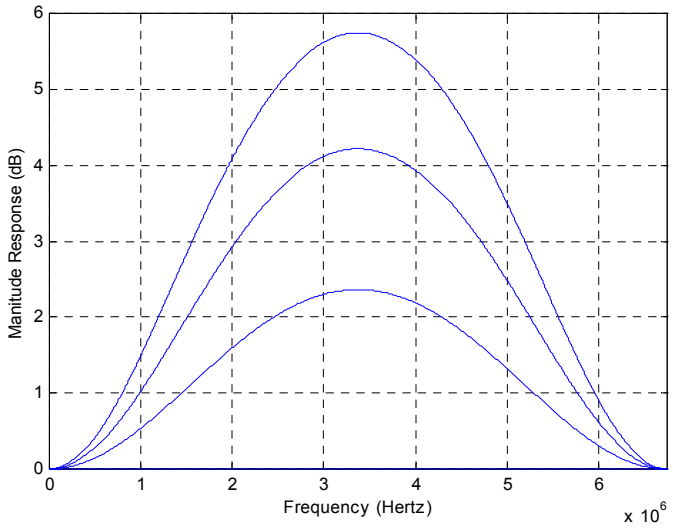


Fig. 4. The Characteristic of Luminance Peaking filter

Chrominance Processing

Chrominance Demodulation

The chrominance demodulation is done by first quadrature mixing for NTSC and PAL. The mixing frequency is equal to the sub-carrier frequency of NTSC and PAL. After the mixing, a LPF is used to remove 2X carrier signal and yield chrominance components. The LPF characteristic can be selected for optimized transient color performance. In case of a mistuned IF source, IF compensation filter makes up for any attenuation at higher frequencies or asymmetry around the color sub-carrier. The gain for the upper chrominance side band is controlled by IFCMP_MD (0x13, 0x53, 0x93, 0xD3) register. Fig. 5 and Fig. 6 show the frequency response of IF-compensation filter and chrominance LPF.

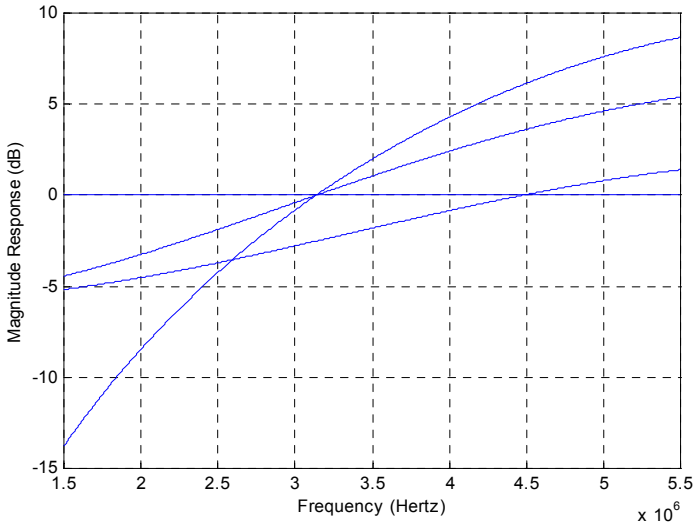


Fig. 5 The Characteristics of IF-compensation Filter

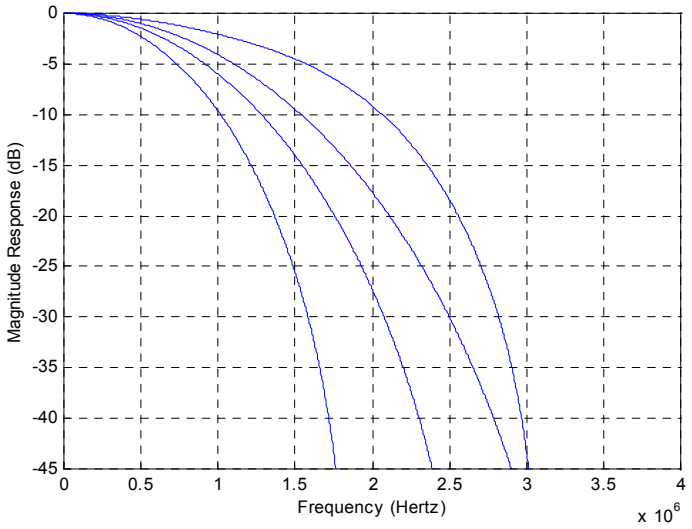


Fig. 6 The Characteristics of Chrominance Low Pass Filter

ACC (Automatic Color gain control)

The ACC (Automatic Color gain Control) compensates for reduced amplitudes caused by high frequency suppression in video signal. The range of ACC is from –6dB to 30dB approximately. For black & white video or very weak & noisy signals, the color will be off by the internal color killing circuit. The color killer function can also be always enabled or disabled by programming CKIL (0x14, 0x54, 0x94, 0xD4) register.

Chrominance Gain, Offset and Hue Adjustment

The color saturation can be adjusted by changing the register SAT (0x10, 0x50, 0x90, 0xD0). The Cb and Cr gain can be also adjusted independently by programming UGAIN (0x3C) and VGAIN (0x3D) register. Likewise, the Cb and Cr offset can be programmed through U_OFF (0x3E) and V_OFF (0x3F) registers. Hue control is achieved with phase shift of the digitally controlled oscillator. The phase shift can be programmed through HUE (0x0F, 0x4F, 0x8F, 0xCF) register.

Video Scaling and Cropping

The TW280X provides two methods to reduce the amount of video pixel data, scaling and cropping. The scaling function provides video image at lower resolution while the cropping function supplies only a portion of the video image.

Video Scaling

The TW280X includes a high quality horizontal and vertical down scaler. The video images can be downscaled in both horizontal and vertical direction to an arbitrary size. The luminance horizontal scaler includes an anti-aliasing filter to reduce image artifacts in the resized image and a 32 poly-phase filter to accurately interpolate the value of a pixel. This results in more aesthetically pleasing video as well as higher compression ratios in bandwidth-limited applications. Fig 7 shows the frequency response of anti-aliasing filter for horizontal scaling and Fig 8 shows the 32 poly-phase filter characteristics. Similarly, the vertical scaler also contains an anti-aliasing filter and 16 poly-phase filter for down scaling. The filter characteristics are shown in Fig. 9.

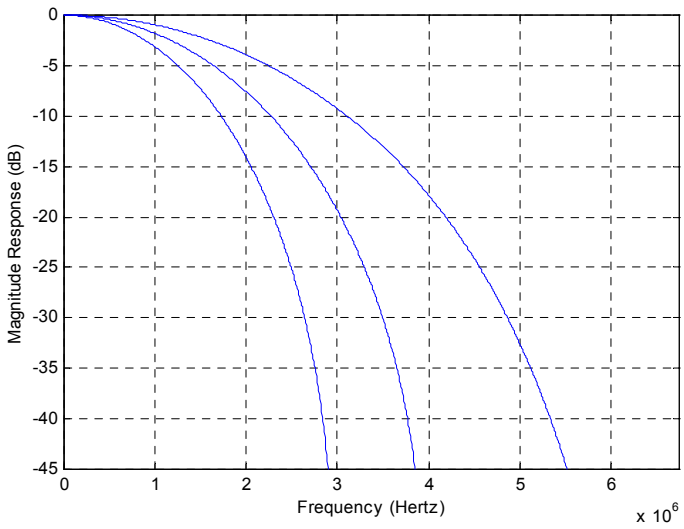


Fig 7 The Characteristics of Anti-aliasing filter for horizontal luminance scaling

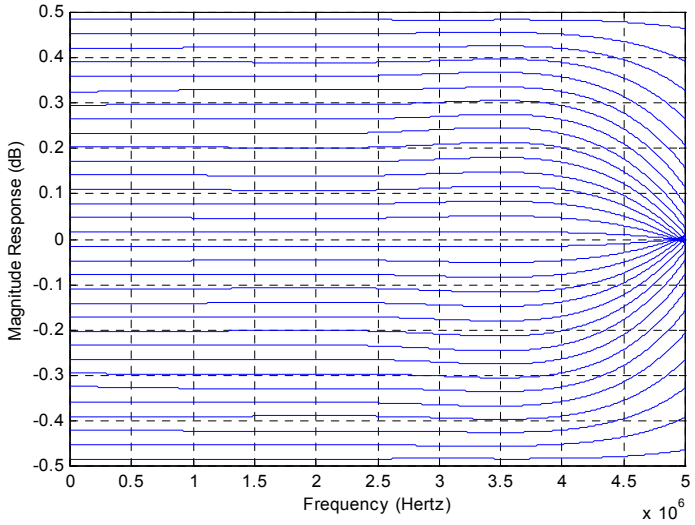


Fig 8 The Characteristics of Group delay for horizontal luminance scaling

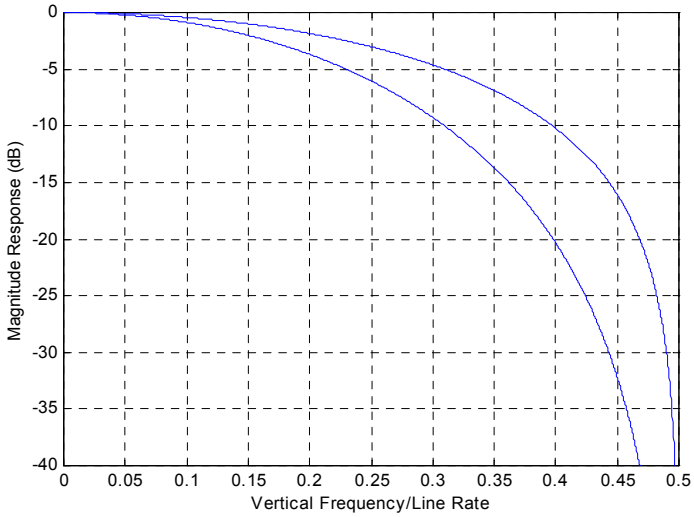


Fig. 9 The Characteristics of Anti-aliasing filter for vertical luminance scaling

Down scaling is achieved by programming the horizontal scaling register (HSCALE) and vertical scaling register (VSCALE). When no scaled video image, the TW280X will output the number of pixels per line as specified by the HACTIVE register. If the number of output pixels required is smaller than the number specified by the HACTIVE register, the 16bit HSCALE register is used to reduce the output pixels to the desired number.

Following equation is used to determine the horizontal scaling ratio to be written into the 16bit HSCALE register.

$$HSCALE = [N_{pixel\_desired} / HACTIVE] * (2^{16} - 1)$$

Where $N_{pixel\_desired}$ is the desired number of active pixels per line

For example, to scale full picture (HACTIVE is 720) to CIF (360 pixels), the HSCALE value can be found as:

$$HSCALE = [320/720] * (2^{16} - 1) = 0x7FFF$$

Following equation is used to determine the vertical scaling ratio to be written into the 16bit VSCALE register.

$$VSCALE = [N_{line\_desired} / VACTIVE] * (2^{16} - 1)$$

Where $N_{line\_desired}$ is the desired number of active lines per field

For example, to scale full picture (VACTIVE is 240or288) to CIF (120/144 lines), the VSCALE value can be found as:

$$VSCALE = [120 / 240] * (2^{16} - 1) = 0x7FFF \text{ for } 60Hz$$

$$VSCALE = [144 / 288] * (2^{16} - 1) = 0x7FFF \text{ for } 50Hz$$

The scaling ratios of popular case are listed in Table 2

Table 2 HSCALE and VSCALE value for some popular video formats

Scaling Ratio	Format	Output Resolution	HSCALE	VSCALE
1	NTSC PAL	720x480 720x576	0xFFFF 0xFFFF	0xFFFF 0xFFFF
1/2 (CIF)	NTSC PAL	360x240 360x288	0x7FFF 0x7FFF	0x7FFF 0x7FFF
1/4 (QCIF)	NTSC PAL	180x120 180x144	0x3FFF 0x3FFF	0x3FFF 0x3FFF

Video Cropping

The cropping function allows only subsection of a video image to be output. The active video region is determined by HDELAY, HACTIVE, VDELAY and VACTIVE register as illustrated in Fig 10. The first active line is defined by the VDELAY register and the first active pixel is defined by the HDELAY register. The VACTIVE register can be programmed to define the number of active lines in a video field, and the HACTIVE register can be programmed to define the number of active pixels in a video line.

The horizontal delay register HDELAY determines the number of pixel delays between the horizontal reference and the leading edge of the active region. The horizontal active register HACTIVE determines the number of active pixels to be processed. Note that these values are referenced to the pixel number before scaling. Therefore, even if the scaling ratio is changed, the active video region used for scaling remains unchanged as set by the HDEALY and HACTIVE register. In order for the cropping to work properly, the following equation should be satisfied.

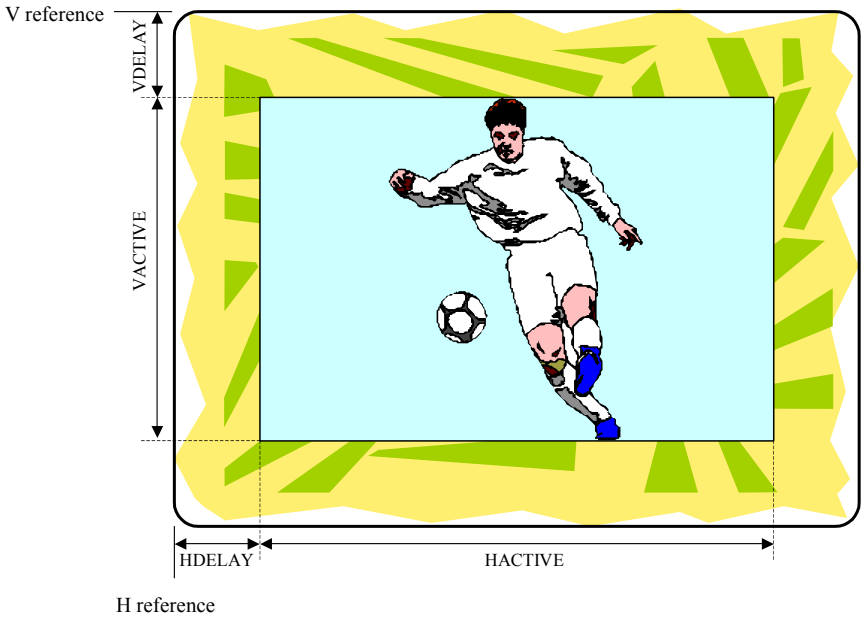
HDELAY + HACTIVE < Total number of pixels per line
Where the total number of pixels per line is 858 for 60Hz and 864 for 50Hz

To process full size region, the HDELAY should be set to 32 and HACTIVE set to 720 for both 60Hz and 50Hz system.

The vertical delay register (VDELAY) determines the number of line delays from the vertical reference to the start of the active video lines. The vertical active register (VACTIVE) determines the number of lines to be processed. These values are referenced to the incoming scan lines before the vertical scaling. In order for the vertical cropping to work properly, the following equation should be satisfied.

VDELAY + VACTIVE < Total number of lines per field
Where the total number of lines per field is 262 for 60Hz and 312 for 50Hz

To process full size region, the VDELAY should be set to 7 and VACTIVE set to 240 for 60Hz and the VDELAY should be also set to 4 and VACTIVE set to 288 for 50Hz.



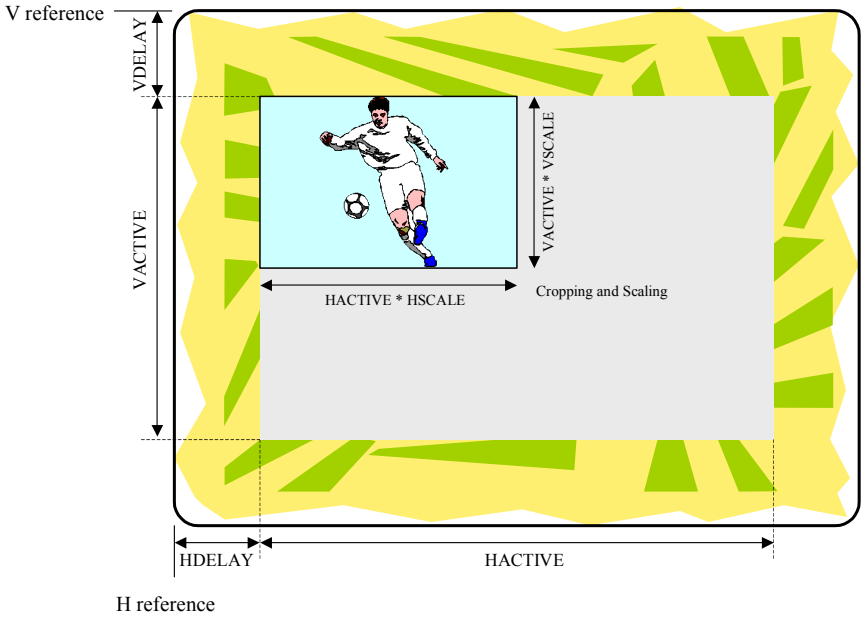


Fig 10 The Effect of Cropping and Scaling Active Registers

Motion Detector

The TW280X supports hardware motion detector for 4 channels individually. The motion detection algorithm built in the TW280X uses difference between two luminance levels of the adjacent two fields. Motion is detected for full screen image and each channel has 144(12x12) mask regions, which enable or disable motion detection for that region. The motion detection has several attributes, sensitivity and velocity of motion detector controlled by programming the register. The Host takes the result of motion detection via IRQ or NVMD pin. Refer to the host Interface for the detail.

Sensitivity Control

The motion detector has three sensitivity control parameters. One is level sensitivity control parameter (LVLSENS), another is spatial sensitivity control parameter (SPTSENS), and a third is temporal sensitivity control parameter (TMPSENS). The recommended values of sensitivity control parameters for a proper operation are listed in Table 3

LVLSENS (Level Sensitivity)

In built-in motion detection algorithm, motion is detected when luminance level difference between two fields is greater than the value, which is defined by LVLSENS. The smaller LVLSENS value makes the motion detector sense more sensitively, and the larger is the opposite. When LVLSENS is too small, the motion detector can be weak in noise.

SPTSENS (Spatial Sensitivity)

Motion detection from only luminance level difference between two fields is very weak in spatial random noise. To remove the fake motion detection from the random noise, spatial filter is used. SPTSENS adjusts the window size of the spatial filter to control the spatial sensitivity so that the large SPTSENS value increases the immunity of spatial random noise.

TMPSENS (Temporal Sensitivity)

Likewise, temporal filter is used to remove the fake motion detection from the temporal random noise. TMPSENS regulates the number of taps in the temporal filter to control the temporal sensitivity so that the large TMPSENS value increases the immunity of temporal random noise.

Table 3 The recommended values of sensitivity parameters for a proper operation

TMPSENS	SPTSENS	LVLSENS		
		More Sensitive		Less Sensitive
0	0	7	~	10
	1	3	~	9
	2	2	~	8
	3	2	~	7
1	0	3	~	9
	1	2	~	8
	2	2	~	7
	3	2	~	6
2	0	3	~	8
	1	2	~	7
	2	1	~	6
	3	1	~	5
3	0	3	~	7
	1	1	~	6
	2	1	~	5
	3	1	~	4

Velocity Control

Motion has various velocities. That is, in a fast motion an object appears and disappears rapidly between the adjacent fields while in a slow motion it is to the contrary. As the built-in motion detection algorithm uses the luminance level difference between two adjacent fields, a slow motion is inferior in detection rate to a fast motion. To compensate this weakness, the MDPERIOD parameter is used. MDPERIOD parameter adjusts the field interval in which the luminance level is compared. Thus, for detection of a fast motion a small value is needed and for a slow motion a large value is required. The parameter MDPERIOD value should be greater than TMPSENS value.

Mask Detection Region

The motion in the specific area can be ignored by the control of mask area. The full screen image is divided into 144 (12x12) mask areas. If the mask bit in specific area is programmed into high, the specific area is ignored in operation of motion detector, as illustrated in Fig. 11. But for proper operation, more than 4 mask areas should be enabled in any case.

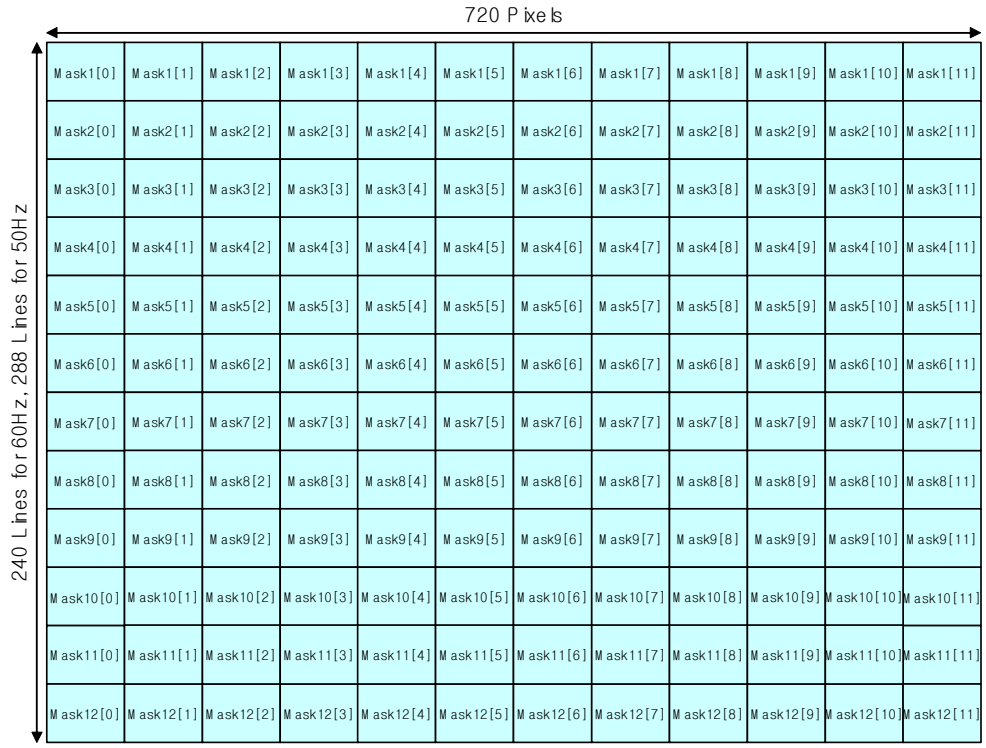


Fig. 11 Motion detection mask windows

Output Format

The TW280X supports three 8bit output formats, ITU-R BT.656, 8bit ITU-R BT.601 and Dual ITU-R BT.656 with 54MHz data format. The output data is synchronous with rising or falling edge of CLK27O for ITU-R BT.656 and 8bit ITU-R BT.601 format and with rising edge of CLK54I for Dual ITU-R BT.656 with 54MHz format. The polarity of CLK27O is controlled by the CK27O_POL register (0x3B). For Dual ITU-R BT.656 with 54MHz format, two kinds of scaled image are time-multiplexed with 54MHz. The output formats are selected by the OUT_FMT register (0x22, 0x62, 0xA2, 0xE2).

ITU-R BT.656 Format

In ITU-R BT.656 format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. During the blanking time, the YCbCr outputs have a value 0x00 for Y, Cr and Cb. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. If scaling is used, the number of active pixels per line is constant with invalid pixel indicated by the blanking code 0x00. The output timing is illustrated in Fig. 12. The SAV and EAV sequences are shown in Table 4. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the NOVID_656 bit (0x22, 0x62, 0xA2, 0xE2).

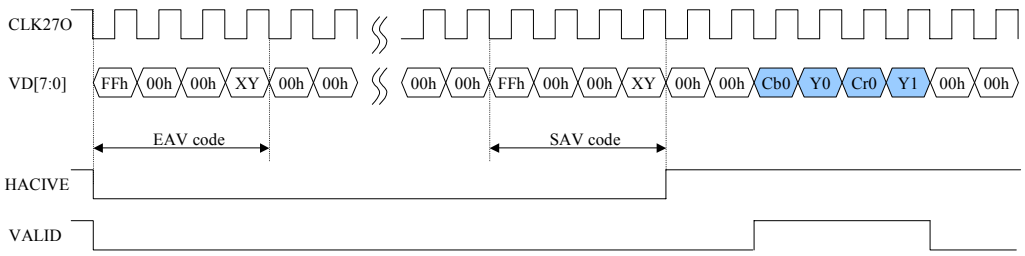


Fig. 12 Timing Diagram of ITU-R BT.656 format on HSCALE = 16'h7FFF

Table 4 ITU-R 656 SAV and EAV Code Sequence

Condition			656 FVH Value			SAV/EAV Code Sequence				
Field	Vertical	Horizontal	F	V	H	First	Second	Third	Fourth	
									Normal	Option (Novideo)
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

8-bit ITU-R BT.601 Format

8-bit ITU-R BT.601 format is 8-bit YCbCr 4:2:2 data stream with additional timing information such as syncs and field flag. The video output timing is illustrated in Fig 13 and Fig 14.

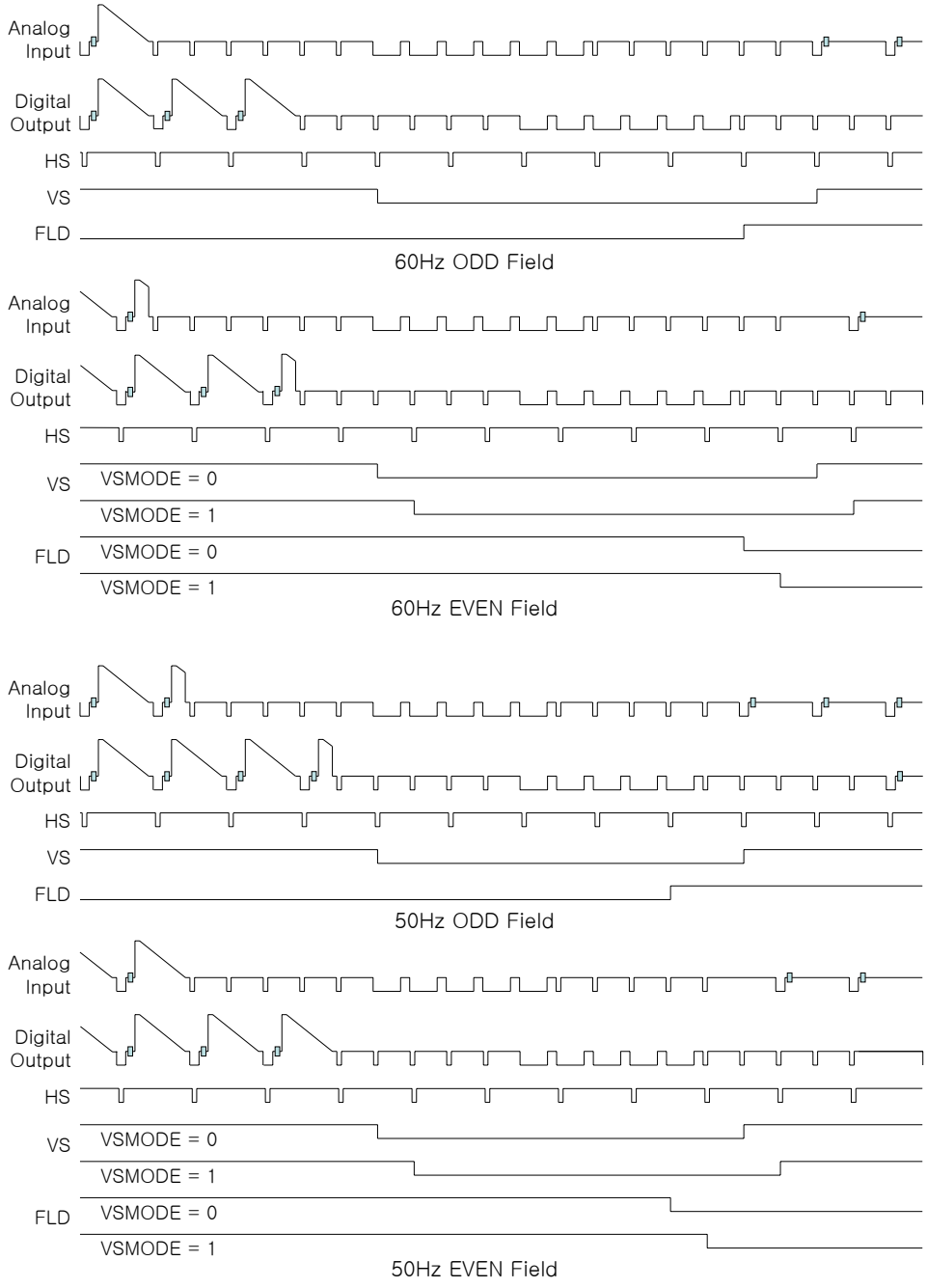
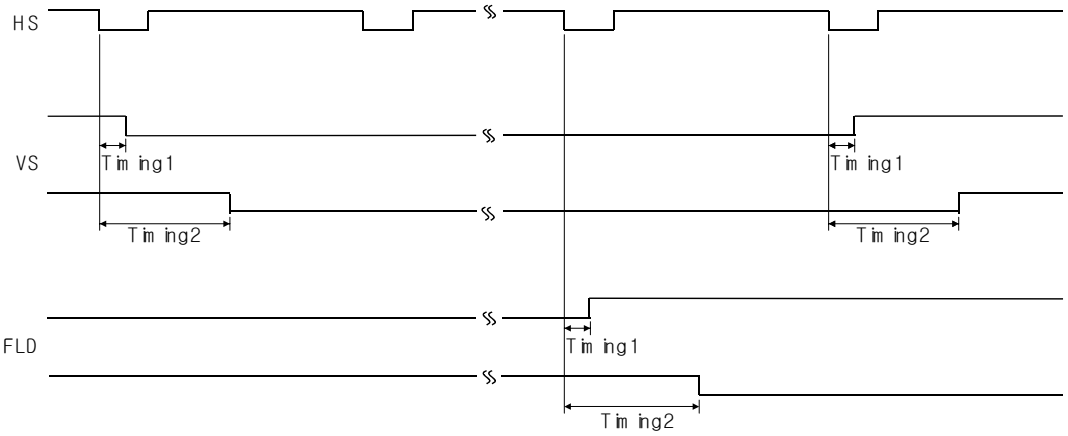


Fig 13 Vertical Timing for 60Hz / 50Hz Video



Timing1 : 40 system clock(54MHz) for the Even field with VSMODE=1 or Odd field
Timing2 : 1760 system clock(54MHz) for the Even field with VSMODE=0

Fig 14 Horizontal and Vertical Timing in Video Output

Dual ITU-R BT.656 Format in 54MHz

Dual ITU-R BT.656 format in 54MHz is very useful to the security applications, which need two independently scaled video images for display and record purpose. In the case of HSCALE_X = 16'h7FFF and HSCALE_Y = 16'hFFFF, the timing diagram of video output is illustrated in Fig 15.

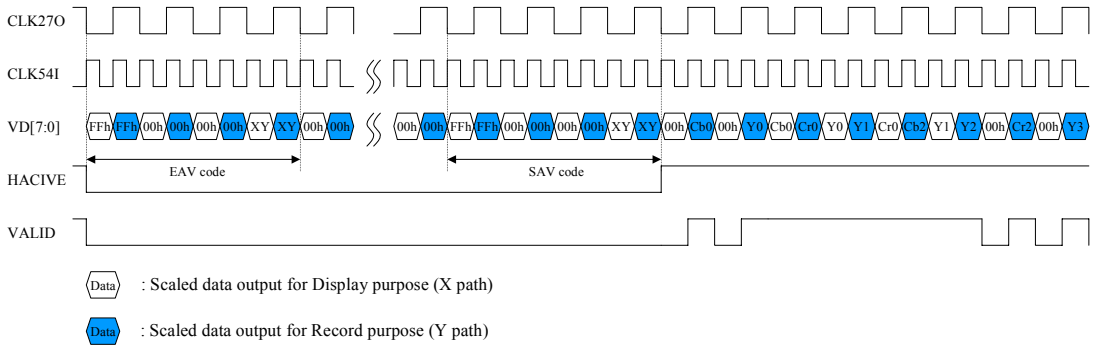


Fig 15 Timing Diagram in Dual ITU-R BT.656 with 54MHz format