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TW2880P-BC2-GR Chip Application Note

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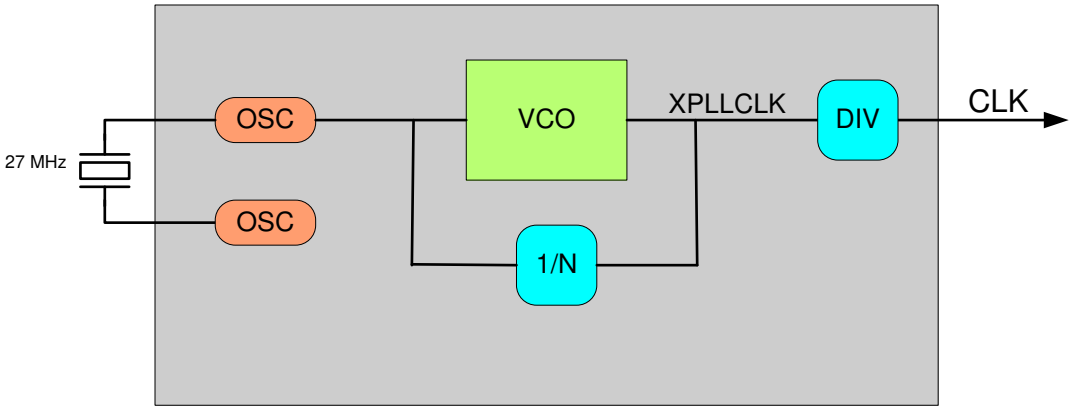
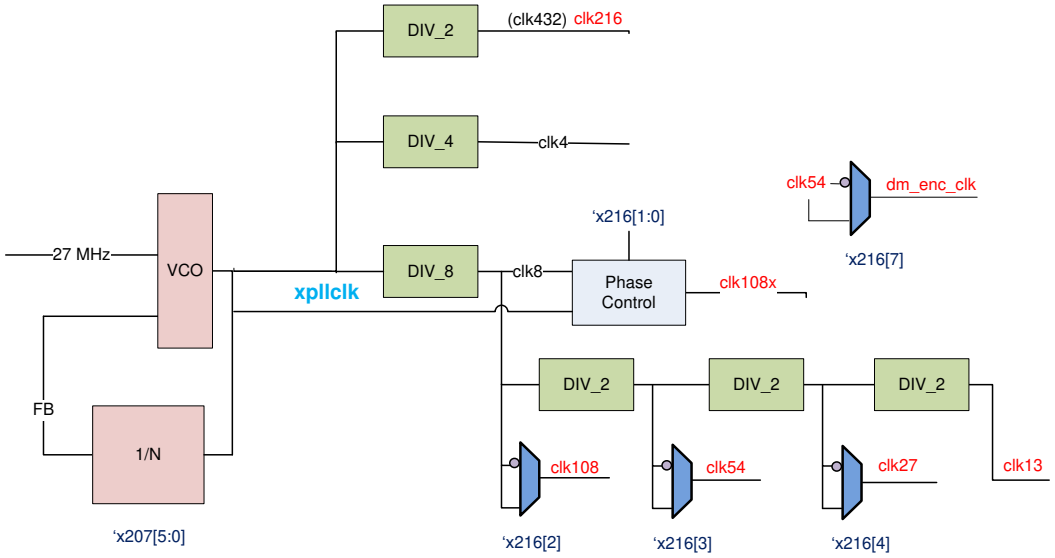
Introduction



TW2880C has three clock domains, they are, system clock domain, memory clock domain and video clock domain. Each clock domain support different kind of functional units. The clocks are generated from three different free running PLLs. The high-speed clock after the VCO stage will go through a series divider and phase select before reach the final circuit. Now we will walk through each clock domain in detail.

SCLK

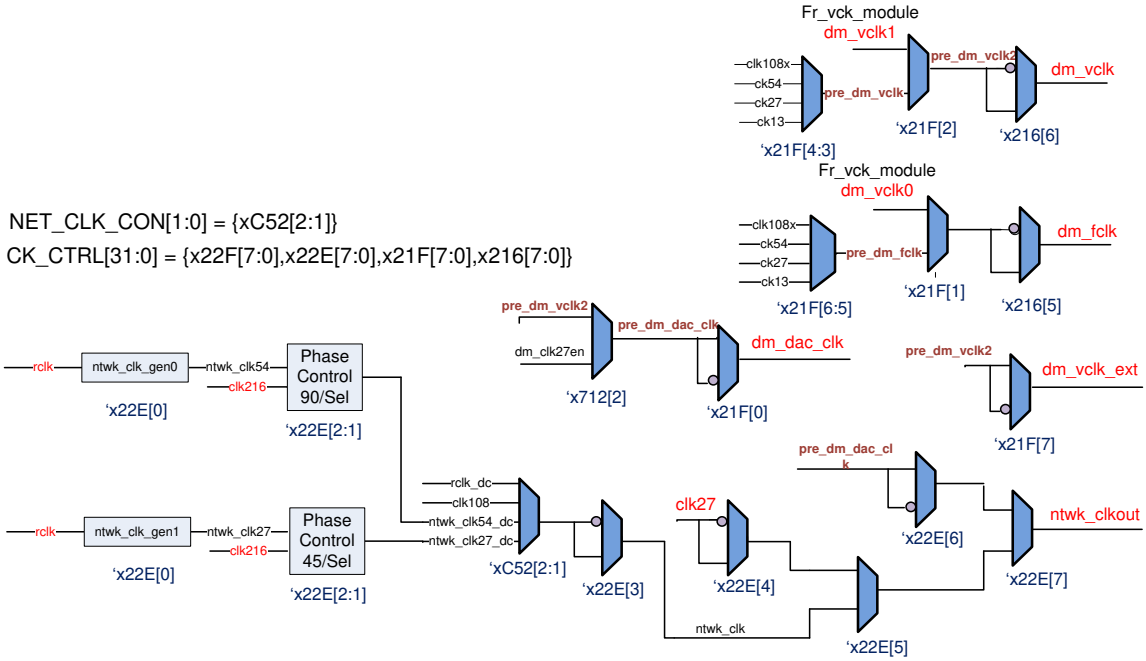
System clock is used throughout the TW2880. The idea is we will also use clocks with multiple of 27 in this clock group. The reason is obvious; 27 MHz clock is the data clock for the BT.656 standard. Because of these characteristics, some video decoders or CVBS output sections will use this clock group.



Clock Listing

12 clocks are generated from this clock group.

- 108 MHz system clock
- 54, 27, 13.5 MHz system using in input / output blocks
- 108 MHz system clock with phase control, used in recording output unit.
- High speed 216 MHz scaler clock (can be 432 MHz)
- Dual monitor TV encoder clock
- Dual monitor video clock
- Dual monitor fast clock for scaler
- Dual monitor DAC clock
- Dual monitor external video clock for VGA
- Network port output clock



Register Setting for SPLL

In normal cases, [0x207] bit[5:0] is designed to have default value of 5'd31 as this will make xpllclk 864 MHz and after divided by 8 circuits will create 108 MHz system clock.

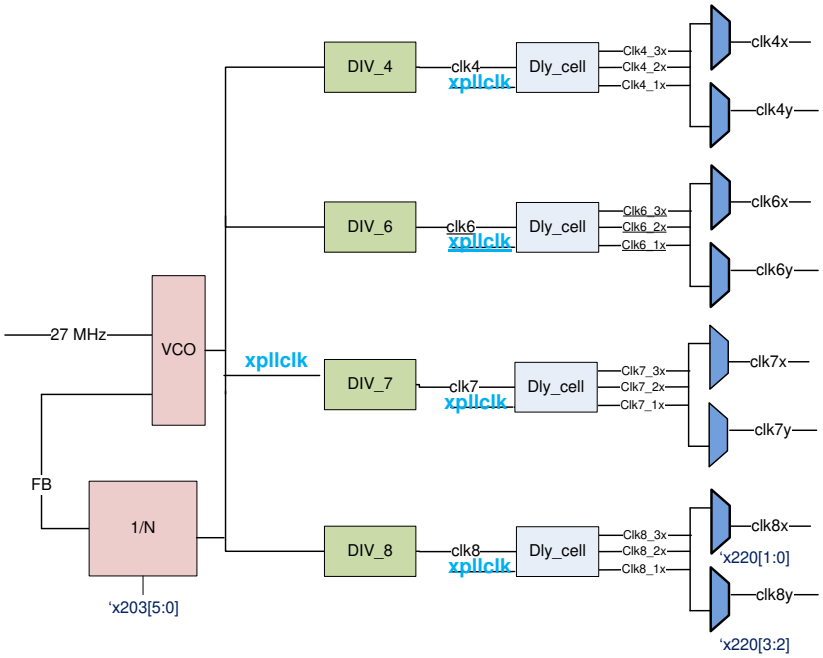
[0x216] bit 2, 3, 4 are used to select the phases of 108 MHz, 54 MHz, and 27 MHz clock.

[0x216] bit 1, 0 are used to select the phases of 108 MHz clock, this to adjust the record port clock / data relationship.

[0x21F] bit 2:1 are used to select the source of dual monitor clock, if CVBS is wanted, we should use the clock generated from the SCLK group. If display mode other than 27 MHz related then we should set these two bits to one and use clock generated from VCLK group.

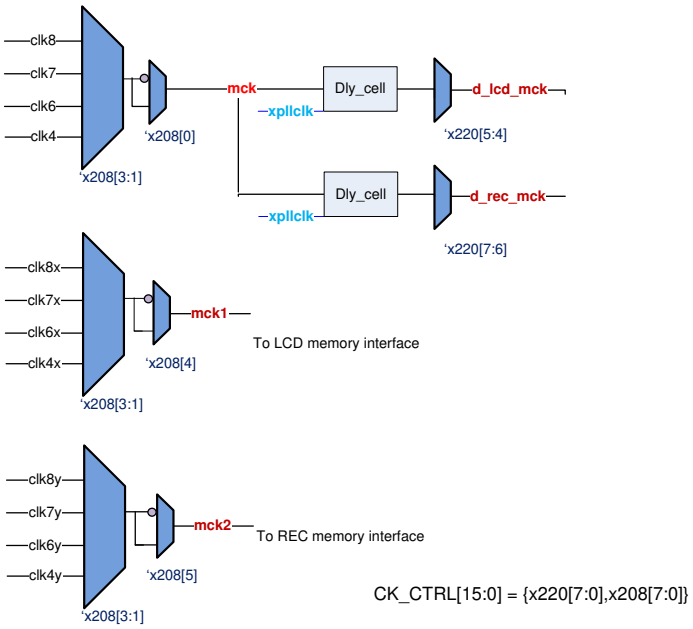
MCLK

Introduction



The memory clock range supported in TW2880C is between 133 – 200 MHz. User needs to program the multiplier register x203[5:0] and choose the desired divider to generate frequency. One thing needs to remember is the larger the divider, the more steps in the delay control. Five clocks are needed to adjust in a TW2880C system. They are:

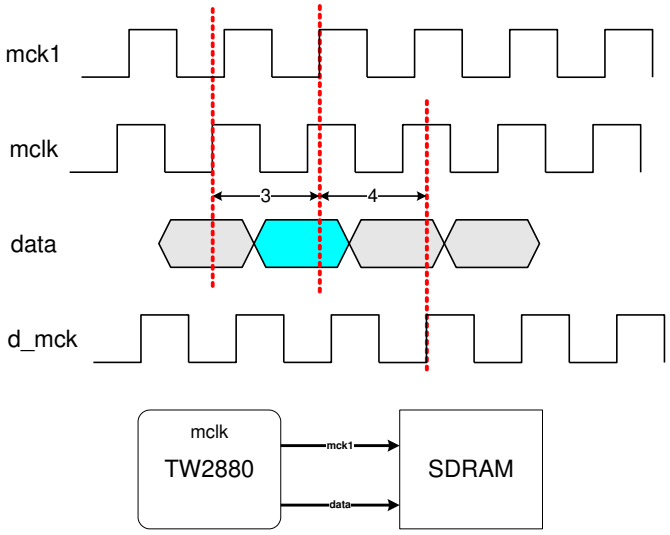
- Master clock for internal memory related blocks
- Clock for external SDRAM to use (Display side)
- Clock for external SDRAM to use (Recording side)
- Delayed version of display memory clock for latching incoming data
- Delayed version of recording memory clock for latching incoming data



Master Clock Calculation

Follow are the examples of popular master clock frequencies based on SDRAM speed grade.

For 133 MHz (-7.5 ns)				
27	19	4	128.25	
27	29	6	130.50	
27	34	7	131.14	
27	39	8	131.63	**Select**
For 166 MHz (-6 ns)				
27	24	4	162.00	
27	37	6	166.50	**Select**
27	43	7	165.86	
27	48	8	162.00	
For 175 MHz (-5 ns)				
27	26	4	175.50	
27	39	6	175.50	**Select**
27	45	7	173.57	
27	52	8	175.50	
For 200 MHz (-5 ns)				
27	29	4	195.75	
27	44	6	198.00	
27	52	7	200.57	
27	59	8	199.13	**Select**

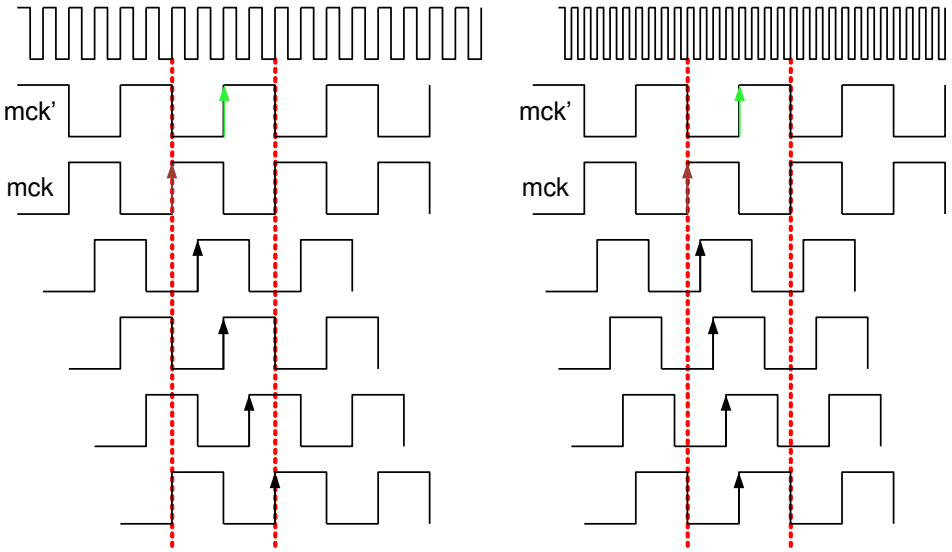


Clock Relationship

Two derivative clocks need to be adjusted to make the memory system work:

1. TW2880 to SDRAM: command, write data, controlled by 0x220[1:0] on the display, 0x220[3:2] for the record.
2. SDRAM to TW2880: read data, controlled by 0x220[5:4] on the display, 0x220[7:6] for the record.

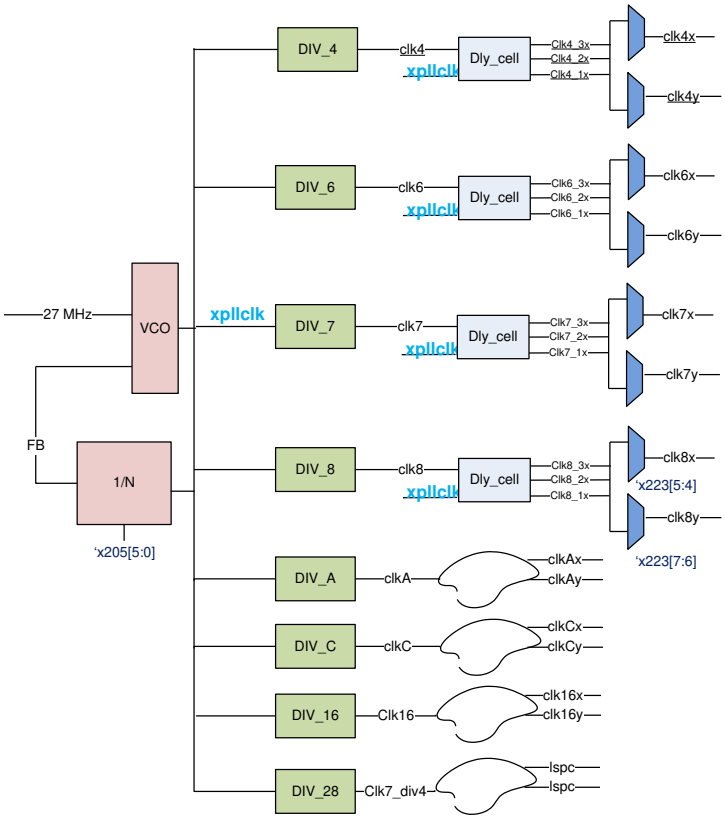
The steps are determined by divider, for example, divided by 4 you have only four steps, divided by 8, 8 steps.

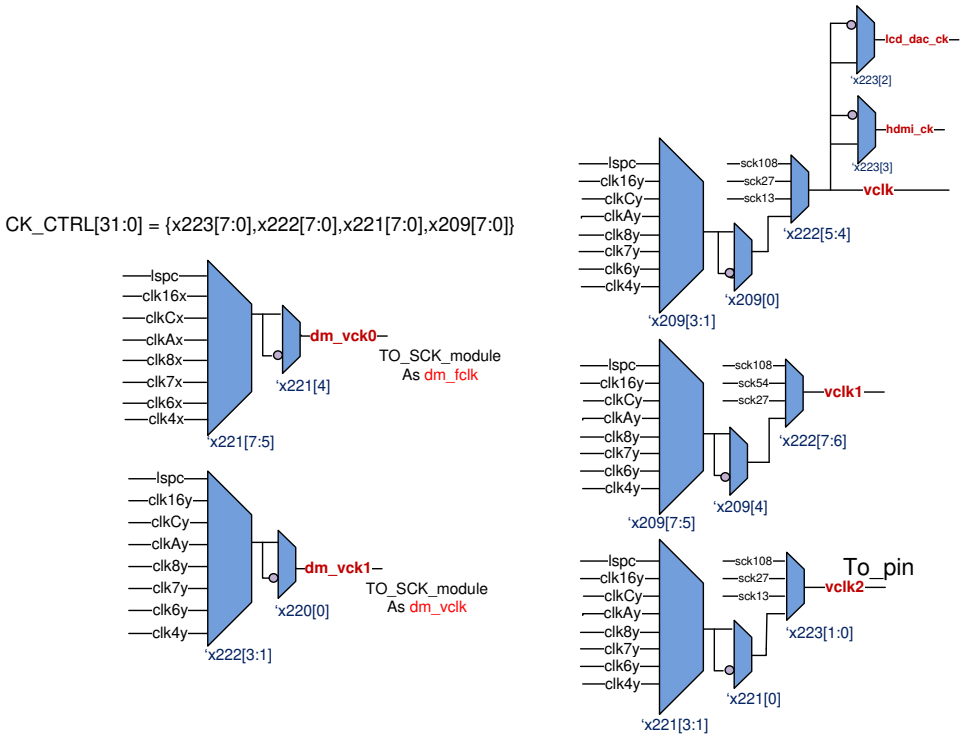


VCLK

The VCLK in TW2880C has the most complicated clock tree in the three as many exact frequencies are needed. To use it user needs to program the multiplier register x205[5:0] and choose the desired divider to generate frequency. 8 dividers are provided to generate correct clock for display. All together, seven clocks are generated:

- Clock for internal video related clock (vclk)
- Clock for VGA DAC
- Clock for HDMI block
- VCLK1 (not used)
- Clock for digital interface
- Two other dual monitor clock mux with SCLK





Popular Main Display Clocks

From the table shown in the following, TW2880C clock generation module can support most VESA standard resolution for the main display and HDMI TV Standard by selecting the proper VCK_N and VCK_Q values.

	Res	FRS	PCLK	VCK_N	VCK_Q	PCLK2	Diff
4:3	640x480	50Hz	19.75	23	28	22.18	-2.43
	640x480	60Hz	23.88	25	28	24.11	-0.23
	800x600	50Hz	31.13	32	28	30.86	0.27
	800x600	60Hz	38.13	40	28	38.57	-0.45
	1024x768	50Hz	51.75	23	12	51.75	0.00
	1024x768	60Hz	64.13	38	16	64.13	0.00
	1280x960	50Hz	83.00	37	12	83.25	-0.25
	1280x960	60Hz	102.00	38	10	102.60	-0.60
	1400x1050	50Hz	99.75	37	10	99.90	-0.15
	1400x1050	60Hz	122.50	32	7	123.43	-0.93
	1600x1200	50Hz	132.38	39	8	131.63	0.75
	1600x1200	60Hz	160.88	24	4	162.00	-1.13
	1600x1200r	60Hz	130.38	29	6	130.50	-0.13
	848x480	60Hz	31.50	33	28	31.82	-0.32
	1064x600	60Hz	51.00	30	16	50.63	0.38
	1280x720	50Hz	60.38	27	12	60.75	-0.38
	1280x720	60Hz	74.38	33	12	74.25	0.13
	1360x768	50Hz	69.50	31	12	69.75	-0.25
	1360x768	60Hz	84.63	25	8	84.38	0.25
	1704x960	50Hz	110.25	41	10	110.70	-0.45
	1704x960	60Hz	134.88	30	6	135.00	-0.13
	1864x1050	50Hz	133.50	30	6	135.00	-1.50
	1864x1050	60Hz	163.25	24	4	162.00	1.25
	1864x1050r	60Hz	131.13	34	7	131.14	-0.02
	1920x1080	50Hz	141.38	42	8	141.75	-0.38
	1920x1080	60Hz	172.73	38	6	171.00	1.72
	1920x1080r	60Hz	138.63	36	7	138.86	-0.23
16:10	768x480	50Hz	23.63	24	28	23.14	0.48
	768x480	60Hz	28.63	30	28	28.93	-0.30
	960x600	50Hz	37.00	38	28	36.64	0.36
	960x600	60Hz	45.88	27	16	45.56	0.31
	1152x720	60Hz	67.25	25	10	67.50	-0.25
	1680x1050	50Hz	120.13	31	7	119.57	0.55
	1680x1050	60Hz	147.00	38	7	146.57	0.43
	1680x1050r	60Hz	119.13	44	10	118.80	0.33
	1728x1080	60Hz	155.50	23	4	155.25	0.25
	1728x1080r	60Hz	125.75	28	6	126.00	-0.25
	1920x1200	50Hz	158.00	41	7	158.14	-0.14
	1920x1200	60Hz	193.13	43	6	193.50	-0.38
	1920x1200r	60Hz	154.13	40	7	154.29	-0.16
5:4	1280x1024	50Hz	89.38	33	10	89.10	0.28
	1280x1024	60Hz	108.88	24	6	108.00	0.88
15:9	1280x768	50Hz	65.13	29	12	65.25	-0.13
	1280x768	60Hz	80.13	24	8	81.00	-0.88
HDMI	1920x1080p	60Hz	148.50	44	8	148.50	0.00
	1920x1080i	30Hz	74.25	44	16	74.25	0.00

Dual Monitor Setting

Dual monitor's clock setting is a little bit different from the main display's settings. As mentioned before in the SCLK group, dual monitor block can take SCLK as clock source if CVBS output is needed. This is done by setting [0x21F] bit 2:1 to zero. When dual monitor block is running at frequencies other than multiples of 27 MHz, for example, driving a progressive VGA monitor, you need to set [0x21F] bit 2:1 to one and select the output from VCLK VCO. The VCO frequency will be the same for both displays and only the dividers are different. For example, the

main display is set at 1080P and the Dual monitor is set at 1280x1024 resolution. Then, select the SCLK (108 MHz) as the dual monitor video clock and set the main display frequency as listed in the following Table.

MAIN DISPLAY RESOLUTION	FRAME RATE	MAIN PCLK	VCK_N	VCK_Q	DUAL MON. RESOLUTION	DUAL MON. PCLK	REG SETTING
1920x1080P	60Hz	148.50	44	8	800x600x60Hz	42.4 MHz	x205= 2B (VCK_N) x209= 66 (div by 8) x221= C6 (div by 28) x222= 0C x216= 02 x21f= 06 (dm sel VCK)
1920x1080P	60Hz	148.50	44	8	1280x1024x60Hz	108	x205= 2B (VCK_N) x209= 66 (div by 8) x221= C6 x222= 0C x216= 02 x21f= 78 (dm sel SCK)
1280x1024	60Hz	108	32	8	1024x768x70Hz	72	x205= 1F (VCK_N) x209= 66 (div by 8) x221= A6 (div by 12) x222= 0A x216= 02 x21f= 06 (dm sel VCK)

When the Dual monitor is used to drive an analog TV, the frequency setting is simply by choosing the 54 Mhz as the dm_vck output. The registers x21F[4:2]='x4

Using SCLK Clock Group For Dual Monitor Clock

Usually, the SCLK frequency should not be changed either for system, record ports, or SPOT displays stability.

The performance of the above ports as well as the host bandwidth will also be affected if SCLK frequency is changed. For Dual monitor, if SCLK clock is used, the registers x21F need to be set properly.

Example

As an illustration, if the main display is in 1080p mode so the output frequency is 148.5 MHz, the dual monitor is VGA with 640x480@72Hz. The dual monitor clock is 31.5 MHz. Therefore, in addition to correcting the RGB register settings, the clock gen registers setting are:

MCLK REGISTERS

REG ADDRESS	DEFAULT SETTING	NEW SETTING	COMMENTS
x202	‘x12		MCLK M
x203	‘x23		MCLK N
x208	‘x02		MCLK CTRL[7:0]
x220	‘x00		MCLK CTRL[15:8]

Default setting is 162 MHz.

VCLK REGISTERS

REG ADDRESS	DEFAULT SETTING	NEW SETTING	COMMENTS
x204	‘x0d		VCLK M
x205	‘x27	‘x20	VCLK N
x209	‘x88	‘x02	VCLK CTRL[7:0]
x221	‘x88	‘xc0	VCLK CTRL[15:8]
x222	‘x00	‘xcc	VCLK CTRL[23:16]
x223	‘x00	‘x00	VCLK CTRL[31:24]

The main display frequency is calculate as 27 * 33 / 6 = 148.5 MHz

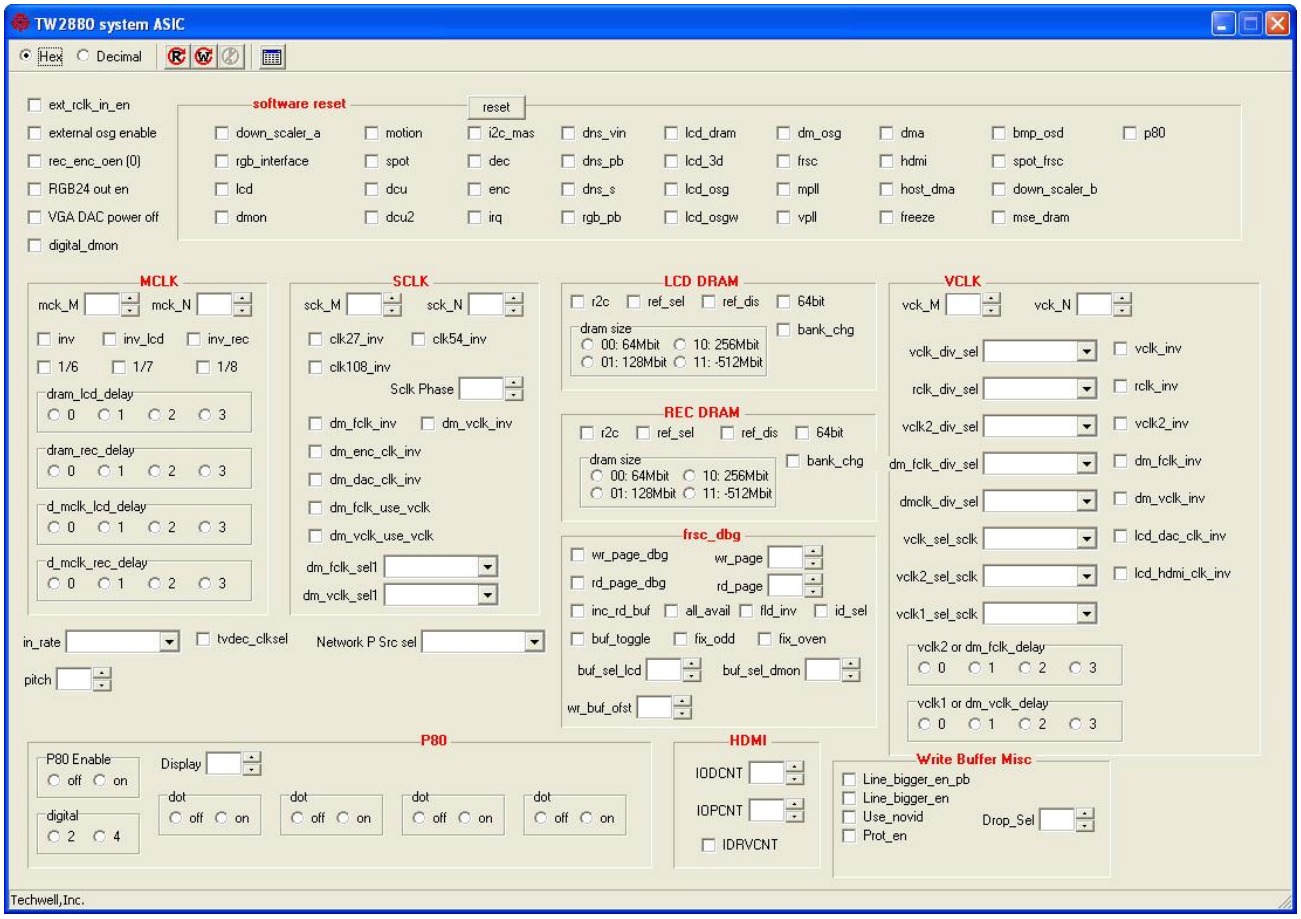
The Dual monitor frequency is selected as 27 * 33 / 28 = 31.8 MHz

VCLK REGISTERS

REG ADDRESS	DEFAULT SETTING	NEW SETTING	COMMENTS
x206	‘x0f		SCLK M
x207	‘x1f		SCLK N
x216	‘x00		SCLK CTRL[7:0]
x21F	‘x78	‘x07	SCLK CTRL[15:8]
x22E	‘x00		SCLK CTRL[23:16]
x22F	‘x00		SCLK CTRL[31:24]
X712	‘x00	‘x04	DM_LCD

Techwell Terminal Tool Setting

Layout of the CFG File



Explanation

In the Terminal, there are bold red characters, which describe the functions along with registers values that can be selected or white boxes that may be filled in to control the behavior of the functions.

- In the software reset section, a checked box would reset the specified module until the box is un-checked.
- In the MCK section, the mck_M is for the mck duty cycle control. The mck_N is the multiplier to the MPLL with the 27 MHz oscillator input, the PLL frequency output equals (mck_N + 1) x 27 MHz. The MPLL output frequency must less 1200 MHz and higher than 600 MHz for the MPLL to operate stable. After the mck_N is set, then final mck frequency is derived from check one of the division 1/6, 1/7, or 1/8. By properly choose the mck_N value and the division, the optimal MCK frequency can be acquired.
- In the MCK section, there are four other delay control selections, which are used for timing control to the DRAM interface. Two MCK outputs delay control such as dram_lcd_delay and dram_rec_delay, are used to clock phase delay respect to data and control signals. When delay 0 is check, the MCK output and the 64b data and control signals are aligned as the chip layout timing. If the PCB timing is not ideal and needs to be adjusted, then the MCK phase control can be set to 90, 180, or 270 degrees with respect to the data and control signals.
- There are two d_mclk_lcd_delay and d_mclk_rec_delay, which are used to adjust the input data to be latched by the TW2880. If 0 is checked, the data are latched by the MCK, otherwise, the data are latched by the delayed MCK.

- In the SCLK section, the M, N values are set as the MCK. The SCLK is set to 108 MHz as the default and should not be changed. Others boxes can be checked or un-checked to tune the inputs or outputs timing as needed. There are some boxes called dm_enc_clk_inv ..., which are used by the DUAL MONITOR module timing control.
- In the VCLK section, the M, N values are set as the MCK. All the boxes in the section are used to control the data timing respect to the VCLK or Dual_Monitor VCLK.
- In the LCD_DRAM or REC_DRAM section, dram size indicates the DRAM size used on the board.
- The 64-bit box is checked indicates the TW2880 interface to DRAM in 64-bit bus. Otherwise, it is 32-bit bus. Other buttons are for internal use only. The SDRAM controller default value should be good enough for everyday use.
- In the frsc_dbg section, the options for write pages and read pages can be controlled for debug purpose.
- In the P80 section. This is the LED control module used for debugging purposes.
- In the HDMI section, the setting is to control the HDMI output. The IODCNT control the output currents, the IOPCNT control the De-Emphasis and IDRVCNT Disable the De-emphasis if the box is checked.
- In the Write Buffer Misc section, these registers are used to protect SDRAM off-screen memory from being overwritten by run away RGB write FIFO process.

Section 2: PCB Layout Guide

Introduction

TW2880 is a complicated VLSI device whose inputs and outputs include several high frequency signal groups. To achieve the best result, the traces and associated discrete components need to carefully designed, placed and connected. To further complicate the board design, there are several power rails used either by digital or by analog functions. This guide served as a general reference for the board designer of TW2880.

Placement Suggestions

The first suggestion in designing TW2880 related PCB is clearly identifying the major functions that you want to include in this board. The second step involves planning the input / output connectors in a way such that do not let the signal trace crossed by traces in other groups if you can, whether it is signal traces or power traces. These are very important steps for getting a clean video output because crosstalk noise between the groups can easily destroy a board.

For the people not familiar with the term, crosstalk is the unwanted coupling of signals between parallel traces. To reduce crosstalk in TW2880 related boards, use dual-stripline layouts, which have two signal layers next to each other, route all traces perpendicular, increase the distance between the two signal layers, and minimize the distance between the signal layer and adjacent plane. Use the following steps to reduce crosstalk in either microstrip or stripline layouts:

- Widen spacing between signal lines as much as routing restrictions will allow. Try not to bring traces closer than three times the dielectric height.
- Design the transmission line so that the conductor is as close to the ground plane as possible. This technique will couple the transmission line tightly to the ground plane and help decouple it from adjacent signals.
- Use differential routing techniques where possible, especially for critical nets (i.e., match the lengths as well as the gyrations that each trace goes through).
- If there is significant coupling, route single-ended signals on different layers orthogonal to each other.

Minimize parallel run lengths between single-ended signals. Route with short parallel sections and minimize long, coupled sections between nets. Crosstalk also increases when two or more single-ended traces run parallel and are not spaced far enough apart. The distance between the centers of two adjacent traces should be at least four times the trace width. To improve design performance, lower the distance between the trace and the ground plane to under 10 mils without changing the separation between two traces.

Signal Integrity

For a single-ended trace, like clock transmission line, it could be improved using the following guidelines:

- Keep clock traces as straight as possible. Use arc-shaped traces instead of right-angle bends.
- Do not use multiple signal layers for clock signals.
- Do not use via in clock transmission lines. Via can cause impedance change and reflection.
- Place a ground plane next to the outer layer to minimize noise. A “grow to fill” function in the layout tool provides exactly this. If you use an inner layer to route the clock trace, sandwich the layer between reference planes.
- Terminate clock signals to minimize reflection.
- Use point-to-point clock traces as much as possible.

Power Regulator and Noise Filtering

TW2880 has 5 voltage tails for analog and digital functions. To get the best possible result but still keep the power consumption down, we suggestion using the switching regulator in the beginning of the power network and switching to LDO in the end to reduce the switching noise. This is especially true if the power is used for analog function. To

decrease the low frequency (below 1 kHz) noise caused by the power supply, filter the noise on power lines at the point where the power connects to the PCB and to each device. Place a 100 µF electrolytic capacitor where the power supply lines enter the PCB and after the first stage voltage regulator VCC signal. (Capacitors not only filter low-frequency noise from the power supply, but also supply extra current when many outputs switch simultaneously in a circuit.)

To filter power supply noise, use a non-resonant, surface-mount ferrite bead large enough to handle the current in series with the power supply. Place a 10 to 100 µF bypass capacitor next to the ferrite bead. (If proper termination, layout, and filtering eliminate enough noise, you do not need to use a ferrite bead.) The ferrite bead acts as a short for high frequency noise coming from the VCC source. Any low frequency noise is filtered by a large 10 µF capacitor after the ferrite bead. Usually, elements on the PCB add high-frequency noise to the power plane. To filter the high-frequency noise at the device, place decoupling capacitors as close as possible to each VCC and GND pair.

Power Distribution

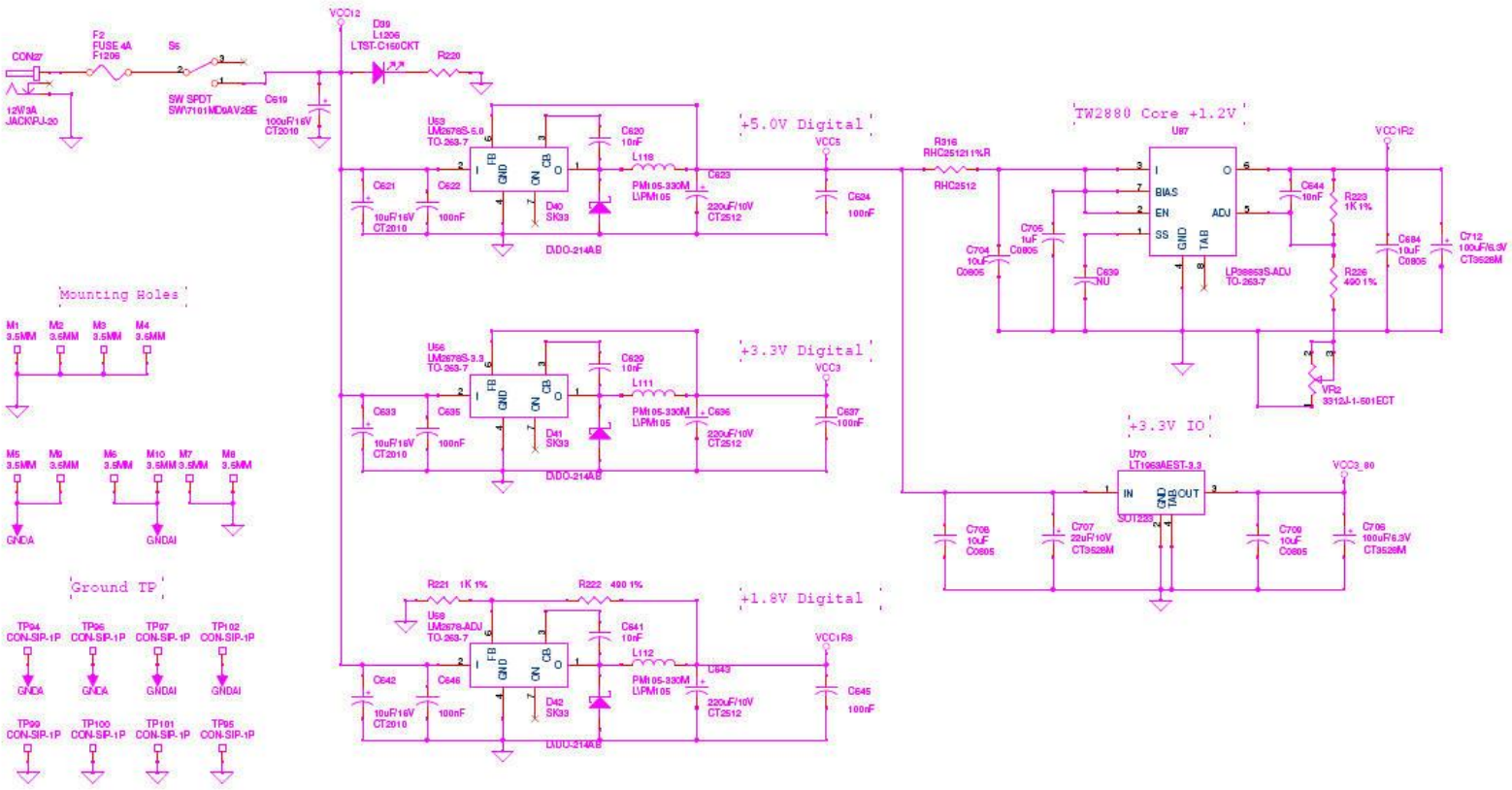
You can distribute power throughout the TW2880 PCB with either power planes or a power bus network. When designing TW2880 related PCB, a multi-layer PCBs that consist of two or more metal layers that carry VCC and GND to TW2880 is highly recommended. Because the power plane covers the full area of the PCB, its DC resistance is very low. The power plane maintains VCC and distributes it equally to all devices while providing very high current-sink capability, noise protection, and shielding for the logic signals on the PCB. It is recommended to use lower planes to distribute power. The power bus network, which consists of two or more wide metal traces that carry VCC and GND to devices, is often used on two-layer PCBs and is less expensive than power planes. When designing with power bus networks, be sure to keep the trace widths as wide as possible. The main drawback to using power bus networks is significant DC resistance. It is recommended to separate analog and digital power planes. For fully digital systems that do not already have a separate analog power plane, it can be expensive to add new power planes. However, you can create partitioned islands (split planes).

If your system shares the same plane between analog and digital power supplies, there may be unwanted interaction between the two circuit types. The following suggestions will help to reduce noise:

- For equal power distribution, use separate power planes for the analog (PLL) power supply. Avoid using trace or multiple signal layers to route the PLL power supply.
- Use a ground plane next to the PLL power supply plane to reduce power-generated noise.
- Place analog and digital components only over their respective ground planes.
- Use ferrite beads to isolate the PLL power supply from digital power supply.

TW2880 Power Rails

There are eleven voltage sources in a TW2880 HQ EV board. There are 5V digital, 3.3V digital, 3.3V TW2880 analog, 3.3V I/O, 1.8V digital, 1.8V analog, 1.2V TW2880 core, 1.2V TW2880 analog, 3.3V analog encoder, 1.8V analog decoder x2. We used a buck-switching regulator to create power source from external 12V DC adapter. In the final stage, we use many LDO to get the desired analog voltage. Please reference to the next two schematics. Please pay special attention to all analog power supplies to TW2880 and the I/O video chip, as this will determine the final visual effect.


+5.0V Digital
+3.3V Digital
+1.8V Digital
TW2880 Core +1.2V
+3.3V IO
Mounting Holes
Ground TP
LTST-C150CKT
LM2678S-5.0
LM2678S-3.3
LM2678-ADJ
LP38853S-ADJ
LT1963AEST-3.3
SW SPDT
JACK/PJ-20
DIDO-214AB
SOT223