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# Triple-Rate (SD/HD/3G) SDI Transmitter with VC-2 Encoder and Audio Decoder

## TW6872

The TW6872 is a triple-rate (SD/HD/3G) SDI transmitter. It receives parallel BT.656/BT.1120/ASI video data from a CMOS sensor/ISP chip. It also receives analog audio, or serial digital audio. The TW6872 serializes the video and audio into an SDI stream and transmits it to an SDI receiver via its integrated cable driver.

In addition to the standard SDI format with uncompressed raw video data, TW6872 can optionally compress video with a visually lossless VC-2 compression algorithm to send the video formats normally running at HD rate (1.5Gbps) on the cable at SD rate (270Mbps), and therefore achieve longer cable reach.

Together, the TW6872 and Intersil's TW6874 SDI receiver provide a complete end-to-end SDI link solution and can operate with or without VC-2 compression. Integrated audio/video test patterns and PRBS checker ease system design and implementation.

The TW6872 is available in a 76 Ld QFN. It is specified for operation over the -40°C to +85°C ambient temperature range and operates on two power supplies: 1V and 3.3V. A single 27MHz crystal is used for all supported audio/video operating modes.

## Applications

- SD/HD/3G-SDI Camera

## Features

- Triple-rate (SD/HD/3G) SDI transmitter for Standard Definition (SD) and High Definition (HD), and 3G 10-bit component video
- Encoding SDI standard of ITU-R BT.656/SMPTE 259M Level C, ITU-R BT.1120/SMPTE ST 292, SMPTE 424M 10-bit parallel component video inputs into 10-bit serial video output
- BT.656/BT.1120 interface for CMOS sensor/ISP chip
- Asynchronous Serial Interface (ASI) for IEC 13818-1 compliant transport streams
- Integrated 75Ω cable driver with pre/de-emphasis
- Integrated VC-2 encoder allows transmission of HD video over SD transmission lengths
- Analog audio and I2S serial audio input interfaces over ancillary field
- Digital audio with PCM encoding for embedding audio samples into the audio ancillary field of SDI stream
- Single 27MHz clock/crystal input
- Optional clock output for use as the ISP chip's clock input to enhance overall jitter
- PRBS7/23 and video/audio pattern generator
- I<sup>2</sup>C for external micro-controller interface
- Low power consumption
- Small footprint LTZ-QFN76L (9mm x9mm) package
- Pb-free (RoHS compliant)

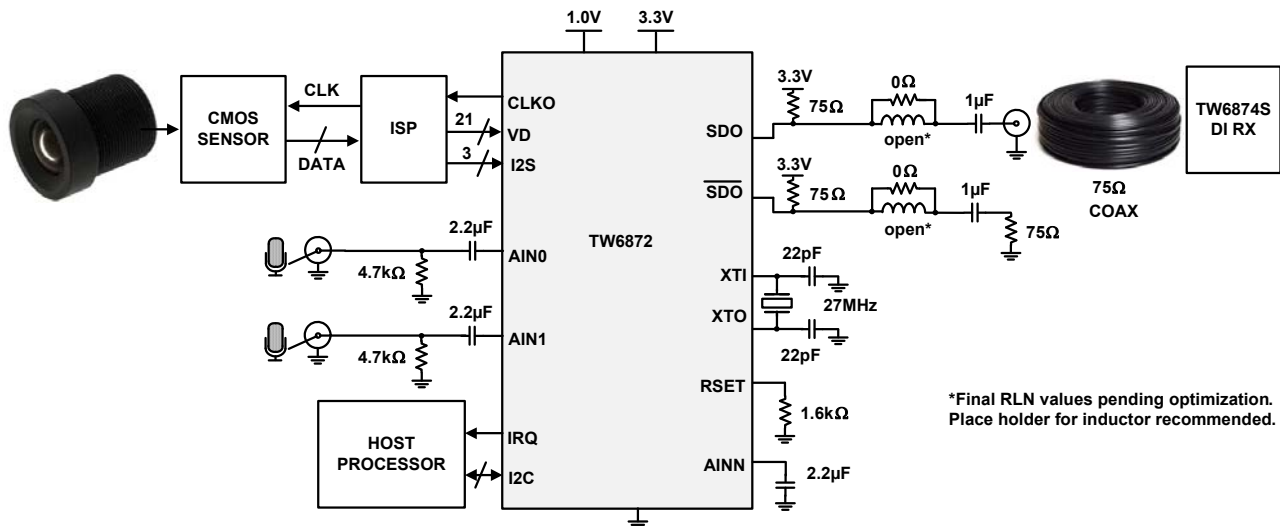
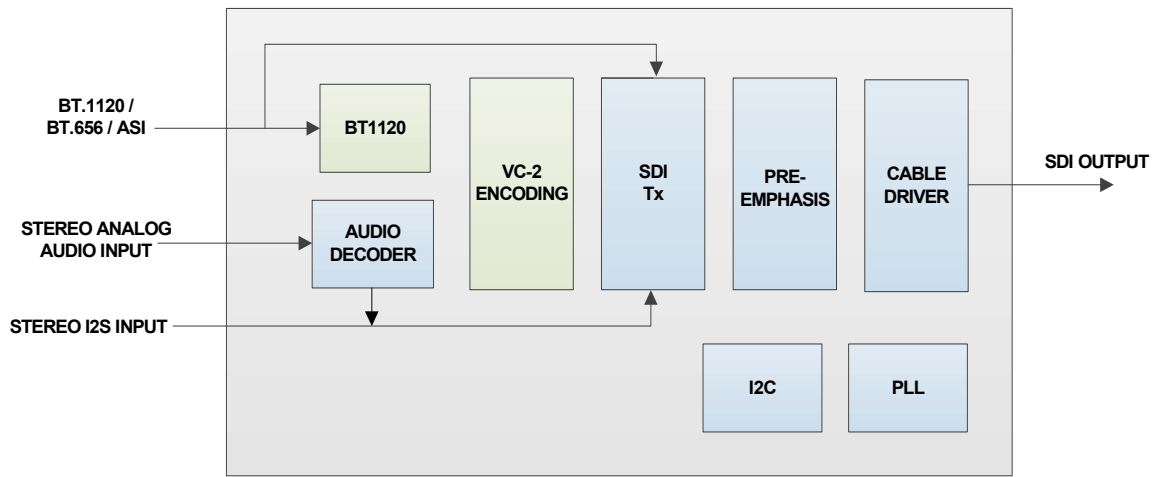


FIGURE 1. TW6872 TYPICAL APPLICATION

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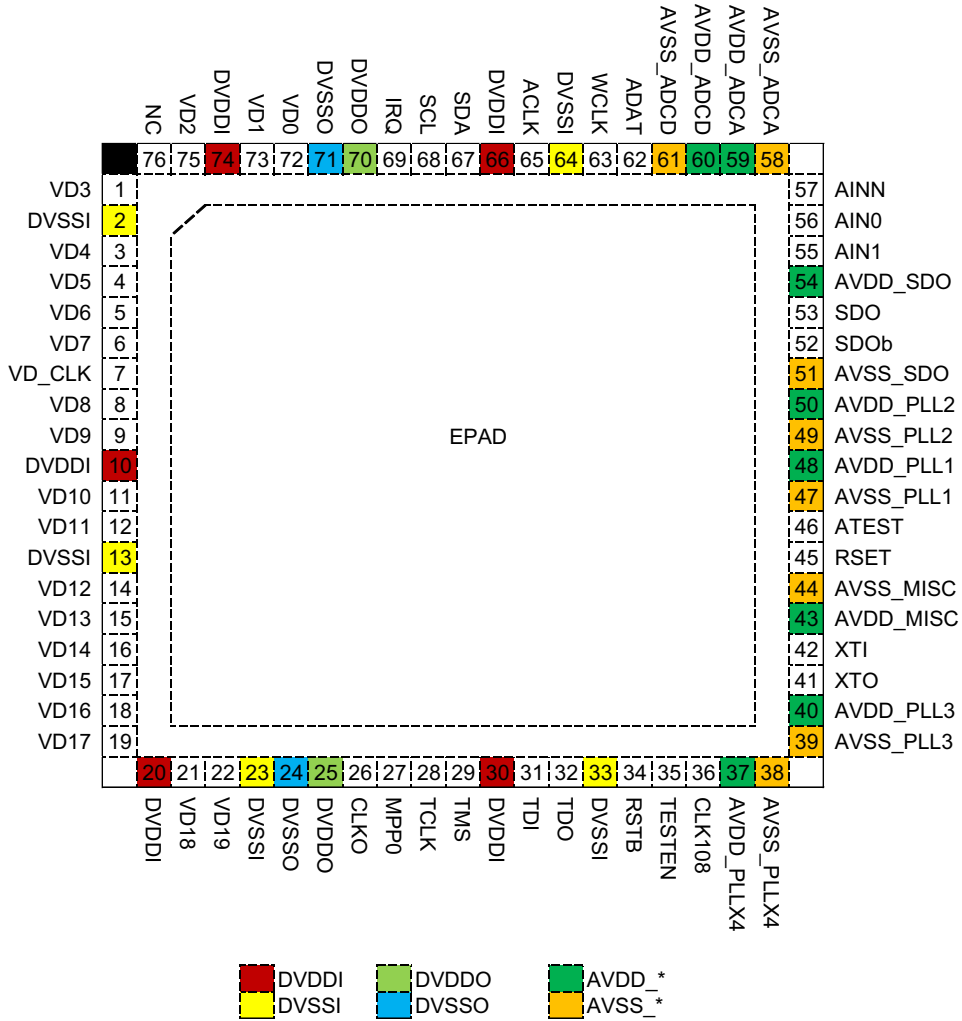
## Block Diagram



# TW6872

## Pin Configuration

TW6872  
(76 PIN QFN)  
TOP VIEW



## Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
<b>PARALLEL DIGITAL VIDEO</b>			
22	VD19	Digital Input	Parallel video data input. HD/3G mode: Chroma (C) data SD mode: not used ASI mode: not used
21	VD18	Digital Input	
19	VD17	Digital Input	
18	VD16	Digital Input	
17	VD15	Digital Input	
16	VD14	Digital Input	
15	VD13	Digital Input	
14	VD12	Digital Input	
12	VD11	Digital Input	
11	VD10	Digital Input	
9	VD9	Digital Input	
8	VD8	Digital Input	
6	VD7	Digital Input	
5	VD6	Digital Input	
4	VD5	Digital Input	
3	VD4	Digital Input	
1	VD3	Digital Input	
75	VD2	Digital Input	
73	VD1	Digital Input	
72	VD0	Digital Input	
7	VD_CLK	Digital Input	Parallel video clock input. 3G mode: 148.5MHz HD mode: 74.25MHz SD mode: 27MHz ASI mode: 27MHz
26	CLKO	Digital Output	Clock source for the ISP in master mode. Generated frequencies are: 27MHz 3G mode: 148.5MHz HD mode: 74.25MHz or 148.5MHz SD mode: 13.5MHz or 27MHz
36	CLK108	Digital I/O	Alternate 108MHz clock source for the ISP in master mode
<b>I2S AUDIO</b>			
62	ADAT	Digital Input	Audio serial data input.
63	WCLK	Digital Input	Audio word clock input.
65	ACLK	Digital Input	Audio serial bit clock.

## Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
<b>I<sup>2</sup>C</b>			
67	SDA	Digital I/O	I <sup>2</sup> C serial data I/O. Requires pull-up resistor to VDDO.
68	SCL	Digital Input	I <sup>2</sup> C serial clock input. Requires pull-up resistor to VDDO.
<b>JTAG</b>			
32	TDO	Digital Output	JTAG test data output.
31	TDI	Digital Input	JTAG test data input.
29	TMS	Digital Input	JTAG test mode start.
28	TCLK	Digital Input	JTAG test clock input.
<b>SYSTEM</b>			
69	IRQ	Digital I/O	Interrupt request.
34	RSTB	Digital Input	Resets chip when pulled LO. Reset must be asserted for 1μs every time the power supplies have powered up and settled to their final value.
35	TESTEN	Digital Input	For internal use only. Tie LO.
27	MPP0	Digital I/O	Multi-purpose pin.
46	ATEST	Analog Output	Analog test output. For internal use only. Do not connect anything to this pin.
76	NC	No Connect	Do not connect anything to this pin.
<b>SERIAL DATA OUTPUT</b>			
53	SDO	Analog Output	SDI serial data output. See <a href="#">“SDO Routing” on page 15</a> for termination guidelines.
52	SDOb	Analog Output	Inverted SDI serial data output. See <a href="#">“SDO Routing” on page 15</a> for termination guidelines.
45	RSET	Analog Output	Tie a 1.6kΩ (1%) resistor from this pin to analog ground. The resistor should be placed as close as possible to the RSET pin. SDI output amplitude can be adjusted by changing the value of the resistor.
<b>CLOCK INPUT</b>			
42	XTI	Analog Input	27MHz crystal connection or 27MHz oscillator input.
41	XTO	Analog Output	27MHz crystal connection.
<b>ANALOG AUDIO</b>			
55	AIN1	Analog Input	Audio input for channel 1. Terminate with 4.7kΩ to ground and AC-couple with 2.2μF.
56	AIN0	Analog Input	Audio input for channel 0. Terminate with 4.7kΩ to ground and AC-couple with 2.2μF.
57	AINN	Analog Input	Audio ADC reference. Terminate with 2.2μF to ground. Do not connect external audio signal to this pin.
<b>DIGITAL POWER</b>			
10, 20, 30, 66, 74	DVDDI	Digital Power	1.0V digital power supply for core. Place a local 0.1μF ceramic bypass capacitor to the digital ground as close to the pin as possible.
2, 13, 23, 33, 64	DVSSI	Digital Ground	Digital ground.
25, 70	DVDDO	Digital Power	3.3V digital power supply for I/O. Place a local 0.1μF ceramic bypass capacitor to the digital ground as close to the pin as possible.
24, 71	DVSSO	Digital Ground	Digital ground.

## Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
<b>ANALOG POWER</b>			
54	AVDD_SDO	Analog Power	3.3V analog power supply for SDO driver. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
51	AVSS_SDO	Analog Ground	Analog ground.
43	AVDD_MISC	Analog Power	3.3V analog power supply for SDO driver. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
44	AVSS_MISC	Analog Ground	Analog ground.
60	AVDD_ADCD	Analog Power	3.3V analog power supply for ADC. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
61	AVSS_ADCD	Analog Ground	Analog ground.
59	AVDD_ADCA	Analog Power	3.3V analog power supply for ADC. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
58	AVSS_ADCA	Analog Ground	Analog ground.
48	AVDD_PLL1	Analog Power	3.3V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
47	AVSS_PLL1	Analog Ground	Analog ground.
50	AVDD_PLL2	Analog Power	3.3V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
49	AVSS_PLL2	Analog Ground	Analog ground.
40	AVDD_PLL3	Analog Power	3.3V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
39	AVSS_PLL3	Analog Ground	Analog ground.
37	AVDD_PLLX4	Analog Power	3.3V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
38	AVSS_PLLX4	Analog Ground	Analog ground.
EPAD	EPAD	Ground	Ground.

## Ordering Information

PART NUMBER <small>(Notes 1, 2)</small>	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
TW6872-NA1-CR	TW6872 NA1-CR	-40 to +85	76 Lead QFN	L76.9x9

### NOTES:

- These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), please see device information page for [TW6872](#). For more information on MSL please see tech brief [TB363](#).



## Absolute Maximum Ratings

### Supply Pins

AVDD_SDO to AVSS_SDO	+4.0V
AVDD_MISC to AVSS_MISC	+4.0V
AVDD_ADCA to AVSS_ADCA	+4.0V
AVDD_ADCC to AVSS_ADCC	+4.0V
AVDD_PLL1 to AVSS_PLL1	+4.0V
AVDD_PLL2 to AVSS_PLL2	+4.0V
AVDD_PLL3 to AVSS_PLL3	+4.0V
AVDD_PLLX4 to AVSS_PLLX4	+4.0V
DVDDI to DVSSI	+1.2V
DVDDO to DVSSO	+4.0V

### Other Pins

Voltage on any Input Pin	DVSSO-0.3 V to DVDDO V
SDO/SDOb Voltage	AVSS_SDO V to AVDD_SDO V
XTI/XTO Voltage	0 V to 1 V
AINO/1/N Voltage	AVSS_ADCA V to AVDD_ADCA V

### ESD Ratings

IEC 61000-4-2 (contact discharge) Analog Audio Pins	6kV
Human Body Model (JEDEC JS-001-2011) all Pins	2kV
Charged Device Model (JESD22-C101)	750V
Latch Up (Tested per JESD78; Class II, Level A)	100mA

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief [TB379](#).
- For  $\theta_{JC}$ , the “case temp” location is the center of the exposed pad on the package underside.

**IMPORTANT NOTE:** All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**Electrical Specifications** DVDDI = 1.0V, AVDD\_SDO = AVDD\_MISC = AVDD\_ADCC = AVDD\_ADCA = AVDD\_PLL1 = AVDD\_PLL2 = AVDD\_PLL3 = AVDD\_PLLX4 = DVDDO = 3.3V,  $T_A = +25^\circ\text{C}$ , unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN ( <a href="#">Note 5</a> )	TYP	MAX ( <a href="#">Note 5</a> )	UNIT
<b>POWER SUPPLY VOLTAGE</b>						
AVDD_SDO	Analog SDO Driver Supply Voltage		3.0	3.3	3.6	V
AVDD_MISC	Analog Misc Supply Voltage		3.0	3.3	3.6	V
AVDD_ADCA	Analog ADC Supply Voltage		3.0	3.3	3.6	V
AVDD_ADCC	Analog ADC Supply Voltage		3.0	3.3	3.6	V
AVDD_PLL1	Analog PLL Supply Voltage		3.0	3.3	3.6	V
AVDD_PLL2	Analog PLL Supply Voltage		3.0	3.3	3.6	V
AVDD_PLL3	Analog PLL Supply Voltage		3.0	3.3	3.6	V
AVDD_PLLX4	Analog PLL Supply Voltage		3.0	3.3	3.6	V
DVDDI	Digital Core Supply Voltage		0.9	1.0	1.1	V
DVDDO	Digital IO Supply Voltage		3.0	3.3	3.6	V
<b>POWER DISSIPATION</b>						
I_AVDD	Analog Supply Current ( <a href="#">Note 10</a> ) (all AVDD_* tied together except SDO)			60		mA
I_AVDD_SDO	Analog SDO Supply Current			60		mA
I_DVDDI	Digital Core Supply Current			90		mA
I_DVDDO	Digital IO Supply Current			6		mA
P_TOT	Total Power			505.8		mW

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{JC}$ ( $^\circ\text{C}/\text{W}$ )
QFN Package ( <a href="#">Notes 3, 4</a> )	22	1.5
Power Dissipation	See “ <a href="#">Electrical Specifications</a> ”	
Maximum Die Temperature	+125 $^\circ\text{C}$	
Storage Temperature	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$	
Pb-Free Reflow Profile	see <a href="#">TB493</a>	

## Recommended Operating Conditions

Ambient Operating Temperature	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
-------------------------------	--

# TW6872

**Electrical Specifications** DVDDI = 1.0V, AVDD\_SDO = AVDD\_MISC = AVDD\_ADCCD = AVDD\_ADCA = AVDD\_PLL1 = AVDD\_PLL2 = AVDD\_PLL3 = AVDD\_PLL4 = DVDDO = 3.3V, T<sub>A</sub> = +25°C, unless otherwise specified. (Continued)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
<b>PARALLEL VIDEO INPUT</b>						
f <sub>VDCLK</sub>	Pixel Clock Frequency		27		148.5	MHz
DCYC <sub>VDCLK</sub>	Pixel Clock Duty Cycle			50		%
t <sub>SU</sub>	Data Set-up Time		3.8			ns
t <sub>HD</sub>	Data Hold Time		0.6			ns
<b>SERIAL DIGITAL OUTPUT</b>						
DR <sub>SDO</sub>	Serial Data Rate		0.27		2.97	Gbps
OS <sub>SDO</sub>	Serial Data Output Swing		720	800	880	mV
OV <sub>SDO</sub>	Serial Data Output Overshoot		-10		+10	%
TT <sub>SDO</sub>	Transition (Rise/Fall) Time (20% to 80%)	270Mbps	400	850	1500	ps
		1.485Gbps		135	270	ps
TTD <sub>SDO</sub>	Difference between Rise/Fall Time	270Mbps		40		ps
		1.485Gbps		10		ps
RL <sub>SDO</sub>	Return Loss (Note 9)	<1.5GHz	-13			dB
		1.5GHz to 3GHz	-10			dB
JIT <sub>SDO</sub>	Output Jitter	270Mbps: timing jitter above 10Hz		0.11		UI <sub>P-P</sub>
		270Mbps: alignment jitter above 1kHz		0.09		UI <sub>P-P</sub>
		1.485Gbps: timing jitter above 10Hz		0.37		UI <sub>P-P</sub>
		1.485Gbps: alignment jitter above 100kHz		0.09		UI <sub>P-P</sub>
<b>CLKO OUTPUT</b>						
f <sub>CLKO</sub>	Nominal Frequency		13.5		148.5	MHz
DCYC <sub>CLKO</sub>	Duty Cycle		45		55	%
<b>DIGITAL INPUTS</b>						
V <sub>IH</sub>	Input High Voltage		2.0		3.6 (DVDDO + 10%)	V
V <sub>IL</sub>	Input Low Voltage		-0.3		0.8	V
I <sub>L</sub>	Input Leakage Current		-10	0	+10	μA
C <sub>IN</sub>	Input Capacitance	f = 1MHz, V <sub>IN</sub> = 2.4V		2		pF
<b>DIGITAL OUTPUTS</b>						
VOH	Output High Voltage	I <sub>O</sub> = -2mA	2.4		DVDDO	V
VOL	Output Low Voltage	I <sub>O</sub> = +2mA		0.2	0.4	V
I <sub>OZ</sub>	Tri-State Current				10	μA
<b>CRYSTAL (CONNECTED to XTI and XTO)</b>						
f <sub>XTAL</sub>	Nominal Frequency (Fundamental)			27		MHz
DEV <sub>XTAL</sub>	Deviation (Note 6)				±50	ppm
CL	Load Capacitance			18		pF
RS	Series Resistor (ESR)			50		Ω
<b>OSCILLATOR INPUT (CONNECTED TO XTI)</b>						
f <sub>OSC</sub>	Nominal Frequency (Fundamental)			27		MHz
T <sub>JOSC</sub>	Total jitter				1.8	ps-pp
DCYC <sub>OSC</sub>	Duty Cycle				55	%

# TW6872

**Electrical Specifications** DVDDI = 1.0V, AVDD\_SDO = AVDD\_MISC = AVDD\_ADCCD = AVDD\_ADCA = AVDD\_PLL1 = AVDD\_PLL2 = AVDD\_PLL3 = AVDD\_PLLX4 = DVDDO = 3.3V, T<sub>A</sub> = +25 °C, unless otherwise specified. (Continued)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
<b>ANALOG AUDIO INPUT</b>						
AUD <sub>RANGE</sub>	Input Voltage Range		0	1.4	2.4	V <sub>P-P</sub>
AUD <sub>FS</sub>	Full Scale Input Voltage Range (Note 7)		0.21	1.4	2.4	V <sub>P-P</sub>
AUD <sub>ISO</sub>	Interchannel Isolation (Note 8)			90		dB
<b>DIGITAL AUDIO INPUT</b>						
T <sub>A_ct</sub>	ACLK Cycle Time			70.76		ns
T <sub>A_dc</sub>	ACLK Duty Cycle			50		%
T <sub>A_su</sub>	WCLK, ADAT Setup Time		30			ns
T <sub>A_h</sub>	WCLK, ADAT Hold Time		5			ns
<b>I<sup>2</sup>C SERIAL CONFIGURATION INTERFACE</b>						
f <sub>SCL</sub>	Maximum SCL Clock Frequency				400	kHz
t <sub>SU:STA</sub>	Set-up Time for a START Condition		370			ns
t <sub>HD:STA</sub>	Hold Time for a START Condition		74			ns
t <sub>SU:STO</sub>	Set-up Time for a STOP Condition		370			ns
t <sub>BUF</sub>	Bus Free Time between a STOP and START Condition		740			ns
t <sub>SU:DAT</sub>	Data Set-up Time		74			ns
t <sub>HD:DAT</sub>	Data Hold Time		50		900	ns
t <sub>r</sub>	Rise Time of SDA and SCL				300	ns
t <sub>f</sub>	Fall Time of SDA and SCL				300	ns
CBUS	Capacitive Load for each Bus Line				400	pF

**NOTES:**

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
6. Crystal deviation is based on normal operating condition.
7. Refer to [Table 79 on page 37](#) for gain settings. F<sub>IN</sub> = 1kHz.
8. Tested at input gain of 0dB. F<sub>S</sub> = 8kHz and 16kHz.
9. Return Loss depends on PCB design.
10. Add 15mA to I<sub>ADD</sub> for Dirac\_Compression.

## Video Input Modes

The TW6872 has a 20-bit wide parallel video input interface. Through this interface, the input can be configured in one of two modes by registers: either the BT.656/BT.1120 mode, or the Asynchronous Serial Interface (ASI) mode. In the BT.656/BT.1120 mode, the video data can be either YC multiplexed (10-bit mode) or YC separated (20-bit mode). In the ASI input mode, the ASI stream data comes in through the 10-bit data bus running at 27MHz.

## Video Bit Mapping

The ISP to TW6872 port mapping depends on the mode used as described in the following. Figure 2 shows the timing relationship for the input clock and data.

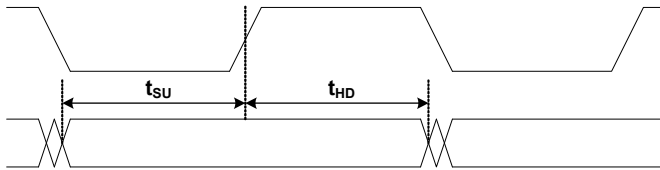


FIGURE 2. VD\_CLK TO VD[19:0] TIMING

## BT.656 MODE

In BT.656 mode, only 10-bit data is used by the SD video (NTSC/PAL). For either ASI or BT.656 formats, the 10-bit BT.656 video data use the lower word (bits 9:0) of the TW6872's 20-bit port and the upper word is not used per Figure 3.

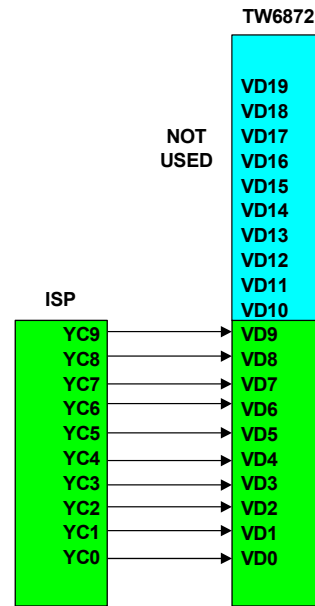


FIGURE 3. BT.656 MAPPING

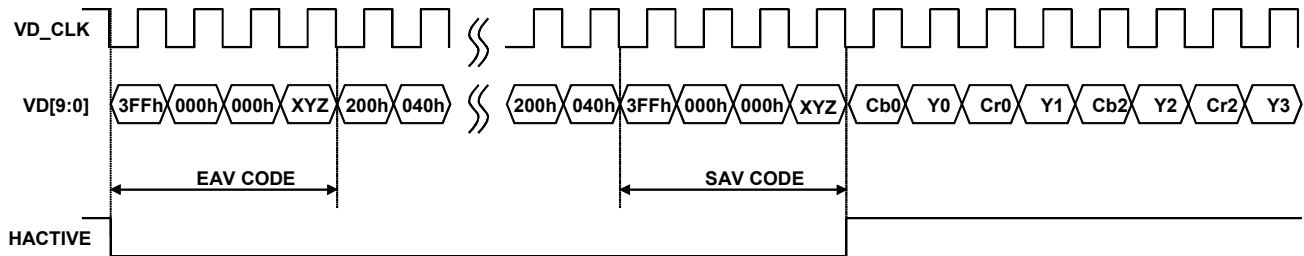


FIGURE 4. BT.656 FORMAT

TABLE 1. SAV/EAV CODE SEQUENCE FOR BT.656 AND BT.1120 DATA

CONDITION			FVH VALUE			SAV/EAV CODE SEQUENCE			
FIELD	VTIME	HTIME	F	V	H	FIRST BYTE	SECOND BYTE	THIRD BYTE	FOURTH BYTE
EVEN	Blank	EAV	1	1	1	0x3FF	0x000	0x000	0x3C4
EVEN	Blank	SAV	1	1	0	0x3FF	0x000	0x000	0x3B0
EVEN	Active	EAV	1	0	1	0x3FF	0x000	0x000	0x368
EVEN	Active	SAV	1	0	0	0x3FF	0x000	0x000	0x31C
ODD	Blank	EAV	0	1	1	0x3FF	0x000	0x000	0x2D8
ODD	Blank	SAV	0	1	0	0x3FF	0x000	0x000	0x2AC
ODD	Active	EAV	0	0	1	0x3FF	0x000	0x000	0x274
ODD	Active	SAV	0	0	0	0x3FF	0x000	0x000	0x200

## BT.1120 MODE

For HD/3G formats, the input data is 20-bit BT.1120 and all 20 bits of the TW6872's video input port are used. The Y and C pixels are placed separately. Y is input on the lower word (bits 9:0) and C is input on the upper word (bits 19:10) per [Figure 5](#). If

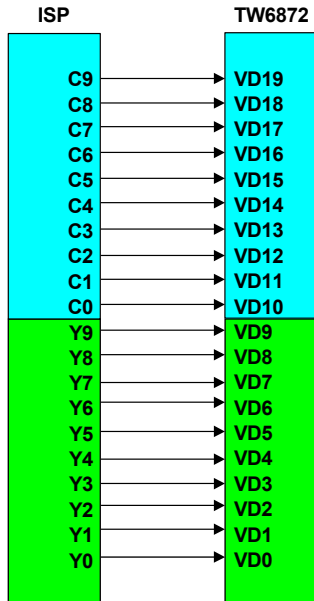


FIGURE 5. 20-BIT BT.1120 MAPPING

the parallel video source only outputs 16 bits, the configuration used in [Figure 6](#) should be used.

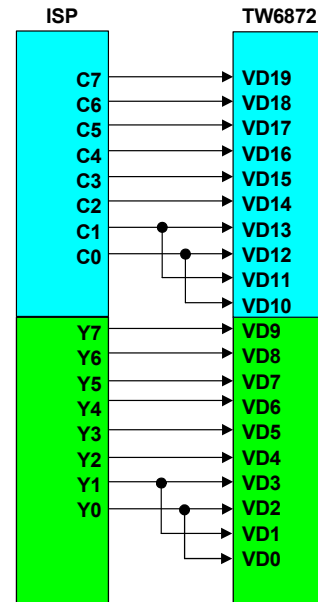


FIGURE 6. 16-BIT BT.1120 MAPPING

The SAV/EAV signals shown in [Table 1](#) are inserted into both the Y and C bus, and are identical on both buses. The timing reference signals and input timing for BT.1120 mode are shown in [Figure 7](#).

The video pixel data of BT.656 and BT.1120 internally run through a parallel-to-serial conversion and then a scrambler circuit before driving the SDI output pin.

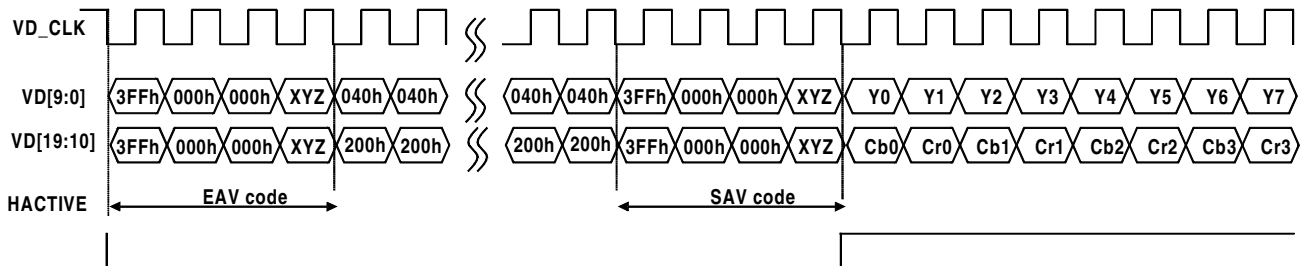


FIGURE 7. BT.1120 FORMAT

## Master/Slave Mode

The TW6872 operates in either master or slave mode. In master mode the TW6872 generates a reference clock for the ISP (CLKO output). In slave mode it uses the ISP's video data clock (VD\_CLK input) for its timing reference (CLKO is not used).

### MASTER MODE

In master mode, the TW6872 generates a low jitter CLKO to drive the ISP master clock. In turn, the ISP device generates the VD\_CLK to drive the BT.656/BT.1120 input. With the common clock basis, master mode provides the best performance with the lowest jitter. The TW6872 can generate the following CLKO frequencies:

- Serial data clock rate/10
  - 27MHz
  - 148.5MHz
  - 148.5/1.001MHz
- Serial data clock rate/20
  - 13.5MHz
  - 74.25MHz
  - 74.25/1.001MHz
  - 148.5MHz
  - 148.5/1.001MHz
- VC-2 compressed
  - 27MHz
  - 27/1.001MHz
  - 74.25MHz
  - 74.25/1.001MHz
- XTI clock rate
  - 27MHz

The previous CLKO frequencies are generated per the selected operating mode by setting ISPCLK\_DIV10\_SEL for a chosen data rate (SD/HD/3G). ISP\_XTALCLK\_SEL bypasses this divider and sends the XTI frequency onto CLKO. If the preceding clock frequencies are not suitable for the ISP, CLK108 can be used to generate a 108MHz clock. This clock maintains the same time base as CLKO and thus allows for master mode operation. This clock can be divided externally to generate other desired frequencies such as 54MHz.

### SLAVE MODE

If ISP cannot accept an external master clock from CLKO, then the TW6872 must operate in slave mode. In slave mode, the ISP generates VD\_CLK independently. If VD\_CLK input may have higher jitter, TW6872 performance will be affected. CLKO is not used and can be powered down. When in slave mode, VD\_CLK input must be present to use TW6872's internal pattern generator.

## Asynchronous Serial Interface Mode

The Asynchronous Serial Interface takes the standard IEC 13818-1 compliant transport stream running at 27MHz into the 10-bit data bus. The incoming pre-compressed stream is converted from 10-bit parallel format into serial 270Mbps data, then driven out the SDI output pin.

## SDI Video Output

The TW6872 serial data output (SDO) electrical specifications and data format are compliant to SMPTE 259M for SD-SDI, SMPTE ST-292 for HD-SDI, and SMPTE 424M for 3G-SDI standards, supporting both video and audio embedded in the serial stream. TW6872 also supports embedding of ancillary data packets that can be used for downstream information purposes. In addition, the TW6872 output driver integrates a programmable pre/de-emphasis feature. This feature is the intentional alteration of the amplitude vs frequency characteristics of the signal to reduce adverse effects of noise. For the maximum cable reach, the PCB layout must be optimized to ensure best signal integrity per the layout guidelines in "[Layout Guidelines](#)" on page 15.

### SDI Video Standard Formats

The supported SDI video formats are:

- 270Mbps (SMPTE 259M Level C)
  - 525i/625i 50, 59.94 fields/s
- 1.485Gbps (SMPTE ST 292)
  - 720p 50, 60 frames/s
  - 1080p 24, 25, 30 frames/s
  - 1080i 50, 60 fields/s
- 1.485/1.001Gbps (SMPTE ST 292)
  - 720p 59.94 frames/s
  - 1080p 23.976, 29.97 frames/s
  - 1080i 59.94 fields/s
- 2.97Gbps (SMPTE 424M)
  - 1080p 50, 60 frames/s
- 2.97/1.001Gbps (SMPTE 424M)
  - 1080p 59.97 frames/s

Any of the above supported video formats can be output on SDO. The video streams are transmitted in 10-bit YCbCr 4:2:2 sampled format.

### Cable Reach

The TW6872 SDI output driver is designed to work with various types of 75Ω coaxial cable including: RG6, RG59, and 3C-2V (SYV 75-3). Within each cable type, there are variations such as bare copper or copper-clad over steel or aluminum core. Actual cable reach is determined by a combination of the cable type, the SDI receiver and system implementation. In general, the TW6872 meets or exceeds cable reach as defined by the HDcctv Alliance version 1.0 SR specification.

### Pre/De-Emphasis

To provide additional cable reach, the TW6872 output driver integrates a programmable pre/de-emphasis feature. Coaxial cable acts as a low-pass filter to the video signal, attenuating the high frequency components of the signal significantly more. The pre/de-emphasis feature boosts the high frequency component of the transmitted signal. Essentially, this means that transition bits have a larger amplitude than the following bits. [Figure 8](#) depicts this graphically. The PREEMPH register controls the value.

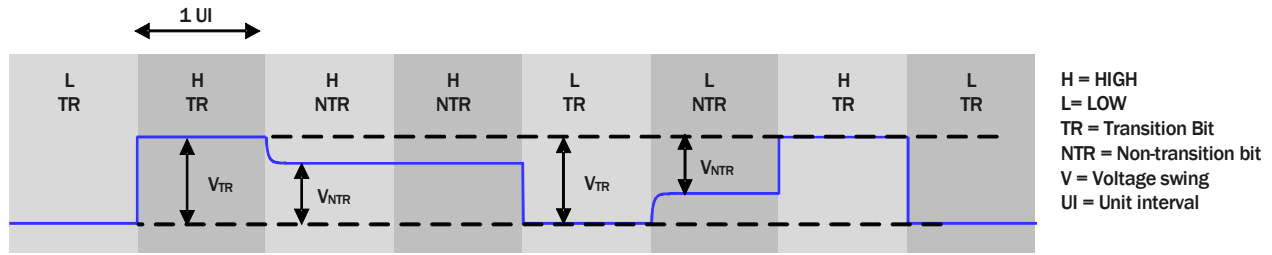


FIGURE 8. PRE/DE-EMPHASIS WAVEFORM. NO PRE/DE-EMPHASIS MEANS  $V_{TR} = V_{NTR} = 800\text{mV}$

## PRE-EMPHASIS

By using the driver in pre-emphasis mode, all bits except the transition bit have the nominal 800mV amplitude ( $V_{NTR}$ ). The transition bit can be programmed to have up to ~1300mV amplitude ( $V_{TR}$ ). Pre-emphasis is defined as:

$$\text{pre-emphasis} = 20 \cdot \log_{10}(V_{TR}/V_{NTR}) \quad (\text{EQ. 1})$$

The allowed pre-emphasis range is 0 to 11.5dB. Due to voltage swing headroom limitations, pre-emphasis settings above 5dB hold  $V_{TR}$  to ~1300mV while reducing the  $V_{NTR}$  amplitude.

## DE-EMPHASIS

By using the driver in de-emphasis mode, the transition bit has the nominal amplitude 800mV amplitude ( $V_{TR}$ ). The non-transition bits can be programmed from ~350mV to 800mV ( $V_{NTR}$ ).  $V_{TR} = V_{NTR}$  means no pre/de-emphasis is applied. De-emphasis is defined as:

$$\text{de-emphasis} = 20 \cdot \log_{10}(V_{NTR}/V_{TR}) \quad (\text{EQ. 2})$$

The allowed de-emphasis range is -7 to 0dB.

## VC-2 Compressed Data

The TW6872 can optionally compress a I-frame subset of 1.485Gbps HD video data into 270Mbps SD video bit stream data using VC-2 Video Compression (also known as Dirac). Using this, Compressed HD video transmitted at 270Mbps achieves the same cable lengths as SD-SDI. The compressed video quality is visually lossless, and is completely satisfactory in applications such as video surveillance.

The TW6872 VC-2 option is compliant to SMPTE ST-2047-4 Level 65 format. The VC-2 Video Compression is specified in SMPTE ST 2042-1, with the level specified in SMPTE ST 2042-2. The carriage of Level 65 VC-2 compressed video data over SD-SDI is specified in SMPTE ST 2047-4.

The following compressed video formats are supported:

- VC-2 compressed 720p 50, 59.94 frames/s
- VC-2 compressed 1080p 25, 29.97 frames/s

Note: The incoming pixel clock for VC-2 PAL should be 74.25 MHz, while VC-2 NTSC input uses 74.25/1.001MHz.

Note: The incoming pixel clock for the uncompressed 25 and 50 frames/s should be 74.25MHz, while the clock for uncompressed 29.97 and 59.94 frames/s should be 74.25/1.001MHz. At the physical layer, the serial signal is SD-SDI compliant as specified in SMPTE 259M. Since the timing references signal (TRS) are

those used in SD-SDI, the frame/field rate carried can only be 25/50 in PAL systems and 29.97/59.94 in NTSC systems. The ancillary audio and ancillary packet data remain embedded in the stream as they would for an SD-SDI stream. Because of this, in order to use the VC-2 compression feature, the incoming video needs to run at 25/50 frame rates for PAL systems and 29.97/59.94 frame rates for NTSC systems. 30/60 frame rates cannot be used for NTSC systems. For those ISPs supporting only 30/60 frame rates using a 27MHz crystal, the TW6872 is able to generate a CLK0 frequency of 27/1.001MHz so that the ISP PLL does not need to do 1.001 division and generate 29.97/59.94 frame rate video.

## Audio Input Interface

The audio subsystem in the TW6872 is composed of two Analog-to-Digital Converters (ADC) processing, an audio detector and digital serial audio interface. The TW6872 can receive two analog audio signals (for stereo left/right channels) or one stereo I2S digital serial audio stream. These audio streams are inserted into and transported by the SDI data stream.

## Analog Audio

The TW6872 has an audio detector for each analog audio channel. There are two kinds of audio detection defined by AAMPMD. One is the detection of absolute amplitude and the second is of differential amplitude. For both detection methods, the accumulating period is defined by the ADET\_FILTER register and the detecting threshold value is defined by the ADET\_TH0/1 registers. Using the differential amplitude method is recommended. The status for audio detection is read by the AUD\_STATE0/1 register for polling programming and it also makes an interrupt request through the IRQ pin for event driven programming.

The analog audio input signal gain for the AINO/1 pins can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN0/1 registers before being sampled by the ADCs.

Analog audio is sampled at 48kHz by an internally generated sampling clock.

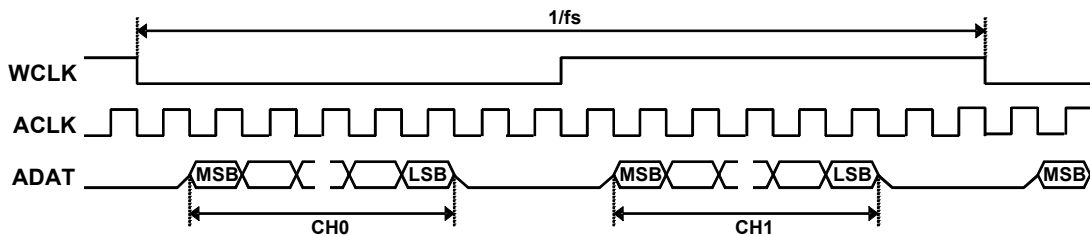


FIGURE 9. SERIAL AUDIO INTERFACE FORMAT

## I2S Digital Audio

The digital serial audio interfaces follows a standard I2S interface as shown in [Figure 9](#).

The ACLK, WCLK and ADAT pins from the I2S decoder block are used to receive digital serial audio input data. The I2S interface only operates in slave mode; these pins are always inputs.

## SDI Ancillary Audio

Either the I2S or analog input audio is inserted into the SDI data stream in ancillary audio format. For 3G/HD-SDI, TW6872 ancillary audio follows the SMPTE ST 299-1 standard, using two 24-bit wide channels at 48kHz sampling frequency. For SD-SDI, TW6872 follows the SMPTE 272M standard, using two 20-bit wide channels at 48kHz sampling frequency.

## Layout Guidelines

Specific printed circuit board (PCB) layout guidelines should be followed for optimal TW6872 performance. Special care should be given to the following subsections in order of layout priority:

- SDO routing
- Power supply routing
- Parallel video routing
- Power supply bypassing

These are each addressed in the following sections.

### SDO Routing

The SDO/SDOb pins can toggle at up to 3Gbps with less than 135ps edge rates. Special care is required in designing the PCB interface for these pins, otherwise poor return loss and suboptimal cable reach will occur.

Typically, the SDO output will consist of: BNC connector, 1 $\mu$ F AC-coupling capacitor, return loss network (75 $\Omega$  resistor in parallel with an inductor, or 0 $\Omega$  resistor if the inductor is not installed), and 75 $\Omega$  termination resistor to 3.3V (AVDDTERM). The SDOb output will be similar, except that it is terminated to 75 $\Omega$ .

Since the termination networks are 75 $\Omega$ , the PCB trace characteristic impedance must also be 75 $\Omega$  single-ended. These traces should be on the top layer and not transition to any other layer, which would cause impedance discontinuities. The adjacent reference (ground) plane should be a solid, continuous copper plane.

A PCB stackup/spacing should be chosen such that the trace width to give 75 $\Omega$  is approximately as wide as the component landing pads in order to minimize impedance discontinuities. In this regard, the physically smallest components should be used. 0201 size is recommended.

The 75 $\Omega$  termination resistors (R1 and R3 in [Figure 10](#)) should be placed as close as possible to the TW6872's SDO/SDOb pins. The return loss network and AC-coupling cap should be adjacent to the termination resistor. SDO and SDOb should be isolated by a ground fill between the signal traces and termination components as shown in [Figure 11](#).

A high quality BNC connector that is rated for 3Gbps operation should be chosen. Typically edge launch BNC connectors, such as the Samtec BNC7T-J-P-XX-ST-EM1, give better frequency response than right angle or vertical connectors. To optimize return loss, the total trace length from the BNC connector to SDO should be as short as possible.

It is advised to follow the reference layout to meet these criteria. [Figures 10](#) and [11](#) show the reference schematic and layout meeting these requirements. The PCB stackup used in this design is:

- Layer 1: 75 $\Omega$  signal
- Layer 2: Ground
- Layer 3: Power
- Layer 4: Power
- Layer 5: Ground
- Layer 6: Signal

A four layer stackup can be used to implement the design. However, if the signal return plane has other traces routed on it, it is important that the solid copper section under the high speed SDO traces not be cut and that it remains solid. Keep other traces away from this area.



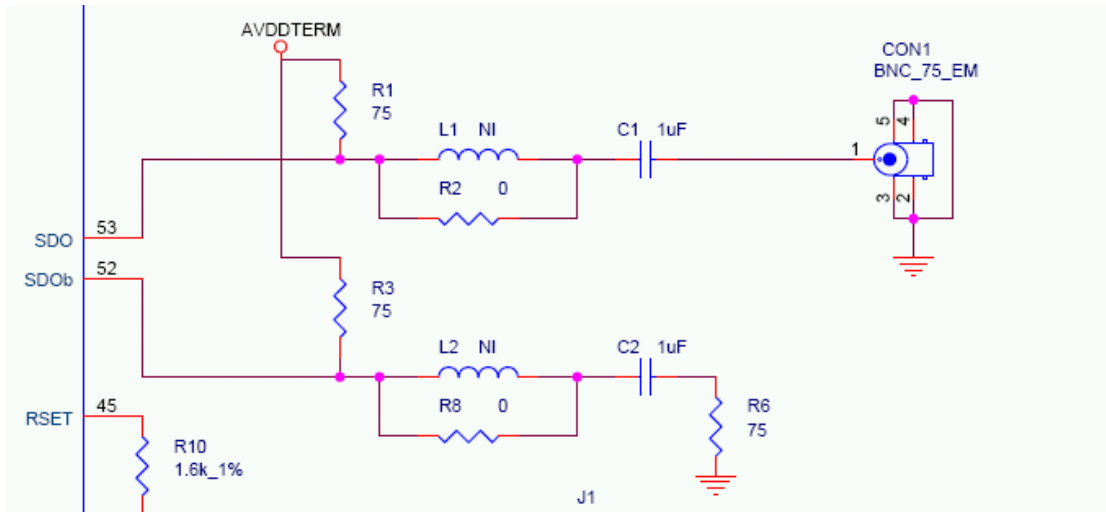


FIGURE 10. SDO/SDOb OUTPUT SCHEMATIC

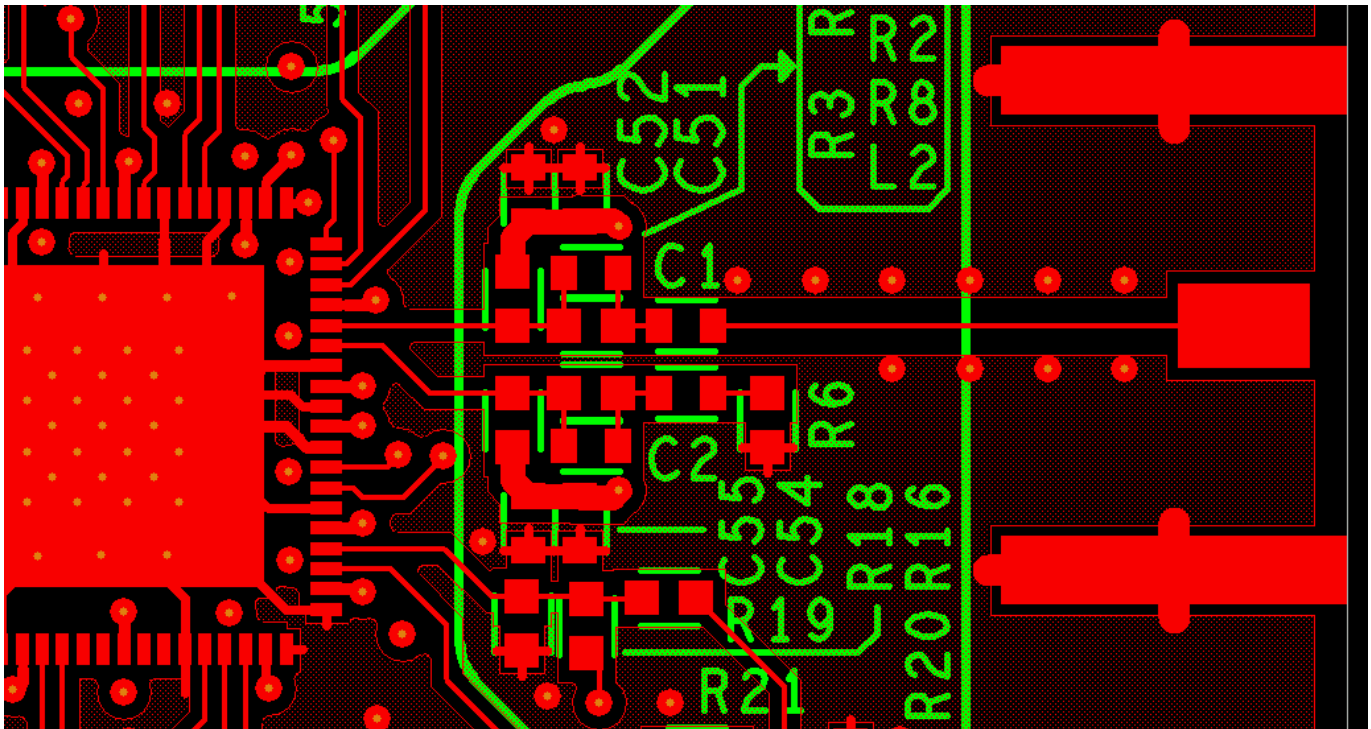


FIGURE 11. SDO/SDOb LAYOUT LAYER 1

### Power Supply Routing

The TW6872 uses eight analog supply plans (one 3.3V pin for each domain) and two digital supply plans (two DVDDO 3.3V pins and five DVDDI 1.0V pins). The SDO output termination resistors also use a 3.3V supply (AVDDTERM). Switching regulators that generate a 3.3V and 1.0V rail can be used; an LDO for the analog 3.3V supply is not necessary.

For the 3.3V regulator, the AVDDTERM/AVDD\_SDO pins should be grouped by one ferrite bead, the remaining seven AVDD pins should be isolated by another ferrite bead, and the two DVDDO pins should be isolated by a third ferrite bead. For DVDDI, a single ferrite bead can be used from the power regulator to the five pins. Figures 12 and 1 show the reference schematic for power supply routing.

Ideally a low impedance plane will route to each pin, but a wide trace can also be used. A single common ground can be used for the analog and digital grounds.

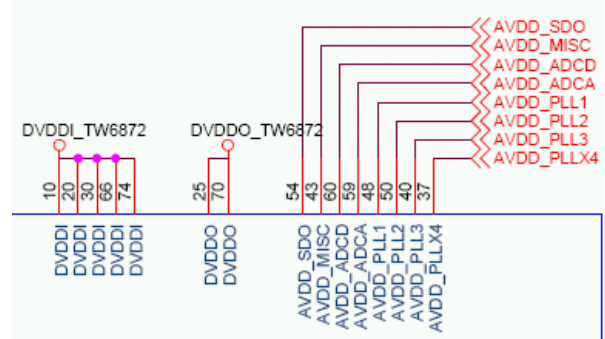
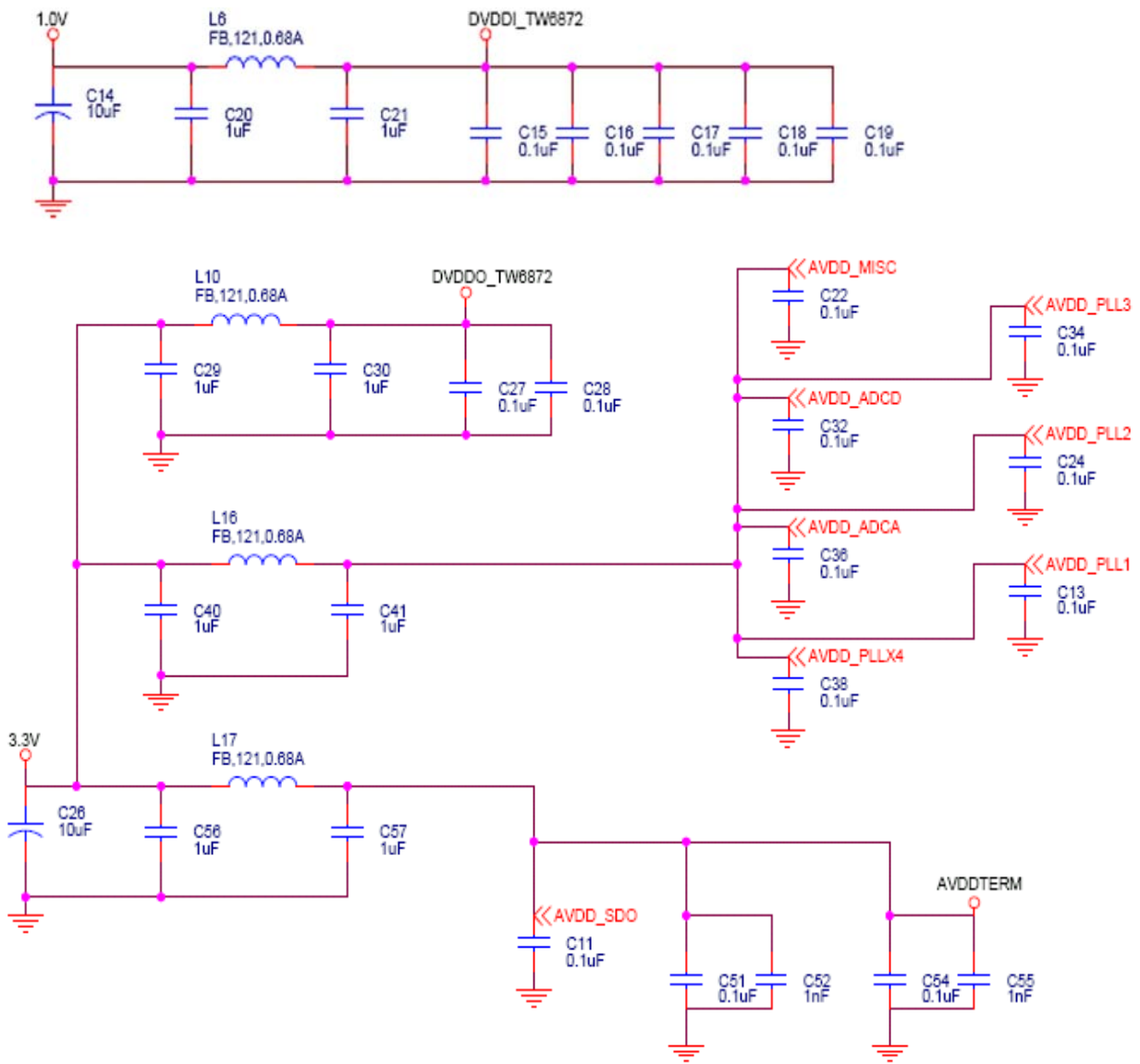


FIGURE 12. TW6872 POWER SUPPLY PINS



PLACE C51/C52 NEAR R1 AND C54/55 NEAR R3

FIGURE 1. POWER SUPPLY ROUTING AND BYPASSING SCHEMATIC

### Parallel Video Routing

The parallel video input pins toggle up to a maximum frequency of 148.5MHz clock. The traces connected to these pins must be matched in length for all 20-bits plus clock.

The LVCMOS traces are typically routed as 50Ω single-ended, but it is not critical. The traces are also allowed to transition between layers for ease of routing. A 33Ω series termination should be placed near each of the ISP's LVCMOS driver pins. Series termination prevents overshoot and ringing, leading to improved EMI performance.

### Power Supply Bypassing

It is important that the various supplies be well bypassed over a wide range of frequencies. A combination of different values of capacitors from 1000pF to 5μF or more with low ESR characteristics is generally required.

### LOCAL BYPASS CAPACITORS

A physically small, low value capacitor should bypass each IC supply pin to ground. Capacitors of 0.1μF offer low impedance in the 10MHz to 20MHz region, and 1000pF capacitors in the 100MHz to 200MHz region. Minimize trace length and vias to minimize inductance and maximize noise rejection.

Figure 13 demonstrates a common but sub optimal PCB layout. The additional trace inductance between the bypass capacitor and the power supply/IC reduces its effectiveness. Figure 14 demonstrates a more optimal layout. In this case there is still series trace inductance (it is impossible to completely eliminate it), but now it is being put to good use, as part of a T-filter, attenuating supply noise before it gets to the IC, and reducing the amount of IC-generated noise that gets injected into the supply. Figures 15 and 16 show the same effect when the bypass capacitor must be placed on the opposite side of the PCB from the IC.

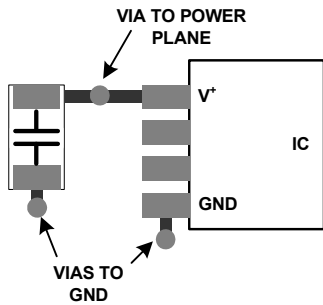


FIGURE 13. SUB-OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT - CAPACITOR AND IC ON SAME PCB LAYER

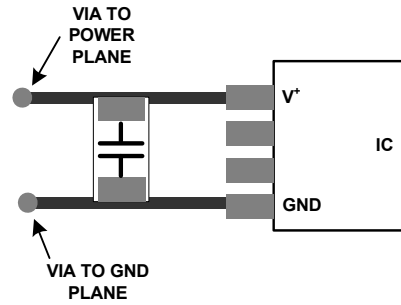


FIGURE 14. OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT - CAPACITOR AND IC ON SAME PCB LAYER (RECOMMENDED)

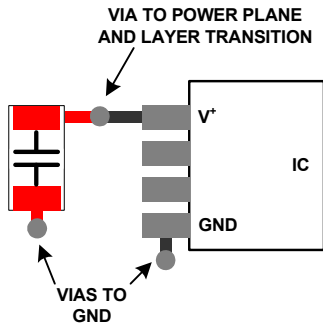


FIGURE 15. SUB-OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT - CAPACITOR AND IC ON OPPOSITE PCB LAYERS

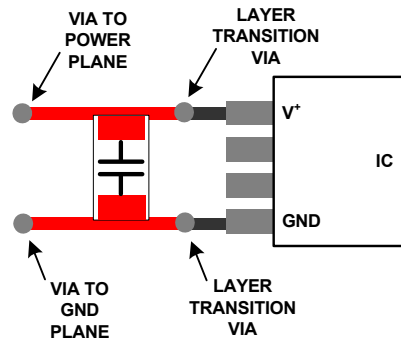


FIGURE 16. OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT - CAPACITOR AND IC ON OPPOSITE PCB LAYERS (RECOMMENDED)

## Other Information

### Power Supply Sequencing

There are no power-up sequencing requirements. However, upon power-up or after a power glitch, and after the power supplies have settled, RSTB must be asserted for 1 $\mu$ s before the TW6872 can be used. For any operating mode change, soft reset followed by the appropriate register configuration must occur.

### Ancillary Data

The TW6872 streams ancillary data such as line number, video payload identifier (VPID), error detection and handling (EDH) or other user defined data per SMPTE 291M. There are four lines per frame that carry ancillary data. ANCO/1/2/3 set the line number. ANCTYPE sets the blanking location. FIFO0/1/2/3CNT set the data byte count.

Audio data is also inserted into the ancillary data space from either the analog audio or I2S interface per SMPTE 299. See [“Audio Input Interface” on page 14](#) for details on how to choose the analog or I2S interface for ancillary audio.

### Hardware Interrupt

The TW6872 provides an interrupt request output using the IRQ pin. The hardware interrupt can be used to indicate when ancillary data has not been transmitted properly and check status of audio detection.

There are four lines per frame to carry ancillary data (not audio), either in HD or SD mode. Whenever an ancillary packet is not completely sent out and is truncated at the end of an ancillary line, an “ancillary data packet miss interrupt” is generated.

ANCTXERRORMASK is used to mask out the four HD mode ancillary line miss, and four SD mode ancillary line miss interrupts. If these are not masked, then an interrupt will be generated if the ancillary packet has been truncated. ANCTXERROR indicates where the failure occurred.

### Crystal and Clock Oscillator

The TW6872 requires an external 27MHz crystal or oscillator. The crystal connects to the XTI/XTO pins. A low ESR, CL = 18pF, 50ppm is recommended.

### Link Checker

The TW6872 has an integrated pseudo random binary sequence (PRBS) 7/23 generator which can be used for bit error rate testing. A bit error would cause one pixel to be the incorrect color for one frame. That wouldn't be noticeable if it only happened once every hour, but might be noticeable if it happened once every minute.

Bit error testing can be used to optimize operation between the TW6872 and the receiver (TW6874 or any other receiver with PRBS 7/23 checker) over the coaxial cable interface. For example, the pre/de-emphasis setting on the TW6872 and/or the receiver's equalizer settings can be adjusted to obtain minimum bit errors, indicating the best settings for that link has been obtained.

## Test Patterns

The TW6872 can generate audio and video test patterns to ease system design. One such pattern is the Checkfield as shown in [Figure 17](#). This pathological image contains two different patterns that can be used to test the link performance in case a PRBS checker is unavailable at the receiver.



FIGURE 17. CHECKFIELD PATTERN

## I<sup>2</sup>C Communication Interface

The TW6872 uses a 2-wire serial bus for communication with its host. The TW6872 operates as a bus slave. SCL is the Serial Clock line, driven by the host, and SDA is the Serial Data line, which can be driven by any device on the bus. SDA is open-drain to allow multiple devices to share the same bus simultaneously. An external pull-up resistor (typically 2.2k $\Omega$  to 4.7k $\Omega$ ) is required for SDA and SCL.

The bus is nominally inactive, with SDA and SCL high. Communication begins when the host issues a START command by taking SDA low while SCL is high ([Figure 19](#)). The TW6872 continuously monitors the SDA and SCL lines for the START condition and will not respond to any command until this condition has been met. The host then transmits the 7-bit slave address plus a R/ $\bar{W}$  bit, indicating if the next transaction will be a Read (R/ $\bar{W}$  = 1) or a Write (R/ $\bar{W}$  = 0).

After transmitting the device address and the R/ $\bar{W}$  bit, the host must release the SDA line while holding SCL low, and wait for an acknowledgment from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDA line low to acknowledge (ACK) the condition ([Figure 20](#)). The host will then continue with the next 8-bit transfer. If no device on the bus responds (NACK, where SDA is kept high during the 9th SCL pulse), the host transmits a STOP condition where SDA rises while SCL is high and ends the cycle ([Figure 19](#)). Notice that a successful transfer always includes nine SCL pulses.

Once the slave address has been transmitted and acknowledged, one byte of information can be written to or read from the slave. Data on the serial bus must be valid for the entire time SCL is high ([Figure 21](#)). Communication with the selected device in the selected direction (read or write) is ended by a STOP command, or a second START command, which is commonly used to reverse data direction without relinquishing the bus.

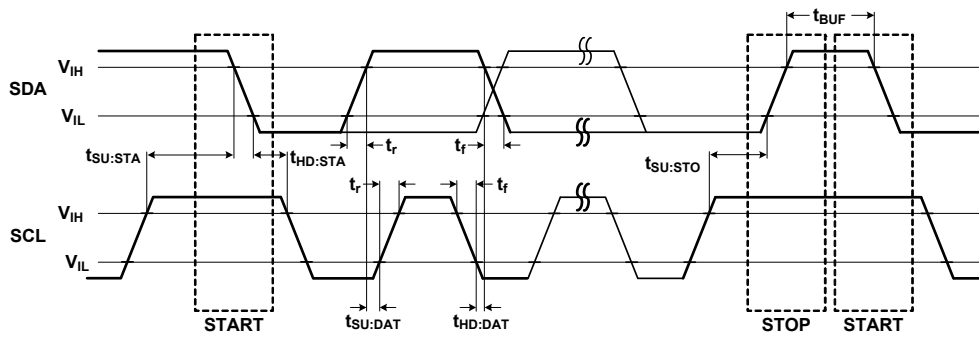


FIGURE 18. I<sup>2</sup>C TIMING DEFINITIONS

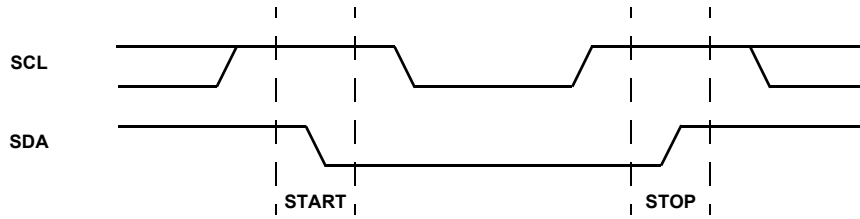


FIGURE 19. VALID START AND STOP CONDITIONS

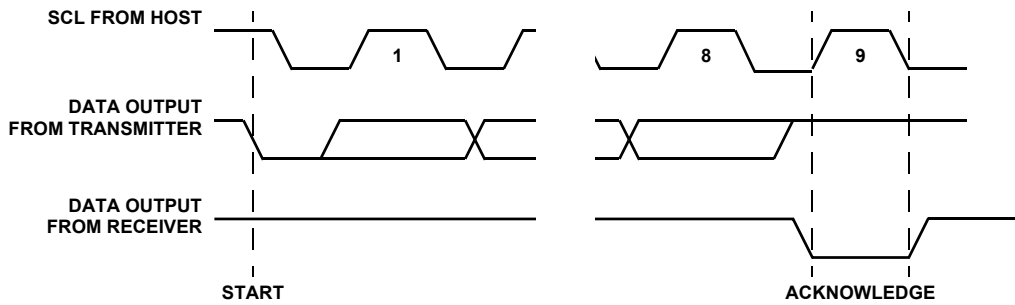


FIGURE 20. ACKNOWLEDGE RESPONSE FROM RECEIVER

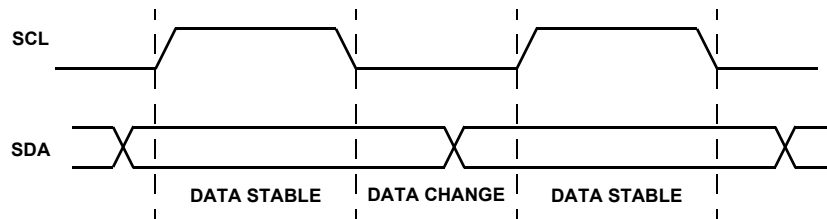


FIGURE 21. VALID DATA CHANGES ON THE SDA BUS

## Configuration Register Write

After receiving the acknowledge bit corresponding to the desired TW6872's slave address byte with  $R/\overline{W} = 0$ , the host sends the desired register address where data is to be written. An internal index register points to this address. After receiving the acknowledge bit corresponding to the desired register address byte, the host sends the data byte to be written. The TW6872 loads the data byte to the register pointed by the internal index register. The TW6872 acknowledges the data write and automatically increments the pointer register to point to the next register address. The host can thus write to sequential ascending register addresses. After each transfer, the TW6872 acknowledges the receipt with an acknowledge pulse. To end all transfers to the TW6872 the host issues a STOP condition.

To write to separate or non-sequential register locations, a full I<sup>2</sup>C START, Device Address ( $R/\overline{W} = 0$ ), Register Address, Data Write/slave ACK..., STOP sequence must be used for each register location.

[Figure 22](#) shows two views of the steps necessary to write one byte to the Configuration Register.

## Configuration Register Read

A TW6872 read cycle has two phases. The first phase is a write to select the desired internal index register. The second phase is the read from the data register. Note that no data is actually written during the first phase.

After receiving the acknowledge bit corresponding to the desired TW6872's slave address byte with  $R/\overline{W} = 0$ , the host sends the desired register address from where data is to be read. An internal index register points to this address. After receiving the acknowledge bit corresponding to the desired register address byte, the host sends either a STOP/START or a REPEATED START condition.

The host then sends the same slave address with  $R/\overline{W} = 1$  to indicate a read. The TW6872 transfers the contents of the desired register during eight SCL pulses (controlled by the host). After transferring the byte, the TW6872 releases SDA and the host acknowledges receipt of the data. The TW6872 automatically increments the pointer register to point to the next register address. The host can thus read from sequential ascending register addresses. The host acknowledges receipt of each byte. To end the read, the host does not acknowledge data receipt, and then issues a STOP condition.

To read from separate or non-sequential register locations, a full I<sup>2</sup>C START, Device Address ( $R/\overline{W} = 0$ ), Register Address, STOP, START, Device Address ( $R/\overline{W} = 1$ ), Data Read/host ACK..., host NACK, STOP sequence must be used for each register location.

[Figure 23](#) shows two views of the steps necessary to read one byte from the Configuration Register.

## I<sup>2</sup>C Slave Address

The TW6872 7-bit I<sup>2</sup>C slave address is 1101000 (binary). The final 8 bit address word transmitted is 1101000r (binary) where "r" is the  $R/\overline{W}$  bit indicating the direction of the next byte(s).

## Register Address

Each configuration register is accessed via a 12-bit address. The upper four bits is the page; the lower byte is the address on the page. The upper four bits of the page is always 0 and should be padded as such to make a full byte. The register map lists each register address in a 12-bit format, for example: 0x123. Hence, this register address's MSB is 0x01 and its LSB is 0x23.

# TW6872

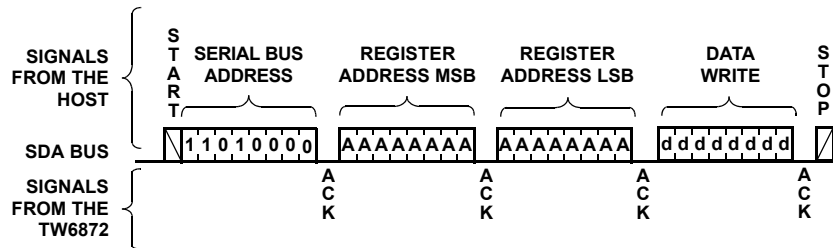
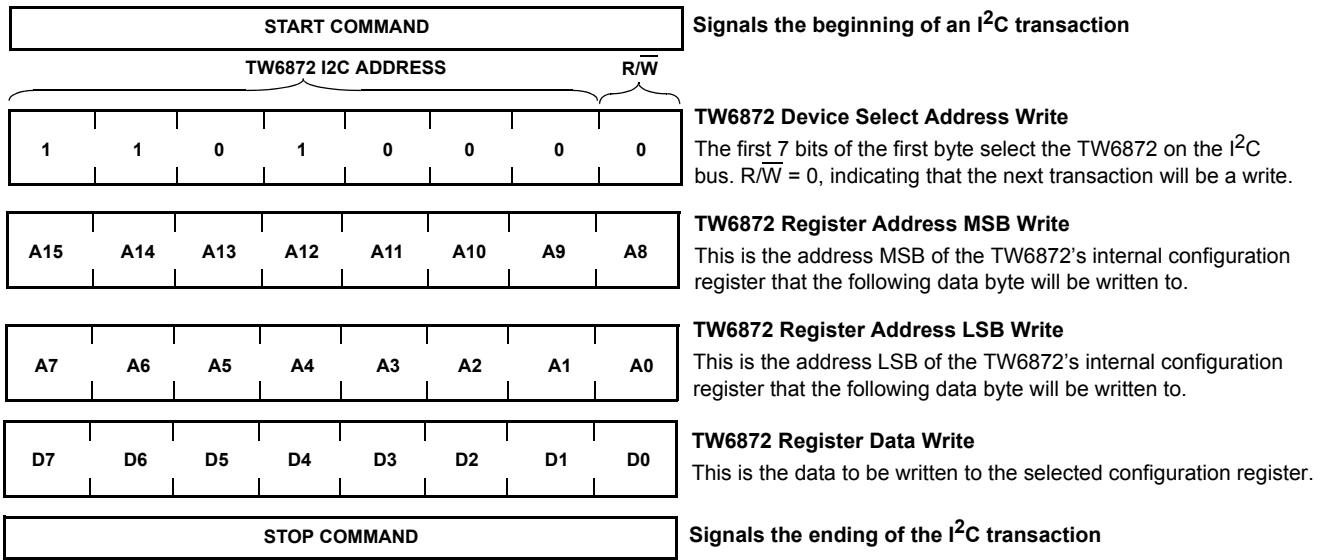


FIGURE 22. CONFIGURATION REGISTER WRITE

# TW6872

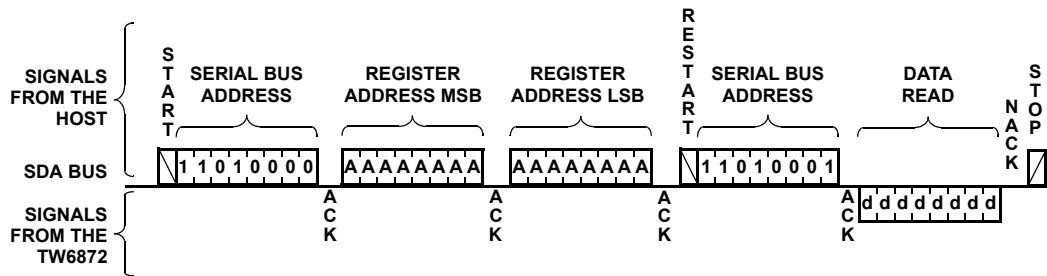
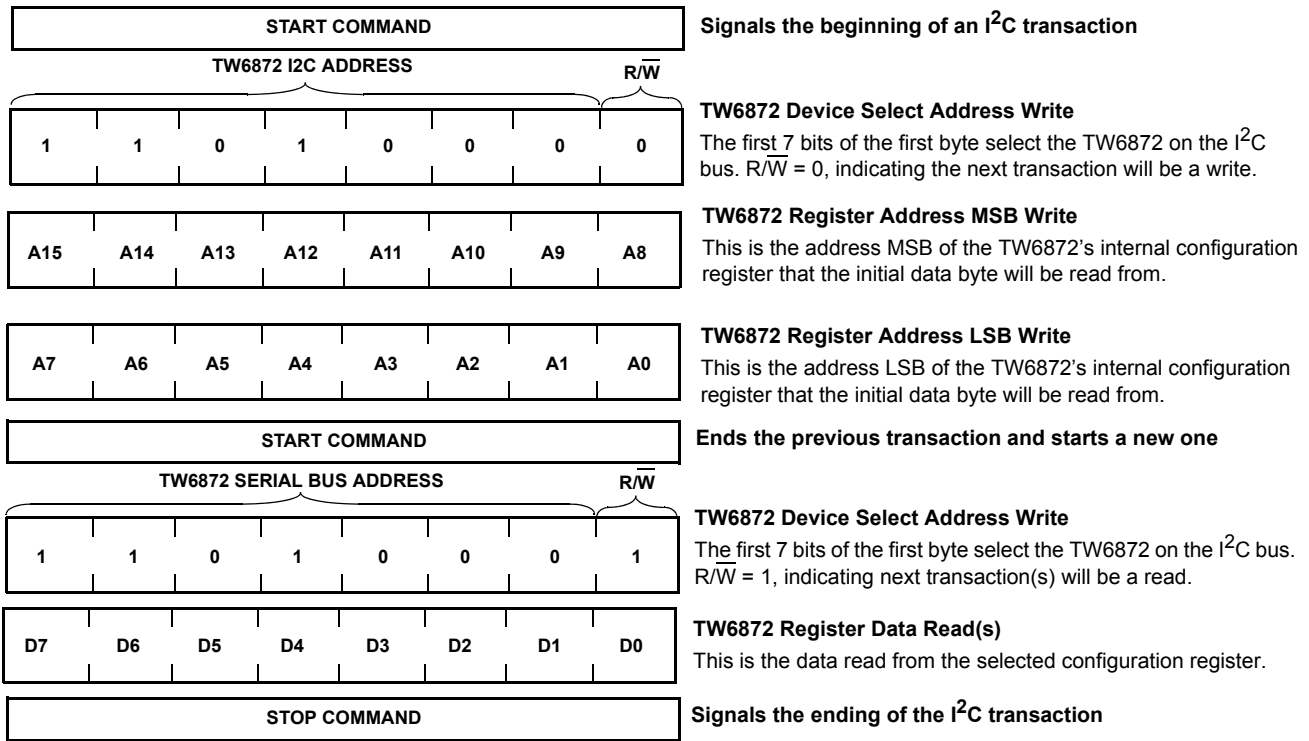


FIGURE 23. CONFIGURATION REGISTER READ



## Register Map

### General

**TABLE 2. VIN\_CTRL: VIDEO INPUT CONTROL** ..... READ-WRITE, DEFAULT=0x00, ADDR=0x010

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	FORMAT	Set video format: 0x0: 720p59.94/60 0x1: 720p50 0x2: 1080i59.94/60 0x3: 1080i50 0x4: 1080p59.94/60 0x5: 1080p50 0x6: 1080p29.97/30 0x7: 1080p25 0x8 NTSC 0x9: PAL 0xA-0xF: reserved	0x0
3	SWAP	YC swap on VD input pins 0: Not swapped 1: Swapped	0
2	RESERVED	Reserved	0
1	VC2ENABLE	VC2 compression 0: Not enabled 1: Enabled	0
0	PATGEN	Selects video source at input 0: External BT.1120 source 1: Internal pattern generator	0

**TABLE 3. TX\_CTRL: TRANSMIT CONTROL** ..... READ-WRITE, DEFAULT=0x00, ADDR=0x011

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	RESERVED	Reserved	0
1:0	RATE	Set TX link speed 0: HD 1: SD/VC2 2: 3G 3: Reserved	0

**TABLE 4. SRST\_CTRL: SYSTEM RESET CONTROL** ..... READ-WRITE, DEFAULT=0x00, ADDR=0x012

BIT	NAME	BIT DEFINITION	DEFAULT
7:5	RESERVED	Reserved	0x0
4	TXRST	Reset SDI TX and PRBS generator blocks. Not self cleared. 0: Normal operation 1: Reset	0
3:2	RESERVED	Reserved	0x0
1	VC2RST	Reset VC2 encoder. Not self cleared. 0: Normal operation 1: Reset	0
0	PIXRST	Reset pattern generator and ASI blocks. Not self cleared. 0: Normal operation 1: Reset	0

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**TABLE 5. DBG\_CTRL: DEBUG CONTROL** ..... READ-WRITE, DEFAULT=0x30, ADDR=0x013

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6	EDH	Insert EDH into SDI stream 0: Do not insert EDH 1: Insert EDH	0
5	LINE	Insert line number into SDI stream 0: Do not insert line number 1: Insert line number	1
4	CRC	Insert CRC into SDI stream 0: Do not insert CRC 1: Insert CRC	1
3:1	RESERVED	Reserved	0x0
0	INTPOL	Interrupt polarity 0: Interrupt is active low 1: Interrupt is active high	0

**TABLE 6. CLK\_CTRL: CLOCK CONTROL** ..... READ-WRITE, DEFAULT=0x00, ADDR=0x014

BIT	NAME	BIT DEFINITION	DEFAULT
7	VDCLKSEL	Video clock selection 0: Input clock from ISP (VD_CLK) 1: Clock internally generated by TW6872 (CLKO). For test purpose only.	0
6	VDCLKINV	Video clock invert 0: Do not invert video clock 1: Invert video clock	0
5	AADCCLKINV	Audio ADC clock invert 0: Do not invert audio ADC clock 1: Invert audio ADC clock	0
4	SDICLKINV	SDI clock invert 0: Do not invert SDI clock 1: Invert SDI clock	0
3	RESERVED	Reserved	0
2	AMCLKPD	AMCLK power-down. This is an internal audio ADC clock. 0: Normal operation 1: Power-down	0
1	CLKOPD	CLKO power-down 0: Normal operation 1: Power-down	0
0	CLK108PD	CLK108 power-down 0: Normal operation 1: Power-down	0

**TABLE 7. PATGEN\_CTRL\_0: PATTERN GENERATOR CONTROL 0** ..... READ-WRITE, DEFAULT=0x00, ADDR=0x015

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	RP219OPT	Select RP 219 color bar option	0x0
5:4	PATSEL	Pattern select 0: RP 219 color bar 1: RP 198 check field 2: 75% color bar 3: Reserved	0x0
3:1	RESERVED	Reserved	0x0
0	PATGENEN	Pattern generator enable 0: Normal operation 1: Enable pattern generator	0