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# Quad (SD/HD) SDI Receiver with Adaptive Equalizer, VC-2 Decoder and Audio CODEC

## TW6874

The TW6874 is a quad (SD/HD) SDI receiver. It has four independent channels, each consisting of an adaptive equalizer, clock data recovery, audio decoder and VC-2 decompression engine. Each channel receives high speed serial data over extended coaxial cable lengths and deserialize the data into video/audio streams for the back-end device.

The video streams are output as: 8-bit BT.656 for SD; BT.1120 in 8/16 bit mode for HD. The audio streams are output through an I2S audio digital interface in a multichannel interleaving format. In addition to the extraction of embedded SDI audio, the TW6874 incorporates a 5-channel audio ADC decoder to decode analog audio inputs and output them through the same I2S interface.

A visually lossless VC-2 (Dirac) compression/decompression engine is implemented in the TW6872/TW6874 SDI Tx/Rx pair to extend the reach of HD-SDI to that of SD-SDI. An interrupt pin can be used to signal the host processor of ancillary data packet detection. Finally, integrated audio test patterns and PRBS checker ease system design and implementation.

## Applications

- SD/HD DVR

## Features

- Quad (SD/HD) SDI receiver for standard (SD) and high (HD) definition 10-bit component video
- Automatic SDI detection of SMPTE 259M Level C (SD-SDI), SMPTE ST 292 (1.5G SDI) signals
- Each SDI input standard supported with ITU-R BT.656 (SD) or ITU-R BT.1120 (1.5G) interface
- Converts 10-bit serial digital component video input to 8-bit parallel video output
- Adaptive equalizer/clock data recovery/VC-2 decompression engine for each channel
- 4 separate video output ports with BT.656/BT.1120 output format
- 5-channel audio ADC (Analog-to-Digital Converter)
- Single multiplexed audio output DAC (Digital-to-Analog Converter)
- Supports I2S master/slave interface for record output and playback input with cascade
- $I^2C$ and SPI interface
- Pb-free (RoHS compliant) 256 ball LFBGA
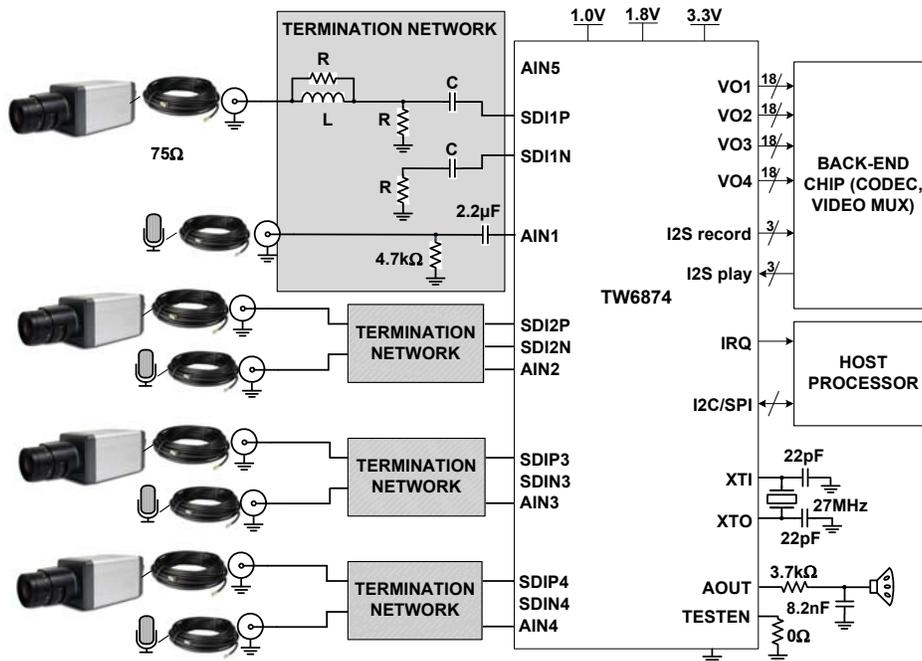


FIGURE 1. TW6874 TYPICAL APPLICATION

# Table of Contents

# Block Diagram



**FIGURE 2. BLOCK DIAGRAM**

# Pin Configuration

TW6874
(256 BALL 13.5mm x 13.5mm LFBGA)
TOP VIEW

## Analog Power

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|
| A | AVSS_CDR1 | AVDD_CDR1 | AVSS_PLL18 | DNC | DNC | DNC | XTO | AVDD_MISC18 | AVDD_GUARD | SPIB | DNC | ASYNP | DNC | TESTEN | MOSI_SDA | ADATR |
| B | SDIP1 | DNC | AVDD_PLL18 | DNC | DNC | DNC | XTI | AVSS_MISC18 | AVSS_GUARD | DNC | ALINKI | DNC | MISO_ADDR1 | ACLKR | SCL | ALINKO |
| C | SDIN1 | AVSS_EQ | AVDD_PLL10 | AVSS_TST1 | AVDD_TST1 | AVSS_ESD | AVDD_XTAL | AVDD_MISC10 | DNC | ADATP | ACLKP | DNC | RSTB | DNC | VD1_14 | VD1_12 |
| D | AVDD_REG1 | AVSS_REG1 | AVSS_PLL10 | AVSS_EQ | AVSS_ESD | AVSS_ESD | AVSS_XTAL | AVSS_MISC10 | DNC | MPP0 | CSB_ADDR0 | IRQ | ASYNR | VD1_13 | VD1_10 | VD1_8 |
| E | AVDD_REG2 | AVSS_REG2 | AVSS_EQ | AVSS_EQ | AVSS_ESD | AVSS_ESD | DVDDE | DVDDE | DVDDE | DVDDE | DVDDE | DVDDI | VD1_15 | VD1_11 | CLKN1 | CLKP1 |
| F | SDIN2 | AVSS_EQ | AVSS_EQ | AVSS_EQ | AVSS_ESD | DVDDE | DVDDE | DVSS | DVSS | DVSS | DVSS | DVDDI | VD1_9 | VD1_7 | VD1_6 | VD1_4 |
| G | SDIP2 | DNC | AVSS_EQ | AVSS_ESD | AVSS_ESD | DVDDE | DVDDE | DVSS | DVSS | DVSS | DVSS | DVDDI | VD1_5 | VD1_3 | VD1_2 | VD1_1 |
| H | AVDD_CDR2 | AVSS_CDR2 | AVDD_BG | AVSS_ESD | AVSS_ESD | AVSS_ESD | DVSS | DVSS | DVSS | DVSS | DVSS | DVDDI | VD1_0 | VD2_14 | VD2_13 | VD2_15 |
| J | AVDD_CDR3 | AVSS_CDR3 | AVSS_BG | AVSS_ESD | AVSS_ESD | AVSS_ESD | DVSS | DVSS | DVSS | DVSS | DVSS | DVDDE | VD2_10 | VD2_8 | VD2_12 | VD2_11 |
| K | SDIP3 | DNC | AVSS_EQ | AVSS_EQ | AVSS_ESD | AVSS_ESD | DVDDI | DVSS | DVSS | DVSS | DVSS | DVDDE | VD2_4 | VD2_6 | VD2_9 | CLKN2 |
| L | SDIN3 | AVSS_EQ | AVSS_EQ | AVSS_EQ | AVSS_ESD | DVDDI | DVDDI | DVSS | DVSS | DVSS | DVSS | DVDDE | VD2_1 | VD2_3 | VD2_7 | CLKP2 |
| M | AVDD_REG3 | AVSS_REG3 | AVSS_EQ | AVSS_EQ | AVSS_ESD | DVDDI | DVDDI | DVDDI | DVDDI | DVDDI | DVDDI | DVDDE | VD3_13 | VD3_15 | VD2_2 | VD2_5 |
| N | AVDD_REG4 | AVSS_REG4 | AVSS_TST4 | AVSS_DAC | AOUT | AIN1 | AVSS_FPLL18 | ADCREF | VD4_5 | VD4_8 | VD4_12 | VD3_2 | VD3_9 | VD3_11 | VD3_12 | VD2_0 |
| P | SDIN4 | AVSS_EQ | AVDD_TST4 | AVDD_DAC | AIN2 | AIN5 | AVDD_FPLL18 | VD4_1 | VD4_3 | VD4_7 | VD4_10 | VD4_14 | VD3_0 | VD3_7 | VD3_10 | VD3_14 |
| R | SDIP4 | DNC | DNC | DNC | AIN3 | AVSS_AFE | AVSS_FPLL10 | VD4_0 | VD4_4 | CLKN4 | VD4_11 | VD4_15 | VD3_3 | VD3_4 | CLKN3 | CLKP3 |
| T | AVSS_CDR4 | AVDD_CDR4 | DNC | DNC | AIN4 | AVDD_AFE | AVDD_FPLL10 | VD4_2 | VD4_6 | CLKP4 | VD4_9 | VD4_13 | VD3_1 | VD3_5 | VD3_6 | VD3_8 |

: Analog 1.0V
: Analog 1.8V
: Analog ground
: VDD/VSS pair

# Pin Configuration (Continued)

TW6874
(256 BALL 13.5mm x 13.5mm LFBGA)
TOP VIEW

## Digital Power

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | AVSS_CDR1 | AVDD_CDR1 | AVSS_PLL18 | DNC | DNC | DNC | XTO | AVDD_MISC18 | AVDD_GUARD | SPIB | DNC | ASYNP | DNC | TESTEN | MOSI_SDA | ADATR |
| B | SDIP1 | DNC | AVDD_PLL18 | DNC | DNC | DNC | XTI | AVSS_MISC18 | AVSS_GUARD | DNC | ALINKI | DNC | MISO_ADDR1 | ACLKR | SCL | ALINKO |
| C | SDIN1 | AVSS_EQ | AVDD_PLL10 | AVSS_TST1 | AVDD_TST1 | AVSS_ESD | AVDD_XTAL | AVDD_MISC10 | DNC | ADATP | ACLKP | DNC | RSTB | DNC | VD1_14 | VD1_12 |
| D | AVDD_REG1 | AVSS_REG1 | AVSS_PLL10 | AVSS_EQ | AVSS_ESD | AVSS_ESD | AVSS_XTAL | AVSS_MISC10 | DNC | MPP0 | CSB_ADDR0 | IRQ | ASYNR | VD1_13 | VD1_10 | VD1_8 |
| E | AVDD_REG2 | AVSS_REG2 | AVSS_EQ | AVSS_EQ | AVSS_ESD | AVSS_ESD | DVDDE | DVDDE | DVDDE | DVDDE | DVDDE | DVDDI | VD1_15 | VD1_11 | CLKN1 | CLKP1 |
| F | SDIN2 | AVSS_EQ | AVSS_EQ | AVSS_EQ | AVSS_ESD | DVDDE | DVDDE | DVSS | DVSS | DVSS | DVSS | DVDDI | VD1_9 | VD1_7 | VD1_6 | VD1_4 |
| G | SDIP2 | DNC | AVSS_EQ | AVSS_ESD | AVSS_ESD | DVDDE | DVDDE | DVSS | DVSS | DVSS | DVSS | DVDDI | VD1_5 | VD1_3 | VD1_2 | VD1_1 |
| H | AVDD_CDR2 | AVSS_CDR2 | AVDD_BG | AVSS_ESD | AVSS_ESD | AVSS_ESD | DVSS | DVSS | DVSS | DVSS | DVSS | DVDDI | VD1_0 | VD2_14 | VD2_13 | VD2_15 |
| J | AVDD_CDR3 | AVSS_CDR3 | AVSS_BG | AVSS_ESD | AVSS_ESD | AVSS_ESD | DVSS | DVSS | DVSS | DVSS | DVSS | DVDDE | VD2_10 | VD2_8 | VD2_12 | VD2_11 |
| K | SDIP3 | DNC | AVSS_EQ | AVSS_EQ | AVSS_ESD | AVSS_ESD | DVDDI | DVSS | DVSS | DVSS | DVSS | DVDDE | VD2_4 | VD2_6 | VD2_9 | CLKN2 |
| L | SDIN3 | AVSS_EQ | AVSS_EQ | AVSS_EQ | AVSS_ESD | DVDDI | DVDDI | DVSS | DVSS | DVSS | DVSS | DVDDE | VD2_1 | VD2_3 | VD2_7 | CLKP2 |
| M | AVDD_REG3 | AVSS_REG3 | AVSS_EQ | AVSS_EQ | AVSS_ESD | DVDDI | DVDDI | DVDDI | DVDDI | DVDDI | DVDDI | DVDDE | VD3_13 | VD3_15 | VD2_2 | VD2_5 |
| N | AVDD_REG4 | AVSS_REG4 | AVSS_TST4 | AVSS_DAC | AOUT | AIN1 | AVSS_FPLL18 | ADCREF | VD4_5 | VD4_8 | VD4_12 | VD3_2 | VD3_9 | VD3_11 | VD3_12 | VD2_0 |
| P | SDIN4 | AVSS_EQ | AVDD_TST4 | AVDD_DAC | AIN2 | AIN5 | AVDD_FPLL18 | VD4_1 | VD4_3 | VD4_7 | VD4_10 | VD4_14 | VD3_0 | VD3_7 | VD3_10 | VD3_14 |
| R | SDIP4 | DNC | DNC | DNC | AIN3 | AVSS_AFE | AVSS_FPLL10 | VD4_0 | VD4_4 | CLKN4 | VD4_11 | VD4_15 | VD3_3 | VD3_4 | CLKN3 | CLKP3 |
| T | AVSS_CDR4 | AVDD_CDR4 | DNC | DNC | AIN4 | AVDD_AFE | AVDD_FPLL10 | VD4_2 | VD4_6 | CLKP4 | VD4_9 | VD4_13 | VD3_1 | VD3_5 | VD3_6 | VD3_8 |

: Digital 1.0V
: Digital 3.3V
: Digital ground

# Pin Configuration (Continued)

TW6874
(256 BALL 13.5mm x 13.5mm LFBGA)
TOP VIEW

## Signals

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | AVSS_CDR1 | AVDD_CDR1 | AVSS_PLL18 | DNC | DNC | DNC | XTO | AVDD_MISC18 | AVDD_GUARD | SPIB | DNC | ASYNP | DNC | TESTEN | MOSI_SDA | ADATR |
| B | SDIP1 | DNC | AVDD_PLL18 | DNC | DNC | DNC | XTI | AVSS_MISC18 | AVSS_GUARD | DNC | ALINKI | DNC | MISO_ADDR1 | ACLKR | SCL | ALINKO |
| C | SDIN1 | AVSS_EQ | AVDD_PLL10 | AVSS_TST1 | AVDD_TST1 | AVSS_ESD | AVDD_XTAL | AVDD_MISC10 | DNC | ADATP | ACLKP | DNC | RSTB | DNC | VD1_14 | VD1_12 |
| D | AVDD_REG1 | AVSS_REG1 | AVSS_PLL10 | AVSS_EQ | AVSS_ESD | AVSS_ESD | AVSS_XTAL | AVSS_MISC10 | DNC | MPP0 | CSB_ADDR0 | IRQ | ASYNR | VD1_13 | VD1_10 | VD1_8 |
| E | AVDD_REG2 | AVSS_REG2 | AVSS_EQ | AVSS_EQ | AVSS_ESD | AVSS_ESD | DVDDE | DVDDE | DVDDE | DVDDE | DVDDE | DVDDI | VD1_15 | VD1_11 | CLKN1 | CLKP1 |
| F | SDIN2 | AVSS_EQ | AVSS_EQ | AVSS_EQ | AVSS_ESD | DVDDE | DVDDE | DVSS | DVSS | DVSS | DVSS | DVDDI | VD1_9 | VD1_7 | VD1_6 | VD1_4 |
| G | SDIP2 | DNC | AVSS_EQ | AVSS_ESD | AVSS_ESD | DVDDE | DVDDE | DVSS | DVSS | DVSS | DVSS | DVDDI | VD1_5 | VD1_3 | VD1_2 | VD1_1 |
| H | AVDD_CDR2 | AVSS_CDR2 | AVDD_BG | AVSS_ESD | AVSS_ESD | AVSS_ESD | DVSS | DVSS | DVSS | DVSS | DVSS | DVDDI | VD1_0 | VD2_14 | VD2_13 | VD2_15 |
| J | AVDD_CDR3 | AVSS_CDR3 | AVSS_BG | AVSS_ESD | AVSS_ESD | AVSS_ESD | DVSS | DVSS | DVSS | DVSS | DVSS | DVDDE | VD2_10 | VD2_8 | VD2_12 | VD2_11 |
| K | SDIP3 | DNC | AVSS_EQ | AVSS_EQ | AVSS_ESD | AVSS_ESD | DVDDI | DVSS | DVSS | DVSS | DVSS | DVDDE | VD2_4 | VD2_6 | VD2_9 | CLKN2 |
| L | SDIN3 | AVSS_EQ | AVSS_EQ | AVSS_EQ | AVSS_ESD | DVDDI | DVDDI | DVSS | DVSS | DVSS | DVSS | DVDDE | VD2_1 | VD2_3 | VD2_7 | CLKP2 |
| M | AVDD_REG3 | AVSS_REG3 | AVSS_EQ | AVSS_EQ | AVSS_ESD | DVDDI | DVDDI | DVDDI | DVDDI | DVDDI | DVDDI | DVDDE | VD3_13 | VD3_15 | VD2_2 | VD2_5 |
| N | AVDD_REG4 | AVSS_REG4 | AVSS_TST4 | AVSS_DAC | AOUT | AIN1 | AVSS_FPLL18 | ADCREF | VD4_5 | VD4_8 | VD4_12 | VD3_2 | VD3_9 | VD3_11 | VD3_12 | VD2_0 |
| P | SDIN4 | AVSS_EQ | AVDD_TST4 | AVDD_DAC | AIN2 | AIN5 | AVDD_FPLL18 | VD4_1 | VD4_3 | VD4_7 | VD4_10 | VD4_14 | VD3_0 | VD3_7 | VD3_10 | VD3_14 |
| R | SDIP4 | DNC | DNC | DNC | AIN3 | AVSS_AFE | AVSS_FPLL10 | VD4_0 | VD4_4 | CLKN4 | VD4_11 | VD4_15 | VD3_3 | VD3_4 | CLKN3 | CLKP3 |
| T | AVSS_CDR4 | AVDD_CDR4 | DNC | DNC | AIN4 | AVDD_AFE | AVDD_FPLL10 | VD4_2 | VD4_6 | CLKP4 | VD4_9 | VD4_13 | VD3_1 | VD3_5 | VD3_6 | VD3_8 |

Legend:
- : Analog SDI input signals
- : Analog audio I/O signals
- : X-tal I/O pins
- : DNC & Misc pins
- : CH1 digital output port
- : CH2 digital output port
- : CH3 digital output port
- : CH4 digital output port

# Pin Descriptions

| PIN LOCATION | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| B1 | SDIP1 | Analog Input | SDI input for channel 1. Terminate with 75Ω to ground and AC-couple with 1µF. |
| C1 | SDIN1 | Analog Input | Inverting SDI input for channel 1. Terminate with 37.4Ω to ground and AC-couple with 1µF. Do not connect the external SDI signal to this pin. |
| G1 | SDIP2 | Analog Input | SDI input for channel 2. Terminate with 75Ω to ground and AC-couple with 1µF. |
| F1 | SDIN2 | Analog Input | Inverting SDI input for channel 2. Terminate with 37.4Ω to ground and AC-couple with 1µF. Do not connect the external SDI signal to this pin. |
| K1 | SDIP3 | Analog Input | SDI input for channel 3. Terminate with 75Ω to ground and AC-couple with 1µF. |
| L1 | SDIN3 | Analog Input | Inverting SDI input for channel 3. Terminate with 37.4Ω to ground and AC-couple with 1µF. Do not connect the external SDI signal to this pin. |
| R1 | SDIP4 | Analog Input | SDI input for channel 4. Terminate with 75Ω to ground and AC-couple with 1µF. |
| P1 | SDIN4 | Analog Input | Inverting SDI input for channel 4. Terminate with 37.4Ω to ground and AC-couple with 1µF. Do not connect the external SDI signal to this pin. |
| N6 | AIN1 | Analog Input | Audio input for channel 1. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF. |
| P5 | AIN2 | Analog Input | Audio input for channel 2. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF. |
| R5 | AIN3 | Analog Input | Audio input for channel 3. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF. |
| T5 | AIN4 | Analog Input | Audio input for channel 4. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF. |
| P6 | AIN5 | Analog Input | Audio input for channel 5. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF. |
| N8 | ADCREF | Analog Input | Audio ADC reference. Terminate with 2.2µF to ground. Do not connect external audio signal to this pin. |
| N5 | AOUT | Analog Output | Analog audio output. |
| H13 | VD1_0 | Digital Output | Video data output for channel 1. |
| G16 | VD1_1 | Digital Output | Video data output for channel 1. |
| G15 | VD1_2 | Digital Output | Video data output for channel 1. |
| G14 | VD1_3 | Digital Output | Video data output for channel 1. |
| F16 | VD1_4 | Digital Output | Video data output for channel 1. |
| G13 | VD1_5 | Digital Output | Video data output for channel 1. |
| F15 | VD1_6 | Digital Output | Video data output for channel 1. |
| F14 | VD1_7 | Digital Output | Video data output for channel 1. |
| D16 | VD1_8 | Digital Output | Video data output for channel 1. |
| F13 | VD1_9 | Digital Output | Video data output for channel 1. |
| D15 | VD1_10 | Digital Output | Video data output for channel 1. |
| E14 | VD1_11 | Digital Output | Video data output for channel 1. |
| C16 | VD1_12 | Digital Output | Video data output for channel 1. |
| D14 | VD1_13 | Digital Output | Video data output for channel 1. |
| C15 | VD1_14 | Digital Output | Video data output for channel 1. |
| E13 | VD1_15 | Digital Output | Video data output for channel 1. |
| E16 | CLKP1 | Digital Output | Reserved |
| E15 | CLKN1 | Digital Output | Clock for VD1. |
| N16 | VD2_0 | Digital Output | Video data output for channel 2. |

# TW6874

## Pin Descriptions (Continued)

| PIN LOCATION | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| L13 | VD2_1 | Digital Output | Video data output for channel 2. |
| M15 | VD2_2 | Digital Output | Video data output for channel 2. |
| L14 | VD2_3 | Digital Output | Video data output for channel 2. |
| K13 | VD2_4 | Digital Output | Video data output for channel 2. |
| M16 | VD2_5 | Digital Output | Video data output for channel 2. |
| K14 | VD2_6 | Digital Output | Video data output for channel 2. |
| L15 | VD2_7 | Digital Output | Video data output for channel 2. |
| J14 | VD2_8 | Digital Output | Video data output for channel 2. |
| K15 | VD2_9 | Digital Output | Video data output for channel 2. |
| J13 | VD2_10 | Digital Output | Video data output for channel 2. |
| J16 | VD2_11 | Digital Output | Video data output for channel 2. |
| J15 | VD2_12 | Digital Output | Video data output for channel 2. |
| H15 | VD2_13 | Digital Output | Video data output for channel 2. |
| H14 | VD2_14 | Digital Output | Video data output for channel 2. |
| H16 | VD2_15 | Digital Output | Video data output for channel 2. |
| L16 | CLKP2 | Digital Output | Reserved |
| K16 | CLKN2 | Digital Output | Clock for VD2. |
| P13 | VD3_0 | Digital Output | Video data output for channel 3. |
| T13 | VD3_1 | Digital Output | Video data output for channel 3. |
| N12 | VD3_2 | Digital Output | Video data output for channel 3. |
| R13 | VD3_3 | Digital Output | Video data output for channel 3. |
| R14 | VD3_4 | Digital Output | Video data output for channel 3. |
| T14 | VD3_5 | Digital Output | Video data output for channel 3. |
| T15 | VD3_6 | Digital Output | Video data output for channel 3. |
| P14 | VD3_7 | Digital Output | Video data output for channel 3. |
| T16 | VD3_8 | Digital Output | Video data output for channel 3. |
| N13 | VD3_9 | Digital Output | Video data output for channel 3. |
| P15 | VD3_10 | Digital Output | Video data output for channel 3. |
| N14 | VD3_11 | Digital Output | Video data output for channel 3. |
| N15 | VD3_12 | Digital Output | Video data output for channel 3. |
| M13 | VD3_13 | Digital Output | Video data output for channel 3. |
| P16 | VD3_14 | Digital Output | Video data output for channel 3. |
| M14 | VD3_15 | Digital Output | Video data output for channel 3. |
| R16 | CLKP3 | Digital Output | Reserved |
| R15 | CLKN3 | Digital Output | Clock for VD3. |
| R8 | VD4_0 | Digital Output | Video data output for channel 4. |
| P8 | VD4_1 | Digital Output | Video data output for channel 4. |
| T8 | VD4_2 | Digital Output | Video data output for channel 4. |
| P9 | VD4_3 | Digital Output | Video data output for channel 4. |
| R9 | VD4_4 | Digital Output | Video data output for channel 4. |
| N9 | VD4_5 | Digital Output | Video data output for channel 4. |

# TW6874

## Pin Descriptions (Continued)

| PIN LOCATION | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| T9 | VD4_6 | Digital Output | Video data output for channel 4. |
| P10 | VD4_7 | Digital Output | Video data output for channel 4. |
| N10 | VD4_8 | Digital Output | Video data output for channel 4. |
| T11 | VD4_9 | Digital Output | Video data output for channel 4. |
| P11 | VD4_10 | Digital Output | Video data output for channel 4. |
| R11 | VD4_11 | Digital Output | Video data output for channel 4. |
| N11 | VD4_12 | Digital Output | Video data output for channel 4. |
| T12 | VD4_13 | Digital Output | Video data output for channel 4. |
| P12 | VD4_14 | Digital Output | Video data output for channel 4. |
| R12 | VD4_15 | Digital Output | Video data output for channel 4. |
| T10 | CLKP4 | Digital Output | Reserved |
| R10 | CLKN4 | Digital Output | Clock for VD4. |
| D12 | IRQ | Digital Output | Interrupt request. |
| B11 | ALINKI | Digital Input | Serial audio multidevice link input. |
| B16 | ALINKO | Digital Output | Serial audio multidevice link output. |
| C11 | ACLKP | Digital I/O | Serial audio playback clock input/output. |
| A12 | ASYNP | Digital I/O | Serial audio playback sync input/output. |
| C10 | ADATP | Digital Input | Serial audio playback data input. |
| B14 | ACLKR | Digital I/O | Serial audio record clock input/output. |
| D13 | ASYNR | Digital I/O | Serial audio record sync input/output. |
| A16 | ADATR | Digital Output | Serial audio record data output. |
| A10 | SPIB | Digital Input | LO: Enable SPI interface.<br>HI: Enable $I^2C$ interface. |
| B15 | SCL | Digital Input | SPI/$I^2C$ clock input. $I^2C$ interface requires pull-up resistor to DVDDE. |
| A15 | MOSI_SDA | Digital I/O | SPI: Serial data input.<br>$I^2C$: Serial data I/O. $I^2C$ interface requires pull-up resistor to DVDDE. |
| B13 | MISO_ADDR1 | Digital I/O | SPI: Serial data output.<br>$I^2C$: Bit 1 of slave address select. |
| D11 | CSB_ADDR0 | Digital Input | SPI: chip-select. SPI interface is active when LO.<br>$I^2C$: Bit 0 of slave address select.<br>ADDR1 ADDR0 address<br>LO LO 0x68<br>LO HI 0x69<br>HI LO 0x6A<br>HI HI 0x6B |
| C13 | RSTB | Digital Input | Resets device when pulled LO. |
| A14 | TESTEN | Digital Input | For internal use only. Tie LO. |
| D10 | MPP0 (= ADATM) | Digital Output | The ADATM is the serial audio mix data output. The ADATM outputs through the MPP0 pin. |
| A4, A5, A6, A11, A13, B2, B4, B5, B6, B10, B12, C9, C12, C14, D9, G2, K2, R2, R3, R4, T3, T4 | DNC | Do Not Connect | Do not connect anything to these pins. |
| A7 | XTO | Analog Output | 27MHz crystal connection. |
| B7 | XTI | Analog Input | 27MHz crystal connection or 27MHz/1.0V oscillator input. |

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## Pin Descriptions (Continued)

| PIN LOCATION | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| A2 | AVDD_CDR1 | Analog Power | 1.0V analog power supply for CDR. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| A1 | AVSS_CDR1 | Analog Ground | Analog ground. |
| H1 | AVDD_CDR2 | Analog Power | 1.0V analog power supply for CDR. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| H2 | AVSS_CDR2 | Analog Ground | Analog ground. |
| J1 | AVDD_CDR3 | Analog Power | 1.0V analog power supply for CDR. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| J2 | AVSS_CDR3 | Analog Ground | Analog ground. |
| T2 | AVDD_CDR4 | Analog Power | 1.0V analog power supply for CDR. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| T1 | AVSS_CDR4 | Analog Ground | Analog ground. |
| C2, D4, E3, E4, F2, F3, F4, G3, K3, K4, L2, L3, L4, M3, M4, P2 | AVSS_EQ | Analog Ground | Analog ground. |
| D1 | AVDD_REG1 | Analog Power | 1.8V analog power supply for regulator. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| D2 | AVSS_REG1 | Analog Ground | Analog ground. |
| E1 | AVDD_REG2 | Analog Power | 1.8V analog power supply for regulator. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| E2 | AVSS_REG2 | Analog Ground | Analog ground. |
| M1 | AVDD_REG3 | Analog Power | 1.8V analog power supply for regulator. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| M2 | AVSS_REG3 | Analog Ground | Analog ground. |
| N1 | AVDD_REG4 | Analog Power | 1.8V analog power supply for regulator. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| N2 | AVSS_REG4 | Analog Ground | Analog ground. |
| H3 | AVDD_BG | Analog Power | 1.8V analog power supply for band-gap. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| J3 | AVSS_BG | Analog Ground | Analog ground. |
| C5 | AVDD_TST1 | Analog Power | 1.0V analog power supply for test outputs. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| C4 | AVSS_TST1 | Analog Ground | Analog ground. |
| P3 | AVDD_TST4 | Analog Power | 1.0V analog power supply for test outputs. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| N3 | AVSS_TST4 | Analog Ground | Analog ground. |
| P4 | AVDD_DAC | Analog Power | 1.8V analog power supply for audio DAC. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| N4 | AVSS_DAC | Analog Ground | Analog ground. |
| T6 | AVDD_AFE | Analog Power | 1.8V analog power supply for audio AFE (Audio Front-End). Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| R6 | AVSS_AFE | Analog Ground | Analog ground. |
| T7 | AVDD_FPLL10 | Analog Power | 1.0V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| R7 | AVSS_FPLL10 | Analog Ground | Analog ground. |
| P7 | AVDD_FPLL18 | Analog Power | 1.8V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |

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## Pin Descriptions (Continued)

| PIN LOCATION | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| N7 | AVSS_FPLL18 | Analog Ground | Analog ground. |
| A9 | AVDD_GUARD | Analog Power | 1.0V analog power supply guard ring. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| B9 | AVSS_GUARD | Analog Ground | Analog ground. |
| C8 | AVDD_MISC10 | Analog Power | 1.0V analog miscellaneous power supply. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| D8 | AVSS_MISC10 | Analog Ground | Analog ground. |
| A8 | AVDD_MISC18 | Analog Power | 1.8V analog miscellaneous power supply. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| B8 | AVSS_MISC18 | Analog Ground | Analog ground. |
| C7 | AVDD_XTAL | Analog Power | 1.0V analog power supply for crystal oscillator. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| D7 | AVSS_XTAL | Analog Ground | Analog ground. |
| C3 | AVDD_PLL10 | Analog Power | 1.0V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| D3 | AVSS_PLL10 | Analog Ground | Analog ground. |
| B3 | AVDD_PLL18 | Analog Power | 1.8V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible. |
| A3 | AVSS_PLL18 | Analog Ground | Analog ground. |
| C6, D5, D6, E5, E6, F5, G4, G5, H4, H5, H6, J4, J5, J6, K5, K6, L5, M5 | AVSS_ESD | Analog Ground | Analog ground. |
| E7, E8, E9, E10, E11, F6, F7, G6, G7, J12, K12, L12, M12 | DVDDE | Digital Power | 3.3V digital power supply for I/O. Place a local 0.1µF ceramic bypass capacitor to the digital ground as close to the pin as possible. |
| E12, F12, G12, H12, K7, L6, L7, M6, M7, M8, M9, M10, M11 | DVDDI | Digital Power | 1.0V digital power supply for core. Place a local 0.1µF ceramic bypass capacitor to the digital ground as close to the pin as possible. |
| F8, F9, F10, F11, G8, G9, G10, G11, H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11 | DVSS | Digital Ground | Digital ground. |

## Ordering Information

| PART NUMBER (Notes 1, 2) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (RoHS Compliant) | PKG. DWG. # |
|---|---|---|---|---|
| TW6874-BB1-CR | TW6874 BB1-CR | 0 to +70 | 256 ball LFBGA (13.5mmx13.5mm) | V256.13.5x13.5 |
| TW6874-BB1-CR-EVALZ | Evaluation Board | | | |

NOTES:
1. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCuNi- e8 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see product information page for TW6874. For more information on MSL please see tech brief TB363.

## Absolute Maximum Ratings

Supply Pins

AVDD_CDR1 to AVSS_CDR1 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
AVDD_CDR2 to AVSS_CDR2 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
AVDD_CDR3 to AVSS_CDR3 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
AVDD_CDR4 to AVSS_CDR4 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
AVDD_FPLL10 to AVSS_FPLL10 . . . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
AVDD_PLL10 to AVSS_PLL10 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
AVDD_XTAL to AVSS_XTAL . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
AVDD_MISC10 to AVSS_MISC10 . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
AVDD_GUARD to AVSS_GUARD . . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
AVDD_TST1 to AVSS_TST1 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
AVDD_TST4 to AVSS_TST4 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
AVDD_BG to AVSS_BG . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +2.5V
AVDD_REG1 to AVSS_REG1 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +2.5V
AVDD_REG2 to AVSS_REG2 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +2.5V
AVDD_REG3 to AVSS_REG3 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +2.5V
AVDD_REG4 to AVSS_REG4 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +2.5V
AVDD_AFE to AVSS_AFE . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +2.5V
AVDD_DAC to AVSS_DAC. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +2.5V
AVDD_FPLL18 to AVSS_FPLL18 . . . . . . . . . . . . . . . . . . . . . . . . . +2.5V
AVDD_PLL18 to AVSS_PLL18 . . . . . . . . . . . . . . . . . . . . . . . . . . . +2.5V
AVDD_MISC18 to AVSS_MISC18 . . . . . . . . . . . . . . . . . . . . . . . . +2.5V
DVDDI to DVSS . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +1.2V
DVDDE to DVSS. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +4.0V

Other Pins

Analog Audio Input Voltage. . . . . . . . . . . . . AVSS_AFE V to AVDD_AFE V
Analog Audio Output Voltage . . . . . . . . . . . AVSS_DAC V to AVDD_DAC V
Voltage on any Digital Pin . . . . . . . . . . . . . . . . . . . . . DVSS V to DVDDE V

ESD Ratings

Human Body Model (JS-001-2010) . . . . . . . . . . . . . . . . . . . . . . . . . . 2kV
Charged Device Model (JESD22-C101E) . . . . . . . . . . . . . . . . . . . . . 750V

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| LFBGA Package (Notes 3, 4). . . . . . . . . . . . | 22.7 | 7.9 |

Power Dissipation. . . . . . . . . . . . . . . See Electrical Specifications page 14
Maximum Die Temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +125°C
Storage Temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .-65°C to +150°C
Pb-free Reflow Profile . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . see TB493

## Recommended Operating Conditions

Ambient Operating Temperature . . . . . . . . . . . . . . . . . . . . . . . 0°C to +70°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

3. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

4. For $\theta_{JC}$, the "case temp" location is taken at the package top center.

# TW6874

**Electrical Specifications**   AVDD_1V0 = AVDD_CDR1 = AVDD_CDR2 = AVDD_CDR3 = AVDD_CDR4 = AVDD_PLL10 = AVDD_FPLL10 = AVDD_XTAL = AVDD_MISC10 = AVDD_GUARD = AVDD_TST1 = AVDD_TST4 = 1.0V, AVDD_1V8 = AVDD_BG = AVDD_REG1 = AVDD_REG2 = AVDD_REG3 = AVDD_REG4 = AVDD_AFE = AVDD_PLL18 = AVDD_FPLL18 = AVDD_MISC18 = AVDD_DAC = 1.8V, DVDD_1V0 = DVDDI = 1.0V, DVDD_3V3 = DVDDE = 3.3V, $T_A$ = +25°C, unless otherwise specified.

| PARAMETER | DESCRIPTION | TEST CONDITIONS | MIN (Note 5) | TYP | MAX (Note 5) | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY VOLTAGE** | | | | | | |
| AVDD_1V0 | Analog 1.0V Supply Voltage | | 0.95 | 1.0 | 1.05 | V |
| AVDD_1V8 | Analog 1.8V Supply Voltage | | 1.7 | 1.8 | 1.9 | V |
| DVDD_1V0 | Digital 1.0V Core Supply Voltage | | 0.95 | 1.0 | 1.05 | V |
| DVDD_3V3 | Digital 3.3V IO Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| **POWER DISSIPATION** | | | | | | |
| I_AVDD_1V0 | Analog 1.0V Supply Current | | | 250 | | mA |
| I_AVDD_1V8 | Analog 1.8V Supply Current | | | 450 | | mA |
| I_DVDD_1V0 | Digital 1.0V Core Supply Current | | | 400 | | mA |
| I_DVDD_3V3 | Digital 3.3V IO Supply Current | 16-bit | | 85 | | mA |
| | | 8-bit | | 215 | | mA |
| $P_{TOTAL}$ | Total Power | 16-bit | | 1740 | | mW |
| | | 8-bit | | 2170 | | mW |
| **PARALLEL VIDEO OUTPUT (Note 8)** | | | | | | |
| $f_{CLK}$ | Pixel Clock Frequency | SD 270Mbps uncompressed serial data input to 8-bit parallel output format. Figure 5 | | 27 | | MHz |
| | | 1. HD 1.485Gbps uncompressed serial data input to 16-bit parallel output format. Figure 6.<br>2. HD 270Mbps compressed serial data input to 16-bit parallel output format. Figure 6. | | 74.25 | | MHz |
| | | 1. HD 1.485Gbps uncompressed serial data input to 8-bit parallel output format. Figure 7.<br>2. HD 270Mbps compressed serial data input to 8-bit parallel output format. Figure 7. | | 148.5 | | MHz |
| DCYC | Pixel Clock Duty Cycle | | 45 | | 55 | % |
| $t_S$ | Setup Time (1a in Figure 4) | From VDn transition to rising edge of CLKNn | 3 | | | ns |
| $t_H$ | Hold Time (1b in Figure 4) | From rising edge of CLKNn to VDn transition | 0.5 | | | ns |
| **SDI ANALOG INPUTS** | | | | | | |
| SDR | Serial Data Rate | | 0.27 | | 1.5 | Gbps |
| VIS | Serial Data Input Swing | | | | 880 | mV |
| CL59 | Achievable Cable Length RG59 (Note 6) | 1.485Gbps | | 150 | | m |
| | | 270Mbps (SD or VC-2) | | 300 | | m |
| CL3C2V | Achievable Cable Length 3C-2V (Note 6) | 1.485Gbps | | 70 | | m |
| | | 270Mbps (SD or VC-2) | | 120 | | m |
| **DIGITAL INPUTS** | | | | | | |
| VIH | Input High Voltage | | 2.0 | | DVDD_3V3 | V |
| VIL | Input Low Voltage | | 0 | | 0.8 | V |
| $I_L$ | Input Leakage Current | | -10 | 0 | +10 | µA |
| $C_{IN}$ | Input Capacitance | f = 1MHz, $V_{IN}$ 2.4V | | 2 | | pF |

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AVDD_1V0 = AVDD_CDR1 = AVDD_CDR2 = AVDD_CDR3 = AVDD_CDR4 = AVDD_PLL10 = AVDD_FPLL10 = AVDD_XTAL = AVDD_MISC10 = AVDD_GUARD = AVDD_TST1 = AVDD_TST4 = 1.0V, AVDD_1V8 = AVDD_BG = AVDD_REG1 = AVDD_REG2 = AVDD_REG3 = AVDD_REG4 = AVDD_AFE = AVDD_PLL18 = AVDD_FPLL18 = AVDD_MISC18 = AVDD_DAC = 1.8V, DVDD_1V0 = DVDDI = 1.0V, DVDD_3V3 = DVDDE = 3.3V, T<sub>A</sub> = +25°C, unless otherwise specified. **(Continued)**

| PARAMETER | DESCRIPTION | TEST CONDITIONS | MIN (Note 5) | TYP | MAX (Note 5) | UNITS |
|---|---|---|---|---|---|---|
| **DIGITAL OUTPUTS** | | | | | | |
| VOH | Output High Voltage | IO = -2mA | 2.4 | | | V |
| VOL | Output Low Voltage | IO = +2mA | | | 0.4 | V |
| $I_{OZ}$ | Tri-State Current | | | | 10 | µA |
| **CRYSTAL** | | | | | | |
| $f_{XTAL}$ | Nominal Frequency (Fundamental) | | | 27 | | MHz |
| $DEV_{XTAL}$ | Deviation (Note 7) | | | | ±30 | ppm |
| CL | Load Capacitance | | | 22 | | pF |
| RS | Series Resistor (ESR) | | | 50 | | Ω |
| **ANALOG AUDIO INPUT** | | | | | | |
| ViFULL | Full Scale Input Voltage Range (Note 9) | | 0.13 | | 1.76 | $V_{P-P}$ |
| | Interchannel Isolation (Note 10) | | | 90 | | dB |
| **ANALOG AUDIO OUTPUT** | | | | | | |
| VOFULL | Full Scale Output Voltage (Note 11) | | | 1.4 | | $V_{P-P}$ |
| | Total Harmonic Distortion (THD) | | | 51 | | dB |
| | Signal to Noise Ratio (SNR) | | | 64 | | dB |
| **DIGITAL AUDIO** | | | | | | |
| $t_{A\_pd}$ | ASYNR, ADATR, ADATM Propagation Delay | | 1.0 | | 4 | ns |
| $t_{A\_hw}$ | ACLKP High Pulse Duration | | 27 | | | ns |
| $t_{A\_lw}$ | ACLKP Low Pulse Duration (Note 12) | | 54 | | | ns |
| $t_{A\_su}$ | ASYNP, ADATP Setup Time (Note 12) | | 26 | | | ns |
| $t_{A\_h}$ | ASYNP, ADATP Hold Time | | 25 | | | ns |
| **I²C SERIAL CONFIGURATION INTERFACE (Figure 25)** | | | | | | |
| $f_{SCL}$ | SCL Clock Frequency | | | | 400 | kHz |
| $t_{SU:STA}$ | Set-up Time for a START Condition | | 370 | | | ns |
| $t_{HD:STA}$ | Hold Time for a START Condition | | 74 | | | ns |
| $t_{SU:STO}$ | Set-up Time for a STOP Condition | | 370 | | | ns |
| $t_{BUF}$ | Bus Free Time between a STOP and START Condition | | 740 | | | ns |
| $t_{SU:DAT}$ | Data Set-up Time | | 74 | | | ns |
| $t_{HD:DAT}$ | Data Hold Time | | 50 | | 900 | ns |
| $t_r$ | Rise Time of SDA and SCL | | | | 300 | ns |
| $t_f$ | Fall Time of SDA and SCL | | | | 300 | ns |
| CBUS | Capacitive Load for each Bus Line | | | | 400 | pF |

# TW6874

## Electrical Specifications
AVDD_1V0 = AVDD_CDR1 = AVDD_CDR2 = AVDD_CDR3 = AVDD_CDR4 = AVDD_PLL10 = AVDD_FPLL10 = AVDD_XTAL = AVDD_MISC10 = AVDD_GUARD = AVDD_TST1 = AVDD_TST4 = 1.0V, AVDD_1V8 = AVDD_BG = AVDD_REG1 = AVDD_REG2 = AVDD_REG3 = AVDD_REG4 = AVDD_AFE = AVDD_PLL18 = AVDD_FPLL18 = AVDD_MISC18 = AVDD_DAC = 1.8V, DVDD_1V0 = DVDDI = 1.0V, DVDD_3V3 = DVDDE = 3.3V, $T_A$ = +25°C, unless otherwise specified. **(Continued)**

| PARAMETER | DESCRIPTION | TEST CONDITIONS | MIN (Note 5) | TYP | MAX (Note 5) | UNITS |
|---|---|---|---|---|---|---|
| **SPI SERIAL CONFIGURATION INTERFACE (Figures 31 and 32)** | | | | | | |
| $f_{SER}$ | SCL Maximum Operating Frequency | | | | 10 | MHz |
| $DC_{SCL}$ | SCL Duty Cycle | | 40 | 50 | 60 | % |
| $t_{EL}$ | CSB High Time | | 20 | | | ns |
| $t_{ERSR}$ | CSB Falling Edge to the First SCL Rising Edge | | 10 | | | ns |
| $t_{DS}$ | MOSI Set-up Time | | 5 | | | ns |
| $t_{DH}$ | MOSI Hold Time | | 5 | | | ns |
| $t_{SREF}$ | Last SCL Rising Edge to CSB Rising Edge | | 10 | | | ns |
| $t_{WRITE}$ | Write Wait Period | | $3*t_{scl}$ | | | ns |
| $t_{READ}$ | Read Wait Period | | $9*t_{scl}$ | | | ns |

NOTES:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
6. Performance is cable dependent. Bare copper conductor cable offers better performance than copper clad steel/aluminum conductor cable.
7. Crystal deviation is based on normal operating condition.
8. CLKn timing is affected by the CLK_DEL register.
9. Tested at input gain of 0dB. $f_{IN}$ = 1kHz.
10. Tested at input gain of 0dB. $f_S$ = 8kHz and 16kHz.
11. Tested at output gain of 0dB. $F_{OUT}$ = 1kHz.
12. $t_{A\_lw}$ and $t_{A\_su}$ Min values are for $f_S$ = 48kHz mode only. If $f_S$ < 48kHz, the Min values are larger. High period of ACLKR/ACLKP is one 36MHz clock period.

# SDI Video Inputs

The TW6874 receives serial digital (SDI) video data on four independent channels. Each channel consists of an equalizer (EQ), a Clock and Data Recovery (CDR) unit, SDI descrambler/deframer, SDI speed/format auto-detection and VC2 decompression.

## SDI Video Formats

The supported SDI video formats include:

- 270Mbps (SMPTE 259M Level C)
  - 525i/625i 50, 59.94 fields/s
  - VC-2 compressed 720p 50, 59.94 frames/s
  - VC-2 compressed 1080p 25, 29.97 frames/s
  - VC-2 compressed 1080i 50, 59.94 fields/s
- 1.485Gbps (SMPTE ST 292)
  - 720p 25, 30 frames/s
  - 720p 50, 60 frames/s
  - 1080PsF 25, 30 frames/s
  - 1080p 24, 25, 30 frames/s
  - 1080i 50, 60 fields/s
- 1.485/1.001Gbps (SMPTE ST 292)
  - 720p 59.94 frames/s
  - 1080PsF 29.97 frames/s
  - 1080p 23.976, 29.97 frames/s
  - 1080i 59.94 fields/s

Any of the supported video formats can be driven into any of the four SDI inputs without limitation. The video streams are received in 10-bit YCbCr 4:2:2 sampled format. The deserialized video outputs are truncated into 8-bit YCbCr 4:2:2 sampled format.

## Adaptive Equalization

The TW6874 adaptive equalizers (EQ) function to compensate for link losses of various frequency components up to 1.5Gbps. The EQ compensates for nonlinear cable attenuation such that overall end-to-end frequency response is flat.

## Clock Data Recovery/Descrambler

The SDI signal embeds its clock in the serialized bit stream. To recover the serial bit data, the embedded clock is recovered from the transition edges of the data stream. The data bit sequence is derived by using the recovered clock to latch the bits from the EQ output signal. The TW6874 clock data recovery module (CDR) recovers the low jitter embedded clock by using a high performance PLL to track the incoming data stream.

To ensure that enough data transitions occur in any video content, the SDI standard employs a scrambling circuit in the transmitter. At the receiver side, after the CDR function is performed, a descrambler circuit is then used to convert the scrambled bit sequences back into the original video data content.

## SDI Auto Detection

The link speed mode of SDI is automatically detected by the hardware auto detection module. When the TW6874 is powered up initially or when the link mode has changed, the hardware switches among HD/SD modes until the CDR locks on to the link data.

Once the PLL has locked to the data stream, the hardware detects valid data from the link. The SDI_MODE_LOCKED bit is set in register 0x000/2/4/6 when the TW6874 has locked to a valid bit rate and received valid SDI data. The detected mode is available from SDI_MODE in the same register.

After the link speed mode is locked, the hardware further detects the video formats such as: video resolution, frame rate and scan mode. When a valid format is detected, the T_LOCKED flag is set in register 0x000/2/4/6 and the detected video format is shown in T_SCAN, T_RATE and T_FAMILY status registers at 0x000~0x007.

## VC-2 (Dirac) Decompression

Compressed VC-2 serial data streams are received at SD-SDI (270Mbps) data rates. The data formats supported are according to SMPTE 259M standard and are as follows:

- Compressed 720p 50, 59.94 frames/s
- Compressed 1080p 25, 29.97 frames/s
- Compressed 1080i 50, 59.94 fields/s

The generated pixel clock is 74.25MHz in BT.1120 16-bit mode or 148.5MHz in BT.1120 8-bit mode.

## Cable Reach

The TW6874 is designed to work with various types of 75Ω coaxial cable: e.g., RG6, RG59, or 3C-2V. Each of these cable types have various core and shielding variations. Cable reach performance is a function of the cable configuration. To achieve the best performance for any given type of cable, the PCB layout guidelines page 88 should be adhered to closely. It is recommended to emulate the reference layout.

# Video Output Format

The TW6874 receives serial data and converts it to the equivalent parallel ITU-R BT.656/BT.1120 format. In BT.656/BT.1120 format, timing reference signals (TRS, consisting of SAV and EAV codes) are inserted into the data stream to indicate the active video time. The output timing is illustrated in Figure 3.

## Video Output Port Mapping

Each video output port maps only from its associated SDI input port. For example, SDI1 maps to VD1; SDI2 maps to VD2, etc. The output data format is: BT.656 for SD; BT.1120 for HD in either 8-bit or 16-bit mode.

For SD formats, the same BT.656 video data is output on lower byte (VDn[7:0]) of the 16-bit port as shown in the Figure 5.

For HD formats, the output data can be either BT.1120 16-bit, or 8-bit mode with the pixel clock running at twice the speed.

In BT.1120 mode, Y is output on the lower byte (bits 7:0) and C is output on the upper byte (bits 15:8). In 8 bit mode, the Y/C data is output on both bytes of the video port as shown in Figure 7.

Figure 4 shows the timing relationship for the output clock and data for single and double clock rate operation. Figures 5 to 7 show the allowed data output formats.

In Figures 4 to 7, n = 1 to 4.
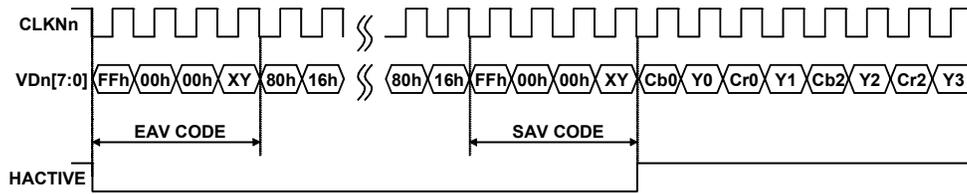


FIGURE 3. BT.656/BT.1120 LIKE FORMAT
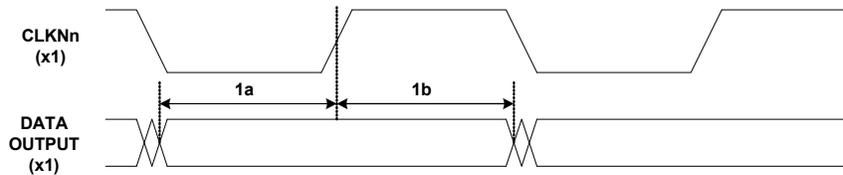


FIGURE 4. CLKNn TO VD[15:0] TIMING

## SD BT.656 Output Format
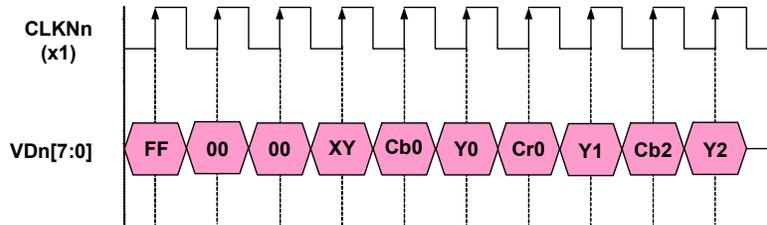


FIGURE 5. ONE SD CHANNEL BT.656 FORMAT, CLKNn AT 27MHz

## HD BT.1120 16-Bit or 8-Bit Output Formats
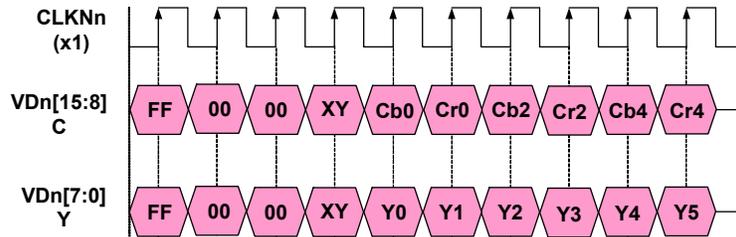


FIGURE 6. ONE HD CHANNEL BT.1120 16-BIT FORMAT, CLKNn AT 74.25MHz (HD)
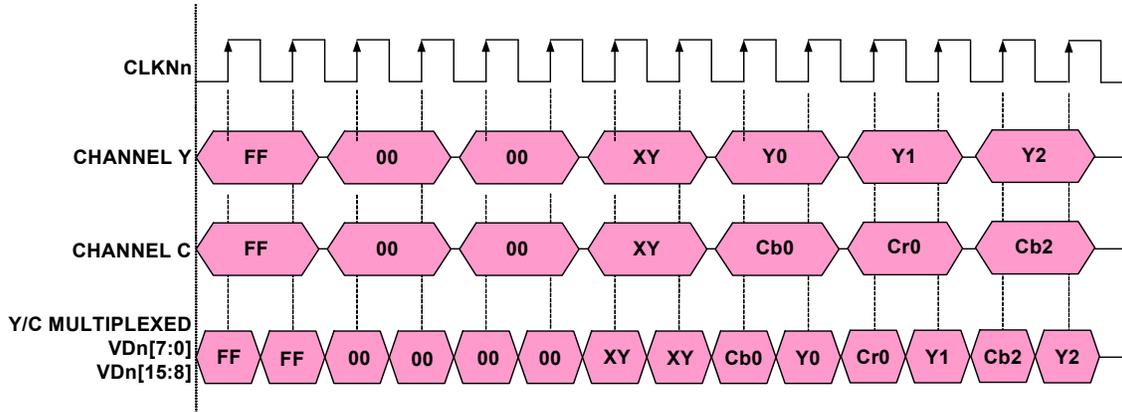


FIGURE 7. ONE HD CHANNEL BT.1120 8-BIT MODE FORMAT, CLKNn AT 148.5MHz

# TW6874

## Audio Interface

### Audio CODEC

The audio CODEC in the TW6874 is composed of five Analog-to-Digital Converters (ADC), one Digital-to-Analog Converter (DAC), audio mixer and digital serial audio interface as shown in Figure 8. The TW6874 can receive 5 analog audio signals, 4 SDI ancillary audio signals and 1 multi-channel digital serial audio stream. It can produce 1 mixing analog audio signal and 2 digital serial audio streams.

The analog audio input signal gain for the AIN1/2/3/4/5 pins can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN1/2/3/4/5 registers before being sampled by the ADCs. If the SDI stream has ancillary audio embedded, these can be used in lieu of AIN1/2/3/4. The ACLKP, ASYNP and ADATP pins from the I2S decoder block are used to receive digital serial audio input data for playback. To record audio data, the I2S encoder block

provides the digital serial audio output via the ACLKR, ASYNR and ADATR pins. The AOUT pin sends analog audio data received from the audio DAC. The output level can be controlled by a programmable gain amplifier via the DAC_GAIN register.

The TW6874 can mix all the audio inputs including analog audio and digital audio according to the predefined mixing ratio for each audio via the MIX_RATIO1/2/3/4/5/PB registers. This mixing audio output can be provided through the analog and digital interfaces. The embedded audio DAC supports the analog mixing audio output. The ADATM pin supports the digital mixing audio output and its digital serial audio timings are provided through the ACLKR and ASYNR pins that are shared with the digital serial audio record timing pins.

The main purpose of the AIN5 pin is to make the standard I2S digital audio output for AIN5 data available on the ADATM pin for audio back channel applications. Usually, AIN1/2/3/4 audio data are output to the CODEC on the ADATR pin.
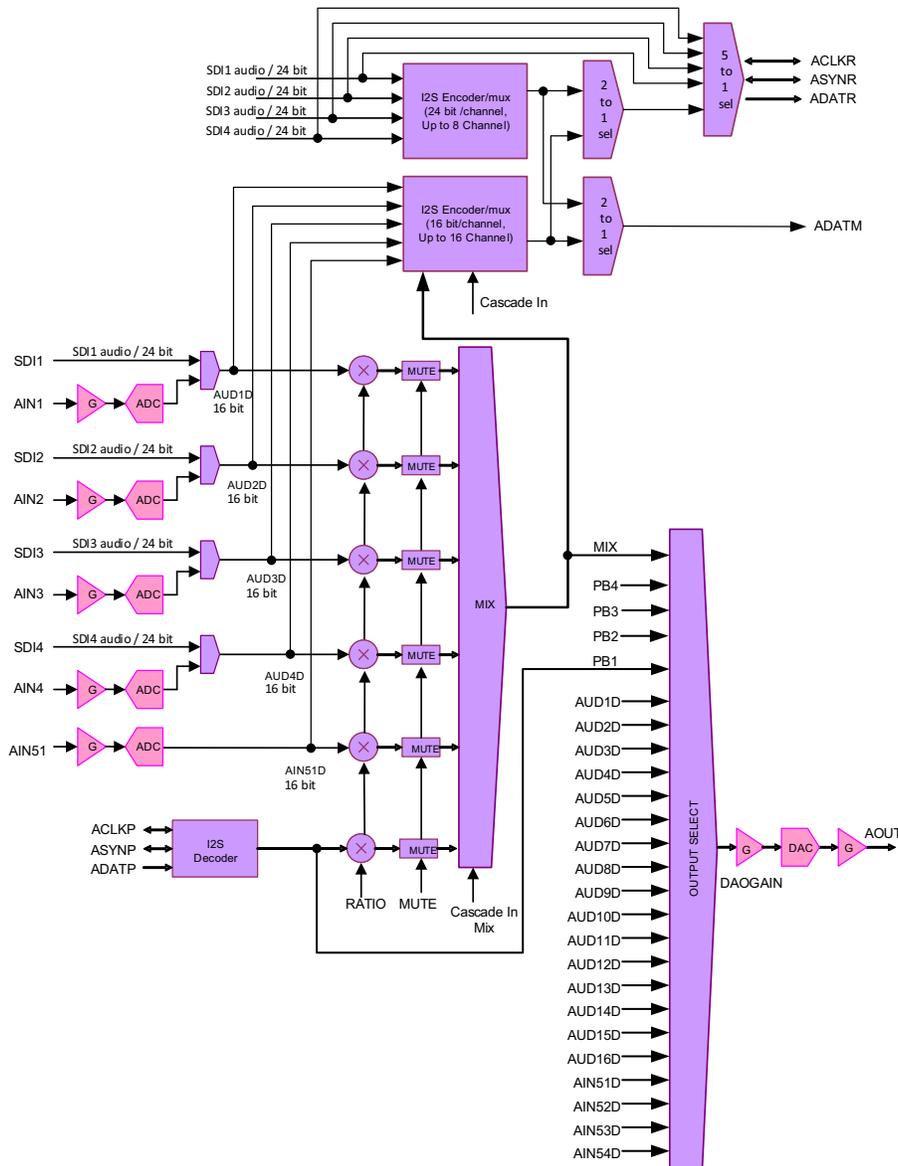


**FIGURE 8. AUDIO CODEC BLOCK DIAGRAM**

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March 25, 2015

# TW6874

## SDI Ancillary Audio

Embedded SDI ancillary audio is formed of 4 groups of 4 channels. Each audio sample is 24 bits wide, depending on whether it is embedded in SD/VC2 or HD. One of these channels can be selected from each SDI input and sent to the TW6874's audio processor. If an SDI audio channel is selected, the respective analog audio input is not used.

SDI ancillary audio uses 48kHz sampling frequencies.

The TW6874 can truncate SDI ancillary audio to 16 bits in order to allow mixing with the analog audio data from channels where SDI audio is not used.

## Serial Audio Interface

There are three kinds of digital serial audio interfaces in the TW6874. The first is a multichannel recording output, the second is a mixing output and the third is a playback input. These three digital serial audio interfaces follow a standard I2S interface as shown in Figure 9. The I2S MUX can output audio channels from each of the SDI channel, multiplexed 24-bit audio channels from 4 SDI channels, or multiplexed 16-bit 16 audio channels from SDI, ADC and I2S input.

### PLAYBACK INPUT

The serial interface using the ACLKP, ASYNP and ADATP pins accepts the digital serial audio data for playback. The ACLKP and ASYNP pins can be operated in master or slave mode. For master mode, these pins work as outputs and generate the standard audio clock and synchronizing signals. For slave mode, these pins are inputs and accept the standard audio clock and synchronizing signals. The ADATP pin is always an input regardless of the operating mode. One channel of audio data (from the left or right channel) should be selected for playback audio by the PB_LRSEL.

### RECORD OUTPUT

To record audio data, the TW6874 provides the digital serial audio data through the ACLKR, ASYNR and ADATR pins. The sampling frequency comes from the 256*$f_S$, 320*$f_S$ or 384*$f_S$ audio system clock setting. Even though the standard I2S and DSP format can have only two audio data on left and right channel, the TW6874 can provide an extended I2S and DSP format, which can have 16 channel audio data through the ADATR pin. The R_MULTCH defines the number of audio channels to be recorded by the ADATR pin. ASYNR's frequency is always at the sampling frequency ($f_S$). Thus, one ASYNR period is always equal to 256*ACLKR periods when AIN5MD = 0. Figure 10 shows the digital serial audio data organization for multichannel audio.

The ACLKR pin can be operated in master or slave mode. For master mode, this pin works as an output and generates the standard audio clock. For slave mode, this pin is an input and accepts the standard audio clock. The ASYNR pin can be operated as an input or output regardless of the operating mode. The ADATR pin is always an output.
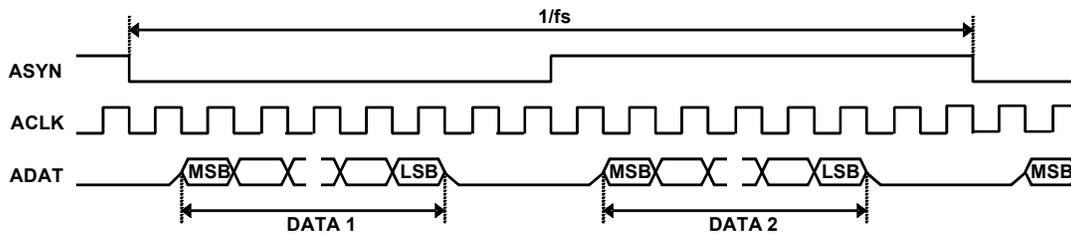


FIGURE 9A. I2S FORMAT
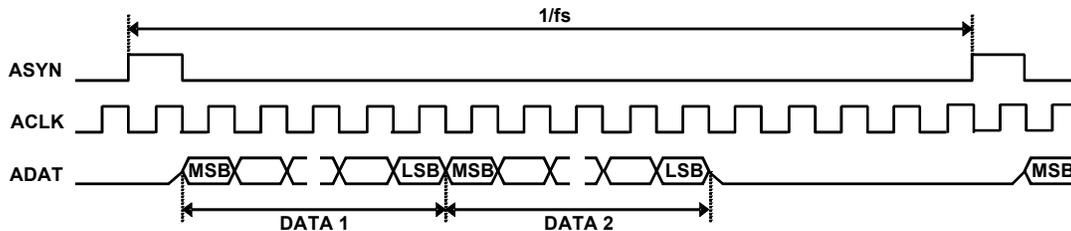


FIGURE 9B. DSP FORMAT

FIGURE 9. SERIAL AUDIO INTERFACE FORMAT

# TW6874
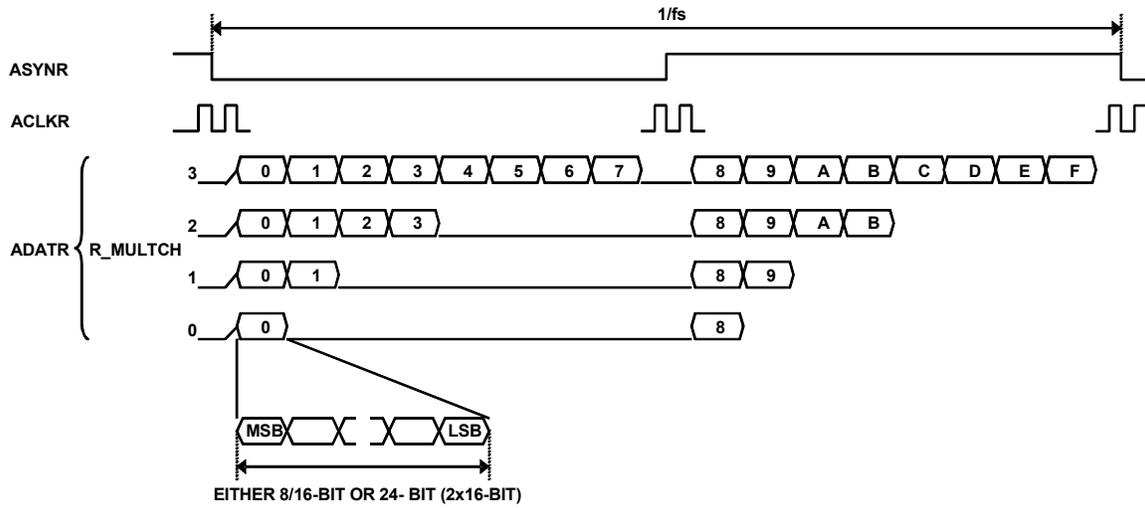


**FIGURE 10A. I2S FORMAT**
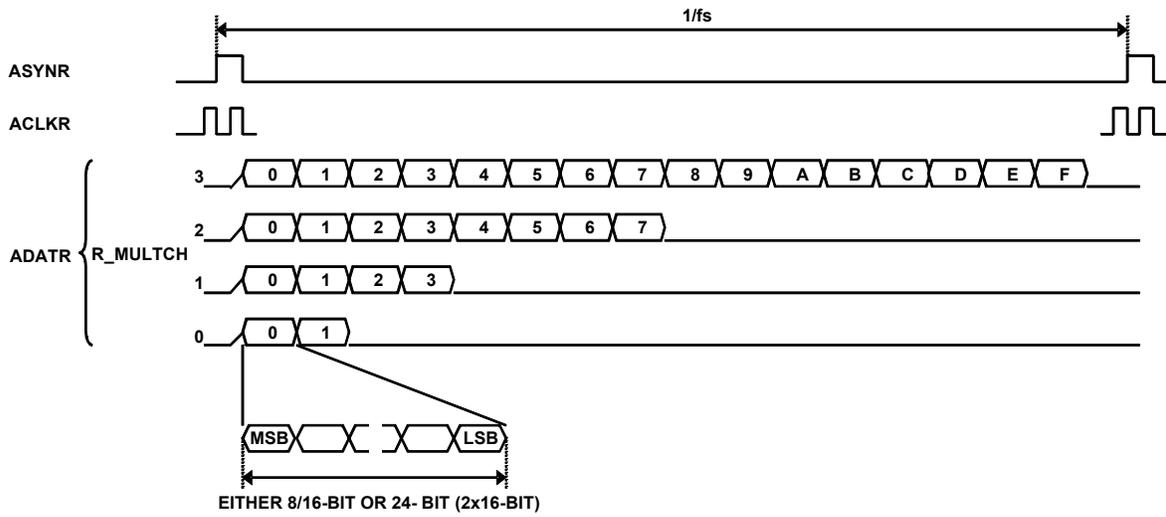


**FIGURE 10B. DSP FORMAT**

**FIGURE 10. MULTICHANNEL AUDIO RECORD FORMAT**

   intersil™     

**TABLE 1.   MULTICHANNEL AUDIO RECORD SEQUENCE (I2S)**

| R_MULTCH | PIN | LEFT CHANNEL | | | | | | | | RIGHT CHANNEL | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | ADATR | 0 | | | | | | | | 8 | | | | | | | |
| | ADATM | F | | | | | | | | 7 | | | | | | | |
| 1 | ADATR | 0 | 1 | | | | | | | 8 | 9 | | | | | | |
| | ADATM | F | E | | | | | | | 7 | 6 | | | | | | |
| 2 | ADATR | 0 | 1 | 2 | 3 | | | | | 8 | 9 | A | B | | | | |
| | ADATM | F | E | D | C | | | | | 7 | 6 | 5 | 4 | | | | |
| 3 | ADATR | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| | ADATM | F | E | D | C | B | A | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**TABLE 2.   MULTICHANNEL AUDIO RECORD SEQUENCE (DSP)**

| R_MULTCH | PIN | LEFT/RIGHT CHANNEL | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | ADATR | 0 | 1 | | | | | | | | | | | | | | |
| | ADATM | F | E | | | | | | | | | | | | | | |
| 1 | ADATR | 0 | 1 | 2 | 3 | | | | | | | | | | | | |
| | ADATM | F | E | D | C | | | | | | | | | | | | |
| 2 | ADATR | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | | | | |
| | ADATM | F | E | D | C | B | A | 9 | 8 | | | | | | | | |
| 3 | ADATR | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| | ADATM | F | E | D | C | B | A | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Tables 1 (I2S) and 2 (DSP) show the sequence of audio data to be recorded for each mode of the R_MULTCH register. The sequences of 0 ~ F do not mean actual audio channel numbers but represent sequence only. The actual audio channel should be assigned to sequence 0~F by the R_SEQ0~R_SEQF registers. The audio sequence of ADATM is also shown in these two tables. The ADATM pin is configured for record via the R_ADATM register.

## MIX OUTPUT

The digital serial audio data on the ADATM has two different audio data: mixing audio and playback audio. The mixing digital serial audio data is the same as the analog mixing output. The sampling frequency, bit width and number of audio channels for the ADATM pin are same as the ADATR pin because the ACLKR and ASYNR pins are shared with the ADATR and ADATM pins.

## Multidevice Cascading

The TW6874 can output 16 channel 8-bit/16-bit audio data on the ACLKR/ASYNR/ADATR outputs simultaneously. Therefore, up to 4 devices can be connected in most multidevice application cases.

Since each stage device can accept 4+1 analog audio signals or 4 SDI audio signals, four cascaded devices will be a 16-channel 16-bit audio controller by default {AFS384, AIN5MD} = 00. The first stage device provides 16-channel 8-bit/16-bit digital serial audio data for record. Even though the first stage device has only one digital serial audio data pin ADATR for record, the TW6874 can generate 16 channel data simultaneously using the multichannel method. This first stage device can also output 16 channel mixing audio data of the digital serial audio data, SDI ancillary audio data (16-bit) and analog audio signal. The first stage device accepts the digital serial audio data for playback. The digital playback data can be converted to analog signal by the DAC in the first stage.

Several master/slave mode configurations are available. Figure 11 is the most recommended and demanded system with Clock Master mode (ACLKRMASTER = 1). Figure 12 is the most recommended system with Clock Slave/Sync Slave mode (ACLKRMASTER = 0, ASYNROEN = 1). Other system combinations are also available dependent upon the application.

In Figures 11 and 12, Mix1-16-51-54/Pb1 means mix output of AIN1-16, AIN51-54 and Playback1. AIN1-16-51-54/Pb1 means one selected audio output from AIN1-16-51-54/Pb1.

If any one of the TW6874s use {AFS384, AIN5MD} = 01 or {AFS384, AIN5MD} = 10, all other cascaded TW6874s must be set up with the same {AFS384 AIN5MD} mode.

In multidevice audio operation mode, the same oscillator clock source needs to be connected to each TW6874 XTI pin.

# TW6874
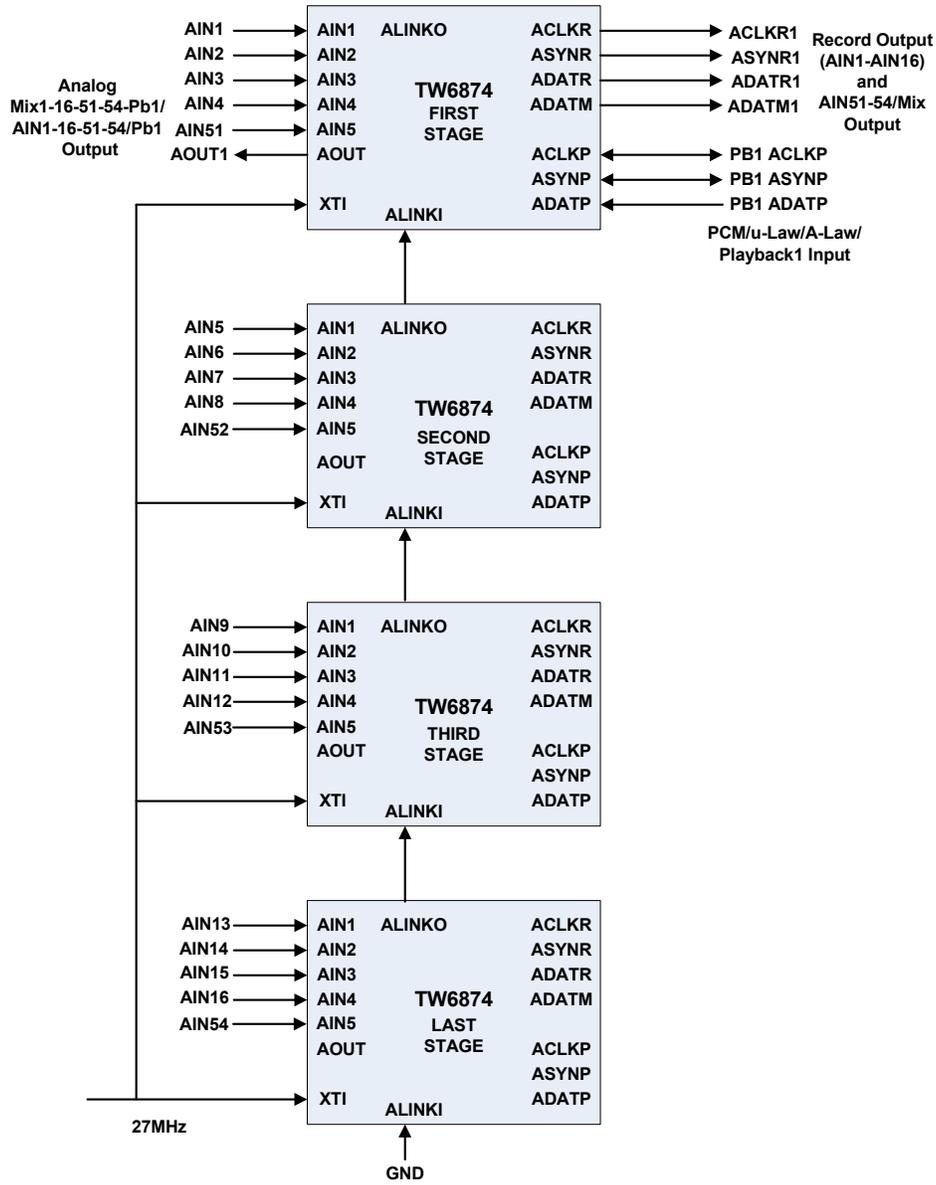


FIGURE 11.  RECOMMENDED CLOCK MASTER CASCADE MODE CONFIGURATION

# TW6874
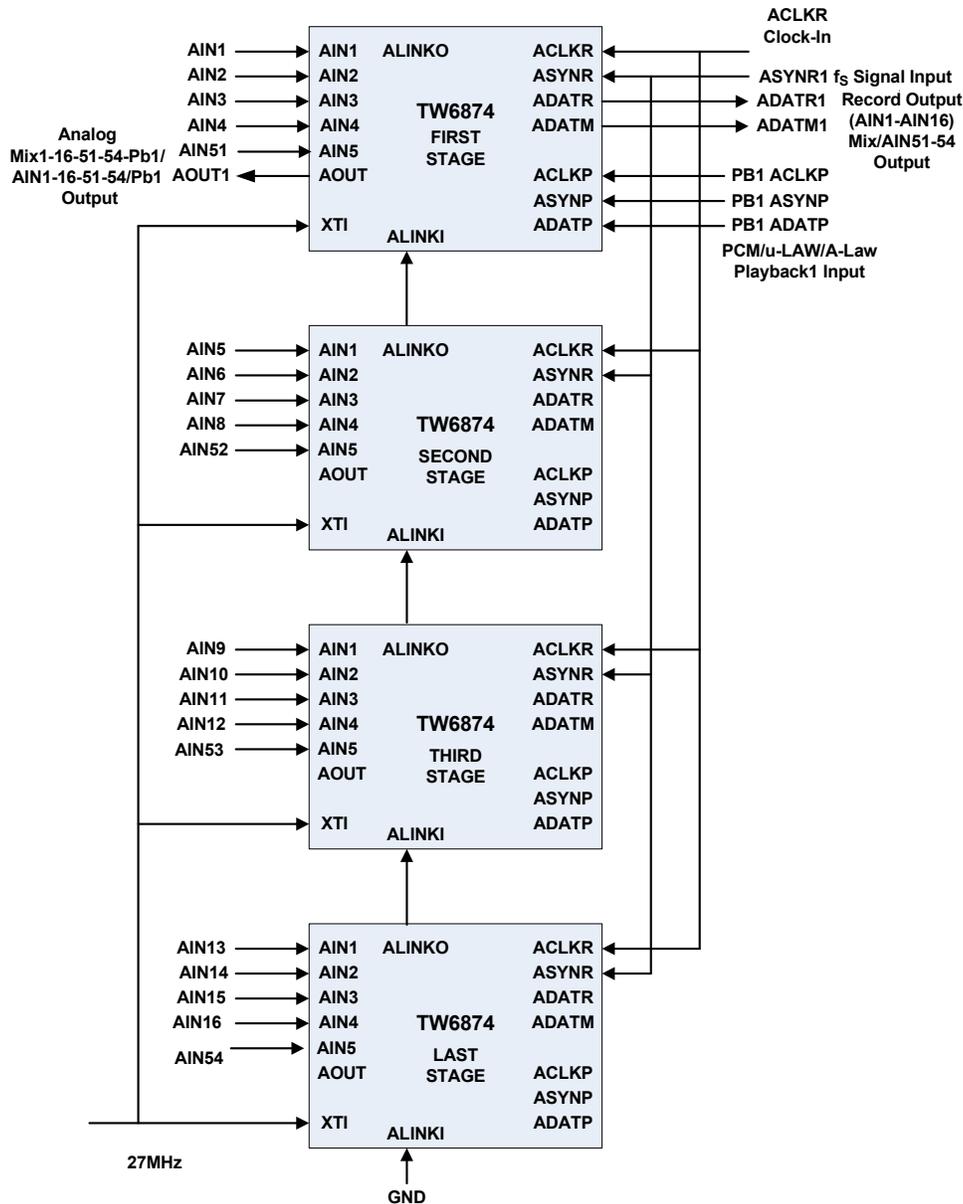


FIGURE 12. RECOMMENDED CLOCK SLAVE/SYNC SLAVE MODE CONFIGURATION

## Audio Clock Master/Slave Mode

The TW6874 has two types of audio clock modes. If the ACLKRMASTER register is set to 1, analog audio is sampled by the audio clock internally generated by the ACKG (Audio Clock Generator). In this master mode, ACLKR/ASYNR pins are outputs. The ASYNROEN register for ASYNR pin should be set to 0 (output enable mode). If the ACLKRMASTER register is set to 0, analog audio is sampled by the audio clock on the ACLKR pin input. A $256*f_S$, $320*f_S$ or $384*f_S$ audio clock should be connected to the ACLKR pin from an external master clock source in this slave mode. The ASYNR pin can be either input or output in slave mode. ASYNR's frequency should match the audio sample frequency ($f_S$) in both master and slave mode. The AIN5MD and AFS384 registers configure the analog audio sample mode per Table 3.

TABLE 3.

| REGISTER | | $f_S$ MODE |
|---|---|---|
| AIN5MD | AFS384 | |
| 0 | 0 | $256*f_S$ |
| 1 | 0 | $320*f_S$ |
| 0 | 1 | $384*f_S$ |

## ACLKR Slave Mode Data Output Timing

The TW6874 always outputs ASYNR/ADATR/ADATM on the falling edge of ACLKR. A new ADATR/ADATM word (or multiple words if using multichannel mode) is output upon each toggle of ASYNR. If ASYNR is an input, it is sampled on the falling edge of ACLKR.