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LCD Video Processor with Built-In Decoder, MCU, OSD, TCON and Analog RGB Input Support

TW8835

The TW8835 incorporates many of the features required to create multipurpose in-car LCD display system in a single package. It integrates a high quality 2D comb NTSC/PAL/SECAM video decoder, triple high speed RGB ADCs, high quality scaler, versatile OSD and high performance MCU. Its image video processing capability includes arbitrary scaling, panoramic scaling, image mirroring, image adjustment and enhancement, black and white stretch, etc. On the input side, it supports a rich combination of CVBS, S-video, component video, analog RGB as well as digital YCbCr/RGB inputs. On the output side, it supports a variety of digital panel types with its built-in timing controller. The integration of additional touch screen controller, LED driver controller, PWM and MCU makes this a versatile solution for many portable applications.

Applications

- In-car display
- Portable DVD and DVR players
- Portable media players

Features

Analog Video Decoder

- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM with automatic format detection
- Three 10-bit ADCs and analog clamping circuit.
- Fully programmable static gain or automatic gain control for the Y or CVBS channel
- Programmable white peak control for the Y or CVBS channel
- Software selectable analog inputs allow composite, S-video, analog YPbPr or RGB
- High quality adaptive 2D comb filter for both NTSC and PAL inputs
- PAL delay line for color phase error correction
- Image enhancement with 2D dynamic peaking and CTI
- Digital subcarrier PLL for accurate color decoding
- Digital horizontal PLL and advanced synchronization processing for VCR playback and weak signal performance
- Programmable hue, brightness, saturation, contrast, sharpness
- High quality horizontal and vertical filtered down scaling with arbitrary scale down ratio

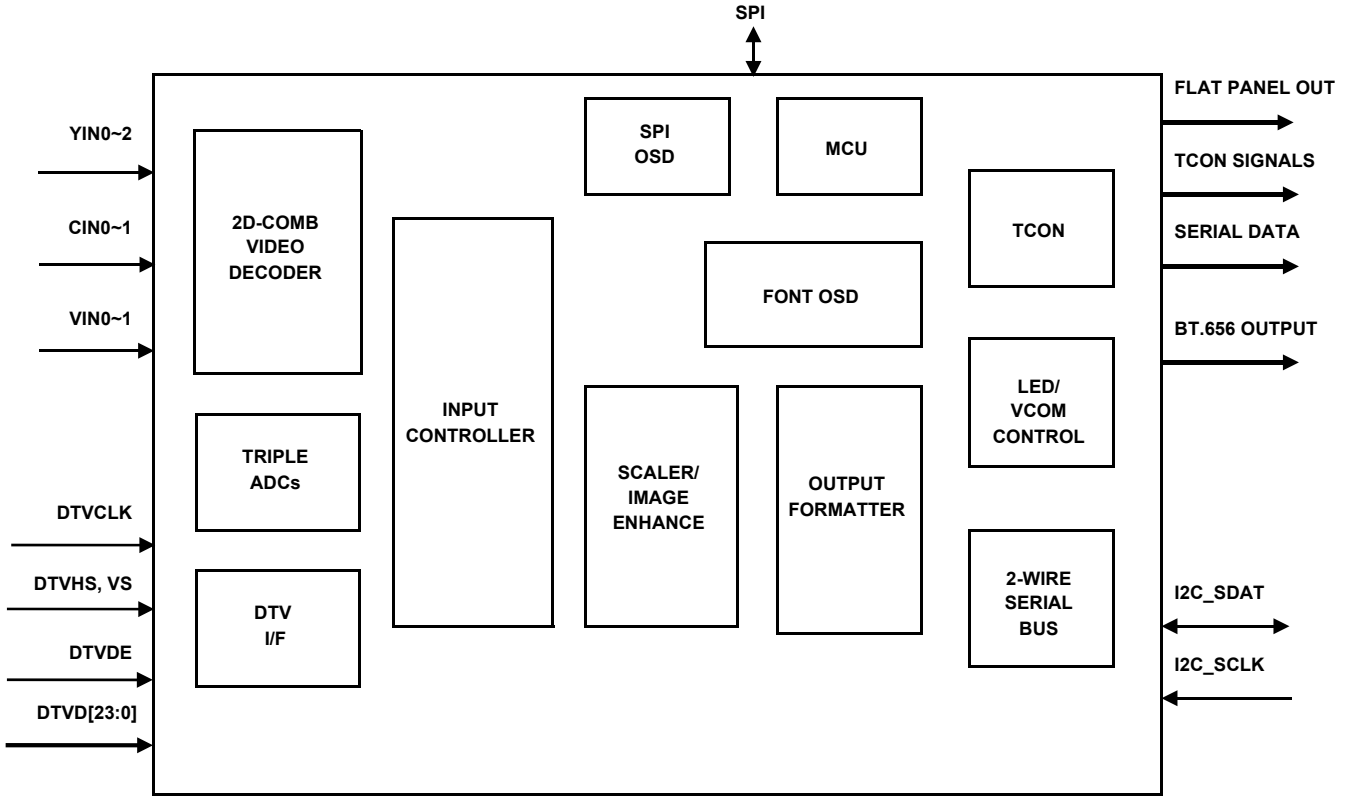


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Features (Continued)

Analog RGB Inputs

- Triple high speed 10-bit ADCs with clamping and programmable gain amplifier
- SOG and H/VSYNC support for YPbPr or RGB input
- Built-in line locked PLL with sync separator
- Supports input resolution up to 1080p

Digital Inputs Support

- Supports both BT.656 and 601 video formats
- Supports YCbCr/RGB 24-bit input
- Supports RGB.565 + BT.656 at the same time
- Supports input resolution up to 1080p

TFT Panel Support

- Built-in programmable timing controller
- Supports 3, 4, 6 or 8 bits per pixel up to 16.8 million colors with built-in dithering engine
- Supports digital panel up to XGA resolution
- Supports serial (8-bit) RGB panel

Font Based On-Screen Display

- Four window font OSD with bordering/shadow
- 10kB programmable font RAM and 512 display RAM
- 1/2/3/4 bits/pixel
- Supports variable width (12/16), height (2~32)

SPI Flash Based On-Screen Display

- Nine bitmap based OSD windows through SPI
- Supports 4/6/8 bits/pixel
- Supports RLE decompression for one window
- Supports overlapping between windows

Image Processing

- High quality scaler with both up/down and panorama scaling support
- Built-in 2D deinterlacing function
- Programmable brightness, contrast, saturation, hue and sharpness
- Programmable color transient improvement control
- Supports programmable cropping of input video and graphics
- Independent RGB gain and offset controls
- DTV hue adjustment
- Programmable 8-bit gamma correction for each color
- Black/white stretch

Clock Generation

- Spread spectrum profile based on triangular modulation with center spread
- Programmable modulation frequency and spread width

Timing Controller (TCON)

- Supports programmable interface signals for control
- Column (source) driver/row (gate) driver

MCU

- Industry standard 8052 based
- Code fetch from external SPI flash memory
- 256B code cache
- 2k XDATA memory
- Support power save mode with 32k internal clock
- ISP (in system programming) with internal boot ROM

Decoder Output

- Independent BT.656 decoder output

Touch Screen Controller

- Built-in 4-wire resistive touch screen
- 12-bit ADC
- 4-channel auxiliary input

Miscellaneous

- Supports 2-wire serial bus interface
- Built-in single LED backlight controller
- Built-in VCOM DC voltage
- Built-in VCOM AC
- Built-in DC/DC converter
- Up to 4 PWMs
- GPIOs
- 1.8/3.3V operation
- Power-down mode
- Single 27MHz crystal
- 128 pin LQFP and 144 pin TFBGA package

Table of Contents

Ordering Information

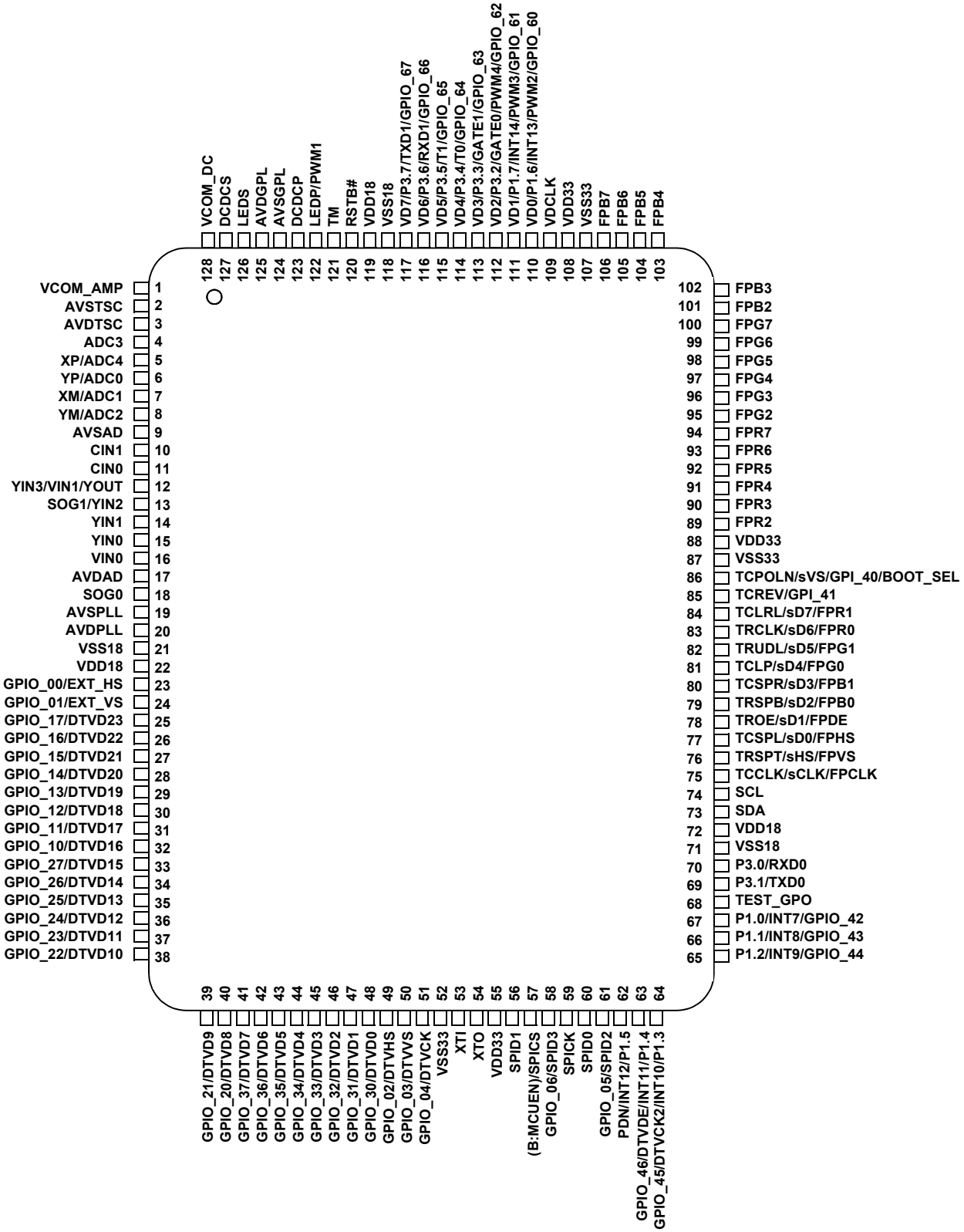
PART NUMBER (Notes 1, 4)	PART MARKING	PACKAGE (RoHS Compliant)	PKG. DWG. #
TW8835-BA2-CR (Note 3)	TW8835 BA2-CR	144 Ball TFBGA (7mmx7mm) Tray (bulk) packaging	V144.7X7A
TW8835-LA2-CR (Note 2)	TW8835 LA2-CR	128 Lead LQFP (14mmx20mm) Tray (bulk) packaging	Q128.14X20F
TW8835AT-LA2-GRH (Notes 2, 5)	TW8835AT LA2-GR	128 Lead LQFP (14mmx20mm) Tray (bulk) packaging	Q128.14X20F

NOTES:

1. Add “T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see product information page for TW8835. For more information on MSL, please see tech brief TB363.
5. “AT” suffix denotes Automotive Grade product. AEC-Q100 Grade 2 qualified, PPAP available upon request.

Pin Configurations

TW8835
(128 LD LQFP)
TOP VIEW



Pin Configurations (Continued)

TW8835
(144 LD TFBGA)
TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12
A	ADC3	AVDTSC	VCOM_DC	AVDGPL	RSTB#	VDD18	VD5/ P3.5/T1/ GPIO_65	VD2/P3.2/ GATE0/ PWM4/ GPIO_62	VDD33	FPB4	FPB3	FPB2
B	ADC0/YP	ADC4/XP	VCOM_AMP	LEDS	LEDP/ PWM1	VD6/P3.6/ RXD1/ GPIO_66	VD3/P3.3/ GATE1/ GPIO_63	VDCLK	FPB7	FPB5	FPG7	FPG6
C	ADC2/ YM	ADC1/XM	AVSTSC	DCDCS	DCDCP	VD7/ P3.7/TXD1/ GPIO_67	VD4/ P3.4/T0/ GPIO_64	VD0/P1.6/ INT13/ PWM2/ GPIO_60	FPB6	FPG5	FPG4	FPG3
D	AVSAD	CIN0	CIN1	YOUT/ VIN1/ YIN3	AVSGPL	TM	VSS18	VD1/P1.7/ INT14/ PWM3/ GPIO_61	VSS33	FPG2	FPR7	FPR6
E	AVDAD	YIN0	YIN1	YIN2/ SOG1	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	FPR5	FPR4	FPR3	FPR2
F	AVDPLL	SOG0	VIN0	AVSPLL	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	VSS33	TCPOLN/ sVS/ GPI_40/ BOOT_SEL	TCREV/ GPI_4	VDD33
G	VDD18	EXT_HS/ GPIO_00	EXT_VS/ GPIO_01	DTVD23/ GPIO_17	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	TCLRL/ sD7/ FPR1	TRCLK/ sD6/ FPR0	TRUDL/ sD5/ FPG1	TCLP/ sD4/ FPG0
H	DTVD22/ GPIO_16	DTVD21/ GPIO_15	DTVD20/ GPIO_14	VSS18	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	Thermal ball (Under Die GND)	TCSPR/ sD3/ FPB1	TRSPB/ sD2/ FPB0	TCSPL/ sD0/ FPHS	TROE/ sD1/ FPDE
J	DTVD19/ GPIO_13	DTVD18/ GPIO_12	DTVD17/ GPIO_11	DTVD16/ GPIO_10	DTVD0/ GPIO_30	VSS33	SPICS/ (B:MCUEN)	SPID0	VSS18	TRSPT/ sHS/ FPVS	SCL	TCCLK/ sCLK/ FPCLK
K	DTVD15/ GPIO_27	DTVD14/ GPIO_26	DTVD13/ GPIO_25	DTVD7/ GPIO_37	DTVD1/ GPIO_31	DTVHS/ GPIO_02	SPID1	SPICK	P1.4/ INT11/ DTVDE/ GPIO_46	SDA	P3.0/ RXD0	VDD18
L	DTVD11/ GPIO_23	DTVD12/ GPIO_24	DTVD8/ GPIO_20	DTVD6/ GPIO_36	DTVD2/ GPIO_32	DTVCK/ GPIO_04	VDD33	SPID3/ GPIO_06	P1.5/ INT12/ PDN	P1.1/ INT8/ GPIO_43	TEST_GPO	P3.1/ TXD0
M	DTVD10/ GPIO_22	DTVD9/ GPIO_21	DTVD5/ GPIO_35	DTVD4/ GPIO_34	DTVD3/ GPIO_33	DTVVS/ GPIO_03	XTI	XTO	SPID2/ GPIO_05	P1.3/ INT10/ DTVCK2/ GPIO_45	P1.2/ INT9/ GPIO_44	P1.0/ INT7/ GPIO_42

Pin Descriptions

This section provides a detailed description of each pin for the TW8835. The pins are arranged in functional groups according to their associated interface.

The active state of the signal is determined by the trailing symbol at the end of the signal name. A "#" symbol indicates that the signal is active or asserted at a low voltage level. When "#" is not present after the signal name, the signal is active at the high voltage level.

The pin description also includes the buffer direction and type used for that pin.

TABLE 1. PIN DESCRIPTIONS

PIN#		I/O	PIN NAME	DESCRIPTION	INTERNAL CONNECTION	RECOMMENDED CONNECTION OF UNUSED PIN	STATUS AT HW RESET
LQFP	TFBGA						
ANALOG I/F SIGNALS AND POWER							
124	D5	P	AVSGPL	Genlock PLL Ground	-	-	Pwr
125	A4	P	AVDGPL	Genlock PLL Power +1.8V			
126	B4	AI	LEDS	LED Sense		Connect to AVSAD	Hi-Z
127	C4	AI	DCDCS	DCDC Sense			
128	A3	AO	VCOM_DC	VCOM out for DC		Open/Unconnected	Hi-Z
1	B3	AO	VCOM_AMP	VCOM out for AMP. TCON-Column Driver Inversion.			
2	C3	P	AVSTSC	Analog TSC Ground		-	Pwr
3	A2	P	AVDTSC	Analog TSC Power +3.3V			
4	A1	AI	ADC3	Auxiliary channel 3		Open/Unconnected	Hi-Z
5	B2	AI	ADC4	Auxiliary channel 4			
		AI	XP	TSC Positive X input			
6	B1	AI	ADC0	Auxiliary channel 0			
		AI	YP	TSC Positive Y input			
7	C2	AI	ADC1	Auxiliary channel 1			
		AI	XM	TSC Negative X input			
8	C1	AI	ADC2	Auxiliary channel 2			
		AI	YM	TSC Negative Y input			
9	D1	P	AVSAD	Analog A/D Ground		-	Pwr
10	D3	AI	CIN1	Analog component C input 1		Connect to AVSAD	Hi-Z
11	D2	AI	CIN0	Analog component C input 0			
12	D4	AO	YOUT	Analog Y output		Open/Unconnected	
		AI	YIN3	Analog composite or luma input 2			
		AI	VIN1	Analog component V input 0			
13	E4	AI	YIN2	Analog composite or luma input 2		Connect to AVSAD	
		AI	SOG1	Sync On Green Input 1			
14	E3	AI	YIN1	Analog composite or luma input 1			
15	E2	AI	YIN0	Analog composite or luma input 0			
16	F3	AI	VIN0	Analog component V input 0			
17	E1	P	AVDAD	Analog A/D Power +1.8V		-	Pwr
18	F2	AI	SOG0	Sync On Green Input 0		Connect to AVSPLL	Hi-Z
19	F4	P	AVSPLL	PLL (Internal Analog) Ground		-	Pwr
20	F1	P	AVDPLL	PLL (Internal Analog) Power +1.8V			

TABLE 1. PIN DESCRIPTIONS (Continued)

PIN#		I/O	PIN NAME	DESCRIPTION	INTERNAL CONNECTION	RECOMMENDED CONNECTION OF UNUSED PIN	STATUS AT HW RESET
LQFP	TFBGA						
DIGITAL I/F SIGNALS							
23	G2	I	EXT_HS	External HSYNC for RGB	Pull Down	Open/Unconnected	0
		I/O	GPIO_00	General Purpose Data I/O			
24	G3	I	EXT_VS	External VSYNC for RGB			
		I/O	GPIO_01	General Purpose Data I/O			
25	G4	I	DTVD23	DTV Input			
		I/O	GPIO_17	General Purpose Data I/O			
26	H1	I	DTVD22	DTV Input			
		I/O	GPIO_16	General Purpose Data I/O			
27	H2	I	DTVD21	DTV Input			
		I/O	GPIO_15	General Purpose Data I/O			
28	H3	I	DTVD20	DTV Input			
		I/O	GPIO_14	General Purpose Data I/O			
29	J1	I	DTVD19	DTV Input			
		I/O	GPIO_13	General Purpose Data I/O			
30	J2	I	DTVD18	DTV Input			
		I/O	GPIO_12	General Purpose Data I/O			
31	J3	I	DTVD17	DTV Input			
		I/O	GPIO_11	General Purpose Data I/O			
32	J4	I	DTVD16	DTV Input			
		I/O	GPIO_10	General Purpose Data I/O			
33	K1	I	DTVD15	DTV Input			
		I/O	GPIO_27	General Purpose Data I/O			
34	K2	I	DTVD14	DTV Input			
		I/O	GPIO_26	General Purpose Data I/O			
35	K3	I	DTVD13	DTV Input			
		I/O	GPIO_25	General Purpose Data I/O			
36	L2	I	DTVD12	DTV Input			
		I/O	GPIO_24	General Purpose Data I/O			
37	L1	I	DTVD11	DTV Input			
		I/O	GPIO_23	General Purpose Data I/O			
38	M1	I	DTVD10	DTV Input			
		I/O	GPIO_22	General Purpose Data I/O			
39	M2	I	DTVD9	DTV Input			
		I/O	GPIO_21	General Purpose Data I/O			
40	L3	I	DTVD8	DTV Input			
		I/O	GPIO_20	General Purpose Data I/O			
41	K4	I	DTVD7	DTV Input			
		I/O	GPIO_37	General Purpose Data I/O			
42	L4	I	DTVD6	DTV Input			
		I/O	GPIO_36	General Purpose Data I/O			
43	M3	I	DTVD5	DTV Input			
		I/O	GPIO_35	General Purpose Data I/O			

TABLE 1. PIN DESCRIPTIONS (Continued)

PIN#		I/O	PIN NAME	DESCRIPTION	INTERNAL CONNECTION	RECOMMENDED CONNECTION OF UNUSED PIN	STATUS AT HW RESET
LQFP	TFBGA						
44	M4	I	DTVD4	DTV Input	Pull Down	Open/Unconnected	0
		I/O	GPIO_34	General Purpose Data I/O			
45	M5	I	DTVD3	DTV Input			
		I/O	GPIO_33	General Purpose Data I/O			
46	L5	I	DTVD2	DTV Input			
		I/O	GPIO_32	General Purpose Data I/O			
47	K5	I	DTVD1	DTV Input			
		I/O	GPIO_31	General Purpose Data I/O			
48	J5	I	DTVD0	DTV Input			
		I/O	GPIO_30	General Purpose Data I/O			
49	K6	I	DTVHS	Horizontal sync for DTV interface			
		I/O	GPIO_02	General Purpose Data I/O			
50	M6	I	DTVVS	Data valid for DTV interface or raw HSYNC for DTV interface			
		I/O	GPIO_03	General Purpose Data I/O			
51	L6	I	DTVCK	Clock Input for DTV Interface	Pull Down	Open/Unconnected	0
		I/O	GPIO_04	General Purpose Data I/O			
53	M7	I	XTI	Crystal terminal or oscillator input	-	-	-
54	M8	O	XTO	Crystal terminal			
56	K7	I/O	SPID1	SPI Data 1	Pull Up	Open/Unconnected	1
57	J7	O	SPICS	SPI Chip Select	-	-	-
		I	MCUEN	(Bootstrap) MCU Enable H: Enable, L: Disable			
58	L8	I/O	SPID3	SPI Data 3	Pull Up	Open/Unconnected	1
		I/O	GPIO_06	General Purpose Data I/O			
59	K8	O	SPICK	SPI Clock Output	-	Open/Unconnected	-
60	J8	I/O	SPID0	SPI Data 0	Pull Up	Open/Unconnected	1
61	M9	I/O	SPID2	SPI Data 2			
		I/O	GPIO_05	General Purpose Data I/O			
62	L9	I/O	P1.5/INT12	MCU Port/Interrupt Input	-	Connect to VDD through 4.7kΩ resister	Hi-Z
		I	PDN	Power Down Control			
63	K9	I/O	P1.4/INT11	MCU Port/Interrupt Input			
		I/O	GPIO_46	General Purpose Data I/O			
		I	DTVDE	Data valid for DTV interface or raw HSYNC for DTV interface			
64	M10	I/O	P1.3/INT10	MCU Port/Interrupt Input			
		I	DTVCK2	Clock Input for DTV Interface			
		I/O	GPIO_45	General Purpose Data I/O			
65	M11	I/O	P1.2/INT9	MCU Port/Interrupt Input			
		I/O	GPIO_44	General Purpose Data I/O			
66	L10	I/O	P1.1/INT8	MCU Port/Interrupt Input			
		I/O	GPIO_43	General Purpose Data I/O			
67	M12	I/O	P1.0/INT7	MCU Port/Interrupt Input			
		I/O	GPIO_42	General Purpose Data I/O			
68	L11	O	TEST_GPO	Multipurpose Test Output	-	Open/Unconnected	1
				For normal operation, keep “High" during Reset			

TABLE 1. PIN DESCRIPTIONS (Continued)

PIN#		I/O	PIN NAME	DESCRIPTION	INTERNAL CONNECTION	RECOMMENDED CONNECTION OF UNUSED PIN	STATUS AT HW RESET
LQFP	TFBGA						
69	L12	I/O	P3.1/TXD0	MCU Port/TXD0	-	Connect to VDD through 4.7kΩ resister	Hi-Z
70	K11	I/O	P3.0/RXD0	MCU Port/RXD0			
73	K10	I/O	SDA	I^2C Data			
74	J11	I	SCL	I^2C Clock			
75	J12	O	TCCLK	TCON Column Driver Clock	Pull down	Open/Unconnected	0
		O	sCLK	Serial Clock Output			
		O	FPCLK	Flat Panel Clock			
76	J10	O	TRSPT	TCON Row Driver Starting Pulse (Top start)			
		O	sHS	Serial HSYNC			
		O	FPVS	Flat Panel VSYNC			
77	H11	O	TCSPL	TCON Column Driver Start Pulse (Left to right scan)			
		O	sD0	Serial Data Output Bit (LSB)			
		O	FPHS	Flat Panel HSYNC			
78	H12	O	TROE	TCON-Row Driver Output Enable			
		O	sD1	Serial Data Output Bit			
		O	FPDE	Flat Panel Data Enable			
79	H10	O	TRSPB	TCON-Row Driver Starting Pulse (Bottom Start)			
		O	sD2	Serial Data Output Bit			
		O	FPB0	Blue Flat Panel Output Bit			
80	H9	O	TCSPR	TCON-Column Driver Start Pulse (Right to left scan)			
		O	sD3	Serial Data Output Bit			
		O	FPB1	Blue Flat Panel Output Bit			
81	G12	O	TCLP	TCON-Column Driver Load Pulse			
		O	sD4	Serial Data Output Bit			
		O	FPG0	Green Flat Panel Output Bit			
82	G11	O	TRUDL	TCON-Up Down selection			
		O	sD5	Serial Data Output Bit			
		O	FPG1	Green Flat Panel Output Bit			
83	G10	O	TRCLK	TCON-Row Driver Shift Clock	Pull Down	Open/Unconnected	0
		O	sD6	Serial Data Output Bit			
		O	FPR0	Red Flat Panel Output Bit			
84	G9	O	TCLRL	TCON-Left Right Selection			
		O	sD7	Serial Data Output Bit (MSB)			
		O	FPR1	Red Flat Panel Output Bit			
85	F11	O	TCREV	Data Inversion Control Output (Inversion: high, Normal: low)			
		I/O	GPI_41	General Purpose Data I/O			
86	F10	O	TCPOLN	TCON-Column Driver Inversion Polarity (Negative)			
		O	sVS	Serial VSYNC			
		I/O	GPI_40	General Purpose Data I/O			
		I	BOOT_SEL	(Bootstrap) Boot selection H: ISP, L: SPI flash			
89	E12	O	FPR2	Red Flat Panel Output Bit			
90	E11	O	FPR3	Red Flat Panel Output Bit			
91	E10	O	FPR4	Red Flat Panel Output Bit			

TABLE 1. PIN DESCRIPTIONS (Continued)

PIN#		I/O	PIN NAME	DESCRIPTION	INTERNAL CONNECTION	RECOMMENDED CONNECTION OF UNUSED PIN	STATUS AT HW RESET
LQFP	TFBGA						
92	E9	O	FPR5	Red Flat Panel Output Bit	Pull Down	Open/Unconnected	0
93	D12	O	FPR6	Red Flat Panel Output Bit			
94	D11	O	FPR7	Red Flat Panel Output Bit			
95	D10	O	FPG2	Green Flat Panel Output Bit			
96	C12	O	FPG3	Green Flat Panel Output Bit			
97	C11	O	FPG4	Green Flat Panel Output Bit			
98	C10	O	FPG5	Green Flat Panel Output Bit			
99	B12	O	FPG6	Green Flat Panel Output Bit			
100	B11	O	FPG7	Green Flat Panel Output Bit			
101	A12	O	FPB2	Blue Flat Panel Output Bit			
102	A11	O	FPB3	Blue Flat Panel Output Bit			
103	A10	O	FPB4	Blue Flat Panel Output Bit			
104	B10	O	FPB5	Blue Flat Panel Output Bit			
105	C9	O	FPB6	Blue Flat Panel Output Bit			
106	B9	O	FPB7	Blue Flat Panel Output Bit			
109	B8	O	VDCLK	656 Clock	-	Open/Unconnected	Hi-Z
110	C8	O	VD0	656 Data Output			
		I/O	GPIO_60	General Purpose Data I/O			
		I/O	P1.6/INT13	MCU Port/Interrupt Input			
		O	PWM2	PWM Control 2			
111	D8	O	VD1	656 Data Output			
		I/O	GPIO_61	General Purpose Data I/O			
		I/O	P1.7/INT14	MCU Port/Interrupt Input			
		O	PWM3	PWM Control 3			
112	A8	O	VD2	656 Data Output			
		I/O	GPIO_62	General Purpose Data I/O			
		I/O	P3.2/GATE0	MCU Port/GATE0 Input			
		O	PWM4	PWM Control 4			
113	B7	O	VD3	656 Data Output			
		I/O	GPIO_63	General Purpose Data I/O			
		I/O	P3.3/GATE1	MCU Port/GATE1 Input			
114	C7	O	VD4	656 Data Output			
		I/O	GPIO_64	General Purpose Data I/O			
		I/O	P3.4/T0	MCU Port/T0			
115	A7	O	VD5	656 Data Output			
		I/O	GPIO_65	General Purpose Data I/O			
		I/O	P3.5/T1	MCU Port/T1			
116	B6	O	VD6	656 Data Output			
		I/O	GPIO_66	General Purpose Data I/O			
		I/O	P3.6/RXD1	MCU Port/RXD1			
117	C6	O	VD7	656 Data Output			
		I/O	GPIO_67	General Purpose Data I/O			
		I/O	P3.7/TXD1	MCU Port/TXD1			
120	A5	I	RSTB#	Reset Pin	Pull up	-	1

TABLE 1. PIN DESCRIPTIONS (Continued)

PIN#		I/O	PIN NAME	DESCRIPTION	INTERNAL CONNECTION	RECOMMENDED CONNECTION OF UNUSED PIN	STATUS AT HW RESET
LQFP	TFBGA						
121	D6	I	TM	Test Mode Input	Pull Down	Connect to VSS	0
122	B5	O	LEDP	LED Control Pulse Out	Pull Down	Open/Unconnected	-
		O	PWM1	PWM Control 1			
123	C5	O	DCDCP	DCDC Pulse Out			
DIGITAL POWER							
55, 88, 108	L7, F12, A9	P	VDD33	Digital I/O Power +3.3V	-	-	Pwr
52, 87, 107	J6, F9, D9	P	VSS33	Digital I/O Ground			
22, 72, 119	G1, K12, A6	P	VDD18	Digital Core Power +1.8V			
21, 71, 118	H4, J9, D7	P	VSS18	Digital Core Ground			
	E5, F5, G5, H5, E6, F6, G6, H6, E7, F7, G7, H7, E8, F8, G8, H8	P	VSS18 (Thermal Ball)	Digital Core Ground	-	-	Pwr

NOTES:

6. Pull-up Resistor 38kΩ (minimum), 54kΩ (typical), 83kΩ (maximum).
7. Pull-down Resistor 35kΩ (min), 57kΩ (typical), 107kΩ (maximum).
8. "-" means N/A

Absolute Maximum Ratings

V_{DDA18} (Measured to V_{SSA18}) 1.8V, VDDAM (Note 9) 1.98V
V_{DDA33} (Measured to V_{SSA33}) 3.3V (Note 9), VDDA33M 3.6V
V_{DD18} (Measured to V_{SS18}) 1.8V (Note 9), VDD18M 1.98V
V_{DD33} (Measured to V_{SS33}) 3.3V, VDD33M 3.6V
Voltage on any Digital Signal Pin (Note 9) . . . . . V_{SS33} - 0.5 to 5.5V
Analog Input Voltage (Supplied by 1.8V) . . . . . V_{SSA18} - 0.5 to 1.98V
ESD Ratings
- Human Body Model (Tested per AEC-Q100-002) 2kV
- Machine Model (Tested per AEC-Q100-003) 200V
- Charged Device Model (Tested per AEC-Q100-011) 750V

Latch-Up (Per JESD-78D; Class 2, Level A; AEC-Q100-004) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Q128.14x14 LQFP (Notes 10, Note 12) . .	42	12
V172.8x8 TFBGA (Notes 11, 12)	35	11

Junction Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range (TW8835) . . . . . -40°C to +85°C
Ambient Temperature Range (TW8835AT) . . . . . -40°C to +105°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

9. V_{DDA18}: AVDAD, AVDPLL
   V_{SSA18}: AVSAD, AVSPLL
   V_{DDA33}: AVDTSC
   V_{SSA33}: AVSTSC
   V_{DD33}: VDD33
   V_{SS33}: VSS33
   V_{DD18}: VDD18
   V_{SS18}: VSS18
10. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
11. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
12. For θ_{JC}, the “case temp” location is taken at the package top center.

Electrical Specifications

Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C (TW8835), -40°C to +105°C (TW8835AT).**

PARAMETER	SYMBOL	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
SUPPLY					
Power Supply — IO 3.3V	V_{DD33}	**3.15**	3.3	**3.6**	V
Power Supply — Digital Core 1.8V	V_{DD18}	**1.62**	1.8	**1.98**	V
Power Supply — Analog 3.3V	V_{DDA33}	**3.15**	3.3	**3.6**	V
Power Supply — Analog 1.8V	V_{DDA18}	**1.62**	1.8	**1.98**	V
Analog Supply Current 1.8V (CVBS)	Iaa18		38.2		mA
(Component 1080p)	Iaa18		189.3		mA
(DTV 1080p)	Iaa18		13		mA
Analog Supply Current 3.3V	Iaa33		3.6		mA
Digital I/O Supply Current 3.3V (Note 14)	Idd33		30		mA
Digital Core Supply Current (Notes 14, 15) (CVBS, 27MHz)	Idd18		116		mA
(CVBS, 108MHz)	Idd18		141		mA
(Component 1080p, 108MHz)	Idd18		161		mA
(DTV 1080p, 108MHz)	Idd18		146		mA
DIGITAL INPUTS					
Input High Voltage (TTL)	V_{IH}	**2**			V
Input Low Voltage (TTL)	V_{IL}			**0.8**	V
Input High Voltage (XTI)	V_{IH}	**2**		**V_{DD33} + 0.5**	V
Input Low Voltage (XTI)	V_{IL}			**0.8**	V
Input High Current (V_{IN} = V_{DD})	I_{IH}			**10**	µA

Electrical Specifications

Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C (TW8835), -40°C to +105°C (TW8835AT). (Continued)**

PARAMETER	SYMBOL	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
Input Low Current (V_{IN} = V_{SS})	I_{IL}			**–10**	µA
Input Capacitance (f = 1MHz, V_{IN} = 2.4V)	C_{IN}		5		pF
DIGITAL OUTPUTS					
Output High Voltage (I_{OH} = –4mA)	V_{OH}	**2.4**	-	**V_{DD33}**	V
Output Low Voltage (I_{OL} = 4mA)	V_{OL}		0.2	**0.4**	V
3-State Current	I_{OZ}			**10**	µA
Output Capacitance	C_O		5		pF
ANALOG INPUT					
Analog Pin Input Voltage	Vi	-	1	-	V_{P-P}
YIN0, YIN1, YIN2 and YIN3 Input Range (AC Coupling Required)		**0.5**	1	**2**	V_{P-P}
CIN0, CIN1 Amplitude Range (AC Coupling Required)		**0.5**	1	**2**	V_{P-P}
VIN0, VIN1 Amplitude Range (AC Coupling Required)		**0.5**	1	**2**	V_{P-P}
SOG0, SOG1 Input Range		**0.02**	0.3	**1.8**	V
LEDS Input Range			-		V
DCDCS			-		V
Analog Pin Input Capacitance	C_A		7		pF
ADCs					
ADC Resolution	ADCR		9		Bits
ADC Integral Nonlinearity	AINL		±1		LSB
ADC Differential Nonlinearity	ADNL		±1		LSB
ADC Clock Rate	f_{ADC}		27	**150**	MHz
Video Bandwidth (-3dB)	BW		9	-	MHz
HORIZONTAL PLL					
Line Frequency (50Hz)	f_{LN}		15.625		kHz
Line Frequency (60Hz)	f_{LN}		15.734		kHz
Static Deviation	Δf_H		-	**6.2**	%
SUBCARRIER PLL					
Subcarrier Frequency (NTSC-M)	f_{SC}		3579545		Hz
Subcarrier Frequency (PAL-BDGHI)	f_{SC}		4433619		Hz
Subcarrier Frequency (PAL-M)	f_{SC}		3575612		Hz
Subcarrier Frequency (PAL-N)	f_{SC}		3582056		Hz
Lock In Range	Δf_H	**±450**	-		Hz
CRYSTAL SPECIFICATIONS (Note 16)					
Nominal Frequency (Fundamental)			27		MHz
Deviation				**±50**	ppm
Load Capacitance	CL		20		pF
Series Resistor	RS	-	80	-	Ω

NOTES:

13. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
14. Digital I/O and core power supply current measurement is base on WVGA output (40MHz clock rate) with SMPTE pattern.
15. 27MHz = MCU/SPI run with 27MHz system clock. Source, 108MHz = MCU/SPI run with 108MHz PLL clock source.
16. Crystal Deviation crossover normal operation temperature range.

Output Timing

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 17)	TYP	MAX (Note 17)	UNIT
Duty Cycle FPCLK		FPCLK DIV = 0	40	50	60	%
FPCLK Low Time	t1	FPCLK = 9~150MHz	3.6		66.7	ns
FPCLK High Time	t2	FPCLK = 9~150MHz	3.6		66.7	ns
Output Hold Time	t3	FPCLK Div = 0, Pol = Low	6.0			ns
		FPCLK Div = 1, Pol = Low	9.0			ns
		FPCLK Div = 2, Pol = High	21.0			ns
		FPCLK Div = 3, Pol = Low	34.5			ns
Output Delay Time	t4	FPCLK Div = 0, Pol = Low		10.5	14.5	ns
		FPCLK Div = 1, Pol = Low		13.5	17.5	ns
		FPCLK Div = 2, Pol = High		25.5	29.5	ns
		FPCLK Div = 3, Pol = Low		39.5	43.5	ns

NOTE:

17. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

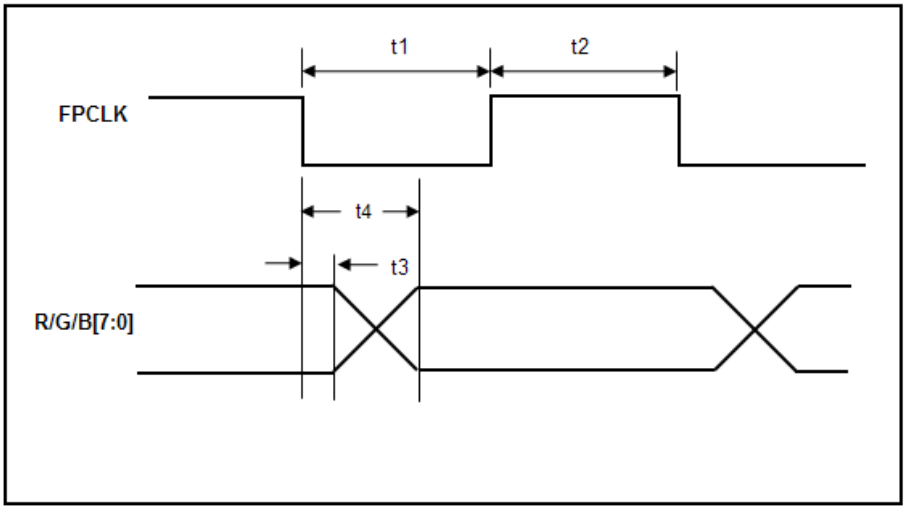


FIGURE 2. OUTPUT TIMING DIAGRAM

Functional Description

Overview

Intersil's TW8835 LCD video processor is a highly integrated TFT panel controller. It integrates a high quality 2D comb NTSC/PAL/SECAM video decoder, scalers, timing controller, flexible font based, SPI based OSD engine and high performance MCU. This unique level of mixed signal integration turns a TFT panel into a flexible display system. It incorporates easy to operate features in a single package for multipurpose in-car LCD display, portable DVD and DVR media players.

It contains all the logic required to convert analog or digital video signals in various formats to the signal formats that are necessary to drive various kind of TFT panel types. It supports different panel resolutions depending on the scaler and panel clock settings. It has built-in TCON for direct connecting with low cost TCON-less panel.

The integrated analog front-end contains ADCs with clamping circuits and an Automatic Gain Control (AGC) circuit as well as an antialiasing filter to minimize external component count. The built-in video decoder employs proprietary 2D Comb filter Y/C separation technologies to produce exceptionally high quality pictures.

The chip's internal logic synchronizes the panel frame rate to the incoming input frame rate. A high quality image scaling engine is used to convert the different input resolution formats to the output panel resolution. An internal deinterlacing engine also allows interlaced video to be displayed.

On-screen display is supported through on-chip multiwindow OSD engine for maximum flexibility.

It also has built-in backlight controller and panel bias voltage generator to further simplify the system design. The host control interface supports the standard 2-wire serial bus.

Analog Front-End

The analog front-end converts analog video signals to the required digital format. Each channel contains automatic clamping circuit, AGC circuit, antialiasing filter and high performance ADCs to minimize the external components used. The clamping circuit restores the signal DC level so it can be properly digitized. The analog inputs source selections are software programmable. Different input source has different signal conditioning logics to properly convert the signal into correct format for further processing.

Video Decoder

SYNC PROCESSOR

The decoder sync processor of video input detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video signal. The processor contains a digital phase-locked loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

Horizontal Sync Processing

The horizontal synchronization processing contains a sync separator, a Phase-Locked Loop (PLL) and the related decision logic.

The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. From there, the PLL also provides orthogonal sampling raster for the down stream processor. It has wide lock-in range for tracking any nonstandard video signal.

Vertical Sync Processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. A detection window controls the determination of sync. This provides more reliable synchronization. It simulates the functionality of a PLL without the complexity of a PLL. The field status is determined at vertical synchronization time based on the vertical and horizontal sync relationship.

COLOR DECODING

Y/C Separation

The color-decoding block contains the luma/chroma separation for the composite video signal and multistandard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/bandpass filter combination. For SECAM standard signals, only notch/bandpass filter is available. The default selection for NTSC/PAL is comb filter. The characteristics of the bandpass filter can be found in the filter curve section.

In the case of comb filter, the decoder separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary adaptive comb algorithm. It leads to good Y/C separation with small cross luma and cross color at both horizontal and vertical edges. Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen.

Color Demodulation

The color demodulation for NTSC and PAL standard is done by quadrature mixing the chroma signal to the base band and extracting the chroma components with low-pass filter. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The SECAM color demodulation process consists of bell filtering, FM demodulator and deemphasis filtering. The chroma carrier frequency is identified in the process and used to control the SECAM color demodulation.

The subcarrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input subcarrier reference (color burst). This arrangement allows any substandard of NTSC and PAL to be demodulated easily.

Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by transmission loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst

on the back porch. This color-burst amplitude is calculated and compared to standard amplitude. The chroma (Cx) signals are then compensated in amplitude accordingly. The range of ACC control is –6db to +24db.

Low Color Detection and Removal

For low color amplitude signals, black and white video or very noisy signals, the color will be “killed”. The color killer uses the burst amplitude measurement to switch off the color when the measured burst amplitude falls below a programmed threshold. The threshold has programmed hysteresis to prevent oscillation of the color killer operation. This function can be disabled by programming a low threshold value.

AUTOMATIC STANDARD DETECTION

The video decoder has its automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

VIDEO FORMAT SUPPORT

The integrated video decoder supports all common video formats as shown in Table 2. It needs to be programmed appropriately for each of the composite video input formats.

TABLE 2. VIDEO INPUT FORMATS SUPPORTED

FORMAT	LINES	FIELDS	FSC (MHz)	COUNTRY
NTSC-M	525	60	3.58	U.S., many others
NTSC-Japan (Note 18)	525	60	3.58	Japan
PAL-B, G, N	625	50	4.43	Many
PAL-D	625	50	4.43	China
PAL-H	625	50	4.43	Belgium
PAL-I	625	50	4.43	Great Britain, others
PAL-M	525	60	3.58	Brazil
PAL-CN	625	50	3.58	Argentina
SECAM	625	50	4.406 4.250	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.43	China
NTSC (4.43)	525	60	4.43	Transcoding

NOTE:

18. NTSC-Japan has 0 IRE setup.

COMPONENT PROCESSING

Luminance Processing

The video decoder adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

It also provides a sharpness control function through a control register. The center frequency of the peaking filter is selectable. A coring function is provided along with the sharpness control to reduce enhancement to the noise.

The Hue and Saturation

When decoding NTSC signals, the decoder can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift can be programmed through a control register.

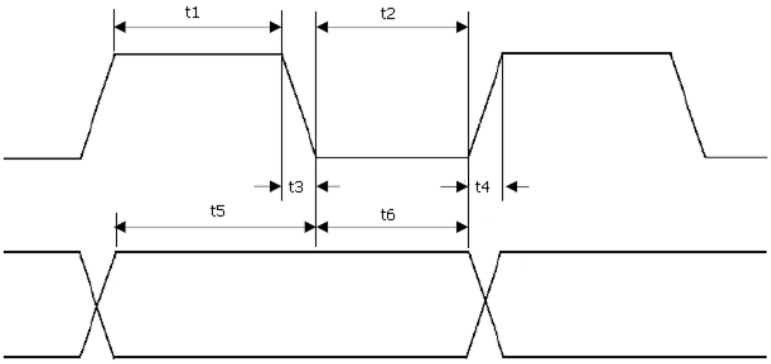
The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

Touch Screen Controller

Built-in 12-bit ADC touch screen controller in the TW8835 provides accurate position reading with simplified digital operation and can also be used to monitor up to four auxiliary inputs with touch interrupt.

Digital Input Support

In addition to analog inputs, it also has dual digital inputs mode for YCbCr/RGB data. The combination could be a RGB 565 plus BT.656 at the same time or a single 24-bit digital input mode up to 150MHz pixel clock. TW8835 supports both digital BT.656 as well as 8/16-bit 601 input. The 656 interface can work with both interlaced and progressive standard.



NOTE: High level is V_{IH} min. and Low level is V_{IL} max. found in the electrical characteristic table.

FIGURE 3. DIGITAL INPUT TIMING DIAGRAM

TABLE 3. DIGITAL INPUT TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DTV Clock Period	tCLK	6.73	-	-	ns
DTV Clock High Time	t1	3.36	-	-	ns
DTV Clock Low Time	t2	3.36	-	-	ns
Falling Time for DTV CLK	t3	-	-	4	ns
Rising Time for DTV CLK	t4	-	-	4	ns
Setup Time for Data, DE, HS, VS	t5	3.0	-	-	ns
Hold Time for Data, DE, HS, VS	t6	1.0	-	-	ns

Input Image Control

The input cropping control provides a way for programming the active display window region for the selected input video or graphic. In the normal operation, the first active line starts with the VSYNC signal. This and the vertical active length register setting are used to determine the active vertical window. The active pixel starts HSYNC. This and the horizontal active width register are used to determine the active horizontal window. The vertical window is programmed in line increments. The horizontal window is programmed in one pixel increments for single pixel input mode or two pixels increments for double pixels input mode. If a data qualifier is used, then only qualified pixels will be counted in the window size.

Image Scaling

The internal high quality image scaling engine operates in several modes. The first is the bypass mode. No image scaling is done in this mode. The number of active output lines per frame and the number of active output pixels per line are identical to the input active lines and pixels, respectively. This mode is best used for displaying computer graphic at panel's native resolution.

By default, the input active window is zoomed up to the full screen for display. This is used for noninterlaced data like PC graphics or progressive scan video. The vertical and horizontal magnification ratio can be adjusted independently. TW8835 has frame-sync mode which does not use frame buffer. In this mode, the zoom ratio and output clock rate should be coordinated appropriately to avoid internal buffer overrun.

The TW8835 has a build in 2D deinterlacing mode to process interlaced video inputs. In this mode, every input field is zoomed to the full output frame resolution. The deinterlaced fields can also be properly compensated to have fields aligned correctly to avoid any artifacts. The offset can be programmed to provide maximum flexibility.

The horizontal scaler can be programmed to perform nonlinear scaling: panorama scaling for displaying 4:3 input on a 16:9 display.

Image Enhancement Processing

BLACK/WHITE STRETCH

This feature is to expand dynamic range of the input image, which creates more vivid image impression.

TFT Panel Support

It supports a variety of active matrix TFT panel types and resolutions.

DITHERING

The TW8835 has the dithering circuit to reduce the output dynamic range to fit the panel type. This allows LCD panels with 3, 4, 6 or 8 bits per color per pixel to display up to 16.8 million colors and LCD panels with 3 bits per color per pixel to can display up to 2.1 million colors. It employs both spatial and frame modulation dithering. When dithering with the least significant 4 bits of input data it uses spatial modulation with 4x4 blocks of pixels. When dithering with the least significant 1 to 3 bits of input data, it uses either spatial modulation with 2x2 pixel blocks, or frame modulation.

GAMMA TABLE

It has an integrated gamma table for each color output and it is fully programmable through host bus.

TCON

The integrated timing controller supports flexible column/row driver control signals to interface with TCON-less panel directly.

Font Based On-Screen Display

The TW8835 supports built-in OSD controller with programmable RAM font. The OSD display is independent of the input active window setting or the scaling ratio.

The on-chip OSD controller is a character-based controller. The predefined character or graphic bit map is stored in the font RAM. It can store up to 379 single color fonts when character is 12 pixels wide by 18 pixels high. The characters can be displayed on the screen in four user defined window locations of any size from 1 to 512 characters. The spaces between characters are also programmable. There is a limit of 512 characters that may be displayed on-screen at one time in all windows combined. The attributes of each window can also be set to give it a shadow effect or 3-D effect. In addition, the characters can be expanded by a factor of 2, 3 or 4 in vertical or horizontal directions and have the blinking effect and border/shadow effect on a character by character basis.

ON CHIP OSD FUNCTIONS

Font SRAM: Max 379 (12x18) User Programmable Single Color Font (10240x8 SRAM)

- Character Register SRAM: 512 Location (9-bit Font Address + 10-bit Character Attribute, 512x19 SRAM)
- Characters
  - Character Color: 16 colors
  - Character Background Color: 16 colors
  - Character Blinking: Enable/Disable, 1Hz Blinking frequency
  - Character Border/Shadow Effect: Enable/Disable

Multi OSD Window Display Case: Chip has a limitation

- Character Space: Both H and V programmable by number of pixels
- Quick Character Change in Window: Programmable Start Address and Buffer Size
- Programmable OSD Color Palette Support
- Number of Windows: 4 Independent Windows
- Window Color: 16 colors
- Window Zoom: 2, 3, 4 times zoom by dot number, H/V separate zooming control
- Window Position: Programmable
  - H Direction: 1-pixel per step, V Direction: 1-Line per step
- Window Size: Both H and V programmable by number of characters
- Window Bordering/Shadowing Effect: 4 Independent Windows Enable/Disable Control
- Window Alpha Blending Control: 4 Independent Windows Control
- → 16 Different Color for Alpha Blending support (4-bit control)
- Window 3-D Effect: 4 Independent Windows Enable/Disable Control
- Window Border Color: 16 Colors
- Window Border Width: programmable

BASIC REGISTER SETTING FLOW EXAMPLE FOR BUILT-IN OSD CONTROLLER

Step_1: OSD_FONT_SIZE_CONFIGURATION

1. Select FONT Width to be 12 or 16 . . . . . - 0x300 (bit4)
1. Set FONT Height . . . . . - 0x350 (bit4-0)
1. Set Sub-Font Total Count . . . . . - 0x351 (bit6-0)

Step_2: OSD_WINDOW_CONFIGURATION setting for **Window#1** (0x310~0x31F)

Note: **Window#2** (0x320~0x32F), **Window#3** (0x330~0x33F), **Window#4** (0x340~0x34F)

1. OSD Window Disable	0x310, bit7
2. OSD Window Zoom multiplier	0x310, bit1-0: V, bit3-2: H
3. OSD Window H/V Border Color	0x31E, bit7-4
4. OSD Window 3-D Effect Top/Bottom Mode Select	0x31B, bit6
5. OSD Window 3-D Effect Level Select	0x31B, bit5
6. OSD Window 3-D Effect Enable/Disable	0x31B, bit7
7. OSD Window H-Start Location (see details on page 21)	0x313, bit7-0 0x312, bit6-4
8. OSD Window V-Start Location (see details on page 21)	0x314, bit7-0 0x312, bit1-0
9. OSD Window Width	0x316, bit5-0
10. OSD Window Height	0x315, bit5-0
11. OSD Window Border Line Width	0x318, bit4-0
12. OSD Window Border Line Color	0x317, bit3-0
13. OSD Window Border Line Enable	0x318, bit7
14. OSD Window Shadow Width	0x31C, bit4-0
15. OSD Window Shadow B color	0x31B, bit3-0
16. OSD Window Shadow Enable	0x31C, bit7
17. OSD Window H-Space Width (Between Border line and Characters)	0x319, bit6-0
18. OSD Window V-Space Width (Between Border line and Characters)	0x31A, bit6-0
19. Character H-Space Width (Between Character and Character)	0x31D, bit7-4 0x31C, bit6
20. Character V-Space Width (Between Character and Character)	0x31D, bit3-0 0x31C, bit5
21. OSD Window Alpha Blending Color Select	0x352, bit4-0
22. OSD Window Alpha Blending Value Control	0x311, bit3-0
23. Window content start address	0x317, bit4 0x31F, bit7-0
24. Repeat 1 – 23 for Window #2~#4	

Step_3: OSD_COLOR_ATTRIBUTE/FONT setting (OSD RAM)

1. Enable OSD RAM Access
   - 0x304 (bit0 = 0)
2. Set Multicolor Start Address
   - 0x305 (bit3-1), 0x30B (bit7-0), 0x353 (bit7-0), 0x354 (bit7-0)
3. OSD RAM Address
   - 0x305 (bit0), 0x306 (bit7-0)
   - The first address is Step_1_23 Window content start address.
4. OSD RAM Data Port High (Font Address)
   - 0x307 Data is written to above address automatically.
   - 0x304 (bit5 = 0) select lower 256 characters. (bit5 = 1) select upper 256 characters.
5. OSD RAM Data Port Bit18 (Border Effect), Bit17 (Blinking Effect), Bit16 (Upper|Lower 256 characters.)
   - 0x304 Bit4, Bit7, and Bit5 Data are written to above address automatically.
6. OSD RAM Data Port Low (Color Attribute)
   - 0x308 Data is written to above address automatically.
7. Repeat steps 3, 4, 5, and 6
   - The address should be increased by one each.

Step_4: COLOR LOOK-UP TABLE setting

1. Select Color Look-Up Table Write Address
   - 0x30C (bit[5:0])
   - BIT[5:0]: These 6 bits specify one of the 64 entries in the look-up table. Each entry is a 16-bit RGB color by its content.
   - There are 65536 colors available. For single color font, only sixteen of them are accessible by OSD controller at a given time.
2. Color Look-Up Table control bits setting
   - 0x30D (High Byte), 0x30E (Low Byte)
   - The data of the Look-Up Table is accessed through 0x30D and 0x30E.
3. Repeat steps 1 and 2 to program each entry of the Look-Up Table.

Step_5: FONT_RAM_DATA setting (FONT RAM)

1. Enable FONT RAM Access
   - 0x304 (bit0 = 1)
2. FONT RAM Address Setting - 9 bits (h000 – h1FF, except 0x0FE/0x0FF/0x1FE/0x1FF)
   - 0x304(bit5), 0x309(bit7-0)
   - h000~h1FF : Single Font RAM (379 Programmable Characters)
3. FONT RAM Data Port
   - 0x30A Data is written to above address automatically.
4. Repeat (3) at 27 times for one FONT RAM Data
   - The internal address automatically increases by one each.
5. New FONT RAM Address Setting – 9 bits
6. Repeat 3), 4), 5)
   - The FONT RAM Address should be increased by one each.

Note: as for the FONT RAM configuration and font bit mapping, see the detailed description

Step_6: End of OSD setting and Enable OSD

1. 1. OSD On/Off Enable Control 0: ON, 1: OFF
   - 0x30C (bit6 = 0)
2. OSD Window Enable
   - 0x310 (bit7 = 1) Window1 Enable

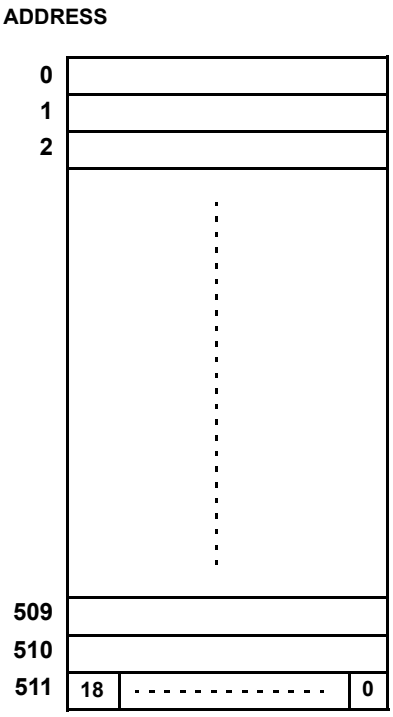
OSD WINDOW START LOCATION: BUILT-IN OSD CONTROLLER

Internal generated OSD DE position delayed from H-SYNC: 0x303[7:0].

OSD window H_start location from start of internal OSD DE: 0x312[6:4], 0x313[7:0] increment by 1 pixel at a time.

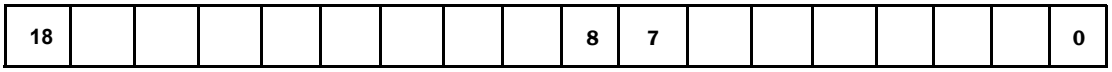
OSD window V_start location from start of VACT: 0x312[1:0], 0x314[7:0] increment by 1 line at a time.

OSD_RAM CONFIGURATION



The characters can be displayed on the screen in eight user defined window locations of any size from 1 to 512 characters. There is a limit of 512 characters that may be displayed on-screen at one time in all windows combined.

Example:
Window #1: Address 0 – 2 (3 character)
Window #2: Address 3 – 100 (98 character)
Window #3: Address 101– 254 (154 character)
Window #4: Address 255 - 511 (257 character)



FONT_ADDRESS (11 Bits)

Bit 18: Border/Shadow
Bit 17: Blinking
Bit 16: Up256
Bit 15-8: FONT Address

FONT_ATTRIBUTE (8 Bits)

Bit 7: Character's Background Color Extension
Bit 6: Character's Background R
Bit 5: Character's Background G
Bit 4: Character's Background B
Bit 3: Character's Color Extension
Bit 2: Character R
Bit 1: Character G
Bit0: Character B

ALPHA BLENDING FOR OSD WINDOW

The TW8835 uses "Alpha Blending" in OSD 4 separation windows and 64 separation colors. The upper 32 separation colors are forced to 0. Alpha blending mixes (adds) the video signal and OSD signal at the following specified levels. In other words, alpha blending determines the transparency of the OSD window each color to in relation to video signal. When alpha blending is disabled, the only OSD data is displayed in OSD window.

The alpha blending level selection are 4-bit assigned, it can support 8 different level controls.

The alpha blending level bits are in register 0x311[3:0] for window#1, 0x321[3:0] for window#2, 0x331[3:0] for window#3, 0x341[3:0] for window#4 and alpha blending color selection bits are in register 0x352[4:0] for 32 separation colors.

ALPHA[3:0]	VIDEO LEVEL (%)
0000	0.00
0001	12.5
0010	25.0
0011	37.5
0100	50.0
0101	62.5
0110	75.0
0111	87.5
1000	100

ALPHA BLENDING CONCEPT

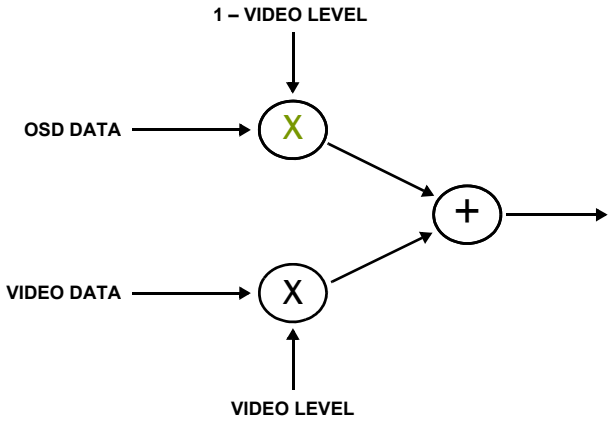


FIGURE 4. ALPHA BLENDING CONCEPT

SPI Flash On-Screen Display

The TW8835 SPIOSD provides a flexible mapping between its display on the LCD and its bit mapped image stored in the SPI memory. There are total nine windows provided. One of the windows is of “Complex” type, the rest are of “Simple” type.

In general, a buffer in the SPI memory is allocated for the image to be displayed. The “Simple” type refers to the windows that have the same buffer size and display size. Whereas the buffer size of a “Complex” window is usually larger than the display size. The SPIOSD Window #0 is designated as “Complex” window. The other eight windows (SPIOSD Window #1 ~ #8) are “Simple” windows.

The bit mapped image stored can be 4, 6 or 8 bits per pixel. During display, the pixel is fetched from the SPI memory and mapped to a 32-bit real color pixel by the LUT (Look-Up Table). This 32-bit real color pixel consists of 24-bit RGB, 7-bit alpha blending attribute, and one bit blinking attribute. The real color pixel is then mixed with video before displaying on the LCD panel.

To reduce the storage size and the access time, RLC (Run Length Code) decode circuitry is provided. However, only one of the eight “Simple” windows can be assigned to receive RLC pixel data. The other windows must receive uncompressed pixel data.

Each of the nine windows has its own set of register but shares a common 512 entry LUT. For each window, LUT Entry Offset register is provided for flexible mapping.

All nine windows can be active and overlapped at the same time without blending among themselves. Blending with video can be pixel based or window based.

Looping control for adjacent buffers is provided for the “Complex” window. Animation can be achieved by properly allocating multiple buffers in the adjacent area and the looping control.

SPIOSD Window Display Starting Location and Sizes

There are four registers used to specify the staring location and size on the LCD:

1. Window i Horizontal Start
2. Window i Vertical Start
3. Window i Horizontal Length
4. Window i Vertical Length

SPIOSD Window Buffer Memory

Two (or three for Complex window) registers define the buffer starting location and boundaries:

1. Window i Buffer Memory Starting Address
2. Window i Buffer Memory Horizontal Length
3. Window i Buffer Memory Vertical Length (Complex window only)

For Complex window two additional registers point to the starting location of the image stored:

1. Window i Image Vertical Start (Complex window only)
2. Window i Image Horizontal Start (Complex window only)

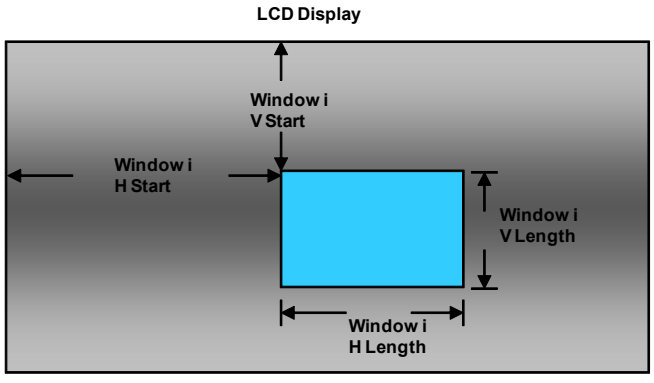


FIGURE 5. SPIOSD WINDOW DISPLAY STARTING LOCATION AND SIZES

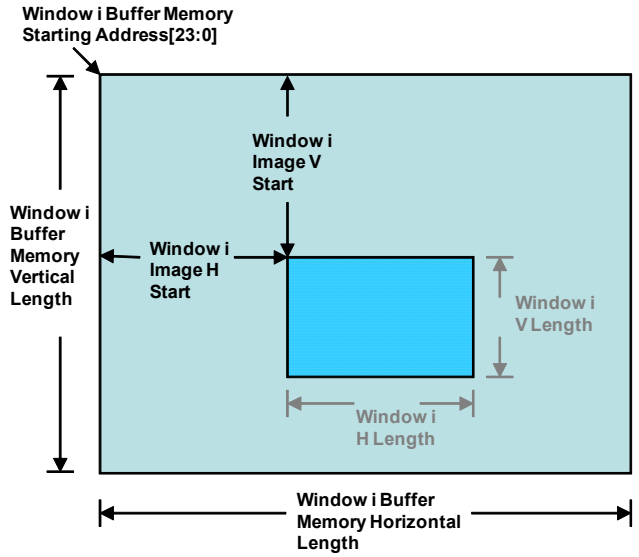


FIGURE 6. SPIOSD WINDOW BUFFER MEMORY

SPIOSD Window Loop Control

For Complex window, three registers are used for loop control:

1. **Window i Looping Horizontal Frame Number** (Complex window only)
2. **Window i Looping Vertical Frame Number** (Complex window only)
3. **Window i Frame Duration** (Complex window only)

In Figure 7, the **Looping Horizontal Frame Number** register contains a value N, and the **Looping Vertical Frame Number** register contains a value M. The display starts from Frame #00 and then moves horizontally to the right and then vertically down. The display order is #00, #01, #02, ... #0N, #10, #11, #12, ... #1N, ... #M0, #M1, ... #MN. Each frame stays on for the time specified by the **Frame Duration** register.

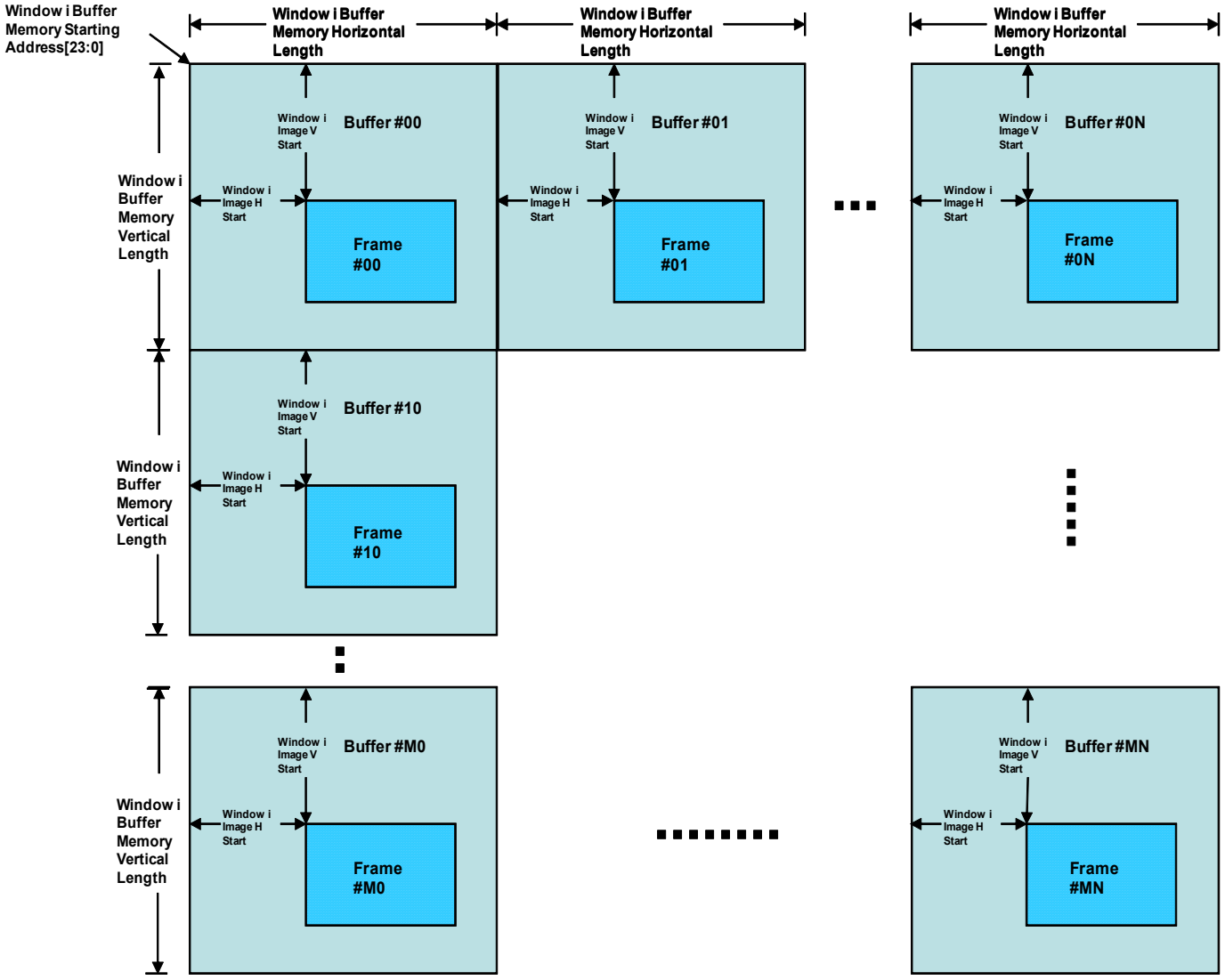


FIGURE 7. SPIOSD WINDOW LOOP CONTROL

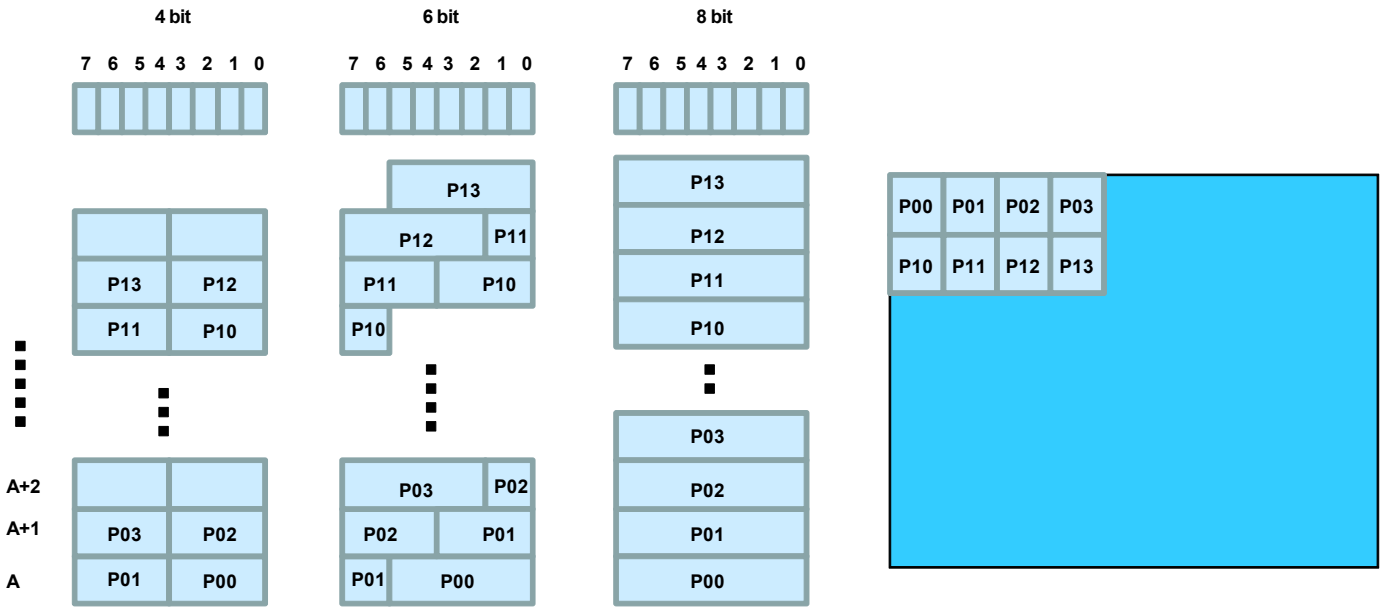


FIGURE 8. PIXEL ORDER

PIXEL ORDER

Pixel data (uncompressed) stored in SPI memory follows Little Endian order.

Figure 8 shows the pixel on LCD display and its corresponding storage order in the SPI memory for pixel width 4-, 6- and 8-bit wide.

RLC DATA FORMAT

RLC data format is shown in Figure 9:

FIGURE 9. RLC DATA FORMAT

T: Type to follow, 0 for Data, 1 for CNT
DATA: Uncompressed data
CNT: Repeat count

The width of DATA and CNT are set by the RLC Control register. The valid DATA width is 4, 6 or 8. The width of CNT can be 2 up to 16.

Figure 10 shows the original data sequence of D0, D1, D2, D3, D4 and D5 before and after compression. In this example, the DATA width is 8 and the CNT width is 4. Data D2, D3 and D4 are the same.

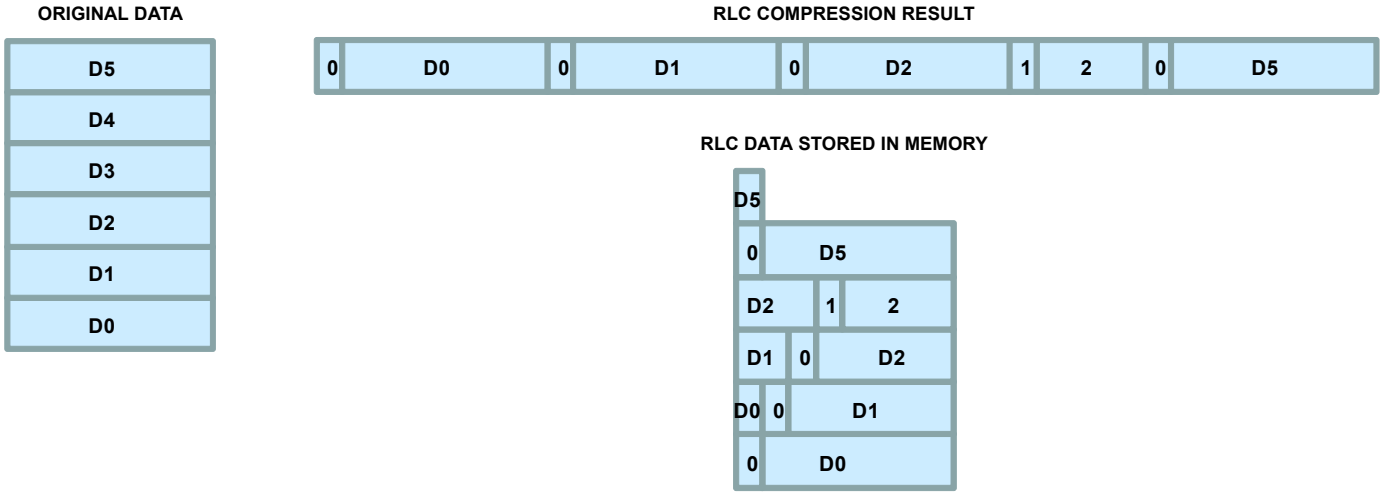


FIGURE 10.