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## **TYN412**

### Standard

**12 A SCR** 

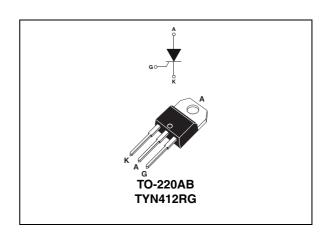
Custom Data

#### **Main features**

Symbol	Value	Unit
I <sub>T(RMS)</sub>	12	Α
V <sub>DRM</sub> /V <sub>RRM</sub>	400	V
I <sub>GT</sub>	15	mA

### **Description**

TYN412 with standard gate triggering levels, is a 12 A SCR suitable to fit all modes of control, found in applications such as overvoltage crowbar protection, motor control circuits in power tools and kitchen aids, inrush current limiting circuits, capacitive discharge ignition and voltage regulation circuits.



#### **Order codes**

Part Numbers	Marking	
TYN412RG	TYN412	

Table 1. Absolute ratings (limiting values)

Symbol	Parameter			Value	Unit
I <sub>T(RMS)</sub>	RMS on-state current (180° conduction angle) $T_c = 105^{\circ}$ C		T <sub>c</sub> = 105° C	12	Α
I <sub>T(AV)</sub>	Average on-state current (180° conduction	on angle)	T <sub>c</sub> = 105° C	8	Α
1.	Non repetitive surge peak on-state current	$t_p = 8.3 \text{ ms}$	T - 25° C	146	А
I <sub>TSM</sub>		t <sub>p</sub> = 10 ms	$T_j = 25^{\circ} C$	140	
l <sup>2</sup> t	I <sup>2</sup> t Value for fusing	t <sub>p</sub> = 10 ms	T <sub>j</sub> = 25° C	98	A <sup>2</sup> s
dI/dt	Critical rate of rise of on-state current $I_G$ = 2 x $I_{GT}$ , $t_r \le 100$ ns	F = 60 Hz	T <sub>j</sub> = 125° C	100	A/µs
I <sub>GM</sub>	Peak gate current $t_p = 20 \mu s$		T <sub>j</sub> = 125° C	4	Α
P <sub>G(AV)</sub>	Average gate power dissipation $T_j = 125^{\circ} C$			1	W
T <sub>stg</sub> T <sub>j</sub>	Storage junction temperature range Operating junction temperature range		- 40 to + 150 - 40 to + 125	° C	
V <sub>RGM</sub>	Maximum peak reverse gate voltage			5	V

Characteristics TYN412

## 1 Characteristics

Table 2. Electrical characteristics (T<sub>i</sub> = 25° C, unless otherwise specified)

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Symbol	Test Conditions			Value	Unit
	$V_D = 12 \text{ V}$ $R_L = 33 \Omega$		MIN.	2	mA
I <sub>GT</sub>	$v_D = 12 \text{ V}$ $n_L = 33 \Omega$	[L = 33 L2		15	IIIA
			MIN.	0.5	V
$V_{GT}$	$V_D = 12 V$ $R_L = 33 \Omega$		TYP.	0.7	
			MAX.	1.3	
$V_{GD}$	$V_D = V_{DRM}$ $R_L = 3.3 \text{ k}\Omega$	T <sub>j</sub> = 125° C	MIN.	0.2	V
I <sub>H</sub>	I <sub>T</sub> = 500 mA Gate open		MAX.	30	mA
IL	I <sub>G</sub> = 1.2 I <sub>GT</sub>		MAX.	60	mA
dV/dt	V <sub>D</sub> = 67 % V <sub>DRM</sub> Gate open	T <sub>j</sub> =125° C	MIN.	200	V/µs
V <sub>TM</sub>	$I_{TM} = 24 \text{ A}$ $t_p = 380  \mu\text{s}$	T <sub>j</sub> = 25° C	MAX.	1.6	V
V <sub>t0</sub>	Threshold voltage	T <sub>j</sub> = 125° C	MAX.	0.85	V
R <sub>d</sub>	Dynamic resistance	T <sub>j</sub> = 125° C	MAX.	30	mΩ
I <sub>DRM</sub>	VV	T <sub>j</sub> = 25° C	MAX.	0.01	mA
$I_{RRM}$	$V_{DRM} = V_{RRM}$	T <sub>j</sub> = 125° C	IVIAA.	3	mA

Table 3. Thermal resistance

P(W)

11 10

9

2

Symbol	Parameter		Unit
R <sub>th(j-c)</sub>	Junction to case (DC)	1.3	° C/W
R <sub>th(j-a)</sub>	Junction to ambient (DC)	60	° C/W

Figure 1. Maximum average power dissipation versus average on-state current

 $I_{T(AV)}(A)$ 

IT(AV)(A)

12

10

8

6

4

2

0

25

50

75

100

125

Figure 2. Average and D.C. on-state current versus case temperature

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TYN412 Characteristics

Figure 4.

 $K=[Z_{th(j-a)}/R_{th(j-a)}]$ 

Figure 3. Relative variation of thermal impedance junction to case versus pulse duration

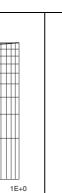
 $K=[Z_{th(j-c)}/R_{th(j-c)}]$ 

1.0

0.5

0.2

0.1 L 1E-3



Relative variation of thermal impedance junction to ambient versus pulse duration

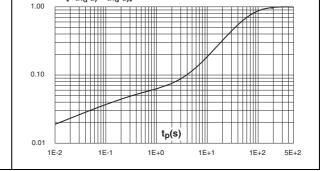
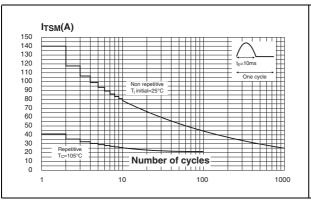


Figure 5. Surge peak on-state current versus Figure 6. number of cycles

1E-1

tp(s)

Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10 ms, and corresponding values of  $l^2t$ 



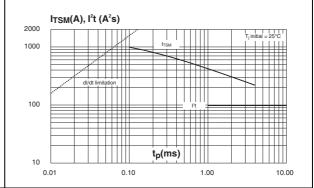
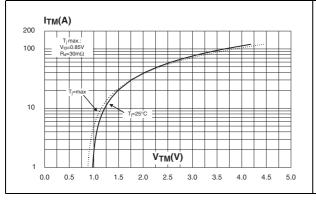
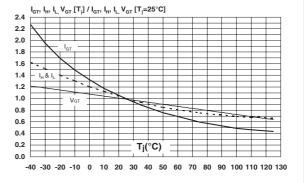


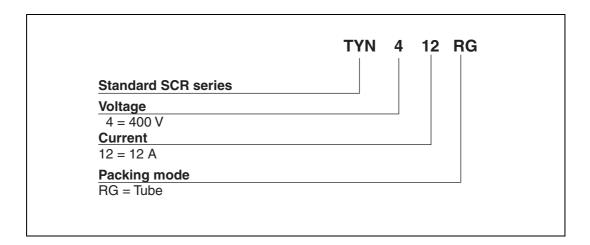
Figure 7. On-state characteristics (maximum Figure 8. values)

Relative variation of gate trigger current, holding current, latching current and gate trigger voltage versus junction temperature (typical values)





# 2 Ordering information scheme

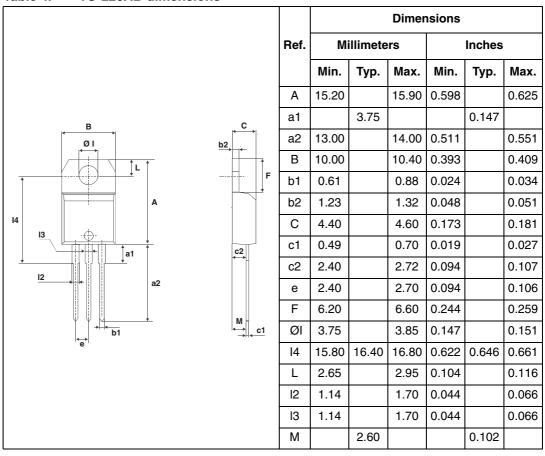


TYN412 Package information

## 3 Package information

Epoxy meets UL94, V0

Table 4. TO-220AB dimensions



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

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Ordering information TYN412

# 4 Ordering information

Ordering type	Marking	Package	Weight	Base qty	Delivery mode	
TYN412RG	TYN412	TO-220AB	2.3 g	50	Tube	

## 5 Revision history

Date	Revision	Description of Changes
06-Apr-2007	1	First issue

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