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TYN60K-1400T

SCR

17 January 2017 Product data sheet

1. General description

Planar passivated Silicon Controlled Rectifier in a SOT1259 (3-lead TO-3P) plastic package intended for use in applications requiring very high inrush current capability and high thermal cycling performance.

2. Features and benefits

- High thermal cycling performance
- Planar passivated for voltage ruggedness and reliability
- High voltage capacity
- Very high current surge capability

3. Applications

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control
- Uninterruptible Power Supply (UPS)
- Solid State Relay (SSR)
- Traction battery charging

4. Quick reference data

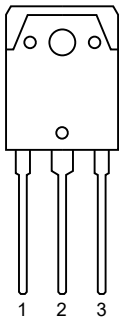
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	1400	V
V_{RRM}	repetitive peak reverse voltage			-	-	1400	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	750	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	-	825	A
T_j	junction temperature			-	-	150	°C
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq$ 124 °C		-	-	60	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq$ 124 °C; Fig. 1; Fig. 2; Fig. 3		-	-	94	A

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7; Fig. 8		-	-	80	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 938 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		1500	-	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathod	 **TO3P (SOT1259)**	
2	A	anode		
3	G	gate		
mb	mb	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
TYN60K-1400T	TO3P	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO3P	SOT1259

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	1400	V
V_{RRM}	repetitive peak reverse voltage			-	1400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 124$ °C		-	60	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 124$ °C; Fig. 1; Fig. 2; Fig. 3		-	94	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	750	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	825	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse		-	2812	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 200$ mA		-	150	A/µs
I_{GM}	peak gate current			-	8	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	20	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	150	°C

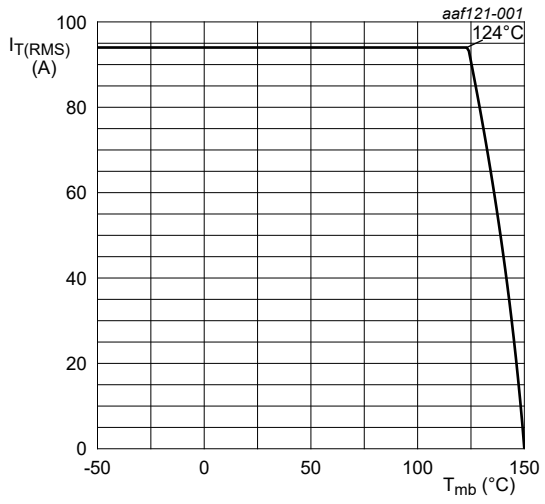
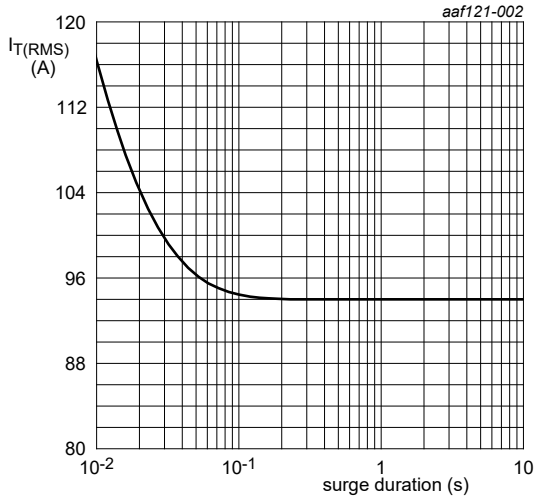
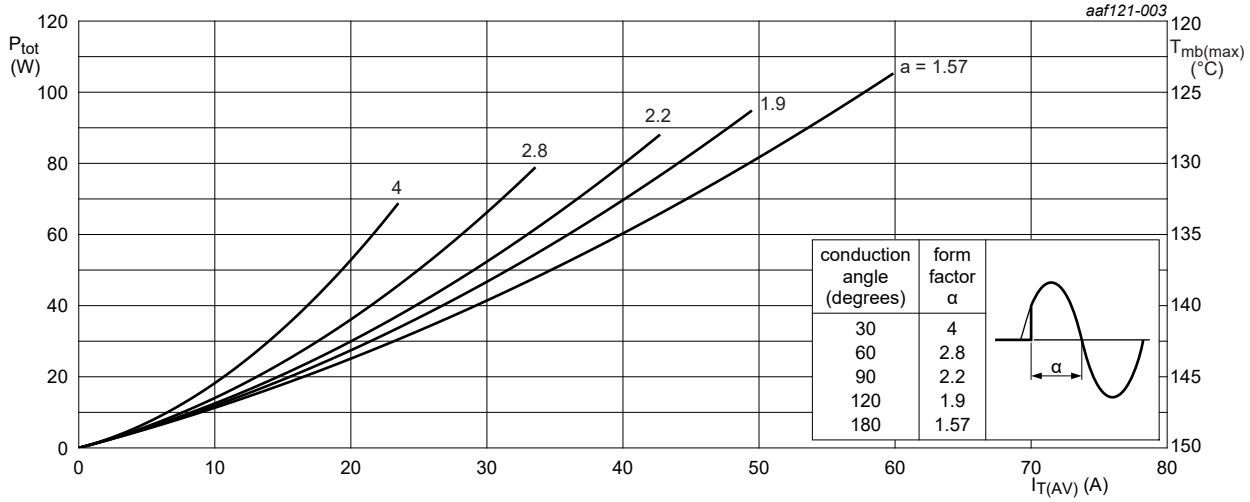


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz; $T_{mb} = 124$ °C

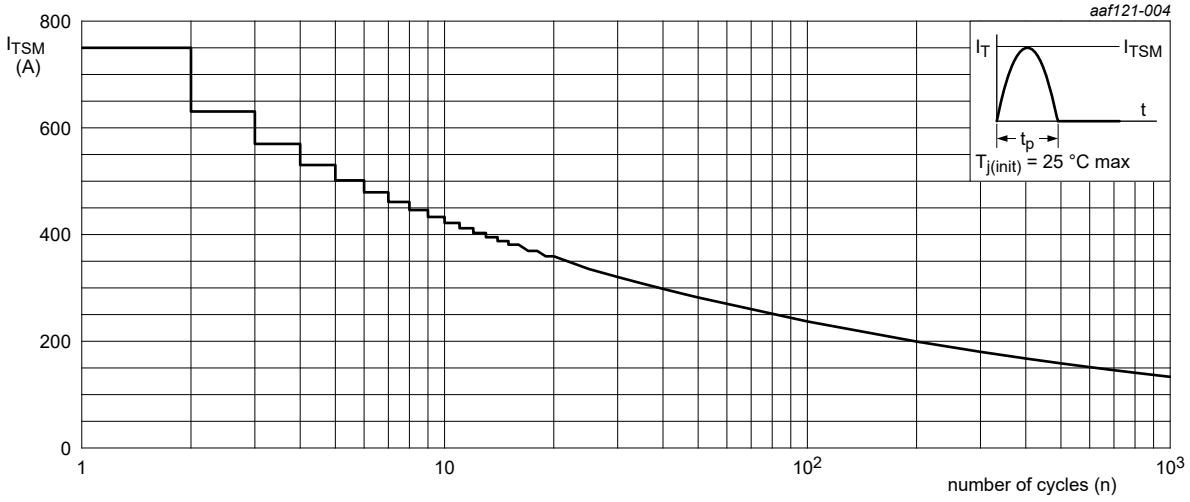
Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle

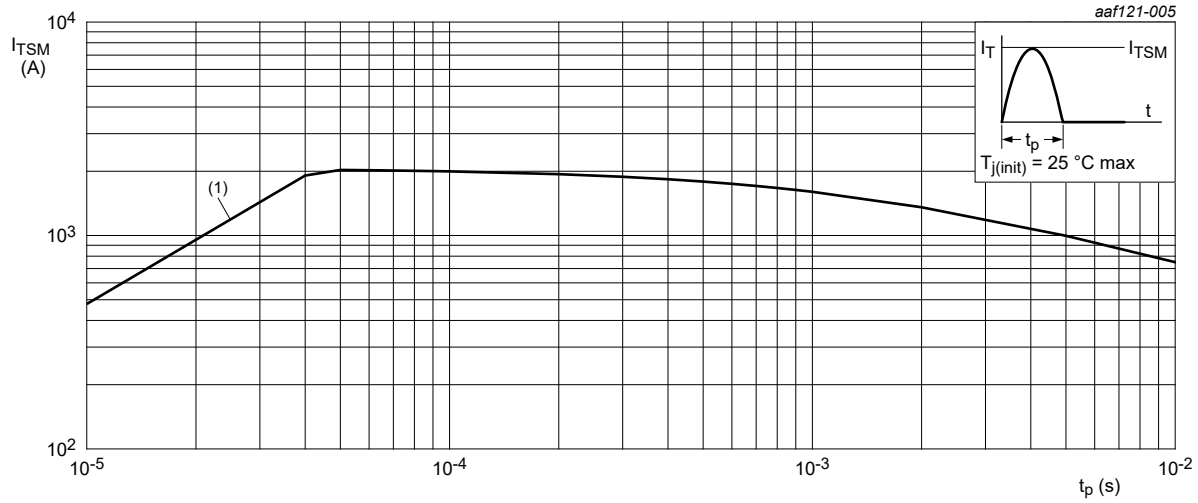
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 6		-	-	0.25	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air		-	50	-	K/W

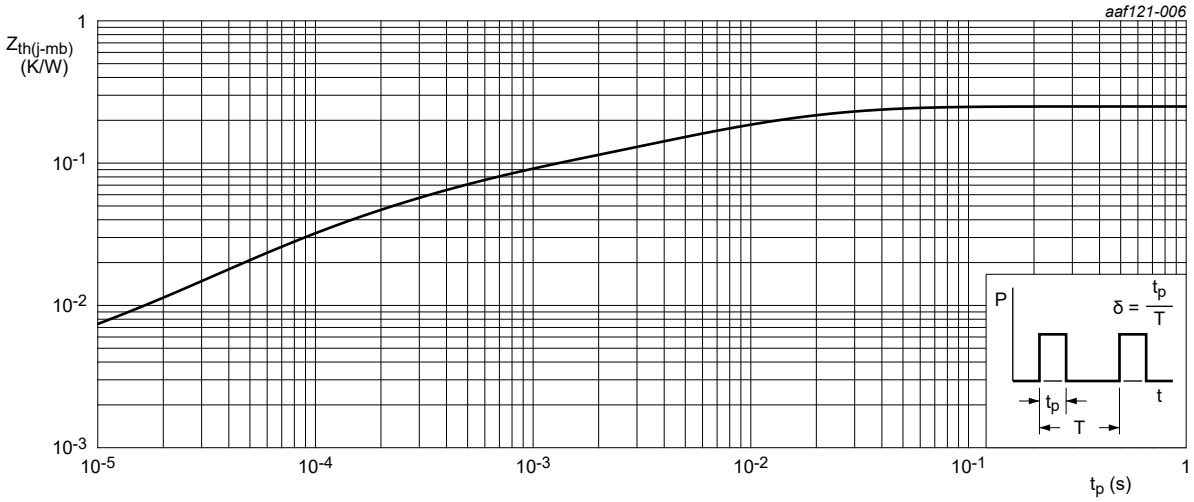


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7; Fig. 8		-	-	80	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 9		-	155	300	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	115	200	mA
V_T	on-state voltage	I_T = 60 A; T_j = 25 °C; Fig. 11		-	-	1.35	V
		I_T = 120 A; T_j = 25 °C; Fig. 11		-	-	1.65	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 12		-	0.7	1	V
		V_D = 800 V; I_T = 0.1 A; T_j = 150 °C; Fig. 12		0.2	0.45	-	V
I_D	off-state current	V_D = 1400 V; T_j = 150 °C		-	5	10	mA
I_R	reverse current	V_R = 1400 V; T_j = 150 °C		-	3	10	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 938 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		1500	-	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 40 A; V_D = 800 V; I_G = 0.1 A; dI_G/dt = 5 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 938 V; T_j = 125 °C; I_{TM} = 20 A; V_R = 25 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 50 V/µs; $R_{GK(ext)}$ = 100 kΩ; (V_{DM} = 67% of V_{DRM})		-	150	-	µs

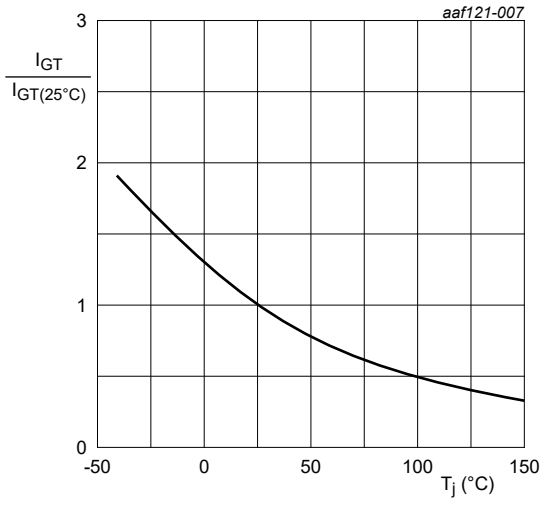


Fig. 7. Normalized gate trigger current as a function of junction temperature

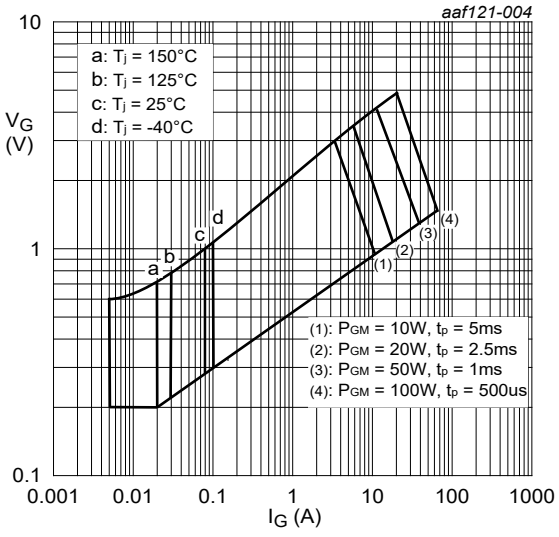


Fig. 8. Gate voltage as a function of gate current

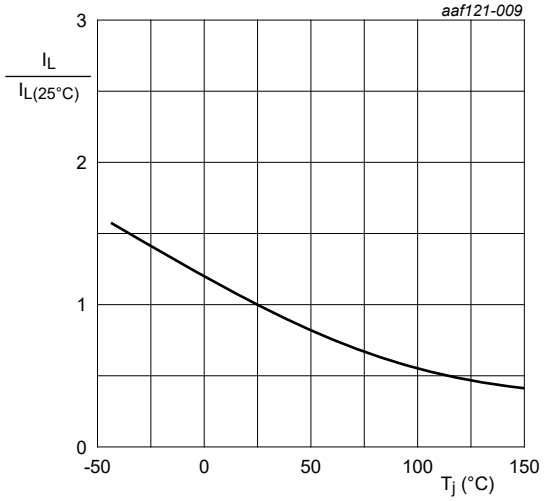


Fig. 9. Normalized latching current as a function of junction temperature

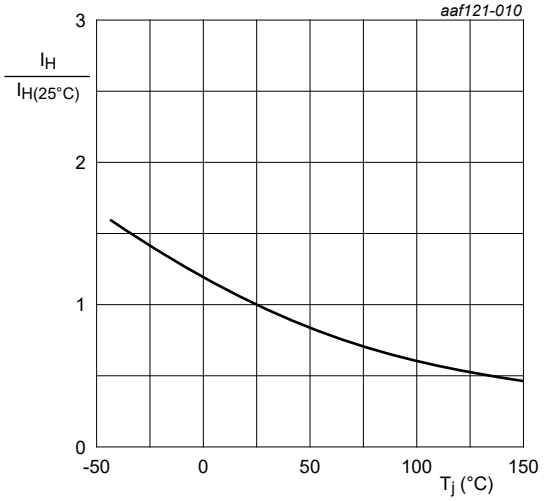
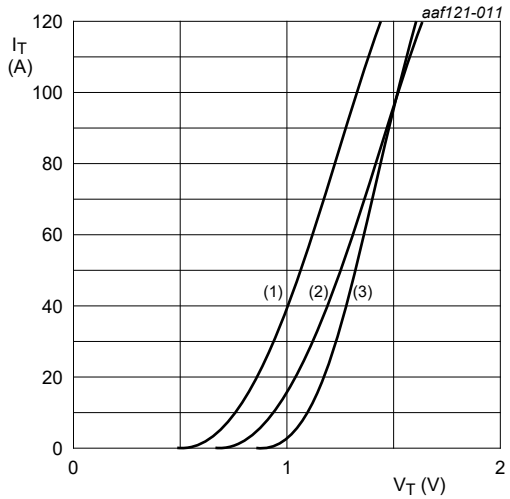


Fig. 10. Normalized holding current as a function of junction temperature



V_o = 1.003 V; R_s = 0.0051 Ω
(1) T_j = 150 °C; typical values
(2) T_j = 150 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 11. On-state current as a function of on-state voltage

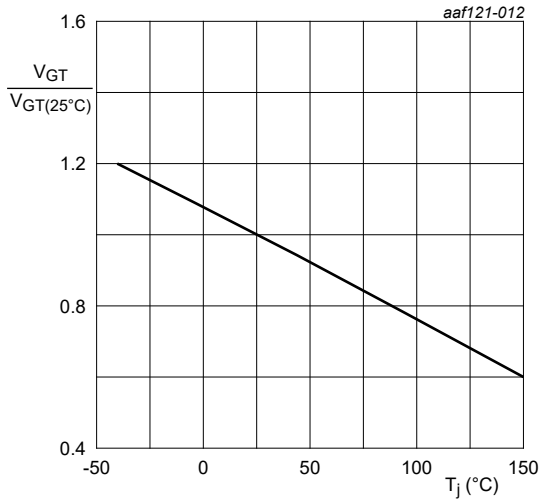
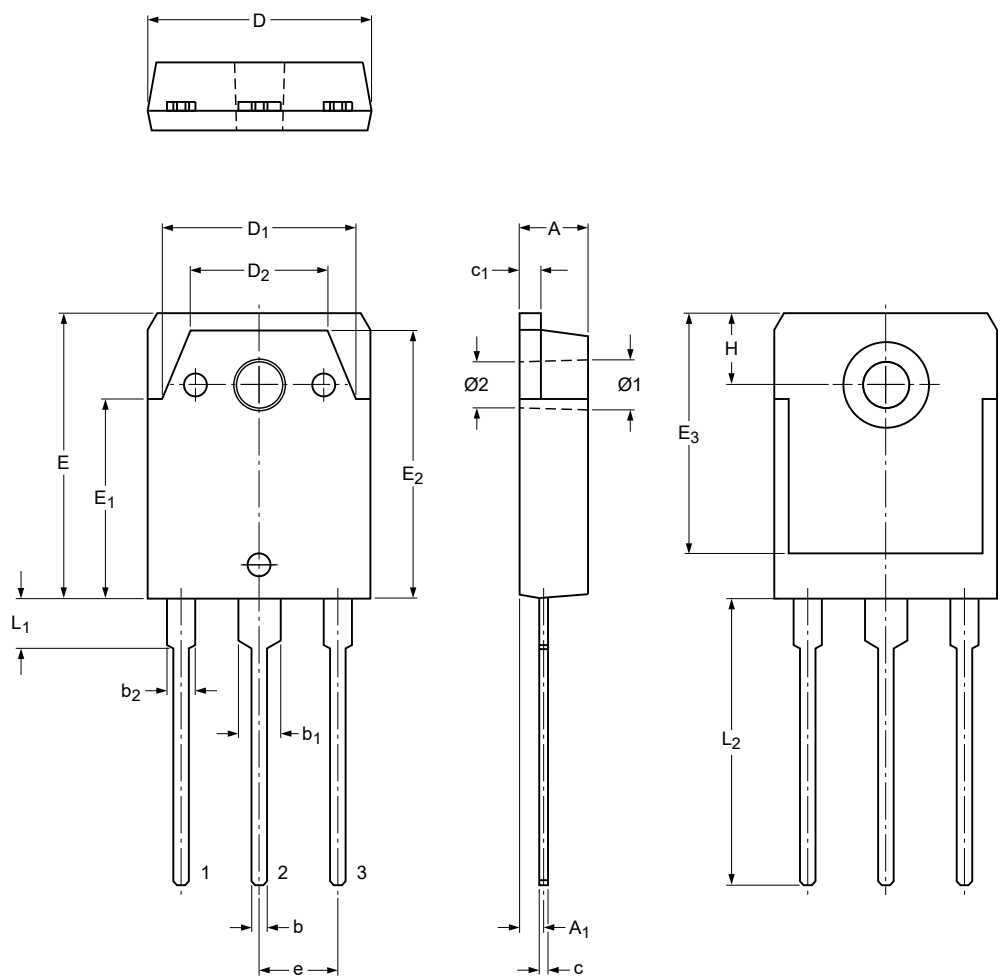


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO3P **SOT1259**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_1	b_2	c	c_1	D	D_1	D_2	e	E	E_1	E_2	E_3	H	L_1	L_2	Ø1	Ø2
mm	max	5.0	1.6	1.2	3.2	2.2	0.75	1.65	15.8	13.8	9.8		20.1	14.1	18.9	17.06	5.2	3.7	20.3	3.5	3.3
	nom											5.45									
	min	4.6	1.2	0.8	2.8	1.8	0.55	1.45	15.4	13.4	9.4	(typ)	19.7	13.7	18.5	16.46	4.8	3.3	19.7	3.3	3.1

sot1259_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1259		TO3P				~~14-10-21~~ 14-10-22

Fig. 13. Package outline TO3P (SOT1259)

11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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