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DATA SHEET

TZA1038HW

High speed advanced analog DVD signal processor and laser supply

Product specification

2003 Sep 03

Philips
Semiconductors

PHILIPS

CONTENTS

High speed advanced analog DVD signal processor and laser supply

TZA1038HW

1 FEATURES

- Operates with DVD-ROM, DVD+RW, DVD-RW, CD-ROM and CD-RW
- Operates up to 64 × CD-ROM and 12 × DVD-ROM
- RF data amplifier with wide, fine pitch programmable noise filter and equalizer equivalent to 64 × CD or 12 × DVD
- Programmable RF gain for DVD-ROM, CD-RW and CD-ROM applications (approximately 50 dB range to cover a large range of disc-reflectivity and OPUs)
- Additional RF sum input
- Balanced RF data signal transfer
- Universal photodiode IC interface using internal conversion resistors and offset cancellation
- Input buffers and amplifiers with low-pass filtering
- Three different tracking servo strategies:
  - Conventional three-beam tracking for CD
  - Differential Phase Detection (DPD) for DVD-ROM, including option to emulate traditional drop-out detection: Drop-Out Concealment (DOC)
  - Advanced push-pull with dynamic offset compensation.
- Enhanced signal conditioning in DPD circuit for optimal tracking performance under noisy conditions
- Radial error signal for Fast Track Counting (FTC)
- RF only mode: servo outputs can be set to 3-state, while RF data path remains active
- Radial servo polarity switch
- Flexible adaption to different light pen configurations
- Two fully automatic laser controls for red and infrared lasers, including stabilization and an on/off switch
- Automatic selection of monitor diode polarity
- Digital interface with 3 and 5 V compatibility.

2 GENERAL DESCRIPTION

The TZA1038HW is an analog preprocessor and laser supply circuit for DVD and CD read-only players. The device contains data amplifiers, several options for radial tracking and focus control. The preamplifier forms a versatile, programmable interface between single light path voltage output CD or DVD mechanisms to Philips digital signal processor family for CD and DVD (for example, Gecko, HDR65 or Iguana). A separate high-speed RFSUM input is available.

The device contains several options for radial tracking:

- Conventional three-beam tracking for CD
- Differential phase detector for DVD
- Push-pull with flexible left and right weighting to compensate dynamic offsets e.g. beam landing offset
- A radial error signal to allow Fast Track Count (FTC) during track jumps.

The dynamic range of this preamplifier and processor combination can be optimized for LF servo and RF data paths. The gain in both channels can be programmed separately and so guarantees optimal playability for all disc types.

The RF path is fully DC coupled. The DC content compensation techniques provide fast settling after disc errors.

The device can accommodate astigmatic, single foucault and double foucault detectors and can be used with P-type lasers with N-sub or P-sub monitor diodes. After an initial adjustment, the circuit will maintain control over the laser diode current. With an on-chip reference voltage generator, a constant stabilized output power is ensured and is independent of ageing.

An internal Power-on reset circuit ensures a safe start-up condition.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA1038HW	HTQFP48	plastic thermal enhanced thin quad flat package; 48 leads; body $7 \times 7 \times 1$ mm; exposed die pad	SOT545-2

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{amb}	ambient temperature		−40	–	+85	°C
Supplies						
V_{DDA1}, V_{DDA2}, V_{DDA3}, V_{DDA4}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD3}	3 V digital supply voltage		2.7	3.3	5.5	V
V_{DDD5}	5 V digital supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current	without laser supply	–	98	120	mA
		STANDBY mode	–	–	1	mA
$V_{I(logic)}$	logic input compatibility	note 1	2.7	3.3	5.5	V
Servo signal processing						
$B_{LF(-3dB)}$	−3 dB bandwidth of LF path		60	75	100	kHz
$I_{O(LF)}$	output current	focus servo output	0	–	12	μA
		radial servo output	0	–	12	μA
$V_{O(FTC)(p-p)}$	FTC output voltage (peak-to-peak value)		2.0	–	–	V
B_{FTC}	FTC bandwidth	FTCHBW = 0	–	600	–	kHz
		FTCHBW = 1; note 2	–	1200	–	kHz
$V_{I(FTCREF)}$	FTC reference input voltage		1.25	–	2.75	V
RF data processing						
A_{RF}	linear current gain	programmable gain				
		RF channels	6	–	49	dB
		RFSUM channels	−6	–	+31	dB
$B_{RF(-3dB)}$	−3 dB bandwidth of RFP and RFN signal path	RFEQEN = 0; RFNFEN = 0	200	300	–	MHz
$f_{0(RF)}$	noise filter and equalizer corner frequency	BWRF = 0	8	12.0	14.5	MHz
		BWRF = 127	100	145	182	MHz
$t_{d(RF)}$	flatness delay in RF data path	equalizer on; flat from 0 to 100 MHz; BWRF = 127	–	–	0.5	ns
Z_i	input impedance of pins A to D		100	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(RF)(FS)}$	input voltage on pins A to D for full-scale at output	at the appropriate signal path gain setting				
		RF signal path	–	–	600	mV
		LF signal path	–	–	700	mV
$V_{i(SUM)(dif)}$	differential input voltage on pins RFSUMP and RFSUMN	G_{RFSUM} = −6 dB	–	–	1800	mV
$V_{I(DC)}$	DC input voltage range on pins RFSUMP and RFSUMN	with respect to V_{SS}	1.3	–	V_{DDA} – 1.0	V
$V_{o(RF)(dif)(p-p)}$	differential output voltage on pins RFP and RFN (peak-to-peak value)		–	–	1.4	V
$V_{O(RF)(DC)}$	DC output voltage on pins RFP and RFN		0.35	–	V_{DDA} – 1.9	V
$V_{i(RFREF)(CM)}$	input reference voltage on pin RFREF for common mode output		0.8	1.2	2.1	V
Laser supply						
$I_{o(laser)(max)}$	maximum current output to laser		−120	–	–	mA
$V_{i(mon)}$	input voltage from laser monitor diode	P-type monitor diode				
		LOW level voltage	–	V_{DDA4} – 0.155	–	V
		HIGH level voltage	–	V_{DDA4} – 0.190	–	V
		N-type monitor diode				
		LOW level voltage	–	0.155	–	V
		HIGH level voltage	–	0.185	–	V

Notes

1. Input logic voltage level follows the supply voltage applied at pin V_{DDD3}.
2. High FTC bandwidth is achieved when I_{S1} and I_{S2} > 1.5 μA.

5 BLOCK DIAGRAM

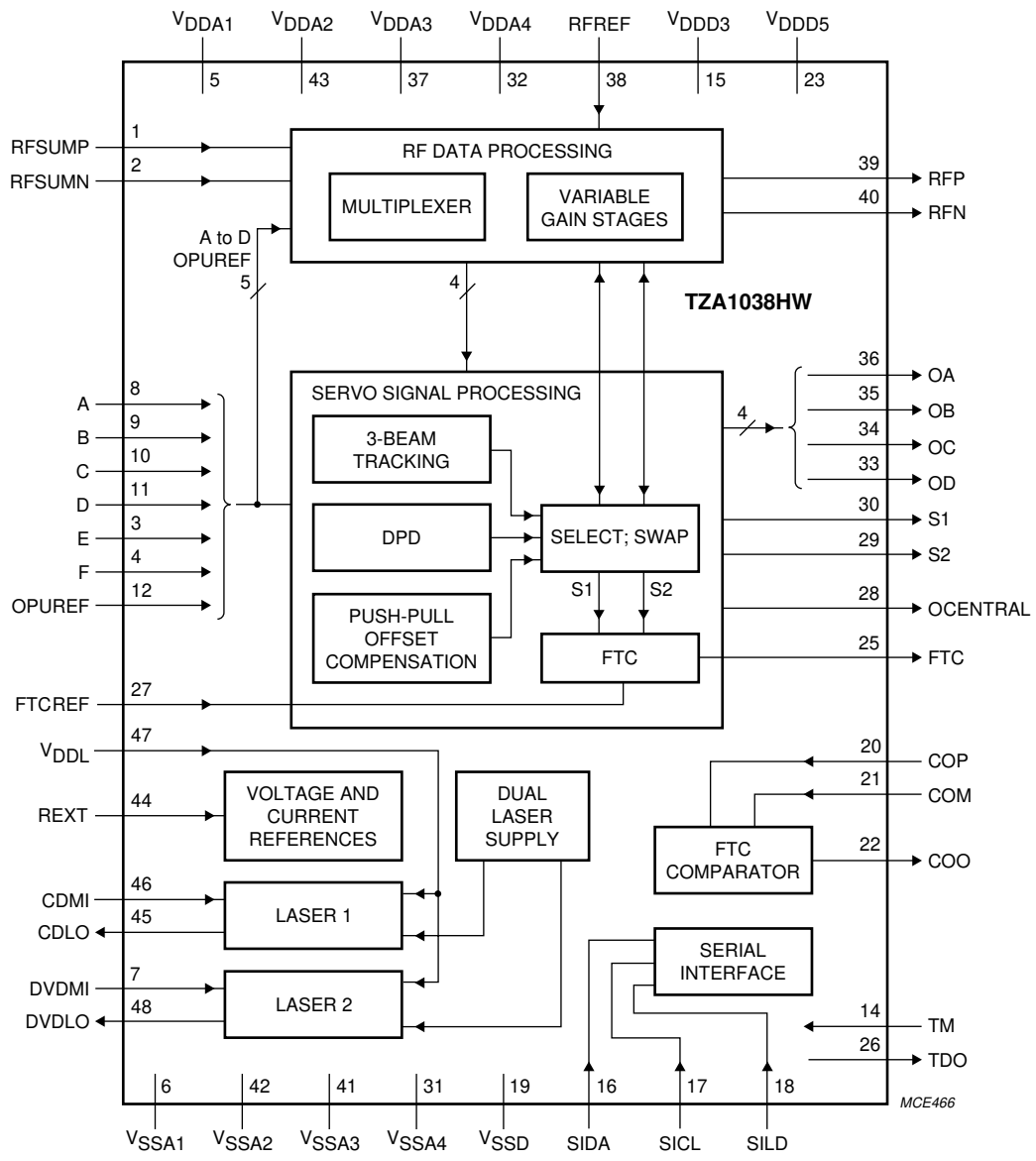


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
RFSUMP	1	positive RF sum input
RFSUMN	2	negative RF sum input
E	3	input E
F	4	input F
V_{DDA1}	5	analog supply voltage 1 (RF input stage)
V_{SSA1}	6	analog ground 1
DVDMI	7	input signal from DVD laser monitor diode
A	8	input A
B	9	input B
C	10	input C
D	11	input D
OPUREF	12	reference input from Optical Pick-Up (OPU)
n.c.	13	not connected
TM	14	test mode input (factory test only)
V_{DDD3}	15	digital supply voltage (serial interface 3 V I/O pads and FTC comparator)
SIDA	16	serial host interface data input
SICL	17	serial host interface clock input
SILD	18	serial host interface load
V_{SSD}	19	digital ground
COP	20	positive FTC comparator input
COM	21	inverting FTC comparator input
COO	22	FTC comparator output
V_{DDD5}	23	digital supply voltage (5 V digital core)
n.c.	24	not connected
FTC	25	fast track count output
TDO	26	test data output (factory test only)
FTCREF	27	FTC reference input
OCENTRAL	28	test pin for offset cancellation
S2	29	servo current output 2 for radial tracking
S1	30	servo current output 1 for radial tracking
V_{SSA4}	31	analog ground 4
V_{DDA4}	32	analog supply voltage 4 (servo signal processing)
OD	33	servo current output for focus D
OC	34	servo current output for focus C
OB	35	servo current output for focus B
OA	36	servo current output for focus A
V_{DDA3}	37	analog supply voltage 3 (RF output stage)
RFREF	38	DC reference input for RF channel common mode output voltage
RFP	39	positive RF output
RFN	40	negative RF output

SYMBOL	PIN	DESCRIPTION
V_{SSA3}	41	analog ground 3
V_{SSA2}	42	analog ground 2
V_{DDA2}	43	analog supply voltage 2 (internal RF data processing)
REXT	44	reference current input (connect via 12.1 kΩ to V_{SSA4})
CDLO	45	CD laser output
CDMI	46	input signal from CD laser monitor diode
V_{DDL}	47	laser supply voltage
DVDLO	48	DVD laser output

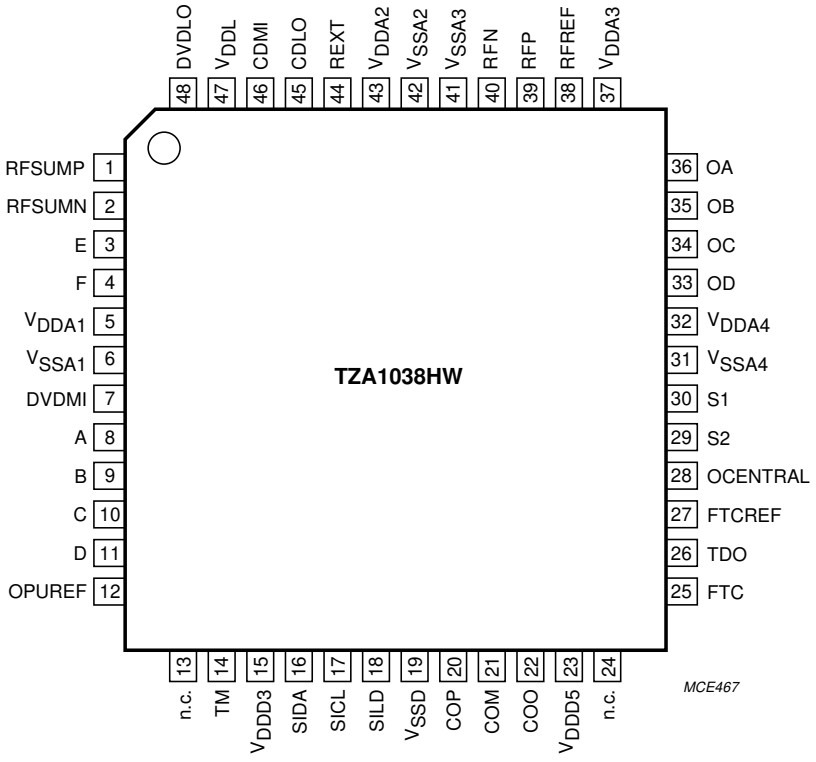


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 RF data processing

The RF data path is a fully DC-coupled, multi-stage amplifier (see Fig.3). The input signal for data can be selected from RF inputs A to D or from the summed RF inputs RFSUMP and RFSUMN. Switching between the two sets of signals is performed by an internal multiplexer. The signals are fully balanced internally to improve signal quality and reduce power supply interference.

RF outputs RFP and RFN can be DC coupled to the Analog-to-Digital Converter (ADC) of the decoder.

The RF input signals are from photodiodes and have a large DC content by nature. This DC component must be removed from the signals for good system performance. Built-in DACs, located after the input stages G_1 and RFSUM, have the ability to do this. The DAC range and resolution is scaled with the gain setting of the first amplifier stage. When the DC content is removed, the RF signal can be DC coupled to the decoder. The main advantage of DC coupling is fast recovery from signal swings due to disc defects since there is no AC coupling capacitance to slow the recovery. When using DC coupling, both AC and DC content in the data signal is known. The Philips Iguana decoders have on-chip control loops to support Automatic Gain Control (AGC) and DC cancellation.

Two separate DACs are available for cases where the left and right side DC conditions can be different.

When it is not possible to have a DC connection between the TZA1038HW and the decoder, the signals on servo outputs OA to OD can be used as they contain the same LP-filtered and DC coupled information.

Summing of the photodiode signals A to D is performed in the second amplifier stage G_2. Each individual diode channel can be switched on, off or inverted with switches SW-A to SW-D.

Switching between photodiode signals and RFSUM input is performed immediately before the third amplifier stage G_3. This stage has a variable gain with fine resolution to allow automatic gain adjustment to be controlled by the decoder.

The filter stage limits the bandwidth according to the maximum playback speed of the disc. This is to optimize the noise performance. The filter stage consists of an equalizer and a noise filter, both of which can be bypassed, also the boost factor of the equalizer can be set. The corner frequencies of the equalizer and noise filter are equal and can be programmed to a 7-bit resolution.

The RF output signals RFP and RFN can be DC coupled to a decoder with a differential input pair (as with Philips Iguana decoders). The common mode output voltage can be set externally at pin RFREF.

The signals for differential phase detection are tapped from the inputs A to D at the RF amplifier G_1 stages. DC cancellation for the A to D and RFSUM signal paths can be set independently or simultaneously.

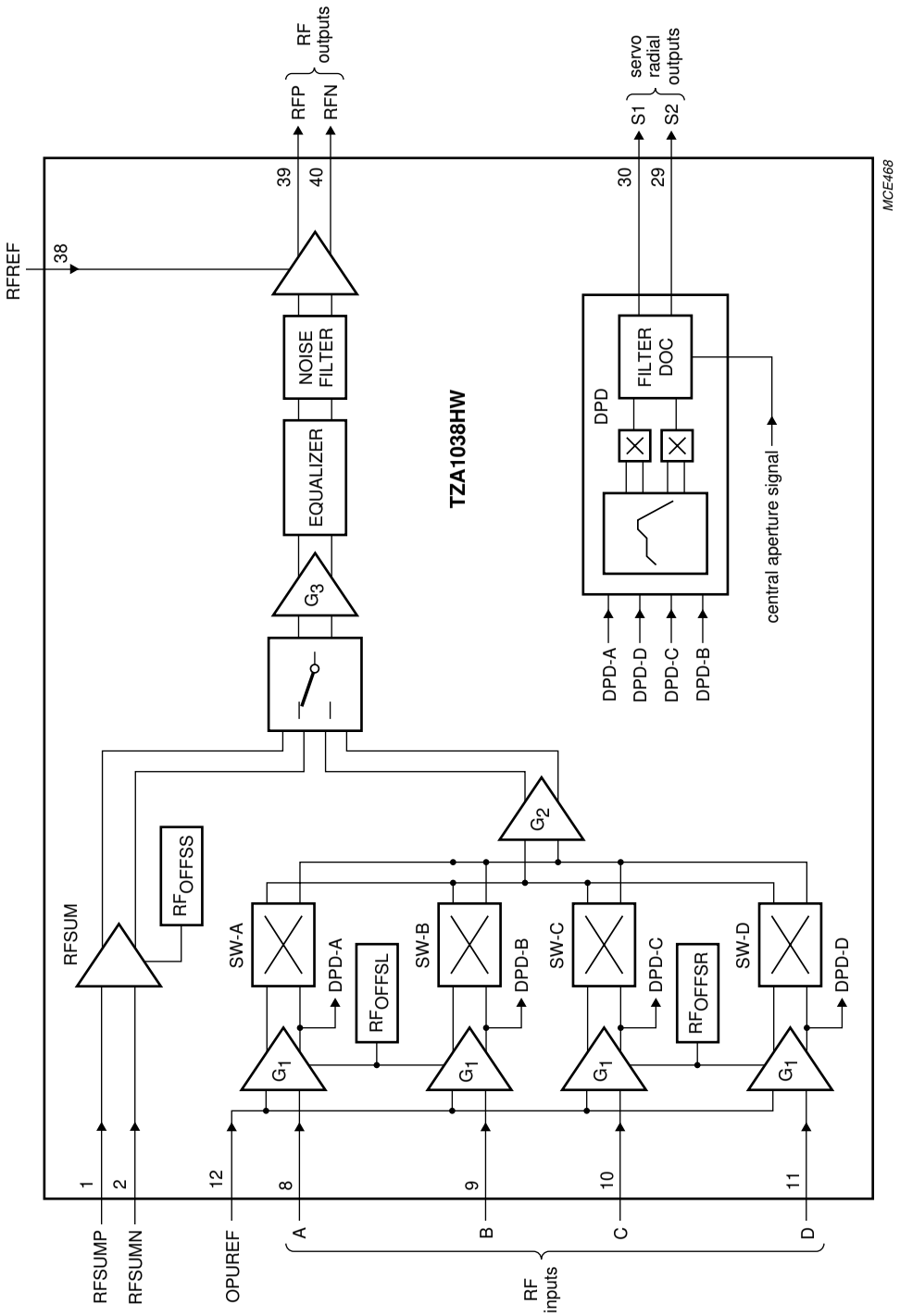


Fig.3 RF data and DPD processing.

7.2 Servo signal processing

The photodiode configurations and naming conventions are shown in Figs 4 and 5.

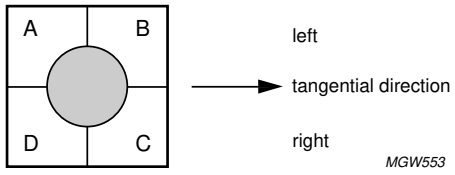
7.2.1 SERVO SIGNAL PATH SET-UP

A block diagram of the servo signal path is shown in Fig.6. In general, the servo signal path comprises:

- A voltage-to-current converter with programmable offset voltage source V_{LFOFFS} that is common to all inputs
- A 4-bit DAC for each of the six channels to compensate for offset per channel
- A variable gain stage to adapt the signal level to the specific pick-up and disc properties
- Low-pass filtering and output stage for the photodiode current signals
- Error output stage in the radial data path for fast track counting.

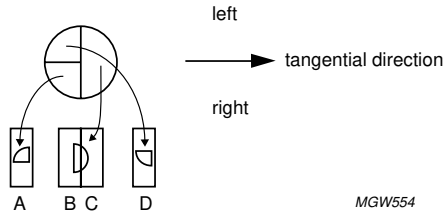
Servo output signals OA to OD, S1 and S2 are unipolar current signals which represent the low-pass filtered photodiode signals. In DPD radial tracking, the S1 and S2 signals are the equivalent of the satellite signals commonly found in traditional CD systems.

The servo output signals OA to OD, S1 and S2 are set to 3-state if bit RFonly = 1 (register 13, bit 11).



Data = A + B + C + D
Push-pull = (A + B) – (C + D)
Focus = (A + C) – (B + D)
DPD2 = phase (A + B, C + D)
DPD4 = phase (A,D) + phase (C,B)

Fig.4 Astigmatic diode configuration.



Data = A + B + C + D
Push-pull = A – D
Focus = C – B
DPD2 = phase (A, D)
DPD4 not applicable

Fig.5 Foucault diode configuration.

7.2.2 FOCUS SERVO

Focus information is reflected in the four outputs OA to OD. Gain and offset can be programmed.

For optical pick-ups where only channels B and C are used for focus, channels A and D can be switched off (bit Focus_mode = 0).

For initial alignment, a copy of the output currents can be made available on pin OCENTRAL.

7.2.3 RADIAL SERVO

Radial information can be obtained from the two output signals S1 and S2, and the gain and offset can be programmed. The TZA1038HW provides differential phase detection, push-pull and three-beam push-pull for radial tracking. The signal FTC is made available for fast track counting and is primarily the voltage error signal derived from signals S1 or S2.

The polarity of the radial loop can be reversed via the serial control bus (RAD_pol).

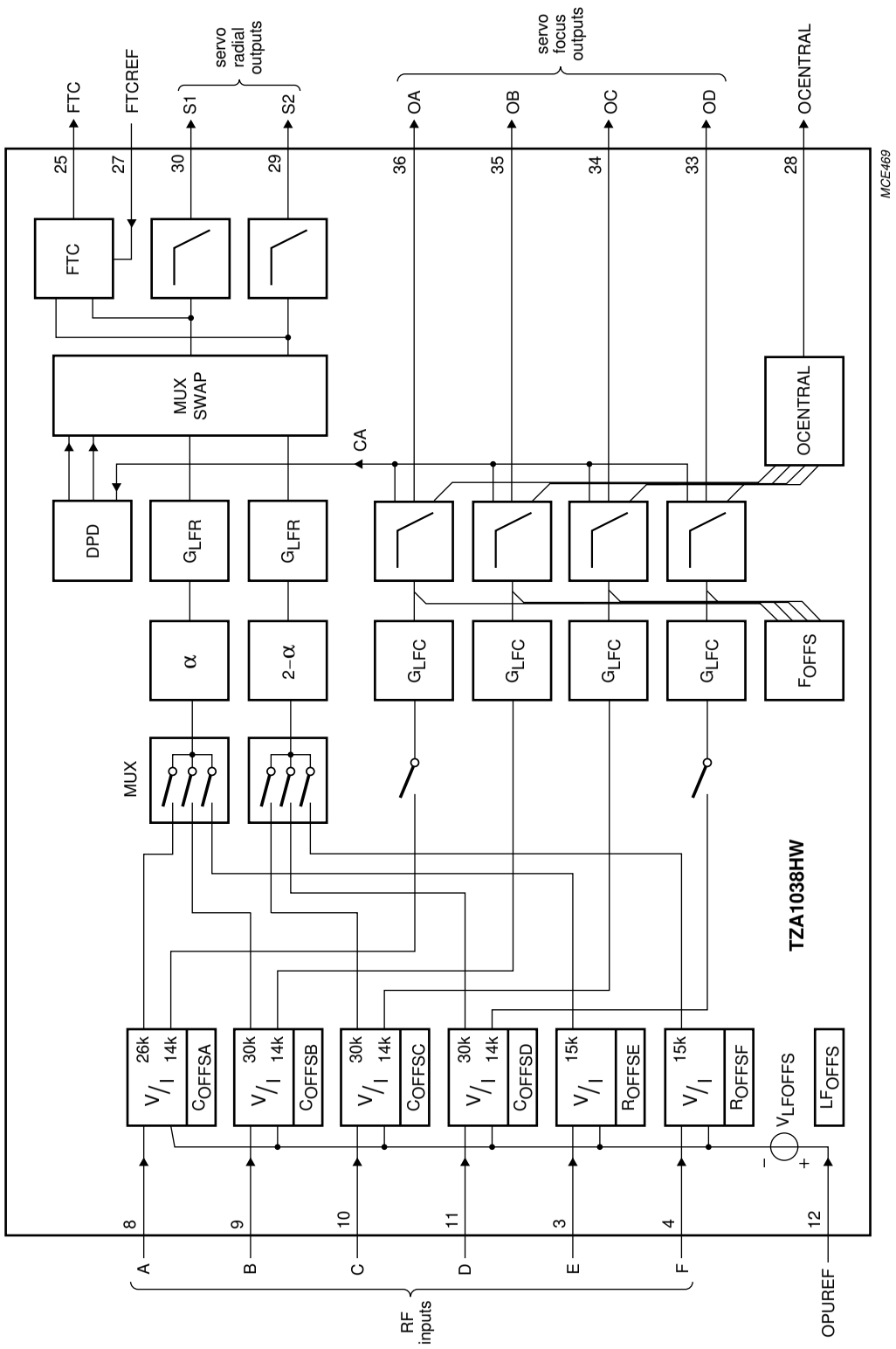


Fig.6 Servo signal path.

7.2.4 DIFFERENTIAL PHASE DETECTION

The TZA1038HW provides differential phase detection to support DVD in various ways:

- DPD2 with four channels programmed to be active gives DPD as required in the standard specification
- Two of the four channels can be excluded from the DPD for pick-ups with an alternative photodiode arrangement
- An increase in performance, dedicated for DVD+RW, can be obtained by using the DPD4 method. Then two truly separated phase detectors are active. After the phase detection of the two input pairs the result is summed.

Input signals for DPD are taken from input pins A to D after the first gain stage G_1 (see Fig.3). Pre-emphasis is applied by means of a programmable lead/lag filter. Additionally, a programmable low-pass filter is available to improve the signal quality under noisy signal conditions at lower speeds. For further signal improvements the DPD pulse stretcher can be programmed to higher values at lower speeds.

The DPD signal is low-pass filtered by two internal capacitors. The signal is then fed to pins S1 and S2, or directed via the drop-out concealment circuit to the outputs (see Section 7.5).

7.2.4.1 Drop-out concealment

A special function is built in for compatibility with drop-out detection strategies, based on level detection in the S1 and S2 signals. When using DPD in a fundamental way, there is no representation of mirror level information from the light pen.

When the drop-out concealment function is enabled (bit DOCEN = 1), a portion of the Central Aperture (CA) signal is added to S1 and S2. Also, when the CA signal drops below the DOC threshold, the DPD signal is gradually attenuated.

The DPD detection cannot work properly when the input signal becomes very small. The output of the DPD may then show a significant offset. The DOC may not conceal this offset completely because:

- DOC is gradually controlled from the CA signal
- The CA signal may not become 0 during disc-defect.

For details see Section 7.5.5.2

7.2.4.2 Push-pull and three-beam push-pull

The TZA1038HW can also provide radial information by means of push-pull signals (from the photodiode inputs) or in a three-spot optical system with Three-Beam Push-Pull (TBPP). The built-in multiplexer gives a flexible method of dealing with many detector arrangements. For push-pull, the input signals are taken from channels A to D. There is also a command that switches off channels B and C, leaving channels A and D for push-pull (bits RT_mode[2:0]).

For TBPP, the input signal is taken from channels E and F, irrespective of bit RFSUM setting.

7.2.4.3 Enhanced push-pull (dynamic offset compensation for beam landing)

This option cancels offsets due to beam landing. A factor α can be programmed to re-balance the signal gain between channels S1 and S2. In a simplified form this can be described as:

$S1 = A_{LFR} \times \alpha \times$ input left

$S2 = A_{LFR} \times (2 - \alpha) \times$ input right.

Factor α can be programmed in a range from 0.6 to 1.35, with 1.0 as the balanced condition (bits α[3:0]).

7.2.4.4 Offset compensation

A provision is made to compensate electrical offset from a light pen. The offset voltage from the light pen can be positive or negative. In general, the offset between any two channels is smaller than the absolute offsets. As negative input signals cannot be handled by the TZA1038HW internal servo channels, a two-step approach is adopted:

- A coarse DAC, common to all the input channels, adds an offset that shifts the input signals in positive direction until all inputs are ≥0. The DAC used (LF_{OFFS}) has a 2-bit resolution (bits LF_{OFF}[1:0]).
- A fine setting per channel is provided to cancel the remainder of the offset between the channels. This is achieved by DACs subtracting the DC component from the signals and bringing the inputs to approximately zero offset (within ≈ 1 mV). The DACs (registers 11 to 13) have a 4-bit resolution.

The range of both DACs can be increased by a factor of three to compensate for higher offset values by means of control parameter bit SERVOOS.

With a switched-off laser, the result of the offset cancellation can be observed at each corresponding output pin, OA to OD, S1 and S2, or via a built-in multiplexer to pin OCENTRAL (central channels only). See registers 11 to 13 for DAC and multiplexer control.

7.2.5 Automatic dual laser supply

The TZA1038HW can control the output power of two lasers; it has an Automatic Laser Power Control (ALPC) that stabilizes the laser output power and compensates the effects of temperature and ageing of the laser.

ALPC automatically detects if there is a P-type or N-type monitor diode in use in either of the laser circuits. The regulation loop formed by the ALPC, the laser, the monitor diode and the associated adjustment resistor will settle at the monitor input voltage. The monitor input voltage can be programmed to HIGH (≈ 180 mV) or LOW (≈ 150 mV), according to frequently-used pre-adjustments of the light pen. This set point can be set independently for both ALPCs. Bandwidth limitation and smooth switch-on behaviour is realized using an internal capacitor.

A protection circuit is included to prevent laser damage due to dips in laser supply voltage V_{DDL}. If a supply voltage dip occurs, the output can saturate and restrict the required laser current. Without the protection circuit, the ALPC would try to maximize the output power with destructive results for the laser when the supply voltage recovers. The protection circuit monitors the supply voltage and shuts off the laser when the voltage drops below a safe value. The ALPC recovers automatically after the dip has passed.

Only one laser can be activated at the same time. An internal break-before-make circuit ensures safe start-up for the laser when a toggle situation between the two lasers is detected. When both lasers are programmed on, neither laser will be activated.

7.2.6 Power-on reset and general power on

When the supply voltage is switched on, bit PWRON is reset by the Power-On Reset (POR) signal. This concludes in a STANDBY mode at power up. POR is intended to prevent the lasers being damaged due to random settings. All other functions may be switched when power is on. The TZA1038HW becomes active when bit PWRON = 1.

7.2.7 Compatibility with TZA1033HL/V1

7.2.7.1 Software compatibility

The TZA1038HW is highly software compatible with the TZA1033HL/V1. Provided that some conditions are met, the software of the TZA1038HW can be used as a successor with just minor modifications. This compatibility is achieved with the implementation of the TZA1038HW mode control bit (bit K2_Mode). When bit K2_Mode = 0, the TZA1038HW will act as a TZA1033HL/V1. When bit K2_Mode = 1, the TZA1038HW will act as a TZA1033HL/K2 and the new functions will be available (but require a software update).

Other conditions or restrictions are:

- Register bits of the TZA1038HW which were not defined are programmed to a logic 0. Registers 9, 10, 14 and 15 may be left undefined
- The G_4 stage high gain setting of the TZA1033HL/V1 is not available in the TZA1038HW; if this value was set to logic 0, there will be no difference
- When bit K2_Mode = 0 the RF bandwidth will be fixed to the minimum value of 10 MHz (typical); bit K2_Mode = 1 to select a higher bandwidth; the bandwidth is now lower than using a TZA1033HL/V1.

7.2.7.2 Hardware compatibility

The package is changed from LQFP64 for the TZA1033HL to LQFP48 for the TZA1038HW.

The hardware differences are:

- Input pins STB, HEADER and LAND of the TZA1033HL are not present
- Input pins CD of TZA1033HL/V1 are not used; TZA1038HW has RFSUM inputs instead; the RFSUM inputs of TZA1038HW may be connected to ground when not used.

7.2.8 INTERFACE TO THE SYSTEM CONTROLLER

Programming the registers of TZA1038HW is done via a serial bus (see Fig.7). The circuitry is formed by a serial input shift register and a number of registers that store the data. The registers can always be programmed, irrespective of STANDBY mode.

If required, the bus lines can be connected in parallel with an I^2C-bus. The protocol needs no switching of the data line during SICL = HIGH. This means that other I^2C-bus devices will not recognise any START or STOP commands. Control words addressed to TZA1038HW should go uniquely with the SILD signal. When SILD = HIGH, the TZA1038HW will not respond to any signal on SIDA or SICL.

During a transmission, the serial data is first stored in an input shift register. At the rising edge of SILD, the content of the input register is copied into the addressed register. This is also the moment the programmed information becomes effective.

The input pins have CMOS compatible threshold levels for both 3.3 and 5 V supplies.

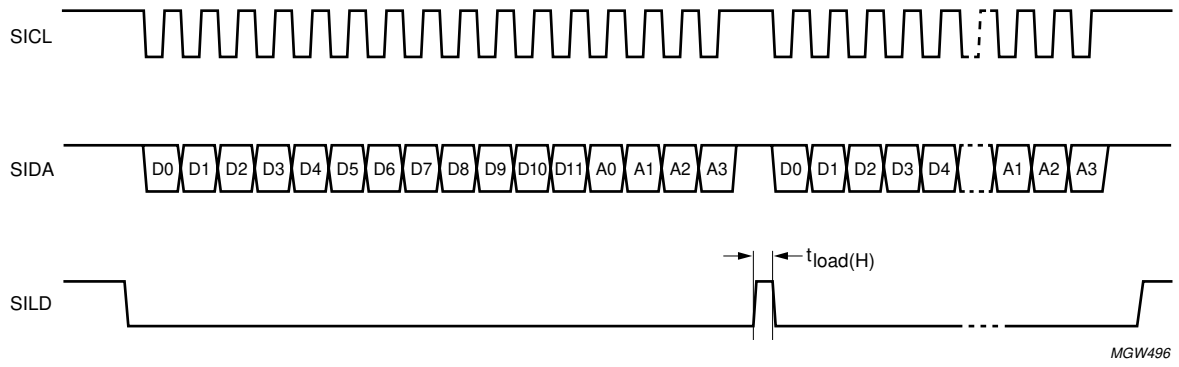


Fig.7 Two word transmission.

7.3 Control registers

The TZA1038HW is controlled by serial registers. To keep programming fast and efficient, the control bits are sent in 16-bit words. Four bits of the word are used for the address and for each address there are 12 data bits.

Table 1 Overview of control parameters

SYMBOL	PARAMETER	VALUES	REGISTER	BITS
Data path				
G_1 (A_1)	gain of first RF amplifier stage (or linear amplification)	0, 6 and 12 dB (1×, 2× and 4×)	3	11 and 10
G_2 (A_2)	gain of second RF amplifier stage (or linear amplification)	6, 12, 18 and 24 dB (2×, 4×, 8× and 16×)	3	9 and 8
G_3 (A_3)	gain of third RF amplifier stage (or linear amplification)	0 to 13 dB in steps of 0.8 dB (1× to 4×)	3	7 to 4
GRFSUM (A_{RFSUM})	gain of RFSUM input stage (or linear amplification)	−6, 0, 6, 12 and 18 dB (0.5×, 1×, 2×, 4× and 8×)	0	7 to 5
BWRF	bandwidth limitation in RF path	$f_{0(RF)}$ = 12 to 145 MHz	14	6 to 0

SYMBOL	PARAMETER	VALUES	REGISTER	BITS
RF_{OFFSL}	DC offset compensation in left RF input path	RFSUM = 0; full range depends on G_1 setting: G_1 = 0 dB: 0 to 450 mV in 7.1 mV steps G_1 = 6 dB: 0 to 225 mV in 3.6 mV steps G_1 = 12 dB: 0 to 120 mV in 1.9 mV steps	4	11 to 6
RF_{OFFSR}	DC offset compensation in right RF input path	RFSUM = 0; full range depends on G_1 setting: G_1 = 0 dB: 0 to 450 mV in 7.1 mV steps G_1 = 6 dB: 0 to 225 mV in 3.6 mV steps G_1 = 12 dB: 0 to 120 mV in 1.9 mV steps	4	5 to 0
RF_{OFFSS}	DC offset compensation in RFSUM path	RFSUM = 1; full range depends on GRFSUM setting: GRFSUM = −6 dB; 0 to 1700 mV GRFSUM = 0 dB; 0 to 850 mV GRFSUM = 6 dB; 0 to 425 mV GRFSUM = 12 dB; 0 to 210 mV GRFSUM = 18 dB; 0 to 105 mV	4 or 5	5 to 0
Servo radial path				
LF_{OFFS}	DC offset compensation for LF path (common for all servo inputs)	SERVOOS = 0: V_{LFOFFS} = 0, 5, 10 or 15 mV	11	11 and 10
		SERVOOS = 1: V_{LFOFFS} = 0, 15, 30 or 45 mV		
R_{LFR}	CD satellite path input transresistance	15 kΩ fixed	–	–
R_{LFPP}	DVD push-pull signal transresistance	30 kΩ fixed	–	–
R_{OFFSE}	DC offset compensation for radial servo path (input E)	SERVOOS = 0: V_{ROFFSE} = 0 to 20 mV SERVOOS = 1: V_{ROFFSE} = 0 to 60 mV	11	7 to 4
R_{OFFSF}	DC offset compensation for radial servo path (input F)	SERVOOS = 0: V_{ROFFSF} = 0 to 20 mV SERVOOS = 1: V_{ROFFSF} = 0 to 60 mV	11	3 to 0
α	dynamic radial offset compensation factor	α = 0.6 to 1.35 in 15 steps of 0.05	6	3 to 0
$I_{(FS)(DPD)}$, $I_{(FS)(DPD)(DOC)}$	full scale DPD current, fixed value based on bandgap voltage across external resistor	DOCEN = 0: fixed value = 20 μA DOCEN = 1: fixed value = 6.6 μA	1	5
$I_{REFRAD(CM)}$	internally generated common mode DC reference current in DPD mode	3.5 μA fixed	–	–
f_{start_DPD}	start frequency lead/lag filter of DPD block	f_{start_DPD} = 1, 5 or 10 MHz (TZA1033HL/V1 compatible)	7	1 and 0
		f_{start_DPD} = 1, 5, 10, 18 or 24 MHz	15	5 to 3

SYMBOL	PARAMETER	VALUES	REGISTER	BITS
G_{LFR} (A_{LFR})	low frequency gain, radial path output stage (or linear amplification)	−15 to +9 dB in steps of 3 dB (0.18× to 2.8×)	6	11 to 8
R_{FTC}	gain of fast track count output	680 kΩ ±20% fixed for ±2 V (p-p)	–	–
Servo focus path				
R_{LFC}	LF path input transresistance	14 kΩ fixed	–	–
C_{OFFSA}	DC offset compensation for central servo path A	SERVOOS = 0: 0 to 20 mV SERVOOS = 1: 0 to 60 mV	12	7 to 4
C_{OFFSB}	DC offset compensation for central servo path B	SERVOOS = 0: 0 to 20 mV SERVOOS = 1: 0 to 60 mV	12	3 to 0
C_{OFFSC}	DC offset compensation for central servo path C	SERVOOS = 0: 0 to 20 mV SERVOOS = 1: 0 to 60 mV	13	7 to 4
C_{OFFSD}	DC offset compensation for central servo path D	SERVOOS = 0: 0 to 20 mV SERVOOS = 1: 0 to 60 mV	13	3 to 0
G_{LFC} (A_{LFC})	low frequency gain, central path output stage (or linear amplification)	−15 to +9 dB in steps of 3 dB (0.18× to 2.8×)	6	7 to 4
β	focus offset compensation	β = 0 to $^{31}/_{32}$	2	4 to 0
F_{OFFSEN}	full range offset compensation for focus	DAC enabled: I_{FOFFS} = 400 nA (fixed) DAC disabled: I_{FOFFS} = 0 nA	2	10

7.3.1 REGISTER 0: POWER CONTROL

Table 2 Register address 0H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	–	–	–	–

BIT	7	6	5	4	3	2	1	0
SYMBOL	GRF SUM2	GRF SUM1	GRF SUM0	DVD_ MILVL	CD_MILVL	DVD_ LDON	CD_LDON	PWRON

Table 3 Description of register bits (address 0H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0000 = address 0H
11 to 8	–	not used
7 to 5	GRFSUM[2:0]	**Gain of RFSUM input stage.** 000 = −6 dB 001 = 0 dB 010 = 6 dB 011 = 12 dB 100 = 18 dB
4	DVD_MILVL	**DVD monitor input level.** 0 = 150 mV; 1 = 180 mV.

BIT	SYMBOL	FUNCTION
3	CD_MILVL	**CD monitor input level.** 0 = 150 mV; 1 = 180 mV.
2	DVD_LDON	**DVD laser on.** 0 = laser off; 1 = laser on.
1	CD_LDON	**CD laser on.** 0 = laser off; 1 = laser on.
0	PWRON	**Power on.** 0 = STANDBY mode; 1 = power on.

7.3.2 REGISTER 1: SERVO AND RF MODES

Table 4 Register address 1H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	DPD_DCC	–	–	RAD_pol

BIT	7	6	5	4	3	2	1	0
SYMBOL	–	–	DOCEN	Focus_ mode	RT_mode2	RT_mode1	RT_mode0	RFSUM

Table 5 Description of register bits (address 1H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0001 = address 1H
11	DPD_DCC	**RF offset DAC for DPD signal control.** 0 = DAC controlled by register 4, bits RF_{OFFSL}[5:0]; 1 = DAC controlled by register 5, bits RF_{OFFSS}[5:0].
10 and 9	–	not used
8	RAD_pol	**Radial polarity switch.** 0 = inverse; 1 = normal (default).
7 and 6	–	not used
5	DOCEN	**Drop-out concealment enable.** 0 = disable; 1 = enable.
4	Focus_mode	**Focus mode.** 0 = two-channel focus (channels B and C only); 1 = four-channel focus.
3 to 1	RT_mode[2:0]	**Radial tracking mode.** 000 = DPD2; DPD = phase (A,D) 001 = push-pull; channels A,D only 100 = DPD2; DPD = phase (A + C, B + D) 101 = push-pull; four channels 110 = DPD4; DPD = phase (A,D) + phase (C,B) X11 = TBPP channels E and F
0	RFSUM	**RF channel selection.** 0 = diode inputs selected; 1 = RFSUM input selected.

7.3.3 REGISTER 2: FOCUS OFFSET DAC

Table 6 Register address 2H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	K2_Mode	F_{OFFSEN}	β4	β3

BIT	7	6	5	4	3	2	1	0
SYMBOL	β2	β1	β0	–	–	–	–	–

Table 7 Description of register bits (address 2H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0010 = address 2H
11	K2_Mode	**K2 mode.** 0 = disable; 1 = enable.
10	F_{OFFSEN}	**Focus offset enable.** 0 = enable; 1 = disable.
9 to 5	β[4:0]	**Focus offset compensation.** 00000 to 11111: β = 0 to β = $^{31}/_{32}$.
4 to 0	–	not used

7.3.4 REGISTER 3: RF PATH GAIN

Table 8 Register address 3H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	$G_1$1	$G_1$0	$G_2$1	$G_2$0

BIT	7	6	5	4	3	2	1	0
SYMBOL	$G_3$3	$G_3$2	$G_3$1	$G_3$0	–	–	–	–

Table 9 Description of register bits (address 3H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0011 = address 3H
11 and 10	G_1[1:0]	**First RF amplifier stage gain.** 00 = 0 dB 01 = 6 dB 10 = 12 dB 11 = not used
9 and 8	G_2[1:0]	**Second RF amplifier stage gain.** 00 = 6 dB 01 = 12 dB 10 = 18 dB 11 = 24 dB
7 to 4	G_3[3:0]	**Third RF amplifier stage gain.** 0000 to 1111: 0 to 13 dB in 0.8 dB steps.
3 to 0	–	not used

7.3.5 Register 4: RF left and right, or sum offset compensation

Table 10 Register address 4H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	$RF_{OFFSL}5$	$RF_{OFFSL}4$	$RF_{OFFSL}3$	$RF_{OFFSL}2$

BIT	7	6	5	4	3	2	1	0
SYMBOL	$RF_{OFFSL}1$	$RF_{OFFSL}0$	$RF_{OFFSR}5$/ $RF_{OFFSS}5$	$RF_{OFFSR}4$/ $RF_{OFFSS}4$	$RF_{OFFSR}3$/ $RF_{OFFSS}3$	$RF_{OFFSR}2$/ $RF_{OFFSS}2$	$RF_{OFFSR}1$/ $RF_{OFFSS}1$	$RF_{OFFSR}0$/ $RF_{OFFSS}0$

Table 11 Description of register bits (address 4H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0100 = address 4H
11 to 6	RF_{OFFSL}[5:0]	**Left channel RF offset compensation definition.** bit RFSUM = 0: left RF channel offset compensation value bit RFSUM = 1: not used
5 to 0	RF_{OFFSR}[5:0]	**Right channel RF offset compensation definition.** bit RFSUM = 0: right RF channel offset compensation value (symbol is RF_{OFFSR}) bit RFSUM = 1 and bit DPD_DCC = 1: not used bit RFSUM = 1 and bit DPD_DCC = 0: the decoder controls DPD and RFSUM channels automatically, in parallel and with same values (symbol is RF_{OFFSS}).

7.3.6 Register 5: RF sum offset compensation

Table 12 Register address 5H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	–	–	–	–

BIT	7	6	5	4	3	2	1	0
SYMBOL	–	–	$RF_{OFFSS}5$	$RF_{OFFSS}4$	$RF_{OFFSS}3$	$RF_{OFFSS}2$	$RF_{OFFSS}1$	$RF_{OFFSS}0$

Table 13 Description of register bits (address 5H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0101 = address 5H
11 to 6	–	not used
5 to 0	RF_{OFFSS}[5:0]	**RF offset compensation definition.** bit RFSUM = 0: not used bit RFSUM = 1 and bit DPD_DCC = 0: not used bit RFSUM = 1 and bit DPD_DCC = 1: the decoder controls RFSUM channels; the DPD channels can be set independently from the microprocessor.

7.3.7 Register 6: servo gain and dynamic radial offset compensation factor

Table 14 Register address 6H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	$G_{LFR}3$	$G_{LFR}2$	$G_{LFR}1$	$G_{LFR}0$

BIT	7	6	5	4	3	2	1	0
SYMBOL	$G_{LFC}3$	$G_{LFC}2$	$G_{LFC}1$	$G_{LFC}0$	$\alpha 3$	$\alpha 2$	$\alpha 1$	$\alpha 0$

Table 15 Description of register bits (address 6H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	0110 = address 6H
11 to 8	G_{LFR}[3:0]	**Low frequency gain, radial path output stage.** 0000 to 1000: –15 to +9 dB in 3 dB steps.
7 to 4	G_{LFC}[3:0]	**Low frequency gain, central path output stage.** 0000 to 1000: –15 to +9 dB in 3 dB steps.
3 to 0	α[3:0]	**Dynamic radial offset compensation factor.** 0000 to 1111: 0.60 to 1.35 in 0.05 steps; 1000 = balanced value (default).

7.3.8 Register 7: servo path gain and bandwidth and RF path bandwidth and pre-emphasis

Definitions in register 7 are intended mainly for software compatibility with the TZA1033HL/V1. New features that require more bit-space to program are moved to registers 14 and 15. Only DPD stretch remains programmed in register 7. Some parameters are slightly modified.

Table 16 Register address 7H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	DPDLPF1	DPDLPF0	DPD_ stretch2	DPD_ stretch1

BIT	7	6	5	4	3	2	1	0
SYMBOL	DPD_ stretch0	DPD_ testmode	DVDALAS_ mode	$EQ_{RF}2$	$EQ_{RF}1$	$EQ_{RF}0$	$f_{start\_DPD}1$	$f_{start\_DPD}0$

Table 17 Description of register bits (address 7H)

BIT	SYMBOL	FUNCTION	
		K2_Mode = 0	K2_Mode = 1
15 to 12	AD[3:0]	0111 = address 7H	0111 = address 7H
11 and 10	DPDLPF[1:0]	**DPD low-pass filter.** 0X : B_{-3dB} = 50 MHz (equivalent to TZA1023) 1X : B_{-3dB} = 10 MHz	not applicable

BIT	SYMBOL	FUNCTION	
		K2_Mode = 0	K2_Mode = 1
9 to 7	DPD_stretch [2:0]	**DPD pulse stretcher (t_P).** 000 = 1.9 ns 001 = 3.8 ns (equivalent to TZA1023) 010 = 7.5 ns 011 = 15 ns 100 = 30 ns 101 = not used	**DPD pulse stretcher (t_P).** 000 = 30 ns 001 = 15 ns 010 = 7.5 ns 011 = 3.8 ns 100 = 1.9 ns 101 = 1.2 ns
6	DPD_ testmode	**For factory test purposes only.**	**For factory test purposes only.**
5	DVDALAS_ mode	**DVDALAS mode bit.** 0 = disables control of bits 11 to 6 and creates behaviour equivalent to TZA1023; 1 = enables DPD low-pass filter and time stretcher equivalent to TZA1033HL/V1.	not applicable
4 to 2	EQ_{RF}[2:0]	**RF channel low-pass filter (B_{RF}).** 001 = 10 MHz	not applicable
1 and 0	f_{start_DPD}[1:0]	**Start frequency lead/lag filter, DPD block.** 00 = 1 MHz 01 = 5 MHz 10 = 10 MHz 11 = not used	not applicable

7.3.9 REGISTER 8: RF CHANNEL SELECTION

Table 18 Register address 8H

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	–	–	–	–

BIT	7	6	5	4	3	2	1	0
SYMBOL	$SW\text{-}D_{mute}$	$SW\text{-}D_{inv}$	$SW\text{-}C_{mute}$	$SW\text{-}C_{inv}$	$SW\text{-}B_{mute}$	$SW\text{-}B_{inv}$	$SW\text{-}A_{mute}$	$SW\text{-}A_{inv}$

Table 19 Description of register bits (address 8H)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	1000 = address 8H.
11 to 8	–	not used
7	$SW\text{-}D_{mute}$	0 = pass D signal; 1 = mute D signal.
6	$SW\text{-}D_{inv}$	0 = pass D signal with no inversion; 1 = pass D signal with inversion.
5	$SW\text{-}C_{mute}$	0 = pass C signal; 1 = mute C signal.
4	$SW\text{-}C_{inv}$	0 = pass C signal with no inversion; 1 = pass C signal with inversion.
3	$SW\text{-}B_{mute}$	0 = pass B signal; 1 = mute B signal.

BIT	SYMBOL	FUNCTION
2	SW-B_{inv}	0 = pass B signal with no inversion; 1 = pass B signal with inversion.
1	SW-A_{mute}	0 = pass A signal; 1 = mute A signal.
0	SW-A_{inv}	0 = pass A signal with no inversion; 1 = pass A signal with inversion.

7.3.10 Register 11: radial servo offset cancellation

Table 20 Register address BH

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	$LF_{OFFS}1$	$LF_{OFFS}0$	SERVOOS	FTCHBW

BIT	7	6	5	4	3	2	1	0
SYMBOL	$R_{OFFSE}3$	$R_{OFFSE}2$	$R_{OFFSE}1$	$R_{OFFSE}0$	$R_{OFFSF}3$	$R_{OFFSF}2$	$R_{OFFSF}1$	$R_{OFFSF}0$

Table 21 Description of register bits (address BH)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	1011 = address BH
11 and 10	LF_{OFFS}[1:0]	**DC offset compensation for LF path (V_{LFOFFS}).** Common for all servo inputs: SERVOOS = 0 / SERVOOS = 1 00 = 0 mV / 00 = 0 mV 01 = 5 mV / 01 = 15 mV 10 = 10 mV / 10 = 30 mV 11 = 15 mV / 11 = 45 mV
9	SERVOOS	**Servo offset scale (DACs R_{OFFSx}, C_{OFFSx} and LF_{OFFS}).** 0 = normal range; 1 = triple range.
8	FTCHBW	**FTC bandwidth.** 0 = 600 kHz (approximately); 1 = 1.2 MHz (approximately.)
7 to 4	R_{OFFSE}[3:0]	**Programmable DC offset compensation for radial servo path (E input).** SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.
3 to 0	R_{OFFSF}[3:0]	**Programmable DC offset compensation for radial servo path (F input).** SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.

7.3.11 Register 12: central servo offset cancellation inputs A and B

Table 22 Register address CH

BIT	15	14	13	12	D11	D10	D9	D8
SYMBOL	AD3	AD2	AD1	AD0	TSTDPDRF	TSTSRV2	TSTSRV1	TSTSRV0

BIT	D7	D6	D5	D4	D3	D2	D1	D0
SYMBOL	$C_{OFFSA}3$	$C_{OFFSA}2$	$C_{OFFSA}1$	$C_{OFFSA}0$	$C_{OFFSB}3$	$C_{OFFSB}2$	$C_{OFFSB}1$	$C_{OFFSB}0$

Table 23 Description of register bits (address CH)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	1100 = address CH
11	TSTDPDRF	**DPD RF test bit.** With this bit the DPD filter performance is checked. 0 = normal operation; 1 = RF signal filtered by the DPD block is connected to the RF output.
10 to 8	TSTSRV[2:0]	**Test matrix for servo signals to pin OCENTRAL.** 000 = normal operation 001 = filter DAC current for test purposes 011 = CA (sum A to D) 100 = channel A 101 = channel B 110 = channel C 111 = channel D
7 to 4	C_{OFFSA}[3:0]	**Central servo input A offset cancellation.** Bit SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.
3 to 0	C_{OFFSB}[3:0]	**Central servo input B offset cancellation.** Bit SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.

7.3.12 Register 13: central servo offset cancellation inputs C and D

Table 24 Register address DH

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	RFonly	–	–	–

BIT	7	6	5	4	3	2	1	0
SYMBOL	$C_{OFFSC}3$	$C_{OFFSC}2$	$C_{OFFSC}1$	$C_{OFFSC}0$	$C_{OFFSC}3$	$C_{OFFSC}2$	$C_{OFFSC}1$	$C_{OFFSC}0$

Table 25 Description of register bits (address DH)

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	1101 = address DH
11	RFonly	**Operation mode.** 0 = normal operation; 1 = RF only mode (servo outputs OA to OD, S1 and S2 are 3-state).
10 to 8	–	not used
7 to 4	C_{OFFSC}[3:0]	**Central servo input C offset cancellation.** Bit SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.
3 to 0	C_{OFFSD}[3:0]	**Central servo input D offset cancellation.** Bit SERVOOS = 0: 0 to 20 mV; bit SERVOOS = 1: 0 to 60 mV.

7.3.13 REGISTER 14: RF FILTER SETTINGS

Table 26 Register address EH

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	–	–	RFNFEN	RFEQEN

BIT	7	6	5	4	3	2	1	0
SYMBOL	RFKEQ	BWRF6	BWRF5	BWRF4	BWRF3	BWRF2	BWRF1	BWRF0

Table 27 Description of register bits (address EH); bit K2_Mode = 1

BIT	SYMBOL	FUNCTION
15 to 12	AD[3:0]	1110 = address EH
11 and 10	–	not used
9	RFNFEN	**Noise filter enable.** 0 = disable; 1 = enable.
8	RFEQEN	**Equalizer enable.** 0 = disable; 1 = enable.
7	RFKEQ	**Boost factor.** 0 = boost factor low; 1 = boost factor high.
6 to 0	BWRF[6:0]	**Bandwidth limitation in RF path.** 000 0000 to 111 1111: $f_{0(RF)}$ = 12 to 145 MHz.

7.3.14 REGISTER 15: DPD FILTER SETTINGS

Table 28 Register address FH

BIT	15	14	13	12	11	10	9	8
SYMBOL	AD3	AD2	AD1	AD0	–	–	–	–

BIT	7	6	5	4	3	2	1	0
SYMBOL	–	–	DPD_LL2	DPD_LL1	DPD_LL0	DPD_LPF2	DPD_LPF1	DPD_LPF0