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DAB One-Chip Channel- and Source Decoder

Description

The U2739M-B is an integrated circuit in advanced CMOS technology for demodulation and decoding of a DAB signal according to ETS 300 401. The channel decoder part includes the main features OFDM demodulation & decoding and time & frequency synchronization algorithms, using the embedded OAK DSP core.

The source decoder consists of an audio and a data decoder part. The audio source decoder supports ISO MPEG 1,2 layer 2 and the data decoder offers 2 independent packet mode decoders.

Several standard interfaces, like I^2C/L3, I^2S, SPDIF or RDI are implemented to offer a flexible utilization.

Moreover the U2739M-B includes a mechanism to replace respectively extend certain software modules by using a special boot mode (so-called USE). For example, the time & frequency synchronization modules can be replaced by down-loading the corresponding user software algorithms to the OAK DSP core.

Electrostatic sensitive device.
Observe precautions for handling.

Block Diagram

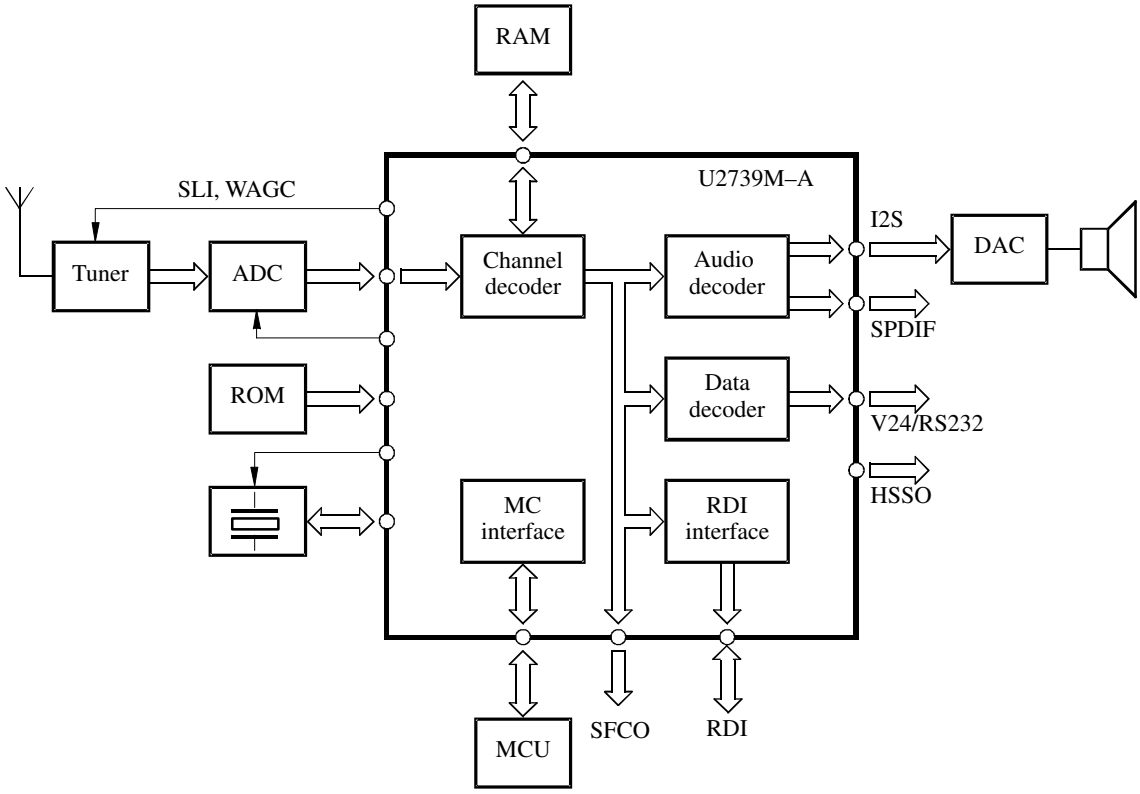

Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2739M-BFT	T–PQFP–G100	Tray
U2739M-BFC	CQFP144	Tray

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1 Features

1.1 General

- Support of mode I, II, III and IV acc. to ETS 300 401
- Time & frequency synchronization with a wide-range parameter set
- Optional implementation of user-defined synchronization strategy by using USE boot mode
- Flexible software configuration:
  set 1 – (temic kernel), set 2 – (user extension) concept
- Automatic mode detection (AMD)
- FIC on-chip memory, access via MC interface
- Generation of receiver status information
- Generation of tuner control signals
- Generation of pulse width modulated VCXO control signal
- Power supply 3.3 V, master clock 24.576 MHz
- Plastic TQFP100 package or
- Ceramic QFP144 package for software development

1.2 Channel Decoder

- Demodulation and decoding of up to 64 UEP/EEP sub-channels
- Support of dynamic multiplex reconfiguration (DMR) without mute state
- Digital Null-Symbol detection (FSYNCH generation)
- Channel filtering (48 dB)
- Optional SAW filter equalization
- Digital AFC (freq. tolerance < 0.5 Hz for mode I)
- Digital AGC with a wide gain control range
- Off-chip de-interleaver memory for full 1.8 Mbit/s decoding data rate
- Time & frequency synchronization on DSP OAK core
- Support of TII decoding and corresponding RDI insertion (set 2)

1.3 Audio Source Decoder

- Supports MPEG1 layer II streams according to ISO/IEC 11172/3
- Supports MPEG2 layer II (half sampling rate) streams according to ISO/IEC 13818–3
- Supports all bit rates defined in the ETS 300 401 standard
- I^2S and SPDIF output interfaces
- Programmable fader
- Programmable DRC
- PAD extraction

1.4 Data Decoder

- 2 independent packet mode decoder
- Flexible configuration via MC commands
- Data group length limited to ~1 kbyte each
- Output via HSSO or V24
- DD1 option: FIDC decoder
- Support of AIC decoding (set 2)

1.5 Interfaces

- Source decoder output interface: I^2S and SPDIF
- Data decoder output interface: V24 or HSSO
- Channel decoder output interface: RDI and SFCO
- Microcontroller interface: I^2C/L3
- RDI:
  - Extended high capacity mode
  - IEC 958 format
  - RDI control channel (RCC)
- SFCO simple full capacity output:
  - window-, serial sub-channel identifier (SbChId)-, data-, error- and clock line
  - 3.072 MHz burst mode interface
- 10-bit ADC interface:
  - ADC sampling clock generation
  - ADC binary or 2's complement format selection
  - support of several intermediate frequencies
- DSP OAK core bootstrap ROM interface
- Voltage controlled reference oscillator (VCXO) interface
- Time de-interleaver SRAM (4 Mbit) interface
- High speed serial output HSSO (PAD, DD1, DD2, CIR) interface, 3-line serial burst mode interface

2 Functional Block Diagram

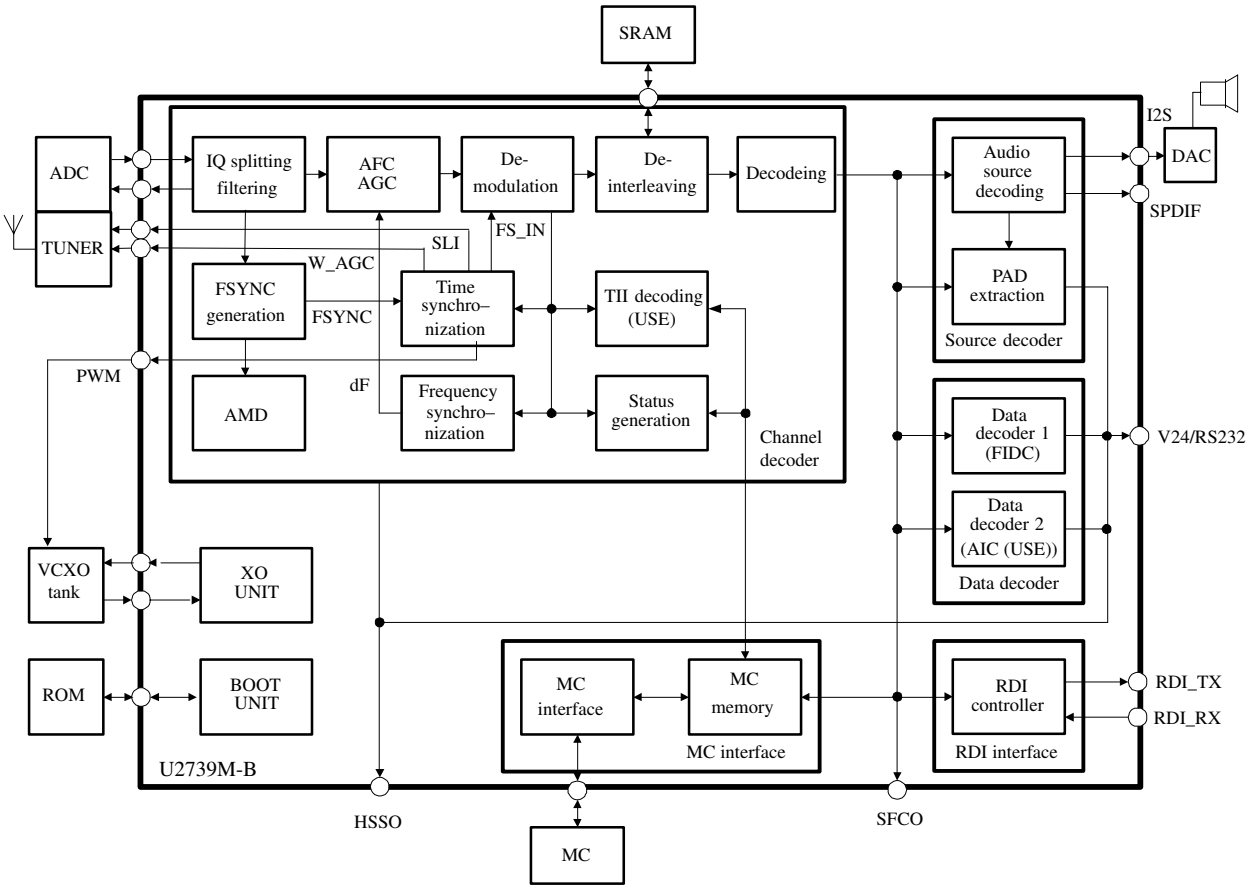


Figure 2. Functional block diagram

3 Pin Description

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
1	1	ADC_CLK	ADC sampling clock output 8.192 MHz	PDO04T	out	
2		TIN0	Test input 0 (pull down)	PDDZ	in	x
3		TIN1	Test input 1 (pull down)	PDDZ	in	x
4	2	ADC_DATA9	ADC data input, bit 9 (MSB)	PDIZ	in	x
5	3	ADC_DATA8	ADC data input, bit 8	PDIZ	in	x
6	4	ADC_DATA7	ADC data input, bit 7	PDIZ	in	x
7	5	ADC_DATA6	ADC data input, bit 6	PDIZ	in	x
8		TIN2	Test input 2 (pull down)	PDDZ	in	x
9		DVSSE	Ground	PVSS1Z, PVSS2Z	gnd	x
10	6	ADC_DATA5	ADC data input, bit 5	PDIZ	in	x
11	7	ADC_DATA4	ADC data input, bit 4	PDIZ	in	x
12	8	ADC_DATA3	ADC data input, bit 3	PDIZ	in	x
13	9	ADC_DATA2	ADC data input, bit 2	PDIZ	in	x
14		TIN3	Test input 3 (pull down)	PDDZ	in	x
15		TIN4	Test input 4 (pull down)	PDDZ	in	x
16	10	ADC_DATA1	ADC data input, bit 1	PDIZ	in	x
17	11	ADC_DATA0	ADC data input, bit 0 (LSB)	PDIZ	in	x
18	12	DVSS1	Digital ground	PVSS1Z, PVSS2Z	gnd	x
19	13	AVSS1	Analog ground	PVSS3Z	gnd	x
20	14	XIN	Oscillator input	PDX02	osc	
21	15	XOUT	Oscillator output	(PDX02)	osc	
22	16	AVDD1	Analog power supply	PVDD3Z	pwr	
23		/C_DR	C-bus data read enable	PRO04T	out	
24	17	/RS	Low active reset	PDIZ	in	x
25	18	PWM	Pulse width modulated control output	PRO04T	out	
26		/C_DW	C-bus data write enable	PRO04T	out	
27	19	W_AGC	Window AGC	PRO04T	out	
28	20	SLI	Synchronization lock indicator	PRO04T	out	
29		/C_PR	C-bus program read enable	PRO04T	out	
30	21	HSSO_WIN	HSSO window signal	PRO04T	out	
31		/C_PW	C-bus program write enable	PRO04T	out	
32	22	HSSO _CLK	HSSO clock signal	PRO04T	out	
33		/ABORT	Low active ABORT signal (pull up)	PDUZ	in	x
34	23	HSSO _DAT	HSSO data signal	PRO04T	out	
35	24	C_ADD0	C-bus address bit 0 (LSB)	PRO04T	out	
36	25	C_ADD1	C-bus address bit 1	PRO04T	out	
37	26	/BOOT_RE	BOOT read enable	PRO04T	out	
38	27	C_ADD2	C-bus address bit 2	PRO04T	out	
39	28	C_ADD3	C-bus address bit 3	PRO04T	out	
40	29	C_ADD4	C-bus address bit 4	PRO04T	out	
41	30	C_ADD5	C-bus address bit 5	PRO04T	out	
42	31	C_ADD6	C-bus address bit 6	PRO04T	out	
43		TOUT0	Test output bit 0	PRO02T	out	
44	32	C_ADD7	C-bus address bit 7	PRO04T	out	

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
45	33	C_ADD8	C-bus address bit 8	PRO04T	out	
46	34	C_ADD9	C-bus address bit 9	PRO04T	out	
47	35	C_ADD10	C-bus address bit 10	PRO04T	out	
48	36	C_ADD11	C-bus address bit 11	PRO04T	out	
49	37	C_ADD12	C-bus address bit 12	PRO04T	out	
50	38	DVDD1	Digital power supply	PVDD1Z, PVDD2Z	pwr	x
51	39	C_ADD13	C-bus address bit 13	PRO04T	out	
52		C_ADD14	C-bus address bit 14	PRO04T	out	
53		C_ADD15	C-bus address bit 15	PRO04T	out	
54	40	C_DATA0/DBG	C-bus data bit 0 (pull down)	PRD04TZ	inout	x
55	41	C_DATA1/BOOT	C-bus data bit 1 (pull down)	PRD04TZ	inout	x
56		C_DATA8	C-bus data bit 8 (pull down)	PRD04TZ	inout	x
57		C_DATA9	C-bus data bit 9 (pull down)	PRD04TZ	inout	x
58	42	DVSS2	Digital ground	PVSS1Z, PVSS2Z	gnd	x
59	43	C_DATA2/URST	C-bus data bit 2 (pull down)	PRD04TZ	inout	x
60	44	C_DATA3/XUSE	C-bus data bit 3 (pull down)	PRD04TZ	inout	x
61		C_DATA10	C-bus data bit 10 (pull down)	PRD04TZ	inout	x
62		C_DATA11	C-bus data bit 11 (pull down)	PRD04TZ	inout	x
63	45	C_DATA4/PSPC	C-bus data bit 4 (pull down)	PRD04TZ	inout	x
64	46	C_DATA5/RDI_VBIT	C-bus data bit 5 (pull down)	PRD04TZ	inout	x
65		C_DATA12	C-bus data bit 12 (pull down)	PRD04TZ	inout	x
66		C_DATA13	C-bus data bit 13 (pull down)	PRD04TZ	inout	x
67	47	C_DATA6/XO12	C-bus data bit 6 (pull down)	PRD04TZ	inout	x
68	48	C_DATA7/ADE	C-bus data bit 7 (pull down)	PRD04TZ	inout	x
69		C_DATA14	C-bus data bit 14 (pull down)	PRD04TZ	inout	x
70		C_DATA15	C-bus data bit 15 (pull down)	PRD04TZ	inout	x
71	49	TEST_MODE/BYPP	Test mode selection (pull down)	PDDZ	in	x
72	50	MCM_TRIGGER	MCM trigger signal	PRO04T	out	
73	51	MC_MODE	Microcontroller mode signal	PDIZ	in	x
74	52	MC_CLK	Microcontroller clock signal	PDIZ	in	x
75	53	MC_DAT	Microcontroller data signal	PRB04TZ	inout	x
76		DVDDE	Digital power supply	PVDD1Z, PVDD2Z	pwr	x
77	54	SPDIF	SPDIF output	PRO04T	out	
78	55	RS232	RS232 output	PRO04T	out	
79	56	I2S_CLK	I2S clock output	PRO04T	out	
80	57	I2S_DAT	I2S data output	PRO04T	out	
81		TOUT1	Test output bit 1	PRO02T	out	
82	58	I2S_WIN	I2S win output	PRO04T	out	
83		TOUT2	Test output bit 2	PRO02T	out	
84	59	TOUT3	Test output bit 3	PRO02T	out	
85	60	RDI_RX	RDI receive data	PDIZ	in	x
86	61	RDI_TX	RDI transmit data	PRO04T	out	
87	62	DVSS3	Digital ground	PVSS1Z, PVSS2Z	gnd	x
88		TOUT4	Test output bit 4	PRO02T	out	

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
89		TOUT5	Test output bit 5	PRO02T	out	
90	63	SFCO_SID	SFCO sub-channel ID	PRO04T	out	
91	64	SFCO_ERR	SFCO errorflag	PRO04T	out	
92	65	SFCO_DAT	SFCO data	PRO04T	out	
93		TOUT6	Test output bit 6	PRO02T	out	
94	66	SFCO_CLK	SFCO clock	PRO04T	out	
95	67	SFCO_WIN	SFCO window	PRO04T	out	
96		TOUT7	Test output bit 7	PRO02T	out	
97	68	DVDD2	Digital power supply	PVDD1Z, PVDD2Z	pwr	x
98	69	TOUT8	Test output bit 8	PRO02T	out	
99		TOUT9	Test output bit 9	PRO02T	out	
100	70	SRAM_D7	SRAM data bit 7	PRB04TZ	inout	x
101	71	SRAM_D6	SRAM data bit 6	PRB04TZ	inout	x
102		TOUT10	Test output bit 10	PRO02T	out	
103	72	SRAM_D5	SRAM data bit 5	PRB04TZ	inout	x
104	73	SRAM_D4	SRAM data bit 4	PRB04TZ	inout	x
105		TOUT11	Test output bit 11	PRO02T	out	
106	74	SRAM_D3	SRAM data bit 3	PRB04TZ	inout	x
107	75	SRAM_D2	SRAM data bit 2	PRB04TZ	inout	x
108		TOUT12	Test output bit 12	PRO02T	out	
109	76	SRAM_D1	SRAM data bit 1	PRB04TZ	inout	x
110	77	SRAM_D0	SRAM data bit 0	PRB04TZ	inout	x
111		TIN5	Test input 5 (pull down)	PDDZ	in	x
112	78	SRAM_WR	SRAM write signal	PRO04T	out	
113	79	SRAM_OE	SRAM output enable	PRO04T	out	
114	80	SRAM_A18	SRAM address bit 18	PRO04T	out	
115		TIN6	Test input 6 (pull down)	PDDZ	in	x
116	81	SRAM_A17	SRAM address bit 17	PRO04T	out	
117	82	SRAM_A16	SRAM address bit 16	PRO04T	out	
118		TOUT13	Test output bit 13	PRO02T	out	
119	83	SRAM_A15	SRAM address bit 15	PRO04T	out	
120	84	SRAM_A14	SRAM address bit 14	PRO04T	out	
121	85	DVSS4	Digital ground	PVSS1Z, PVSS2Z	gnd	x
122		TIN7	Test input 7 (pull down)	PDDZ	in	x
123	86	SRAM_A13	SRAM address bit 13	PRO04T	out	
124	87	SRAM_A12	SRAM address bit 12	PRO04T	out	
125		TOUT14	Test output bit 14	PRO02T	out	
126	88	SRAM_A11	SRAM address bit 11	PRO04T	out	
127	89	SRAM_A10	SRAM address bit 10	PRO04T	out	
128		TOUT15	Test output bit 15	PRO02T	out	
129	90	SRAM_A9	SRAM address bit 9	PRO04T	out	
130	91	SRAM_A8	SRAM address bit 8	PRO04T	out	

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
131		TOUT16	Test output bit 16	PRO02T	out	
132	92	SRAM_A7	SRAM address bit 7	PRO04T	out	
133	93	SRAM_A6	SRAM address bit 6	PRO04T	out	
134	94	DVDD3	Digital power supply	PVDD1Z, PVDD2Z	pwr	
135		TOUT17	Test output bit 17	PRO02T	out	
136	95	SRAM_A5	SRAM address bit 5	PRO04T	out	
137	96	SRAM_A4	SRAM address bit 4	PRO04T	out	
138		TMUX0	Test mux in bit 0 (LSB) (pull down)	PDDZ	in	x
139	97	SRAM_A3	SRAM address bit 3	PRO04T	out	
140	98	SRAM_A2	SRAM address bit 2	PRO04T	out	
141		TMUX1	Test mix in bit 1 (pull down)	PDDZ	in	x
142	99	SRAM_A1	SRAM address bit 1	PRO04T	out	
143	100	SRAM_A0	SRAM address bit 0	PRO04T	out	
144		TMUX2	Test mux in bit 2 (pull down)	PDDZ	in	x

4 Strap Pins

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir	Comment
16	10	ADC_DATA1	ADC data input, bit 1	PDIZ	in	Strap pin OCSEL 1
17	11	ADC_DATA0	ADC data input, bit 0	PDIZ	in	Strap pin OCSEL 0
54	40	C_DATA0/DBG	C-bus data bit 0	PRD04TZ	inout	Strap pin C_DATA0/DBG
55	41	C_DATA1/BOOT	C-bus data bit 1	PRD04TZ	inout	Strap pin C_DATA1/BOOT
59	43	C_DATA2/URST	C-bus data bit 2	PRD04TZ	inout	Strap pin C_DATA2/URST
60	44	C_DATA3/XUSE	C-bus data bit 3	PRD04TZ	inout	Strap pin C_DATA3/XUSE
63	45	C_DATA4/PSPC	C-bus data bit 4	PRD04TZ	inout	Strap pin C_DATA4/PSPC
64	46	C_DATA5/ RDI_VBIT	C-bus data bit 5	PRD04TZ	inout	Strap pin C_DATA5/RDI_VBIT 0 RDI spec.: validity bit 1 1 IEC958 spec.: validity bit 0
67	47	C_DATA6/XO12	C-bus data bit 6	PRD04TZ	inout	Strap pin C_DATA6/XO12 0 external oscillator 24.576 MHz 1 external oscillator 12.288 MHz
68	48	C_DATA7/ADE	C-bus data bit 7 ADC_DATA strap pin function enable	PRD04TZ	inout	Strap pin C_DATA7/ADE 0 ADC_DATA strap pin function disabled 1 ADC_DATA strap pin function enabled
71	49	TEST_MODE/BYPP	Test mode selection	PDDZ	in	Strap pin TEST_MODE/BYPP 0 PLL activated 1 PLL bypassed
73	51	MC_MODE	Microcontroller mode signal	PDIZ	in	Strap pin I2C/L3 0 I2C 1 L3

5 Pin Configuration

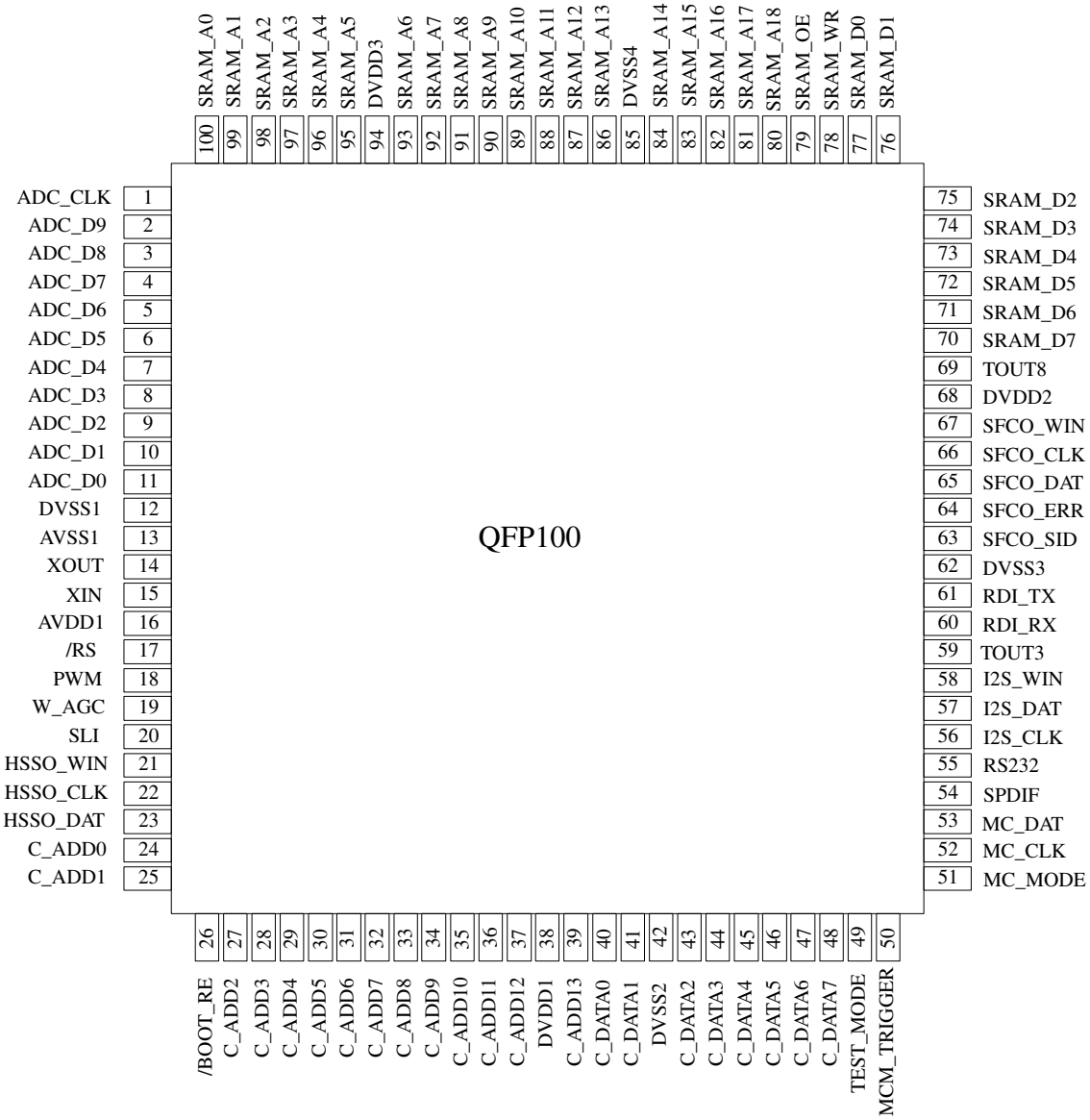


Figure 3. Production version QFP100

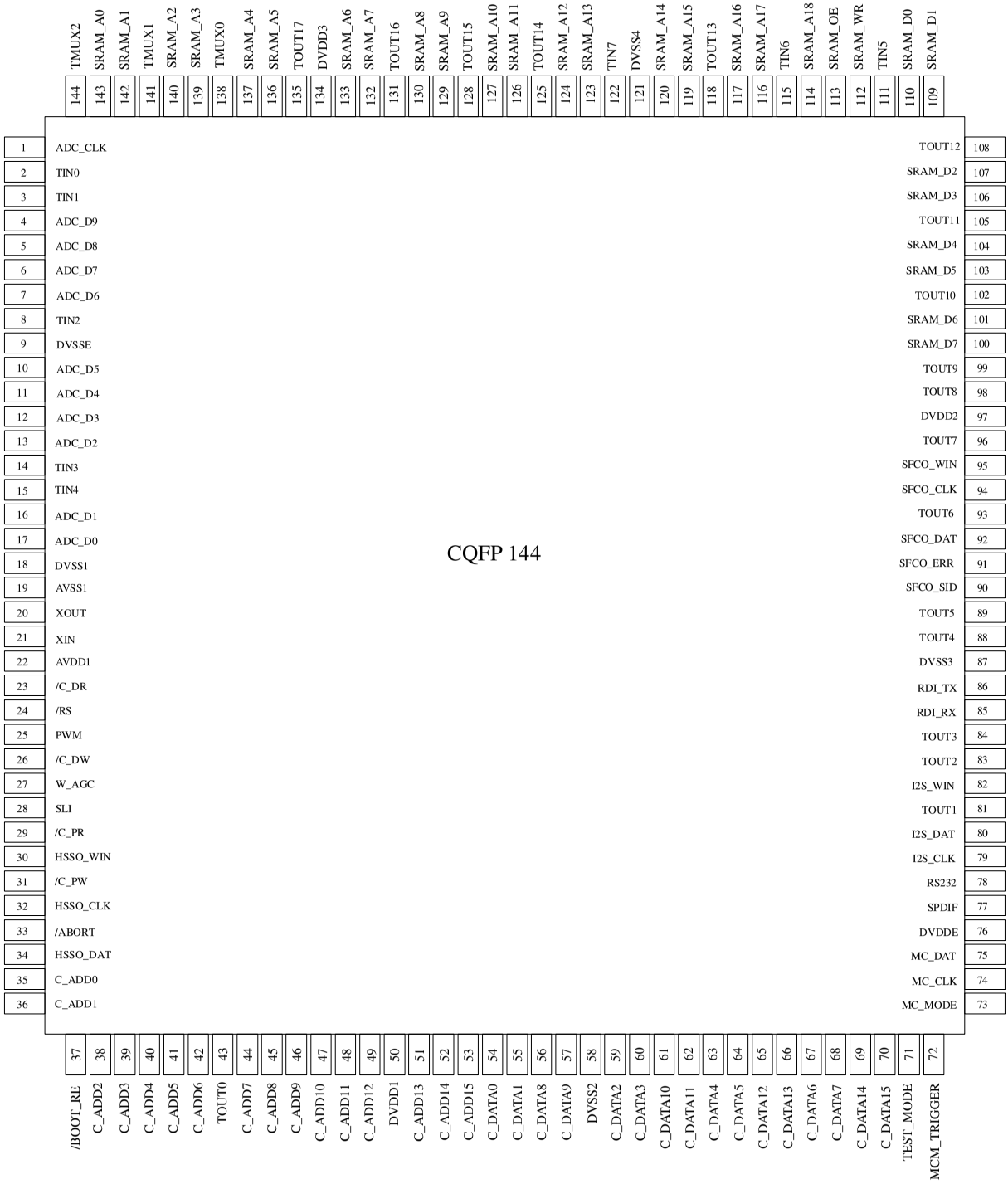


Figure 4. Software development version QFP144

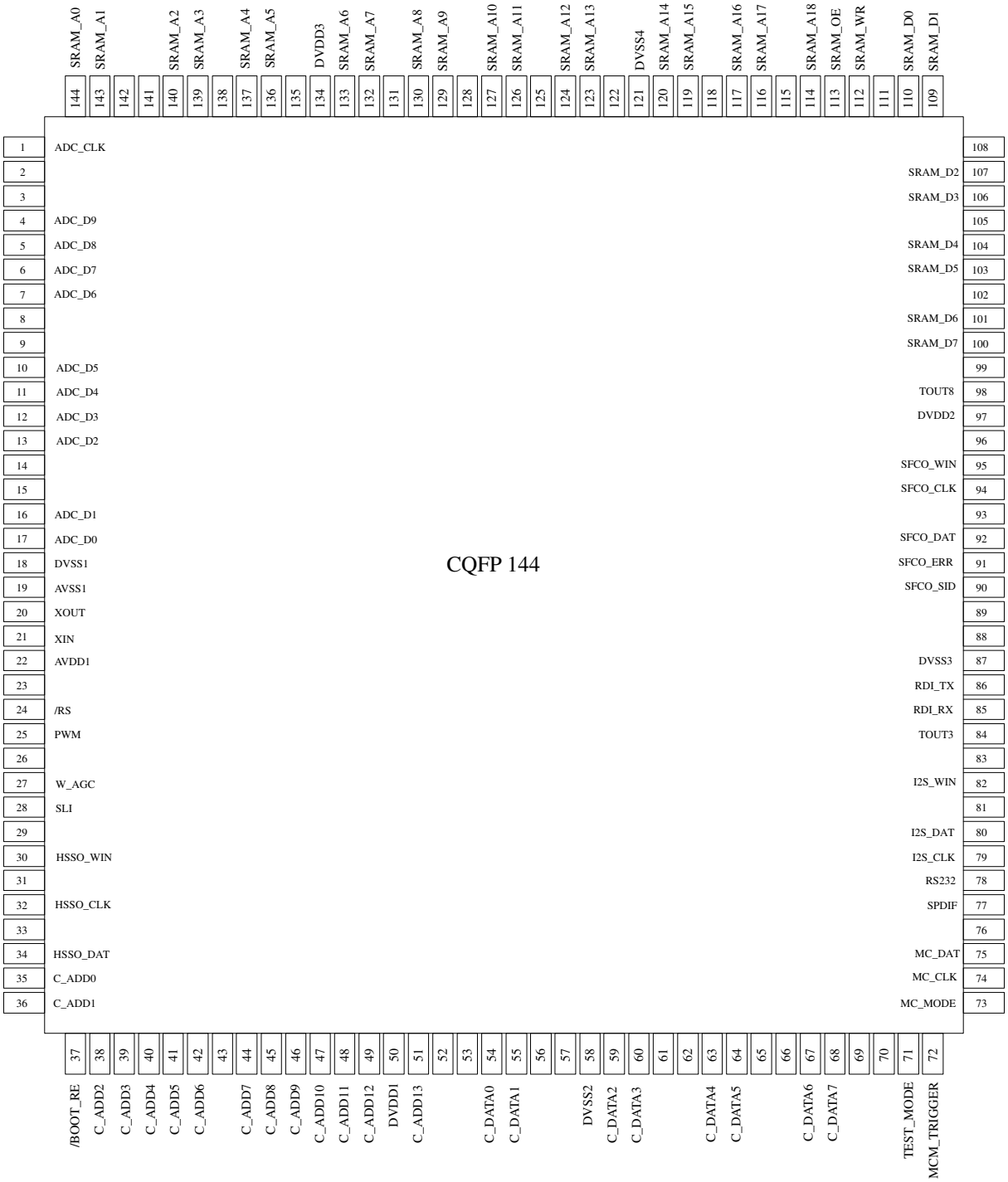


Figure 5. Version QFP144 used as production version

6 Interface Description

6.1 Overview

The interface description explains the purpose, the utilization and the meaning of every interface and every signal. It is divided into twelve sections, which are related to the different interfaces. An overview of all interfaces is shown in the functional block diagram below. Several standard output interfaces like I^2S or SPDIF are used to offer a flexible usage of the U2739M-B.

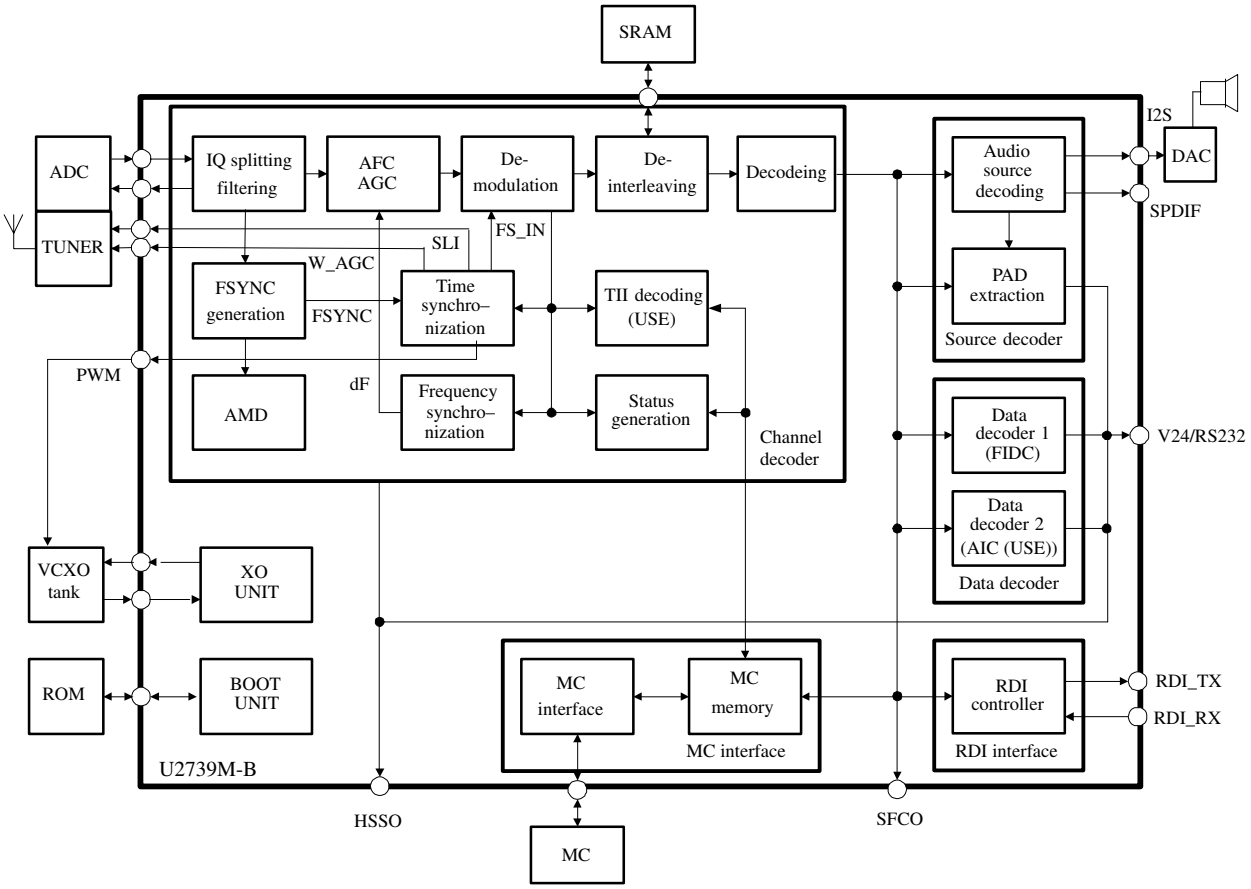


Figure 6. Functional block diagram

6.2 ADC Interface

6.2.1 ADC Interface Signal Description

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
1	1	ADC_CLK	ADC sampling clock output 8.192 MHz	PDO04T	out	
4	2	ADC_DATA9	ADC data input, bit 9 (MSB)	PDIZ	in	x
5	3	ADC_DATA8	ADC data input, bit 8	PDIZ	in	x
6	4	ADC_DATA7	ADC data input, bit 7	PDIZ	in	x
7	5	ADC_DATA6	ADC data input, bit 6	PDIZ	in	x
10	6	ADC_DATA5	ADC data input, bit 5	PDIZ	in	x
11	7	ADC_DATA4	ADC data input, bit 4	PDIZ	in	x
12	8	ADC_DATA3	ADC data input, bit 3	PDIZ	in	x
13	9	ADC_DATA2	ADC data input, bit 2	PDIZ	in	x
16	10	ADC_DATA1	ADC data input, bit 1	PDIZ	in	x
17	11	ADC_DATA0	ADC data input, bit 0 (LSB)	PDIZ	in	x

6.2.2 ADC Interface Description

The ADC interface as shown in figure 6 consists of the ADC data input signal ADC_DATA(9:0) and the ADC sampling clock output signal ADC_CLK. The U2739M-B can be connected to every standard AD with either binary or 2's complement output format. The sampling frequency is 8.192 MHz and a bandwidth of 2 MHz is necessary. The possible IF's, which are supported in conjunction with the IF input signal mode (parameter IFM) are given by the formula.

f_{if} = 2.048 MHz + n × 4.096 MHz, with n = 0, 1, 2, 3 ....

Thus possible IFs are 2.048 MHz, 6.144 MHz, ... 38.912 MHz. The parameter IFM is defined by the MC command 'set global configuration' [Atmel Wireless & Microcontrollers U2739M documentation set – "U2739M_MC_Command_set_vxxx.pdf"]. The analog input bandwidth of the A/D converter must be chosen accordingly. The ADC_DATA input is 10 bit wide. The typical output delay (td3 in figure 7) of the AD converter related to the falling edge of the sampling clock CLK8192 should be 20 ns. The generated 8.192 MHz output clock take over the ADC_DATA with his rising edge of ADC_CLK. The format 'binary offset' or '2's complement' of the A/D converter can be selected by the parameter ADCF. This parameter is also defined by the 'set global configuration' MC command [Atmel Wireless & Microcontrollers U2739M documentation set – "U2739M_MC_Command_set_vxxx.pdf"].

Furthermore, the sampling clock generation is performed by the U2739M-B. The input data appearing at the ADC_DATA port are assumed to be generated by an A/D converter. The effective resolution of this converter should be greater than 9 bit in order to use the full dynamic range implemented in the U2739M-B. The sampling clock required for the external A/D converter is derived inside U2739M-B. It has to be 8.192 MHz.

6.2.3 ADC Interface Timing Diagram

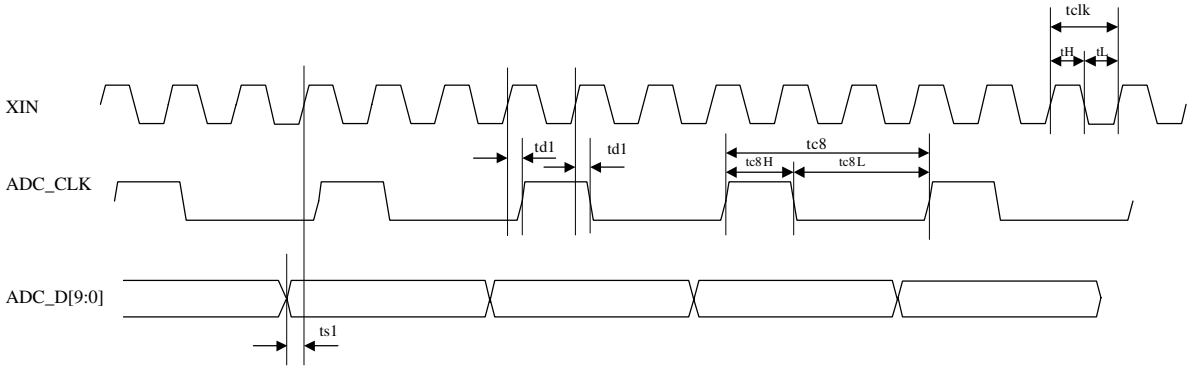


Figure 7. ADC interface timing diagram

6.2.4 ADC Interface Timing Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
XIN clock period	tclk		40.7		ns
XIN clock high	tH	15.0	20.35	25.0	ns
XIN clock low	tL	15.0	20.35	25.0	ns
ADC_CLK clock period	tc8		3 × 40.7		ns
ADC_CLK clock high	tc8H		1 × 40.7		ns
ADC_CLK clock low	tc8L		2 × 40.7		ns
Setup time ADC_D(9:0)	ts1	5.0			ns
Output delay of ADC_CLK	td1	12.0	20.0	28.0	ns

6.3 Tuner Interface

6.3.1 Tuner Interface Signal Description

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
27	19	W_AGC	Window AGC 0 during COFDM symbols 1 during the NULL symbol	PRO04T	out	
28	20	SLI	Synchronization lock indicator 0 receiver synchronization not locked 1 receiver synchronization locked	PRO04T	out	

6.3.2 Tuner Interface Description

In order to implement a flexible AGC concept of a DAB receiver the signals W_AGC and SLI can be used to control the tuner IC U2731B. The influence of W_AGC and SLI to the RF AGC voltage generation block is described in the U2731B preliminary datasheet.

The WAGC signal must be controlled by the MC by using the set WAGC configuration MC command. The WAGC signal does not follow the moving FFT window. The rising and falling edge can be adjusted by the MC. The MC can use the differential dT, which correspond to the FFT window shift, from the read synchronization status command to adjust the WAGC rising and falling edge.

6.4 MC Interface

6.4.1 MC Interface Signal Description

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
72	50	MCM_TRIGGER	MCM trigger signal	PRO04T	out	
73	51	MC_MODE	Microcontroller mode signal 0 I2C bus protocol 1 L3 bus protocol	PDIZ	in	x
74	52	MC_CLK	Microcontroller clock signal	PDIZ	in	x
75	53	MC_DAT	Microcontroller data signal	PRB04TZ	inout	x

6.4.2 MC Interface Description

The MC interface is used for data transmission between the U2739M-B (slave) and an external microcontroller (master). It can be configured for L3- or I2C protocol depending on the status of the MC_MODE line during reset (/RS = LOW):

MC_MODE = HIGH ☐ L3 bus selected

MC_MODE = LOW ☐ I2C bus selected

The MCM_TRIGGER line indicates the status of the internal interface controller.

The external MCU is able to communicate with the U2739M-B during LOW phases of MCM_TRIGGER only !

Further the MCM trigger signal indicates the synchronization status. If the MCM trigger has period of 8 ms, then the U2739M-B is not locked. In the synchronized (‘locked’) state the MCM trigger period correspond to the CIF frame, which is provided every 24 ms. The complete FIC is processed at the beginning of the transmission frame.

6.4.3 L3 Bus Interface Timing Diagram

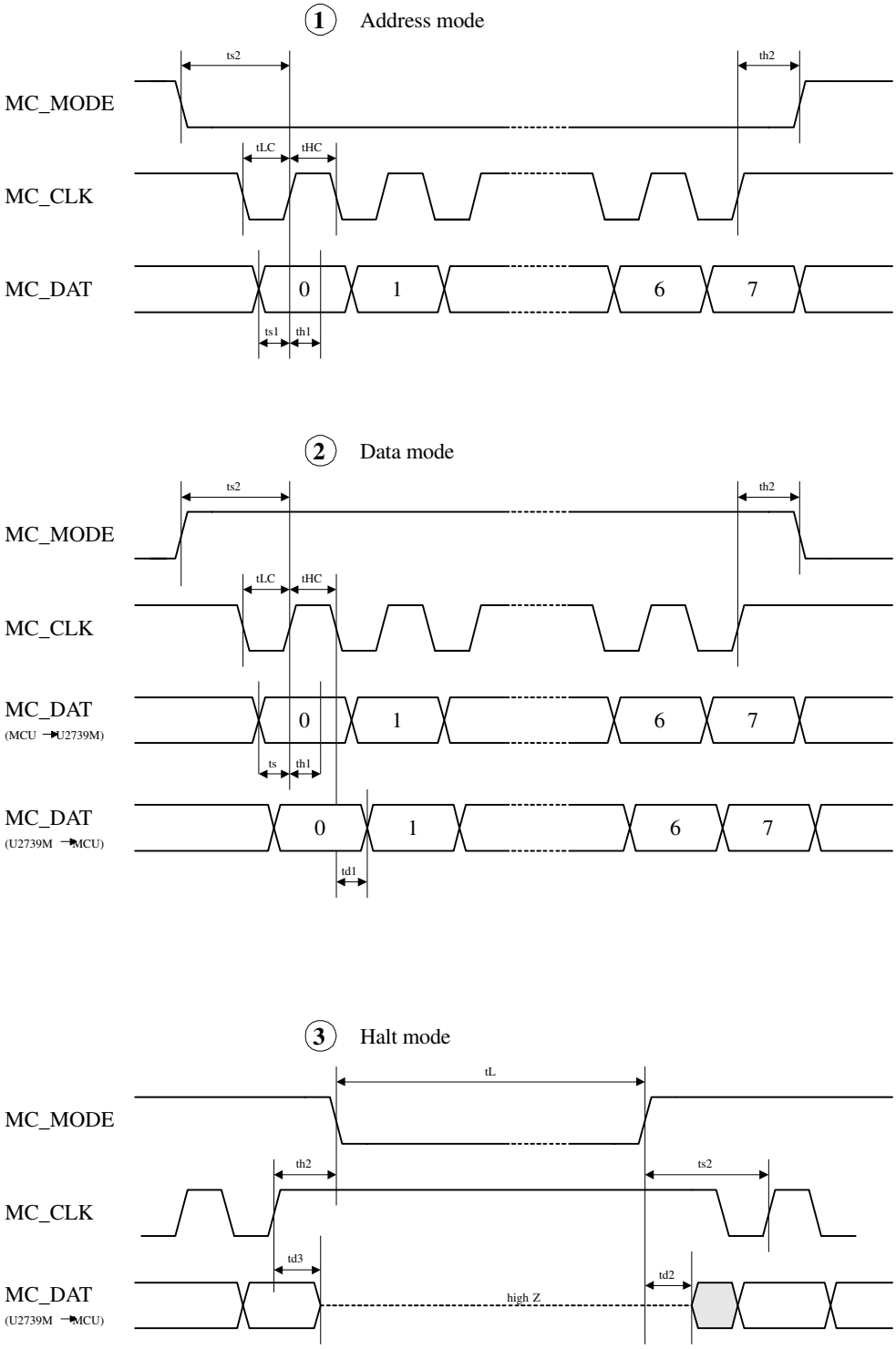


Figure 8. MC L3 bus interface timing diagram

6.4.4 L3 Bus Timing Parameter

Parameter	Symbol	Min.	Typ.	Max.	Unit
MC_CLK low phase	tLC	61			ns
MC_CLK high phase	tHC	61			ns
MC_DAT input setup time	ts1	61			ns
MC_DAT input hold time	th1	61			ns
MC_MODE hold time	th2	61			ns
MC_MODE setup time	ts2	61			ns
MC_CLK(h/l) / MC_DAT delay	td1	20		100	ns
MC_MODE(l/h) / MC_DAT (output driven)	td2	110		130	ns
MC_CLK(l/h) / MC_DAT(high Z)	td3	120		160	ns

6.4.5 I2C Bus Interface Timing Diagram

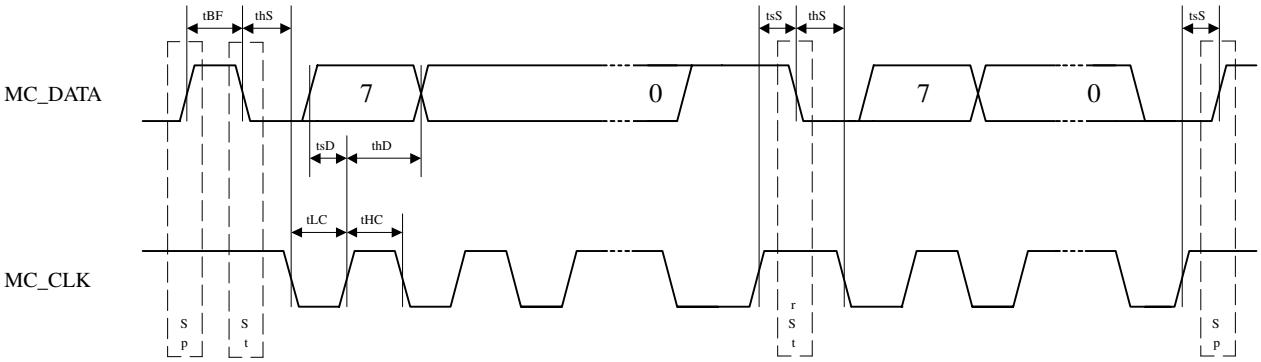


Figure 9. MC I2C bus timing diagram

6.4.6 I2C Bus Timing Parameter

Parameter	Symbol	Min.	Typ.	Max.	Unit
Bus free time between STOP and START condition	tBF	400			ns
Hold time (repeated) START condition	thS	200			ns
Setup time data	tsD	120			ns
Hold time data	thD	320			ns
Low period clock	tLC	300			ns
High period clock	tHC	200			ns
Setup time: repeated START condition, STOP condition	tsS	240			ns

6.5 C-Bus / BOOT Bus Interface

6.5.1 C-Bus Signal Description

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
23		/C_DR	C-bus data read enable	PRO04T	out	
26		/C_DW	C-bus data write enable	PRO04T	out	
29		/C_PR	C-bus program read enable	PRO04T	out	
31		/C_PW	C-bus program write enable	PRO04T	out	
35	24	C_ADD0	C-bus address bit 0 (LSB)	PRO04T	out	
36	25	C_ADD1	C-bus address bit 1	PRO04T	out	
37	26	/BOOT_RE	BOOT read enable	PRO04T	out	
38	27	C_ADD2	C-bus address bit 2	PRO04T	out	
39	28	C_ADD3	C-bus address bit 3	PRO04T	out	
40	29	C_ADD4	C-bus address bit 4	PRO04T	out	
41	30	C_ADD5	C-bus address bit 5	PRO04T	out	
42	31	C_ADD6	C-bus address bit 6	PRO04T	out	
44	32	C_ADD7	C-bus address bit 7	PRO04T	out	
45	33	C_ADD8	C-bus address bit 8	PRO04T	out	
46	34	C_ADD9	C-bus address bit 9	PRO04T	out	
47	35	C_ADD10	C-bus address bit 10	PRO04T	out	
48	36	C_ADD11	C-bus address bit 11	PRO04T	out	
49	37	C_ADD12	C-bus address bit 12	PRO04T	out	
51	39	C_ADD13	C-bus address bit 13	PRO04T	out	
52		C_ADD14	C-bus address bit 14	PRO04T	out	
53		C_ADD15	C-bus address bit 15	PRO04T	out	
54	40	C_DATA0/DBG	C-bus data bit 0 (pull down)	PRD04TZ	inout	x
55	41	C_DATA1/BOOT	C-bus data bit 1 (pull down)	PRD04TZ	inout	x
56		C_DATA8	C-bus data bit 8 (pull down)	PRD04TZ	inout	x
57		C_DATA9	C-bus data bit 9 (pull down)	PRD04TZ	inout	x
59	43	C_DATA2/URST	C-bus data bit 2 (pull down)	PRD04TZ	inout	x
60	44	C_DATA3/XUSE	C-bus data bit 3 (pull down)	PRD04TZ	inout	x
61		C_DATA10	C-bus data bit 10 (pull down)	PRD04TZ	inout	x
62		C_DATA11	C-bus data bit 11 (pull down)	PRD04TZ	inout	x
63	45	C_DATA4/PSPC	C-bus data bit 4 (pull down)	PRD04TZ	inout	x
64	46	C_DATA5/RDI_VBIT	C-bus data bit 5 (pull down)	PRD04TZ	inout	x
65		C_DATA12	C-bus data bit 12 (pull down)	PRD04TZ	inout	x
66		C_DATA13	C-bus data bit 13 (pull down)	PRD04TZ	inout	x
67	47	C_DATA6/XO12	C-bus data bit 6 (pull down)	PRD04TZ	inout	x
68	48	C_DATA7/BYPP	C-bus data bit 7 (pull down)	PRD04TZ	inout	x
69		C_DATA14	C-bus data bit 14 (pull down)	PRD04TZ	inout	x
70		C_DATA15	C–-bus data bit 15 (pull down)	PRD04TZ	inout	x

6.5.2 C-Bus / BOOT Bus Interface Description

The C-Bus is a multiplexed program as well as data bus system to communicate with external components. The complete bus system is available only in the QFP144 package version and needed for debugging the internal OAK DSP core.

The BOOT bus covers a subset of the C-Bus signals. The user is able to download his own so-called 'User Software Extensions' using this bus system to replace or extend the Atmel Wireless & Microcontrollers firmware. The BOOT bus is a standard ROM interface (address/ data buses, read enable line) and the read access is always with 16 wait states (referring the OAK internal 49.152 MHz clock) to support slow devices.

The BOOT bus is available in both package versions. The timing diagram refers to the BOOT bus signals only.

6.5.3 BOOT Bus Timing Diagram

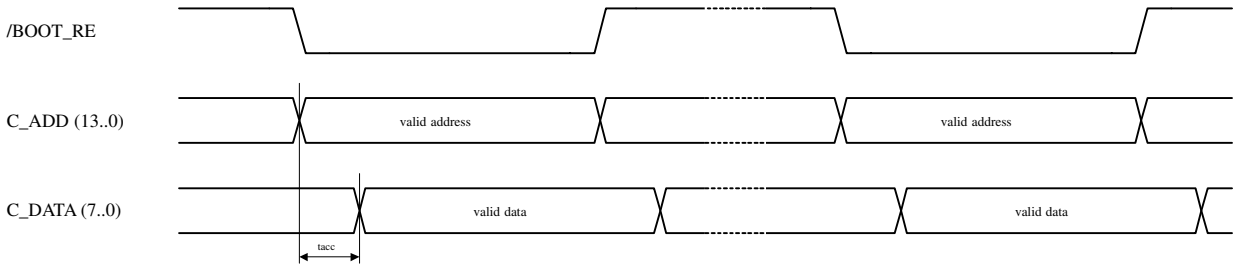


Figure 10. C-bus interface timing diagram

6.5.4 BOOT Bus Timing Parameter

Parameter	Symbol	Min.	Typ.	Max.	Unit
BOOT ROM access time	tacc			120	ns

6.6 SRAM Interface

6.6.1 SRAM Interface Signal Description

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
100	70	SRAM_D7	SRAM data bit 7	PRB04TZ	inout	x
101	71	SRAM_D6	SRAM data bit 6	PRB04TZ	inout	x
103	72	SRAM_D5	SRAM data bit 5	PRB04TZ	inout	x
104	73	SRAM_D4	SRAM data bit 4	PRB04TZ	inout	x
106	74	SRAM_D3	SRAM data bit 3	PRB04TZ	inout	x
107	75	SRAM_D2	SRAM data bit 2	PRB04TZ	inout	x
109	76	SRAM_D1	SRAM data bit 1	PRB04TZ	inout	x
110	77	SRAM_D0	SRAM data bit 0	PRB04TZ	inout	x
112	78	SRAM_WR	SRAM write signal	PRO04T	out	
113	79	SRAM_OE	SRAM output enable	PRO04T	out	
114	80	SRAM_A18	SRAM address bit 18	PRO04T	out	
116	81	SRAM_A17	SRAM address bit 17	PRO04T	out	
117	82	SRAM_A16	SRAM address bit 16	PRO04T	out	
119	83	SRAM_A15	SRAM address bit 15	PRO04T	out	
120	84	SRAM_A14	SRAM address bit 14	PRO04T	out	
123	86	SRAM_A13	SRAM address bit 13	PRO04T	out	
124	87	SRAM_A12	SRAM address bit 12	PRO04T	out	
126	88	SRAM_A11	SRAM address bit 11	PRO04T	out	
127	89	SRAM_A10	SRAM address bit 10	PRO04T	out	
129	90	SRAM_A9	SRAM address bit 9	PRO04T	out	
130	91	SRAM_A8	SRAM address bit 8	PRO04T	out	
132	92	SRAM_A7	SRAM address bit 7	PRO04T	out	
133	93	SRAM_A6	SRAM address bit 6	PRO04T	out	
136	95	SRAM_A5	SRAM address bit 5	PRO04T	out	
137	96	SRAM_A4	SRAM address bit 4	PRO04T	out	
139	97	SRAM_A3	SRAM address bit 3	PRO04T	out	
140	98	SRAM_A2	SRAM address bit 2	PRO04T	out	
142	99	SRAM_A1	SRAM address bit 1	PRO04T	out	
143	100	SRAM_A0	SRAM address bit 0	PRO04T	out	

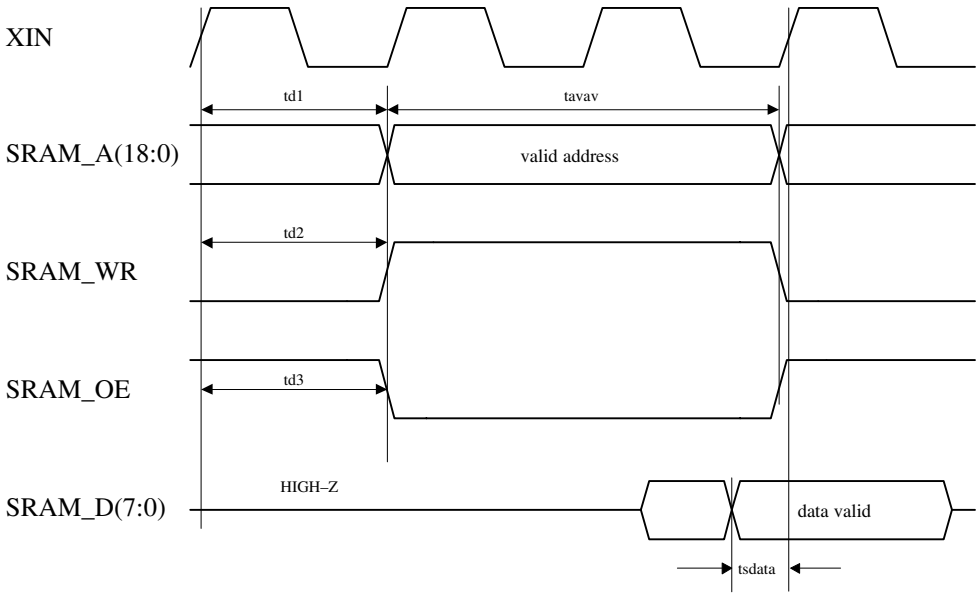
6.6.2 SRAM Interface Descriptions

For time de-interleaving and further task an external static random access memory of 4 MB is necessary. The organization of the SRAM is 512 k × 8 bit.

Due to the high data rates a fast SRAM with a access time of 18 ns or below is necessary.

6.6.3 SRAM Interface Timing Diagram

READ CYCLE



WRITE CYCLE

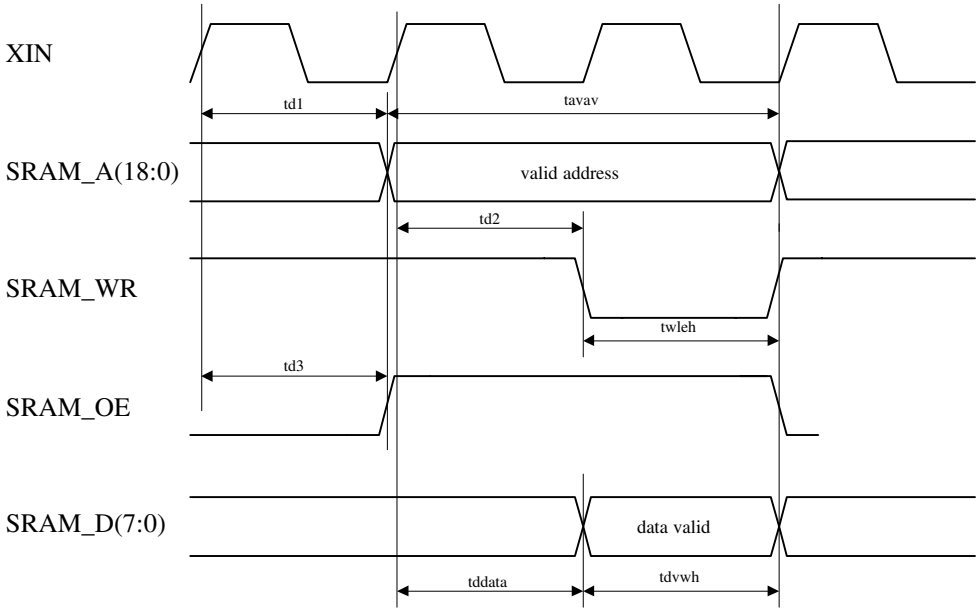


Figure 11. SRAM interface timing diagram

6.6.4 SRAM Interface Timing Parameter

Parameter	Symbol	Min.	Typ.	Max.	Unit
Read/ write cycle time	tavav		40.7		ns
Output delay SRAM_A(18:0)	td1	15.0	25.0	35.0	ns
Output delay SRAM_WR	td2	12.0	20.0	28.0	ns
Output delay SRAM_OE	td3	16.0	24.0	32.0	ns
Setup time SRAM_D(7:0)	tsdata	2.0			ns
Write pulse with	twleh	33.0	40.7	48.0	ns
Output delay SRAM_D(7:0)	tddata	15.0	23.0	31.0	ns
Data valid to end of write	tdvwh	33.0	40.7	48.0	ns

6.7 VCXO Interface

6.7.1 VCXO Interface Signal Description

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
19	13	AVSS1	Analog ground	PVSS3Z	gnd	x
20	14	XIN	Oscillator input	PDX02	osc	
21	15	XOUT	Oscillator output	(PDX02)	osc	
22	16	AVDD1	Analog power supply	PVDD3Z	pwr	
25	18	PWM	Pulse width modulated control output	PRO04T	out	

6.7.2 VCXO Interface Description

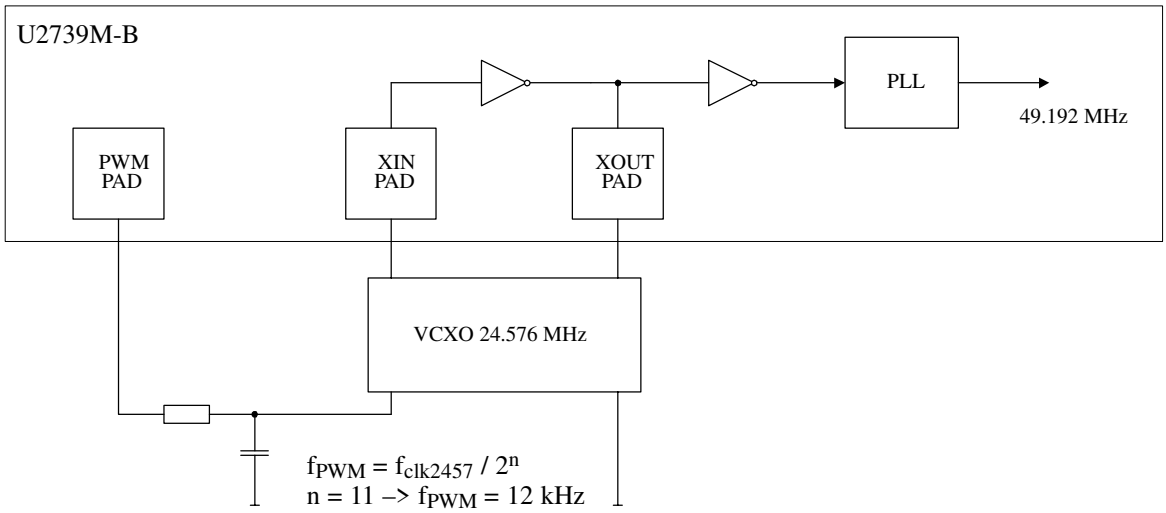


Figure 12. VCXO application circuit

The U2739M-B master clock should be derived from a voltage-controlled reference oscillator. The pulse width modulated output signal PWM of the U2739M-B can be used to control the VCXO frequency of 24.576 MHz.

6.8 Audio Interfaces

6.8.1 I2S Interface Signal Description

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
79	56	I2S_CLK	I2S clock line	PRO04T	out	
80	57	I2S_DAT	I2S data line	PRO04T	out	
82	58	I2S_WIN	I2S window line	PRO04T	out	

6.8.2 I2S Interface Description

The I2S interface is a standard continuous audio interface consisting of bit clock (_CLK), word select (_WIN) and data (_DAT) lines. The word select line indicates the transmitted channel: LOW for left, HIGH for right. Please be aware of the 1 cycle delay of the data word MSB corresponding to the I2S_WIN edge !

As in the DAB system the I2S_WIN clock is fixed as 48 kHz (MPEG1) or 24 kHz (MPEG2) the bit clock depends on the data word length. The standard word length is 16 bit, hence the bit clock is fixed at 1.536 MHz resp. 768 kHz.

6.8.3 I2S Interface Timing Diagram

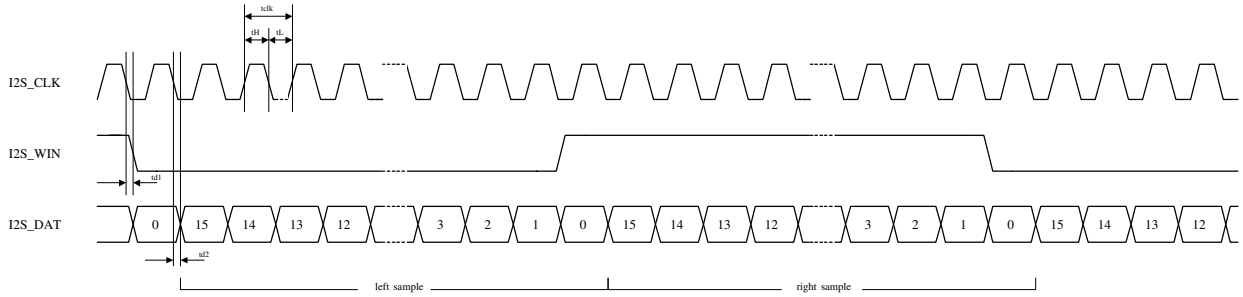


Figure 13. I2S interface timing diagram

6.8.4 I2S Interface Timing Parameter

Parameter	Symbol	Min.	Typ.	Max.	Unit
I2S clock period	tclk		16.28		us
I2S clock high	tH		14.28		us
I2S clock low	tL		14.28		us
I2S_WIN output delay	td1	–5.0	0.0	5.0	ns
I2S_DAT output delay	td2	–5.0	0.0	5.0	ns

6.8.5 SP-DIF Interface Signal Description

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
77	54	SPDIF	SPDIF output	PRO04T	out	

6.8.6 SP-DIF Interface Description

The SP-DIF format is frame based, which means one frame represents one audio sampling period. Every frame comprises 2 subframes a 32 bit referring to the left and right sample. The data is transmitted in bi-phase coded format. The frame synchronization pattern are based on biphase violations and indicate whether a left or right subframe follows.

The last 4 bi-phase coded bits of each subframe represent the V (validity flag), U (user channel data), C (channel status data) and P (parity) information as described in the SP-DIF specification.

Complete frames (left and right sample according to 64 × 2 bit due to bi-phase coding) are transmitted at the audio sampling rate (48 resp. 24 kHz).

6.8.7 SP-DIF Interface Timing Parameter

The SP-DIF interface was designed according the digital audio interface IEC958 specification [CEI/ISO 958 Digital Audio Interface Standard].

6.8.8 SP-DIF Interface Timing Diagram

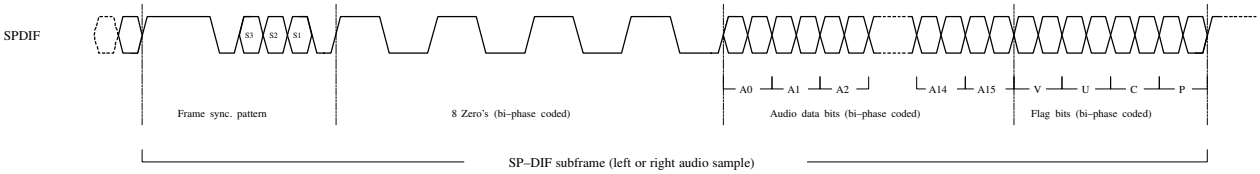


Figure 14. SP-DIF interface timing diagram

6.9 RDI Interface

6.9.1 RDI Interface Signal Description

QFP144	QFP100	Pin Name	Signal Description	Pad Type	Dir.	5 V Tol.
64	46	C_DATA5/RDI_VBIT	C–bus data bit 5 (pull down)	PRD04TZ	inout	x
85	60	RDI_RX	RDI receive data	PDIZ	in	x
86	61	RDI_TX	RDI transmit data	PRO04T	out	

6.9.2 RDI Interface Description

The RDI interface is designed according to the 'Digital Audio Broadcasting System: Specification of the Receiver Data Interface (RDI)' [Digital Audio Broadcasting System: Specification of the Receiver Data Interface (RDI), Issue 1.4]. The RDI frames are embedded into the IEC 958 interface. The RDI output data is provided in the extended format of the high capacity mode. Further the RDI Control Channel (RCC) can be implemented according to the preliminary specification [Digital Audio Broadcasting System: Preliminary Specification of the RDI Control Channel], [Proposal of DAB Command Set for Receiver (DCSR)].

6.9.3 RDI Interface Timing Diagram

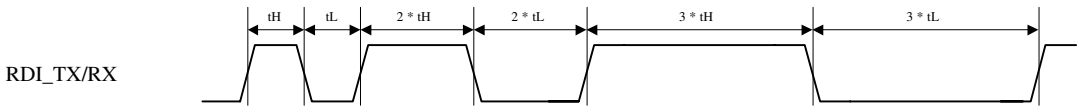


Figure 15. RDI interface timing diagram