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Features

- **Minimal External Circuitry Requirements, No RF Components on the PC Board Except Matching to the Receiver Antenna**
- **High Sensitivity, Especially at Low Data Rates**
- **Sensitivity Reduction Possible Even While Receiving**
- **Fully Integrated VCO**
- **Low Power Consumption Due to Configurable Self Polling with a Programmable Time Frame Check**
- **Supply Voltage 4.5 V to 5.5 V**
- **Operating Temperature Range -40°C to 105°C**
- **Single-ended RF Input for Easy Adaptation to λ/4 Antenna or Printed Antenna on PCB**
- **Low-cost Solution Due to High Integration Level**
- **ESD Protection According to MIL-STD 883 (4KV HBM) Except Pin POUT (2KV HBM)**
- **High Image Frequency Suppression due to 1 MHz IF in Conjunction with a SAW Front-end Filter**
  - **Up to 40 dB is Thereby Achievable with Newer SAWs.**
- **Programmable Output Port for Sensitivity Selection or for Controlling External Periphery**
- **Communication to the Microcontroller Possible via a Single, Bi-directional Data Line**
- **Power Management (Polling) is also Possible by Means of a Separate Pin via the Microcontroller**
- **2 Different IF Bandwidth Versions are Available (300 kHz and 600 kHz)**

Description

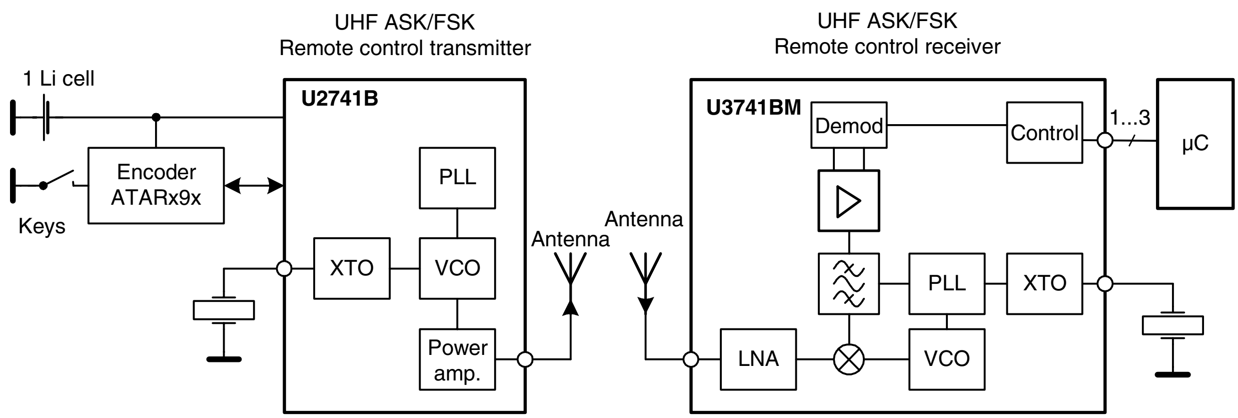
The U3741BM is a multi-chip PLL receiver device supplied in an SO20 package. It has been specially developed for the demands of RF low-cost data transmission systems with low data rates from 1 kBaud to 10 kBaud (1 kBaud to 3.2 kBaud for FSK) in Manchester or Bi-phase code. The receiver is well suited to operate with Atmel's PLL RF transmitter U2741B. Its main applications are in the areas of telemetering, security technology and keyless-entry systems. It can be used in the frequency receiving range of f_0 = 300 MHz to 450 MHz for ASK or FSK data transmission. All the statements made below refer to 433.92-MHz and 315-MHz applications.

UHF ASK Receiver IC

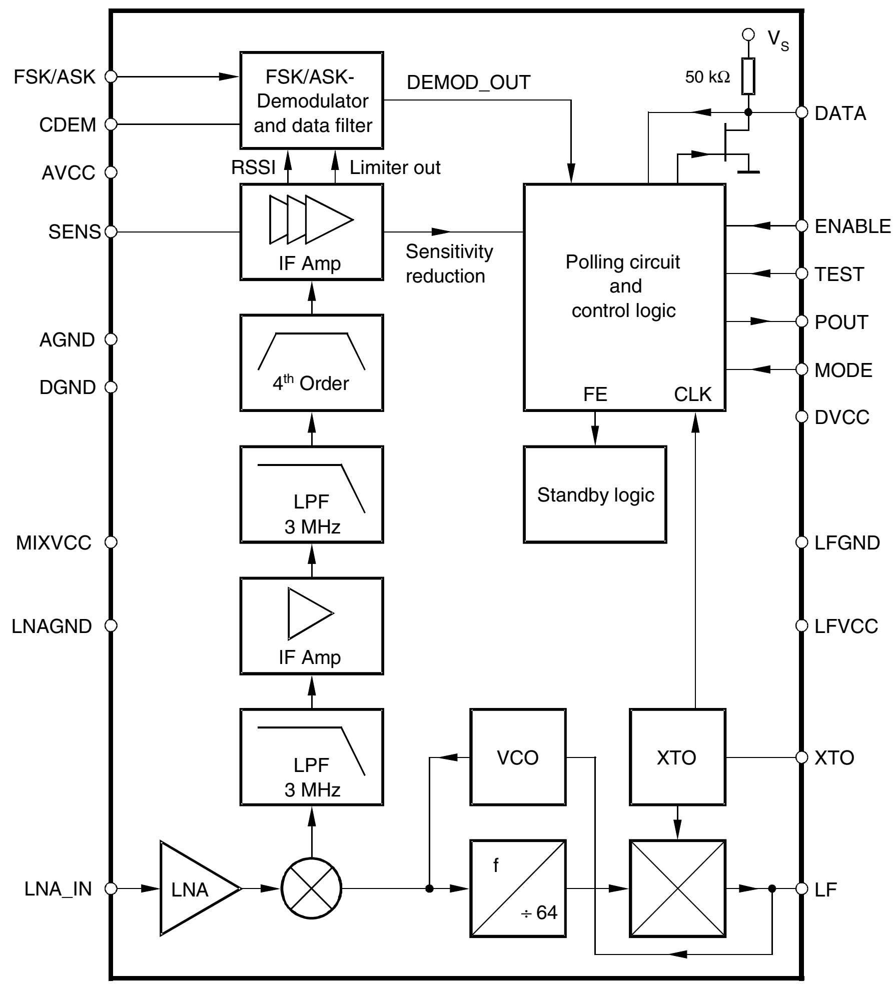
U3741BM

Rev. 4662B–RKE–10/04

System Block Diagram

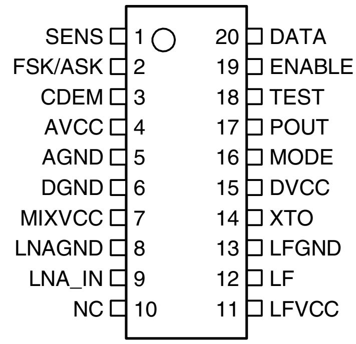


Block Diagram



Pin Configuration

Figure 1. Pinning SO20



Pin Description

Pin	Symbol	Function
1	SENS	Sensitivity-control resistor
2	FSK/ASK	Selecting FSK/ASK. Low: FSK, High: ASK
3	CDEM	Lower cut-off frequency data filter
4	AVCC	Analog power supply
5	AGND	Analog ground
6	DGND	Digital ground
7	MIXVCC	Power supply mixer
8	LNAGND	High-frequency ground LNA and mixer
9	LNA_IN	RF input
10	NC	Not connected
11	LFVCC	Power supply VCO
12	LF	Loop filter
13	LFGND	Ground VCO
14	XTO	Crystal oscillator
15	DVCC	Digital power supply
16	MODE	Selecting 433.92 MHz/315 MHz. Low: 4.90625 MHz (USA). High: 6.76438 (Europe)
17	POUT	Programmable output port
18	TEST	Test pin, during operation at GND
19	ENABLE	Enables the polling mode Low: polling mode off (sleep mode) H: polling mode on (active mode)
20	DATA	Data output/configuration input

RF Front End

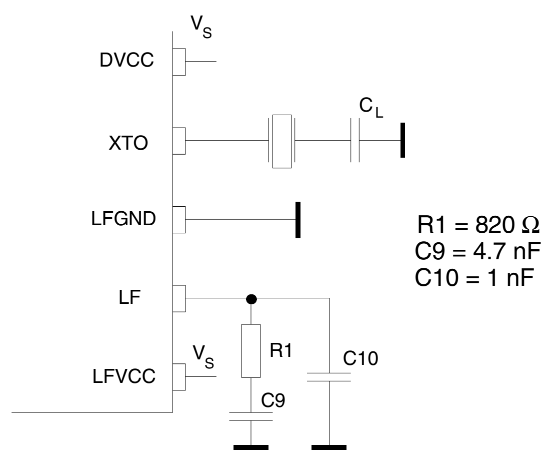
The RF front end of the receiver is a heterodyne configuration that converts the input signal into a 1-MHz IF signal. According to the block diagram, the front end consists of an LNA (low noise amplifier), LO (local oscillator), a mixer and RF amplifier.

The LO generates the carrier frequency for the mixer via a PLL synthesizer. The XTO (crystal oscillator) generates the reference frequency f_{XTO}. The VCO (voltage-controlled oscillator) generates the drive voltage frequency f_{LO} for the mixer. f_{LO} is dependent on the voltage at pin LF. f_{LO} is divided by a factor of 64. The divided frequency is compared to f_{XTO} by the phase frequency detector. The current output of the phase frequency detector is connected to a passive loop filter and thereby generates the control voltage V_{LF} for the VCO. By means of that configuration, V_{LF} is controlled in a way that $f_{LO}/64$ is equal to f_{XTO}. If f_{LO} is determined, f_{XTO} can be calculated using the following formula:

$$f_{XTO} = \frac{f_{LO}}{64}$$

The XTO is a one-pin oscillator that operates at the series resonance of the quartz crystal. According to Figure 2, the crystal should be connected to GND via a capacitor CL. The value of that capacitor is recommended by the crystal supplier. The value of CL should be optimized for the individual board layout to achieve the exact value of f_{XTO} and hereby of f_{LO}. When designing the system in terms of receiving bandwidth, the accuracy of the crystal and XTO must be considered.

Figure 2. PLL Peripherals



The passive loop filter connected to pin LF is designed for a loop bandwidth of B_{Loop} = 100 kHz. This value for B_{Loop} exhibits the best possible noise performance of the LO. Figure 2 shows the appropriate loop filter components to achieve the desired loop bandwidth. If the filter components are changed for any reason, please note that the maximum capacitive load at pin LF is limited. If the capacitive load is exceeded, a bit check may no longer be possible since f_{LO} cannot settle in time before the bit check starts to evaluate the incoming data stream. Therefore, self polling also does not work in that case.

f_{LO} is determined by the RF input frequency f_{RF} and the IF frequency f_{IF} using the following formula:

$$f_{LO} = f_{RF} - f_{IF}$$

To determine f_{LO}, the construction of the IF filter must be considered at this point. The nominal IF frequency is f_{IF} = 1 MHz. To achieve a good accuracy of the filter's corner frequencies, the filter is tuned by the crystal frequency f_{XTO}. This means that there is a fixed relation between f_{IF} and f_{LO} that depends on the logic level at pin mode. This is described by the following formulas:

$$\text{MODE} = 0 \text{ (USA) } f_{IF} = \frac{f_{LO}}{314}$$

$$\text{MODE} = 0 \text{ (Europe) } f_{IF} = \frac{f_{LO}}{432.92}$$

The relation is designed to achieve the nominal IF frequency of f_{IF} = 1 MHz for most applications. For applications where f_{RF} = 315 MHz, the MODE must be set to '0'. In the case of f_{RF} = 433.92 MHz, the MODE must be set to '1'. For other RF frequencies, f_{IF} is not equal to 1 MHz. f_{IF} is then dependent on the logical level at pin MODE and on f_{RF}. Table 1 summarizes the different conditions.

The RF input either from an antenna or from a generator must be transformed to the RF input pin LNA_IN. The input impedance of that pin is provided in the electrical parameters. The parasitic board inductances and capacitances also influence the input matching. The RF receiver U3741BM exhibits its highest sensitivity at the best signal-to-noise ratio in the LNA. Hence, noise matching is the best choice for designing the transformation network.

A good practice when designing the network is to start with power matching. From that starting point, the values of the components can be varied to some extent to achieve the best sensitivity.

If a SAW is implemented into the input network, a mirror frequency suppression of ΔP_{Ref} = 40 dB can be achieved. There are SAWs available that exhibit a notch at Δf = 2 MHz. These SAWs work best for an intermediate frequency of IF = 1 MHz. The selectivity of the receiver is also improved by using a SAW. In typical automotive applications, a SAW is used.

Figure 3 on page 6 shows a typical input matching network for f_{RF} = 315 MHz and f_{RF} = 433.92 MHz using a SAW. Figure 4 on page 6 illustrates an input matching to 50 Ω without a SAW. The input matching networks shown in Figure 4 are the reference networks for the parameters given in the "Electrical Characteristics".

Table 1. Calculation of LO and IF Frequency

Conditions	Local Oscillator Frequency	Intermediate Frequency
f_{RF} = 315 MHz, MODE = 0	f_{LO} = 314 MHz	f_{IF} = 1 MHz
f_{RF} = 433.92 MHz, MODE = 1	f_{LO} = 432.92 MHz	f_{IF} = 1 MHz
300 MHz < f_{RF} < 365 MHz, MODE = 0	$f_{LO} = \frac{f_{RF}}{1 + \frac{1}{314}}$	$f_{IF} = \frac{f_{LO}}{314}$
365 MHz < f_{RF} < 450 MHz, MODE = 1	$f_{LO} = \frac{f_{RF}}{1 + \frac{1}{432.92}}$	$f_{IF} = \frac{f_{LO}}{432.92}$

Figure 3. Input Matching Network with SAW Filter

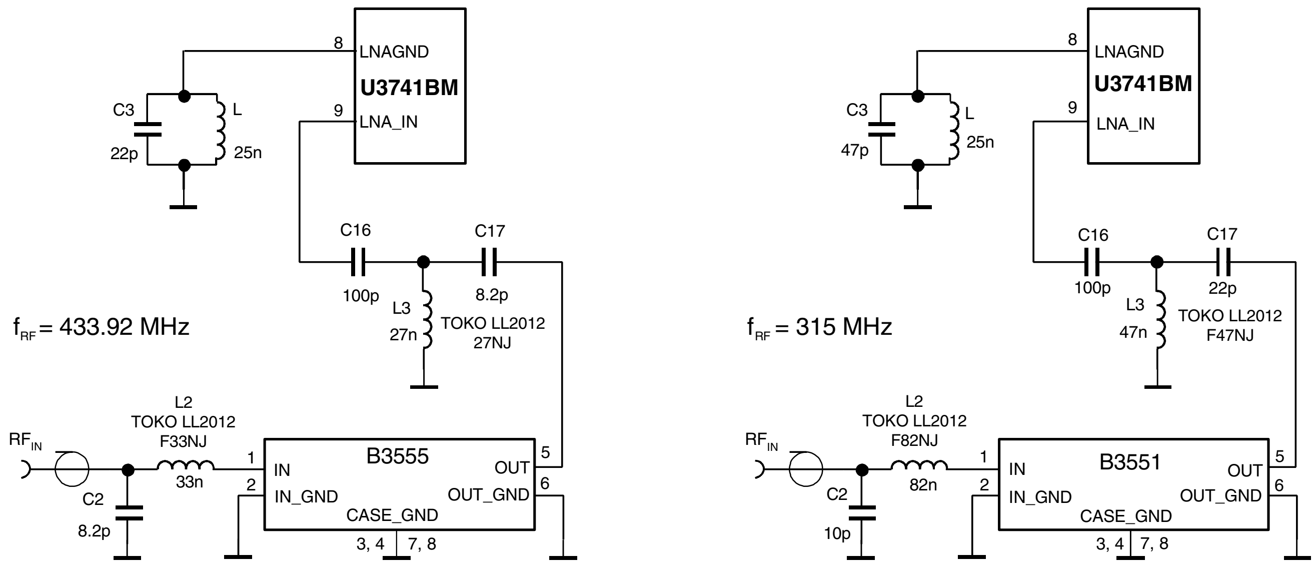
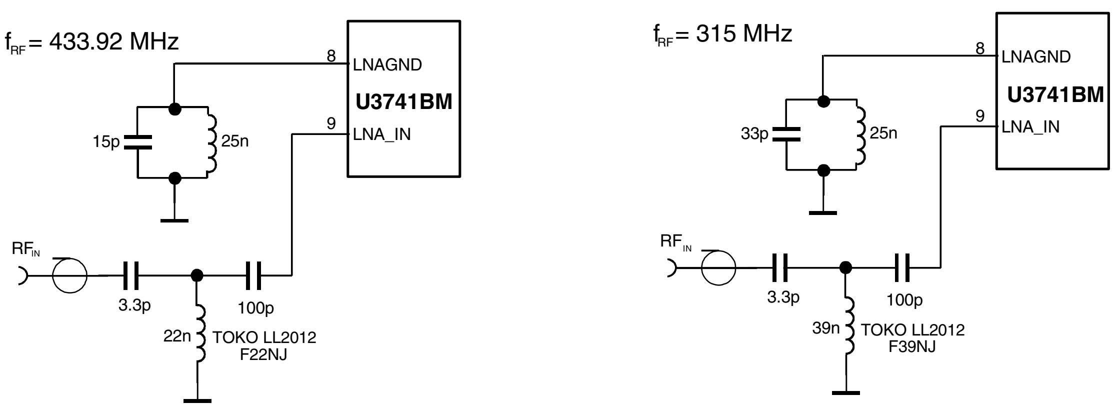


Figure 4. Input Matching Network without SAW Filter



Please note that for all coupling conditions (see Figure 3 and Figure 4), the bond wire inductivity of the LNA ground is compensated. C3 forms a series resonance circuit together with the bond wire. L = 25 nH is a feed inductor to establish a DC path. Its value is not critical but must be large enough not to detune the series resonance circuit. For cost reduction, this inductor can be easily printed on the PCB. This configuration improves the sensitivity of the receiver by about 1 dB to 2 dB.

Analog Signal Processing

IF Amplifier

The signals coming from the RF front end are filtered by the fully integrated 4th-order IF filter. The IF center frequency is f_{IF} = 1 MHz for applications where f_{RF} = 315 MHz or f_{RF} = 433.92 MHz is used. For other RF input frequencies, refer to Table 1 to determine the center frequency.

The U3741BM is available with 2 different IF bandwidths. U3741BM-M2, the version with B_{IF} = 300 kHz, is well suited for ASK systems where Atmel's PLL transmitter U2741B is used. The receiver U3741BM-M3 employs an IF bandwidth of B_{IF} = 600 kHz. This version can be used together with the U2741B in FSK and ASK mode. If used in ASK applications, it allows higher tolerances for the receiver and PLL transmitter crystals. SAW transmitters exhibit much higher transmit frequency tolerances compared to PLL transmitters. Generally, it is necessary to use B_{IF} = 600 kHz together with such transmitters.

RSSI Amplifier

The subsequent RSSI amplifier enhances the output signal of the IF amplifier before it is fed into the demodulator. The dynamic range of this amplifier is DR_{RSSI} = 60 dB. If the RSSI amplifier is operated within its linear range, the best S/N ratio is maintained in ASK mode. If the dynamic range is exceeded by the transmitter signal, the S/N ratio is defined by the ratio of the maximum RSSI output voltage and the RSSI output voltage due to a disturber. The dynamic range of the RSSI amplifier is exceeded if the RF input signal is about 60 dB higher compared to the RF input signal at full sensitivity.

In FSK mode, the S/N ratio is not affected by the dynamic range of the RSSI amplifier.

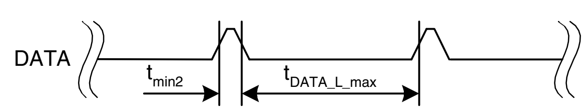
The output voltage of the RSSI amplifier is internally compared to a threshold voltage VTh_red. VTh_red is determined by the value of the external resistor R_{Sense}. R_{Sense} is connected between pin Sense and GND or VS. The output of the comparator is fed into the digital control logic. By this means it is possible to operate the receiver at lower sensitivity.

If R_{Sense} is connected to VS, the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of R_{Sense}, the maximum sensitivity by the signal-to-noise ratio of the LNA input. The reduced sensitivity is dependent on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is illustrated in Figure 4 on page 6 and exhibits the best possible sensitivity.

R_{Sense} can be connected to VS or GND via a microcontroller or by the digital output port POUT of the U3741BM receiver IC. The receiver can be switched from full sensitivity to reduced sensitivity or vice versa at any time. In polling mode, the receiver will not wake up if the RF input signal does not exceed the selected sensitivity. If the receiver is already active, the data stream at pin DATA will disappear when the input signal is lower than defined by the reduced sensitivity. Instead of the data stream, the pattern according to Figure 5 is issued at pin DATA to indicate that the receiver is still active.

Figure 5. Steady L State Limited DATA Output Pattern



FSK/ASK Demodulator and Data Filter

The signal coming from the RSSI amplifier is converted into the raw data signal by the ASK/FSK demodulator. The operating mode of the demodulator is set via pin ASK/FSK. Logic 'L' sets the demodulator to FSK, Logic 'H' sets it into ASK mode.

In ASK mode an automatic threshold control circuit (ATC) is employed to set the detection reference voltage to a value where a good signal-to-noise ratio is achieved. This circuit also implies the effective suppression of any kind of in-band noise signals or competing transmitters. If the S/N ratio exceeds 10 dB, the data signal can be detected properly.

The FSK demodulator is intended to be used for an FSK deviation of $\Delta f \geq 20$ kHz. Lower values may be used but the sensitivity of the receiver is reduced in that condition. The minimum usable deviation is dependent on the selected baud rate. In FSK mode, only BR_Range0 and BR_Range1 are available. In FSK mode, the data signal can be detected if the S/N Ratio exceeds 2 dB.

The output signal of the demodulator is filtered by the data filter before it is fed into the digital signal processing circuit. The data filter improves the S/N ratio as its bandpass can be adopted to the characteristics of the data signal. The data filter consists of a 1st-order high-pass and a 1st-order low-pass filter.

The high-pass filter cut-off frequency is defined by an external capacitor connected to pin CDEM. The cut-off frequency of the high-pass filter is defined by the following formula:

$$f_{cu\_DF} = \frac{1}{2 \times \pi \times 30\ k\Omega \times CDEM}$$

In self-polling mode, the data filter must settle very rapidly to achieve a low current consumption. Therefore, CDEM cannot be increased to very high values if self polling is used. On the other hand, CDEM must be large enough to meet the data filter requirements according to the data signal. Recommended values for CDEM are given in the "Electrical Characteristics" on page 23. The values are slightly different for ASK and FSK mode.

The cut-off frequency of the low-pass filter is defined by the selected baud rate range (BR_Range). BR_Range is defined in the OPMODE register (refer to section "Configuration of the Receiver" on page 17). BR_Range must be set in accordance to the used baud rate.

The U3741BM is designed to operate with data coding where the DC level of the data signal is 50%. This is valid for Manchester and Bi-phase coding. If other modulation schemes are used, the DC level should always remain within the range of VDC_min = 33% and VDC_max = 66%. The sensitivity may be reduced by up to 1.5 dB in that condition.

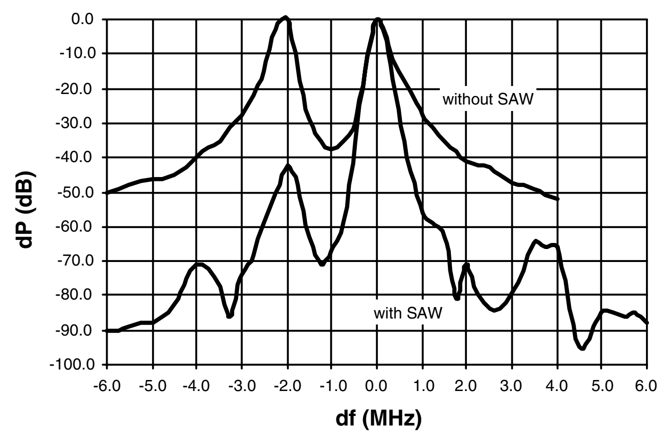
Each BR_Range is also defined by a minimum and a maximum edge-to-edge time (tee_sig). These limits are defined in the "Electrical Characteristics" on page 23. They should not be exceeded to maintain full sensitivity of the receiver.

Receiving Characteristics

The RF receiver U3741BM can be operated with and without a SAW front-end filter. In a typical automotive application, a SAW filter is used to achieve better selectivity. The selectivity with and without a SAW front end-filter is illustrated in Figure 6. This example relates to ASK mode and the 300-kHz bandwidth version of the U3741BM. FSK mode and the 600-kHz version of the receiver exhibit similar behavior. Note that the mirror frequency is reduced by 40 dB. The plots are printed relative to the maximum sensitivity. If a SAW filter is used, an insertion loss of about 4 dB must be considered.

When designing the system in terms of receiving bandwidth, the LO deviation must be considered as it also determines the IF center frequency. The total LO deviation is calculated to be the sum of the deviation of the crystal and the XTO deviation of the U3741BM. Low-cost crystals are specified to be within ±100 ppm. The XTO deviation of the U3741BM is an additional deviation due to the XTO circuit. This deviation is specified to be ±30 ppm. If a crystal of ±100 ppm is used, the total deviation is ±130 ppm in that case. Note that the receiving bandwidth and the IF-filter bandwidth are equivalent in ASK mode but not in FSK mode.

Figure 6. Receiving Frequency Response



Polling Circuit and Control Logic

The receiver is designed to consume less than 1 mA while being sensitive to signals from a corresponding transmitter. This is achieved via the polling circuit. This circuit enables the signal path periodically for a short time. During this time the bit check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected the receiver remains active and transfers the data to the connected microcontroller. If there is no valid signal present, the receiver is in sleep mode most of the time resulting in low current consumption. This condition is called polling mode. A connected microcontroller is disabled during that time.

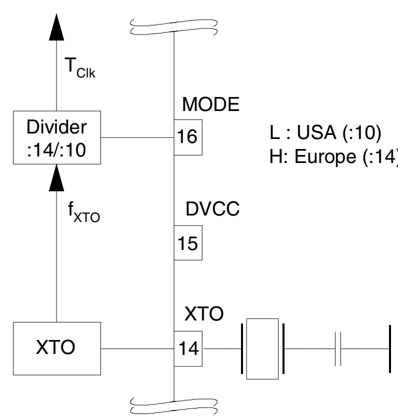
All relevant parameters of the polling logic can be configured by the connected microcontroller. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate etc.

Regarding the number of connection wires to the microcontroller, the receiver is very flexible. It can be either operated by a single bi-directional line to save ports to the connected microcontroller, it can be operated by up to three uni-directional ports.

Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry and the analog filtering is derived from one clock. According to Figure 7, this clock cycle T_{Clk} is derived from the crystal oscillator (XTO) in combination with a divider. The division factor is controlled by the logical state at pin MODE. According to section “RF Front End” on page 4, the frequency of the crystal oscillator (f_{XTO}) is defined by the RF input signal (f_{RFin}) which also defines the operating frequency of the local oscillator (f_{LO}).

Figure 7. Generation of the Basic Clock Cycle



Pin MODE can now be set in accordance with the desired clock cycle T_{Clk}. T_{Clk} controls the following application-relevant parameters:

- Timing of the polling circuit including bit check
- Timing of analog and digital signal processing
- Timing of register programming
- Frequency of the reset marker
- F filter center frequency (f_{IF0})

Most applications are dominated by two transmission frequencies: f_{Send} = 315 MHz is mainly used in the USA, f_{Send} = 433.92 MHz in Europe. In order to ease the usage of all T_{Clk}-dependent parameters, the electrical characteristics display three conditions for each parameter.

- USA Applications
  (f_{XTO} = 4.90625 MHz, MODE = L, T_{Clk} = 2.0383 µs)
- Europe Applications
  (f_{XTO} = 6.76438 MHz, MODE = H, T_{Clk} = 2.0697 µs)
- Other applications
  (T_{Clk} is dependent on f_{XTO} and on the logical state of pin MODE. The electrical characteristic is given as a function of T_{Clk}).

The clock cycle of some function blocks depends on the selected baud rate range (BR_Range) which is defined in the OPMODE register. This clock cycle T_{XClk} is defined by the following formulas for further reference:

BR_Range =	BR_Range0:	$T_{XClk} = 8 \times T_{Clk}$
	BR_Range1:	$T_{XClk} = 4 \times T_{Clk}$
	BR_Range2:	$T_{XClk} = 2 \times T_{Clk}$
	BR_Range3:	$T_{XClk} = 1 \times T_{Clk}$

Polling Mode

According to Figure 3 on page 6, the receiver stays in polling mode in a continuous cycle of three different modes. In sleep mode, the signal processing circuitry is disabled for the time period T_{Sleep} while consuming a low current of $I_S = I_{Soff}$. During the start-up period, $T_{Startup}$, all signal processing circuits are enabled and settled. In the following bit check mode, the incoming data stream is analyzed bit by bit against a valid transmitter signal. If no valid signal is present, the receiver is set back to sleep mode after the period $T_{Bitcheck}$. This period varies check by check as it is a statistical process. An average value for $T_{Bitcheck}$ is given in "Electrical Characteristics" on page 23. During $T_{Startup}$ and $T_{Bitcheck}$ the current consumption is $I_S = I_{Son}$. The average current consumption in polling mode is dependent on the duty cycle of the active mode and can be calculated as:

$$I_{Spoll} = \frac{I_{Soff} \times T_{Sleep} + I_{Son} \times (T_{Startup} + T_{Bitcheck})}{T_{Sleep} + T_{Startup} + T_{Bitcheck}}$$

During T_{Sleep} and $T_{Startup}$, the receiver is not sensitive to a transmitter signal. To guarantee the reception of a transmitted command, the transmitter must start the telegram with an adequate preburst. The required length of the preburst is dependent on the polling parameters T_{Sleep}, $T_{Startup}$, $T_{Bitcheck}$ and the startup time of a connected microcontroller ($T_{Start,\mu C}$). $T_{Bitcheck}$ thus depends on the actual bit rate and the number of bits ($N_{Bitcheck}$) to be tested.

The following formula indicates how to calculate the preburst length.

$$T_{Preburst} \geq T_{Sleep} + T_{Startup} + T_{Bitcheck} + T_{Start\_\mu C}$$

Sleep Mode

The length of period T_{Sleep} is defined by the 5-bit word Sleep of the OPMODE register, the extension factor X_{Sleep}, according to Figure 10 on page 13, and the basic clock cycle T_{Clk}. It is calculated to be:

$$T_{Sleep} = Sleep \times X_{Sleep} \times 1024 \times T_{Clk}$$

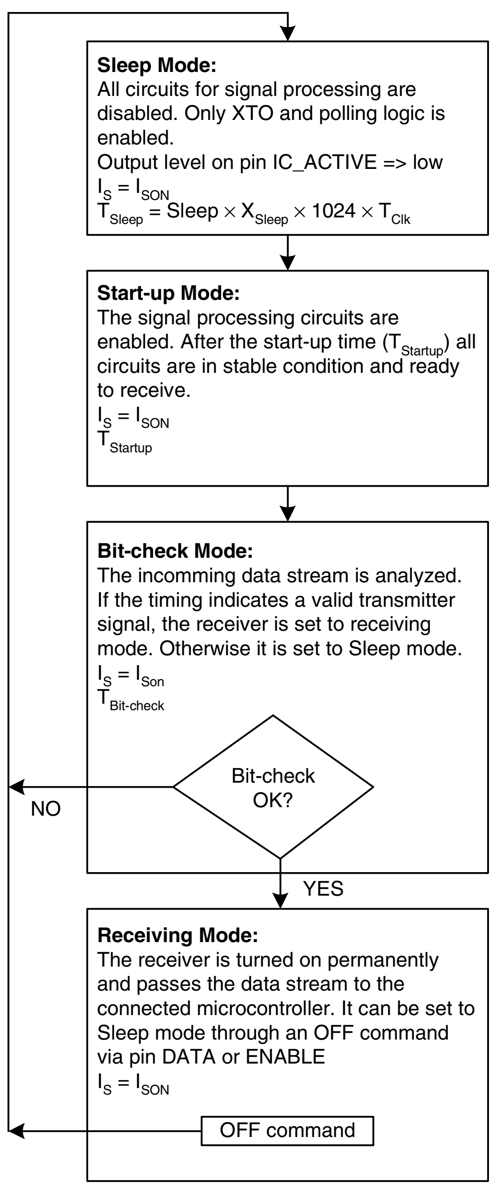
In US and European applications, the maximum value of T_{Sleep} is about 60 ms if X_{Sleep} is set to 1. The time resolution is about 2 ms in that case. The sleep time can be extended to almost half a second by setting X_{Sleep} to 8. X_{Sleep} can be set to 8 by bit $X_{SleepStd}$ or by bit $X_{SleepTemp}$ resulting in a different mode of action as described below:

$X_{SleepStd}$ = 1 implies the standard extension factor. The sleep time is always extended.

$X_{SleepTemp}$ = 1 implies the temporary extension factor. The extended sleep time is used as long as every bit check is OK. If the bit check fails once, this bit is set back to 0 automatically resulting in a regular sleep time. This functionality can be used to save current in presence of a modulated disturber similar to an expected transmitter signal. The connected microcontroller is rarely activated in that condition. If the disturber disappears, the receiver switches back to regular polling and is again sensitive to appropriate transmitter signals.

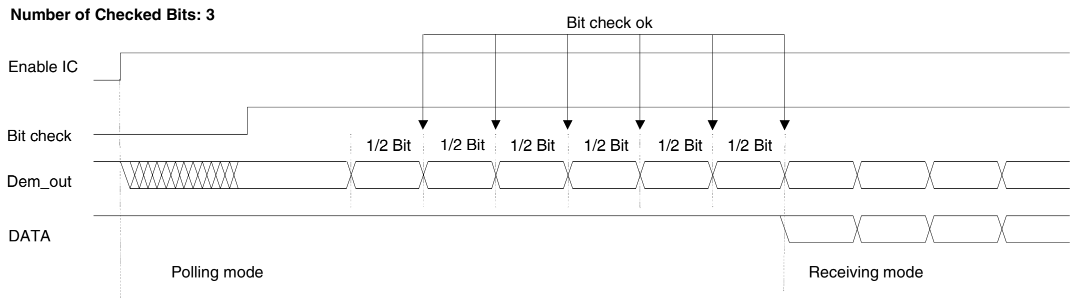
According to Table 7 on page 19, the highest register value of Sleep sets the receiver to a permanent sleep condition. The receiver remains in that condition until another value for Sleep is programmed into the OPMODE register. This function is desirable where several devices share a single data line.

Figure 8. Polling Mode Flow Chart



Sleep:	5-bit word defined by Sleep0 to Sleep4 in OPMODE register
X_{Sleep}:	Extension factor defined by $X_{SleepTemp}$ according to Table 8
T_{Clk}:	Basic clock cycle defined by f_{XTO} and pin MODE
$T_{Startup}$:	Is defined by the selected baud rate range and T_{Clk}. The baud-rate range is defined by Baud0 and Baud1 in the OPMODE register.
$T_{Bit\text{-}check}$:	Depends on the result of the bit check. If the bit check is ok, $T_{Bit\text{-}check}$ depends on the number of bits to be checked ($N_{Bit\text{-}checked}$) and on the utilized data rate. If the bit check fails, the average time period for that check depends on the selected baud-rate range on T_{Clk}. The baud-rate range is defined by Baud0 and Baud1 in the OPMODE register.

Figure 9. Timing Diagram for a Completely Successful Bit Check



Bit Check Mode

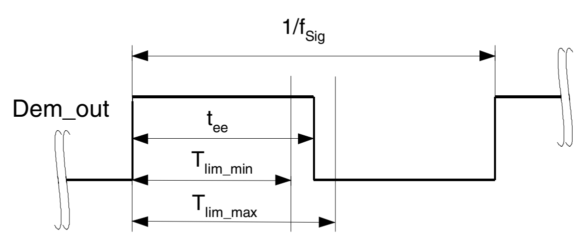
In bit check mode, the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter and signals due to noise. This is done by subsequent time frame checks where the distances between 2 signal edges are continuously compared to a programmable time window. The maximum count of this edge-to-edge test, before the receiver switches to receiving, mode is also programmable.

Configuring the Bit Check

Assuming a modulation scheme that contains 2 edges per bit, two time frame checks are verifying one bit. This is valid for Manchester, Bi-phase and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6 or 9 bits via the variable $N_{Bitcheck}$ in the OPMODE register. This implies 0, 6, 12 and 18 edge-to-edge checks respectively. If $N_{Bitcheck}$ is set to a higher value, the receiver is less likely to switch to the receiving mode due to noise. In the presence of a valid transmitter signal, the bit check takes less time if $N_{Bitcheck}$ is set to a lower value. In polling mode, the bit check time is not dependent on $N_{Bitcheck}$. Figure 9 shows an example where 3 bits are tested successfully and the data signal is transferred to pin DATA.

According to Figure 10, the time window for the bit check is defined by two separate time limits. If the edge-to-edge time t_{ee} is in between the lower bit check limit T_{Lim_min} and the upper bit check limit T_{Lim_max}, the check will be continued. If t_{ee} is smaller than T_{Lim_min} or t_{ee} exceeds T_{Lim_max}, the bit check will be terminated and the receiver switches to sleep mode.

Figure 10. Valid Time Window for Bit Check



For best noise immunity it is recommended to use a low span between T_{Lim_min} and T_{Lim_max}. This is achieved using a fixed frequency at a 50% duty cycle for the transmitter preburst. A '11111...' or a '10101...' sequence in Manchester or Bi-phase is a good choice in this regard. A good compromise between receiver sensitivity and susceptibility to noise is a time window of ±25% regarding the expected edge-to-edge time t_{ee}. Using preburst patterns that contain various edge-to-edge time periods, the bit check limits must be programmed according to the required span.

The bit check limits are determined by means of the formula below:

$T_{Lim\_min} = Lim\_min \times T_{XClk}$
$T_{Lim\_max} = (Lim\_max - 1) \times T_{XClk}$

Lim_min and Lim_max are defined by a 5-bit word each within the LIMIT register.

Using the above formulas, Lim_min and Lim_max can be determined according to the required T_{Lim_min}, T_{Lim_max} and T_{XClk}. The time resolution when defining T_{Lim_min} and T_{Lim_max} is T_{XClk}. The minimum edge-to-edge time t_{ee} ($t_{DATA\_L\_min}$, $t_{DATA\_H\_min}$) is defined according to the section “Receiving Mode” on page 15. Due to this, the lower limit should be set to Lim_min ≥ 10. The maximum value of the upper limit is Lim_max = 63.

Figure 11, Figure 12 and Figure 13 on page 15 illustrate the bit check for the default bit check limits Lim_min = 14 and Lim_max = 24. When the IC is enabled, the signal processing circuits are enabled during $T_{Startup}$. The output of the ASK/FSK demodulator (Dem_out) is undefined during that period. When the bit check becomes active, the bit check counter is clocked with the cycle T_{XClk}.

Figure 11 shows how the bit check proceeds if the bit-check counter value CV_Lim is within the limits defined by Lim_min and Lim_max at the occurrence of a signal edge. In Figure 12, the bit check fails as the value CV_lim is lower than the limit Lim_min. The bit check also fails if CV_Lim reaches Lim_max. This is illustrated in Figure 13 on page 15.

Figure 11. Timing Diagram During Bit Check

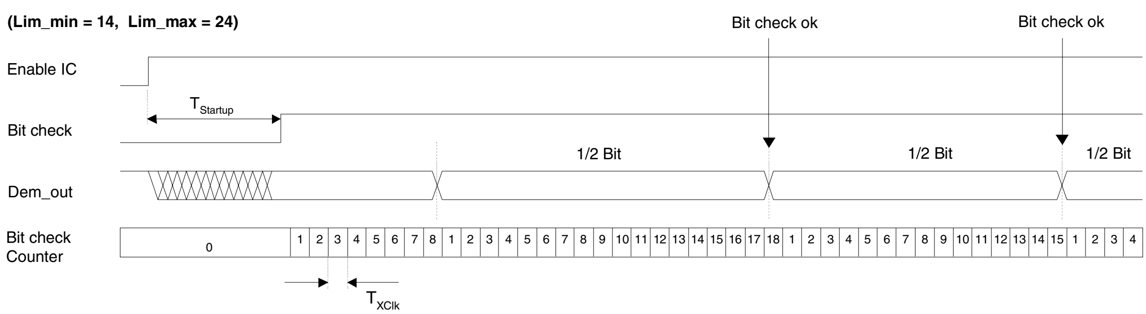


Figure 12. Timing Diagram for Failed Bit Check (Condition: CV_Lim < Lim_min)

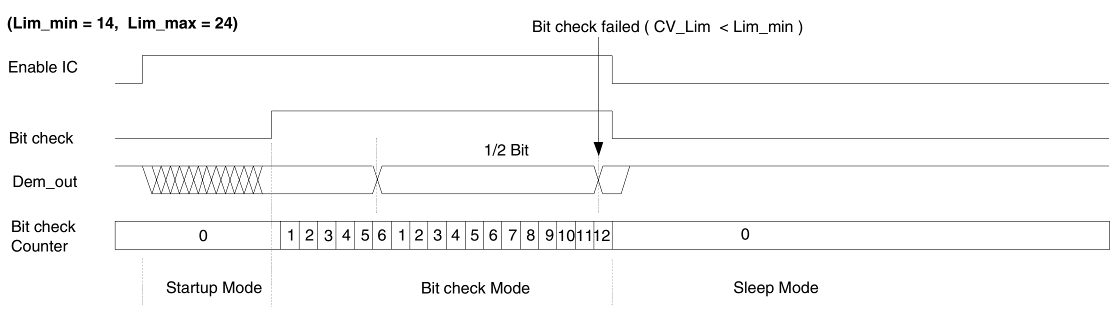
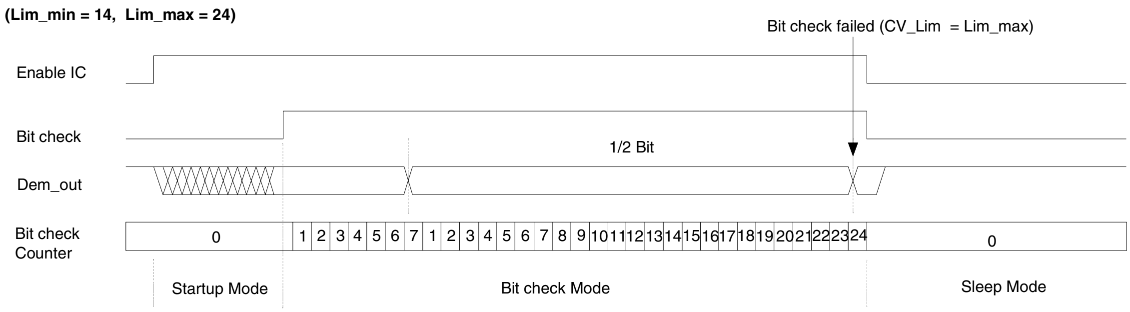


Figure 13. Timing Diagram for Failed Bit Check (Condition: CV_Lim ≥ Lim_max)



Duration of the Bit Check

If no transmitter signal is present during the bit check, the output of the ASK/FSK demodulator delivers random signals. The bit check is a statistical process and $T_{Bitcheck}$ varies for each check. Therefore, an average value for $T_{Bitcheck}$ is given in "Electrical Characteristics". $T_{Bitcheck}$ depends on the selected baud rate range and on T_{Clk}. A higher baudrate range causes a lower value for $T_{Bitcheck}$ resulting in lower current consumption in polling mode.

In the presence of a valid transmitter signal, $T_{Bitcheck}$ is dependant on the frequency of that signal, f_{Sig} and the count of the checked bits, $N_{Bitcheck}$. A higher value for $N_{Bitcheck}$ thereby results in a longer period for $T_{Bitcheck}$ requiring a higher value for the transmitter preburst $T_{Preburst}$.

Receiving Mode

If the bit check has been successful for all bits specified by $N_{Bitcheck}$, the receiver switches to receiving mode. According to Figure 9 on page 13, the internal data signal is switched to pin DATA in that case. A connected microcontroller can be woken up by the negative edge at pin DATA. The receiver stays in that condition until it is switched back to polling mode explicitly.

Digital Signal Processing

The data from the ASK/FSK demodulator (Dem_out) is digitally processed in different ways and as a result converted into the output signal data. This processing depends on the selected baud rate range (BR_Range). Figure 14 on page 16 illustrates how Dem_out is synchronized by the extended clock cycle T_{XClk}. This clock is also used for the bit check counter. Data can change its state only after T_{XClk} elapsed. The edge-to-edge time period t_{ee} of the Data signal as a result is always an integral multiple of T_{XClk}.

The minimum time period between two edges of the data signal is limited to $t_{ee} \geq T_{DATA\_min}$. This implies an efficient suppression of spikes at the DATA output. At the same time, it limits the maximum frequency of edges at DATA. This eases the interrupt handling of a connected microcontroller. T_{DATA_min} is to some extent affected by the preceding edge-to-edge time interval t_{ee} as illustrated in Figure 15. If t_{ee} is in between the specified bit check limits, the following level is frozen for the time period T_{DATA_min} = tmin1, in case of t_{ee} being outside that bit check limits T_{DATA_min} = tmin2 is the relevant stable time period.

The maximum time period for DATA to be low is limited to $T_{DATA\_L\_max}$. This function ensures a finite response time during programming or switching off the receiver via pin DATA. $T_{DATA\_L\_max}$ is thereby longer than the maximum time period indicated by the transmitter data stream. Figure 16 gives an example where Dem_out remains low after the receiver has switched to receiving mode.

Figure 14. Synchronization of the Demodulator Output

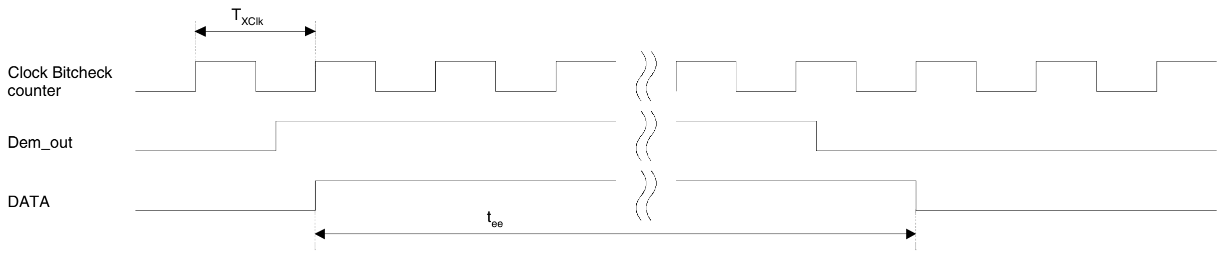


Figure 15. Debouncing of the Demodulator Output

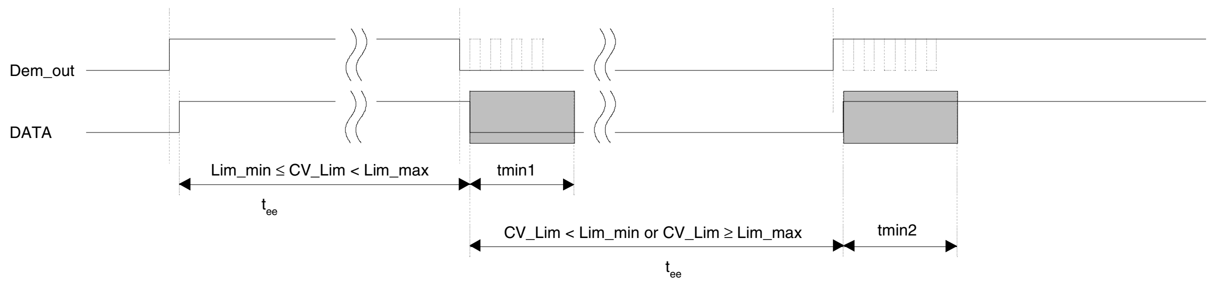
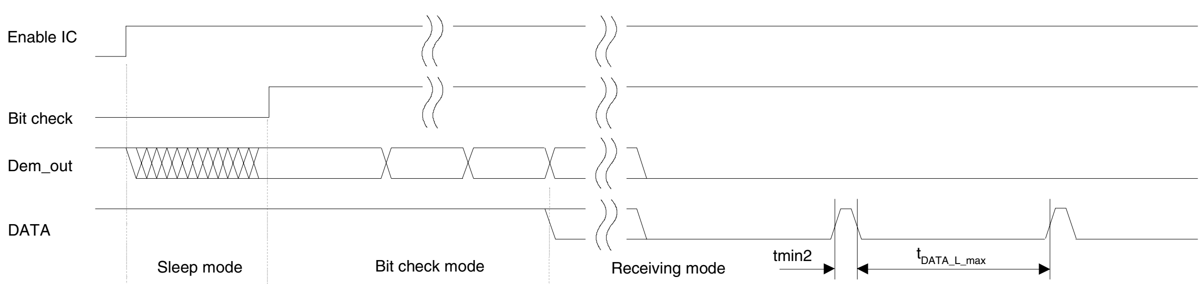


Figure 16. Steady L State Limited DATA Output Pattern after Transmission



After the end of a data transmission, the receiver remains active and random noise pulses appear at pin DATA. The edge-to-edge time period t_{ee} of the majority of these noise pulses is equal to or slightly higher than T_{DATA_min}.

Switching the Receiver Back to Sleep Mode

The receiver can be set back to polling mode via pin DATA or via pin ENABLE.

When using pin DATA, this pin must be pulled to low for the period t1 by the connected microcontroller. Figure 17 illustrates the timing of the OFF command (see also Figure 21 on page 21). The minimum value of t1 depends on the BR_Range. The maximum value for t1 is not limited but it is recommended not to exceed the specified value to prevent erasing the reset marker. This item is explained in more detail in the section “Configuration of the Receiver” on page 17. Setting the receiver to sleep mode via DATA is achieved by programming bit 1 of the OPMODE register to 1. Only one sync pulse (t3) is issued.

The duration of the OFF command is determined by the sum of t1, t2 and t10. After the OFF command, the sleep time T_{Sleep} elapses. Note that the capacitive load at pin DATA is limited. The resulting time constant τ together with an optional external pull-up resistor may not be exceeded to ensure proper operation.

If the receiver is set to polling mode via pin ENABLE, an 'L' pulse (T_{Doze}) must be issued at that pin. Figure 18 illustrates the timing of that command. After the positive edge of this pulse, the sleep time T_{Sleep} elapses. The receiver remains in sleep mode as long as ENABLE is held to 'L'. If the receiver is polled exclusively by a microcontroller, T_{Sleep} can be programmed to 0 to enable a instantaneous response time. This command is the faster option than via pin DATA at the cost of an additional connection to the microcontroller.

Figure 17. Timing Diagram of the OFF Command Via Pin DATA

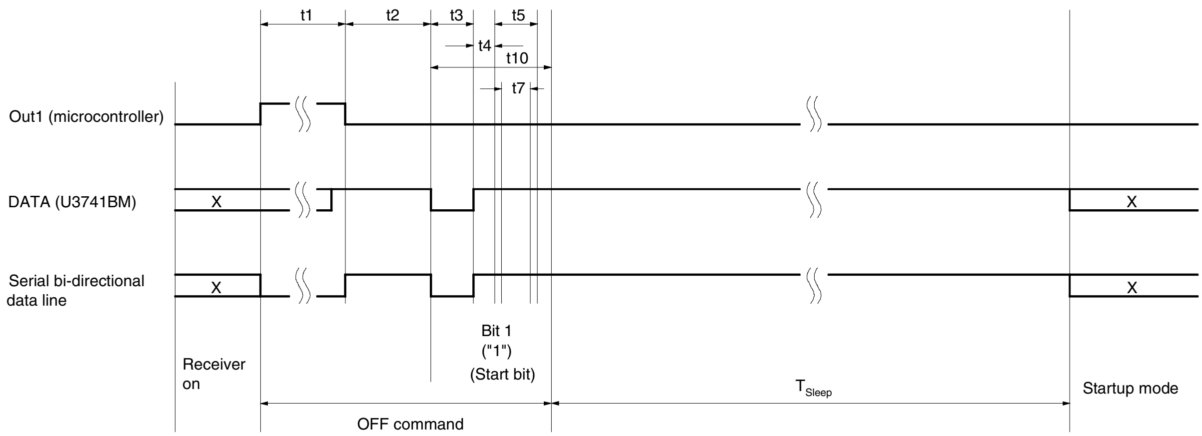
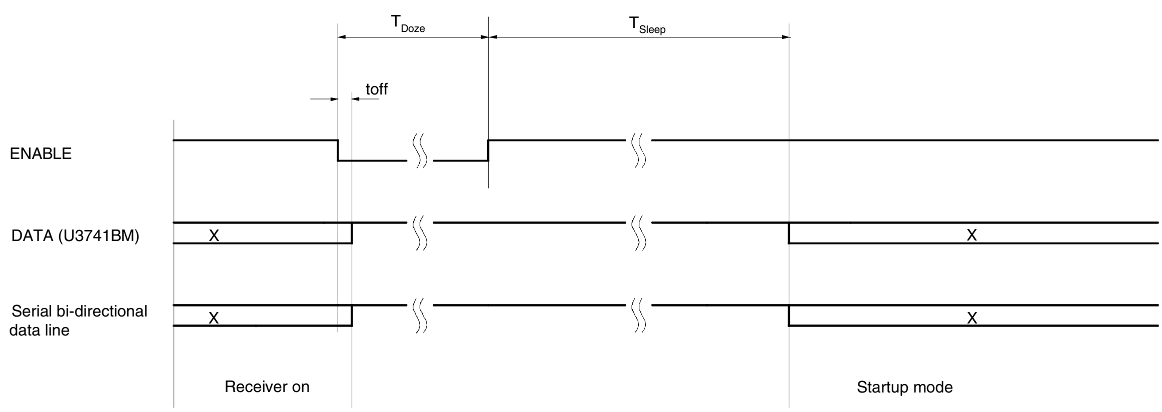


Figure 18. Timing Diagram of the OFF Command Via Pin ENABLE



Configuration of the Receiver

The U3741BM receiver is configured via two 12-bit RAM registers called OPMODE and LIMIT. The registers can be programmed by means of the bi-directional DATA port. If the register contents have changed due to a voltage drop, this condition is indicated by a certain output pattern called reset marker (RM). The receiver must be reprogrammed in that case. After a power-on reset (POR), the registers are set to default mode. If the receiver is operated in default mode, there is no need to program the registers.

Table 3 on page 18 shows the structure of the registers. According to Table 2 on page 18, bit 1 defines if the receiver is set back to polling mode via the OFF command, (see section "Receiving Mode" on page 15) or if it is programmed. Bit 2 represents the register address. It selects the appropriate register to be programmed.

Table 2. Effect of Bit 1 and Bit 2 in Programming the Registers

Bit 1	Bit 2	Action
1	x	The receiver is set back to polling mode (OFF command)
0	1	The OPMODE register is programmed
0	0	The LIMIT register is programmed

Table 4 and the following illustrate the effect of the individual configuration words. The default configuration is highlighted for each word.

BR_Range sets the appropriate baud rate range. At the same time it defines XLim. XLim is used to define the bit check limits T_{Lim_min} and T_{Lim_max} as shown in Table 4.

POUT can be used to control the sensitivity of the receiver. In that application, POUT is set to 1 to reduce the sensitivity. This implies that the receiver operates with full sensitivity after a POR.

Table 3. Effect of the Configuration Words within the Registers

Bit1	Bit2	Bit2	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14
OFF Command													
1													
OPMODE Register													
0	1	BR_Range		$N_{Bitcheck}$		V_{POUT}	Sleep					X_{Sleep}	
0	1	Baud1	Baud0	BitChk1	BitChk0	POUT	Sleep4	Sleep3	Sleep2	Sleep1	Sleep0	$X_{Sleep\ Std}$	$X_{Sleep\ Temp}$
(Default)		0	0	1	0	0	0	1	0	1	1	0	0
LIMIT Register													
0	0	Lim_min						Lim_max					
0	0	Lim_min5	Lim_min4	Lim_min3	Lim_min2	Lim_min1	Lim_min0	Lim_max5	Lim_max4	Lim_max3	Lim_max2	Lim_max1	Lim_max0
(Default)		0	0	1	1	1	0	0	1	1	0	0	0

Table 4. Effect of the Configuration Word BR_Range

BR_Range		
Baud1	**Baud0**	**Baud Rate Range/Extension Factor for Bit Check Limits (XLim)**
0	0	BR_Range0 (application USA/Europe: BR_Range0 = 1.0 kBaud to 1.8 kBaud) (Default) XLim = 8 (Default)
0	1	BR_Range1 (application USA/Europe: BR_Range1 = 1.8 kBaud to 3.2 kBaud) XLim = 4
1	0	BR_Range2 (application USA/Europe: BR_Range2 = 3.2 kBaud to 5.6 kBaud) XLim = 2
1	1	BR_Range3 (Application USA/Europe: BR_Range3 = 5.6 kBaud to 10 kBaud) XLim = 1

Table 5. Effect of the Configuration Word $N_{Bitcheck}$

$N_{Bitcheck}$		
BitChk1	**BitChk0**	**Number of Bits to be Checked**
0	0	0
0	1	3
1	0	6 (Default)
1	1	9

Table 6. Effect of the Configuration Bit VPOUT

VPOUT	Level of the Multi-purpose Output Port POUT
POUT	
0	0 (Default)
1	1

Table 7. Effect of the Configuration Word Sleep

Sleep					
Sleep4	**Sleep3**	**Sleep2**	**Sleep1**	**Sleep0**	**Start Value for Sleep Counter (T_{Sleep} = Sleep × X_{Sleep} × 1024 × T_{Clk})**
0	0	0	0	0	0 (Receiver is continuously polling until a valid signal occurs)
0	0	0	0	1	1 ($T_{Sleep} \approx$ 2ms for X_{Sleep} = 1 in US-/European applications)
0	0	0	1	0	2
0	0	0	1	1	3
. . .	. . .	. . .	. . .	. . .	. . .
0	1	0	1	1	11 (USA: T_{Sleep} = 22.96 ms, Europe: T_{Sleep} = 23.31 ms) (Default)
. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31 (Permanent sleep mode)

Table 8. Effect of the Configuration Word X_{Sleep}

X_{Sleep}		
$X_{SleepStd}$	$X_{SleepTemp}$	**Extension Factor for Sleep Time (T_{Sleep} = Sleep × X_{Sleep} × 1024 × T_{Clk})**
0	0	1 (Default)
0	1	8 (X_{Sleep} is reset to 1 if bit check fails once)
1	0	8 (X_{Sleep} is set permanently)
1	1	8 (X_{Sleep} is set permanently)

Table 9. Effect of the Configuration Word Lim_min

Lim_min						Lower Limit Value for Bit Check
Lim_min < 10 is not applicable						(T_{Lim_min} = Lim_min × XLim × T_{Clk})
0	0	1	0	1	0	10
0	0	1	0	1	1	11
0	0	1	1	0	0	12
0	0	1	1	0	1	13
0	0	1	1	1	0	14 (Default) (USA: T_{Lim_min} = 228 µs, Europe: T_{Lim_min} = 232 µs)
. . .	. . .	. . .	. . .	. . .	. . .	
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Table 10. Effect of the Configuration Word Lim_max

Lim_max						Upper Limit Value for Bit Check
Lim_max < 12 is not applicable						(T_{Lim_max} = (Lim_max - 1) × XLim × T_{Clk})
0	0	1	1	0	0	12
0	0	1	1	0	1	13
0	0	1	1	1	0	14
. . .	. . .	. . .	. . .	. . .	. . .	
0	1	1	0	0	0	24 (Default) (USA: T_{Lim_max} = 375 µs, Europe: T_{Lim_max} = 381 µs)
. . .	. . .	. . .	. . .	. . .	. . .	
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Conservation of the Register Information

The U3741BM has an integrated power-on reset and brown-out detection circuitry to provide a mechanism to preserve the RAM register information.

According to Figure 19 on page 21, a power-on reset (POR) is generated if the supply voltage V_S drops below the threshold voltage $V_{ThReset}$. The default parameters are programmed into the configuration registers in that condition. Once V_S exceeds $V_{ThReset}$, the POR is canceled after the minimum reset period t_{Rst}. A POR is also generated when the supply voltage of the receiver is turned on.

To indicate that condition, the receiver displays a reset marker (RM) at pin DATA after a reset. The RM is represented by the fixed frequency f_{RM} at a 50% duty cycle. RM can be canceled via an 'L' pulse t1 at pin DATA. The RM implies the following characteristics:

- f_{RM} is lower than the lowest feasible frequency of a data signal. By this means, RM cannot be misinterpreted by the connected microcontroller.
- If the receiver is set back to polling mode via pin DATA, RM cannot be canceled by accident if t1 is applied according to the proposal in the section "Programming the Configuration Register" on page 21.

By means of that mechanism, the receiver cannot lose its register information without communicating that condition via the reset marker RM.

Figure 19. Generation of the Power-on Reset

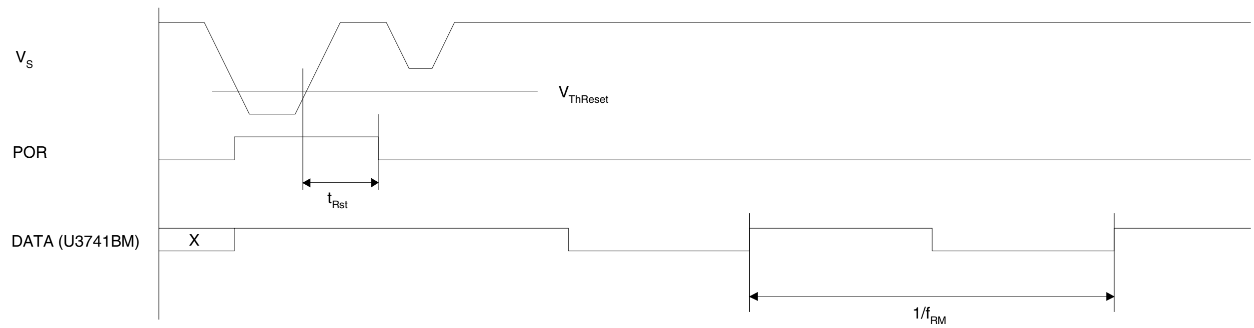
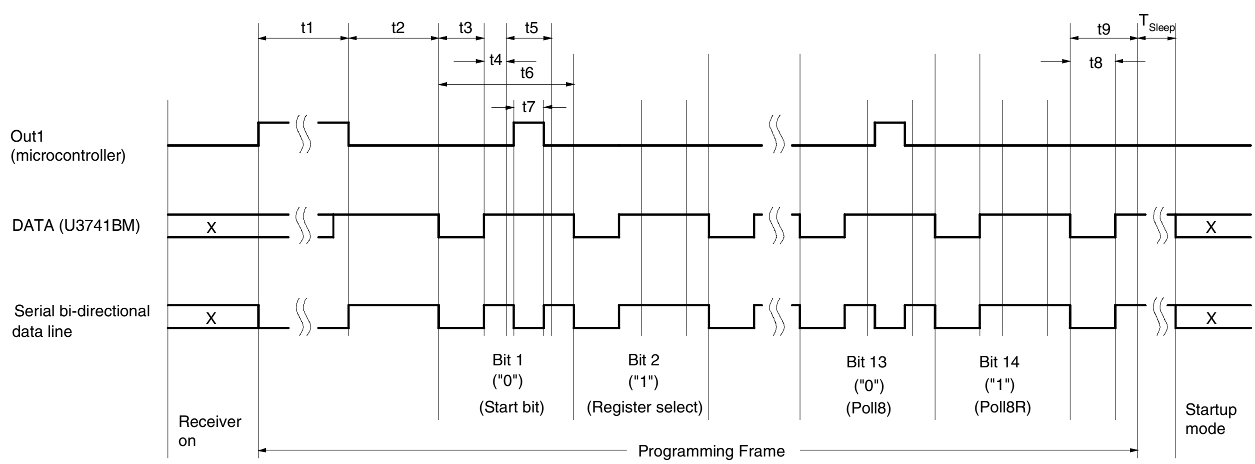


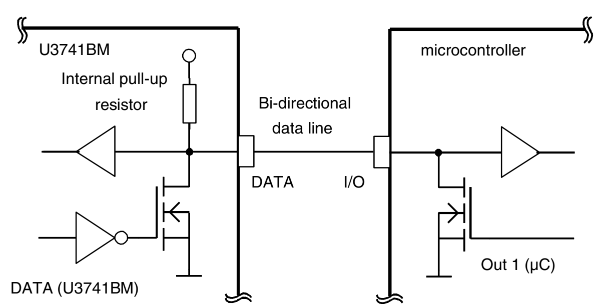
Figure 20. Timing of the Register Programming



Programming the Configuration Register

The configuration registers are programmed serially via the bi-directional data line according to Figure 20 and Figure 21.

Figure 21. One-wire Connection to a Microcontroller



To start programming, the serial data line DATA is pulled to ‘L’ for the time period t1 by the microcontroller. When DATA has been released, the receiver becomes the master device. When the programming delay period t2 has elapsed, it emits 14 subsequent synchronization pulses with the pulse length t3. After each of these pulses, a programming window occurs. The delay until the program window starts is determined by t4, the duration is defined by t5. Within the programming window, the individual bits are set. If the microcontroller pulls down pin DATA for the time period t7 during t5, the according bit is set to ‘0’. If no programming pulse t7 is issued, this bit is set to ‘1’. All 14 bits are subsequently programmed in this way. The time frame to program a bit is defined by t6.

Bit 14 is followed by the equivalent time window t9. During this window, the equivalent acknowledge pulse t8 (E_Ack) occurs if the mode word just programmed is equivalent to the mode word that was already stored in that register. E_Ack should be used to verify that the mode word was correctly transferred to the register. The register must be programmed twice in that case.

Programming of a register is possible both during sleep and active mode of the receiver.

During programming, the LNA, LO, low-pass filter, IF-amplifier and the demodulator are disabled.

The programming start pulse t1 initiates the programming of the configuration registers. If bit 1 is set to ‘1’, it represents the OFF command to set the receiver back to polling mode at the same time. For the length of the programming start pulse t1, the following convention should be considered:

- $t1(min) < t1 < 1535 \times T_{Clk}$: [t1(min) is the minimum specified value for the relevant BR_Range]

Programming (respectively OFF command) is initiated if the receiver is not in reset mode. If the receiver is in reset mode, programming (respectively Off command) is not initiated, and the reset marker RM is still present at pin DATA.

This period is generally used to switch the receiver to polling mode. In a reset condition, RM is not canceled by accident.

- $t1 > 5632 \times T_{Clk}$

Programming (respectively OFF command) is initiated in any case. RM is cancelled if present. This period is used if the connected microcontroller detected RM. If a configuration register is programmed, this time period for t1 can generally be used.

Note that the capacitive load at pin DATA is limited. The resulting time constant t together with an optional external pull-up resistor may not be exceeded to ensure proper operation.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_S		6	V
Power dissipation	P_{tot}		450	mW
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	-55	+125	°C
Ambient temperature	T_{amb}	-40	+105	°C
Maximum input level, input matched to 50 W	P_{in_max}		10	dBm

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	100	K/W

Electrical Characteristics

All parameters refer to GND, T_{amb} = -40°C to +105°C, V_S = 4.5 V to 5.5 V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (V_S = 5 V, T_{amb} = 25°C)

			6.76438-Mhz Osc. (Mode 1)			4.90625-Mhz Osc. (Mode 0)			Variable Oscillator			
Parameter	**Test Condition**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Basic Clock Cycle of the Digital Circuitry												
Basic clock cycle	MODE = 0 (USA) MODE = 1 (Europe)	T_{Clk}		2.0697			2.0383			$1/(f_{XTO}/10)$ $1/(f_{XTO}/14)$		µs µs
Extended basic clock cycle	BR_Range0 BR_Range1 BR_Range2 BR_Range3	T_{XClk}		16.6 8.3 4.1 2.1			16.3 8.2 4.1 2.0			$8 \times T_{Clk}$ $4 \times T_{Clk}$ $2 \times T_{Clk}$ $1 \times T_{Clk}$		µs µs µs µs
Polling Mode												
Sleep time	Sleep and X_{Sleep} are defined in the OPMODE register	T_{Sleep}		Sleep × X_{Sleep} × 1024 × 2.0697			Sleep × X_{Sleep} × 1024 × 2.0383			Sleep × X_{Sleep} × 1024 × T_{Clk}		ms
Start-up time	BR_Range0 BR_Range1 BR_Range2 BR_Range3	$T_{Startup}$		1855 1061 1061 663			1827 1045 1045 653			896.5 512.5 512.5 320.5 × T_{Clk}		µs µs µs µs
Time for Bit Check	Average bit check time while polling BR_Range0 BR_Range1 BR_Range2 BR_Range3	$T_{Bitcheck}$		0.45 0.24 0.14 0.14			0.47 0.26 0.16 0.15					ms ms ms ms
	Bit check time for a valid input signal f_{Sig} $N_{Bitcheck}$ = 0 $N_{Bitcheck}$ = 3 $N_{Bitcheck}$ = 6 $N_{Bitcheck}$ = 9	$T_{Bitcheck}$	$3/f_{Sig}$ $6/f_{Sig}$ $9/f_{Sig}$		$3.5/f_{Sig}$ $6.5/f_{Sig}$ $9.5/f_{Sig}$	$3/f_{Sig}$ $6/f_{Sig}$ $9/f_{Sig}$		$3.5/f_{Sig}$ $6.5/f_{Sig}$ $9.5/f_{Sig}$			T_{XClk} $3.5/f_{Sig}$ $6.5/f_{Sig}$ $9.5/f_{Sig}$	ms ms ms ms

Electrical Characteristics (Continued)

All parameters refer to GND, T_{amb} = -40°C to +105°C, V_S = 4.5 V to 5.5 V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (V_S = 5 V, T_{amb} = 25°C)

Parameter	Test Condition	Symbol	6.76438-Mhz Osc. (Mode 1)			4.90625-Mhz Osc. (Mode 0)			Variable Oscillator			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Receiving Mode												
Intermediate frequency	MODE=0 (USA) MODE=1 (Europe)	f_{IF}		1.0			1.0			f_{XTO} × 64/314 f_{XTO} × 64/432.92		MHz MHz
Baud rate range	BR_Range0 BR_Range1 BR_Range2 BR_Range3	BR_Range	1.0 1.8 3.2 5.6		1.8 3.2 5.6 10.0	1.0 1.8 3.2 5.6		1.8 3.2 5.6 10.0		BR_Range0 × 2 µs/T_{Clk} BR_Range1 × 2 µs/T_{Clk} BR_Range2 × 2 µs/T_{Clk} BR_Range3 × 2 µs/T_{Clk}		kBaud kBaud kBaud kBaud
Minimum time period between edges at pin DATA (Figure 15)	BR_Range0 BR_Range1 BR_Range2 BR_Range3 	T_{DATA_min} tmin1 tmin2 tmin1 tmin2 tmin1 tmin2 tmin1 tmin2		149 182 75 91 37.3 45.5 18.6 22.8			147 179 73 90 36.7 44.8 18.3 22.4			9 × T_{XClk} 11 × T_{XCl} 9 × T_{XClk} 11 × T_{XClk} 9 × T_{XClk} 11 × T_{XClk} 9 × T_{XClk} 11 × T_{XClk}		µs µs µs µs µs µs µs µs
Maximum low period at DATA (Figure 16)	BR_Range0 BR_Range1 BR_Range2 BR_Range3	$T_{DATA\_L\_max}$		2169 1085 542 271			2136 1068 534 267			131 × T_{XClk} 131 × T_{XClk} 131 × T_{XClk} 131 × T_{XClk}		µs µs µs µs
OFF command at pin ENABLE (Figure 18)		t_{Doze}	3.1			3.05			1.5 ¥ T_{Clk}			µs
Configuration of the Receiver												
Frequency of the reset marker (Figure 19)		f_{RM}		117.9			119.8			$\frac{1}{4096 \times T_{CLK}}$		Hz
Programming start pulse (Figure 17, Figure 20)	BR_Range0 BR_Range1 BR_Range2 BR_Range3 after POR	t1	2188 1104 561 290 11656		3176 3176 3176 3176	2155 1087 553 286 11479		3128 3128 3128 3128	1057 × T_{Clk} 533 × T_{Clk} 271 × T_{Clk} 140 × T_{Clk} 5632 × T_{Clk}		1535 × T_{Clk} 1535 × T_{Clk} 1535 × T_{Clk} 1535 × T_{Clk}	µs
Programming delay period (Figure 17, Figure 20)		t2	795		798	783		786	384.5 × T_{Clk}		385.5 × T_{Clk}	µs
Synchronization pulse (Figure 17, Figure 20)		t3		265			261			128 × T_{Clk}		µs

Electrical Characteristics (Continued)

All parameters refer to GND, T_{amb} = -40°C to +105°C, V_S = 4.5 V to 5.5 V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (V_S = 5 V, T_{amb} = 25°C)

			6.76438-Mhz Osc. (Mode 1)			4.90625-Mhz Osc. (Mode 0)			Variable Oscillator			
Parameter	Test Condition	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Delay until the program window starts (Figure 17, Figure 20)		t4		131			129			$63.5 \times T_{Clk}$		µs
Programming window (Figure 17, Figure 20)		t5		530			522			$256 \times T_{Clk}$		µs
Time frame of a bit (Figure 20)		t6		1060			1044			$512 \times T_{Clk}$		µs
Programming pulse (Figure 17, Figure 20)		t7	133		529	131		521	$64 \times T_{Clk}$		$256 \times T_{Clk}$	µs
Equivalent acknowledge pulse: E_Ack (Figure 20)		t8		265			261			$128 \times T_{Clk}$		µs
Equivalent time window (Figure 20)		t9		534			526			$258 \times T_{Clk}$		µs
OFF-bit programming window (Figure 17)		t10		930			916			$449.5 \times T_{Clk}$		µs

Electrical Characteristics

All parameters refer to GND, T_{amb} = -40°C to +105°C, V_S = 4.5 V to 5.5 V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (V_S = 5 V, T_{amb} = 25°C)

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Current consumption	Sleep mode (XTO and polling logic active)	IS_{off}		190	350	µA
	IC active (startup-, bit check-, receiving mode) pin DATA = H	IS_{on}		7.0	8.6	mA
LNA Mixer						
Third-order intercept point	LNA/mixer/IF amplifier input matched according to Figure 4	IIP3		-28		dBm
LO spurious emission at RF_{In}	Input matched according to Figure 4, required according to I-ETS 300220	IS_{LORF}		-73	-57	dBm
Noise figure LNA and mixer (DSB)	Input matching according to Figure 4	NF		7		dB
LNA_IN input impedance	at 433.92 MHz at 315 MHz	Zi_{LNA_IN}		1.0 || 1.56 1.3 || 1.0		kΩ || pF kΩ || pF
1 dB compression point (LNA, mixer, IF amplifier)	Input matched according to Figure 4, referred to RF_{in}	IP_{1db}		-40		dBm