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Standard 8K x 8 SRAM

Features

- 8192 x 8 bit static CMOS RAM
- 70 ns Access Times
- Common data inputs and outputs
- Three-state outputs
- Typ. operating supply current
  70 ns: 10 mA
- Standby current:
  < 2 µA at $T_a \leq 70$ °C
- Data retention current at 2 V:
  < 1 µA at $T_a \leq 70$ °C
- TTL/CMOS-compatible
- Automatic reduction of power dissipation in long Read or Write cycles
- Power supply voltage 5 V
- Operating temperature ranges:
  0 to 70 °C
  -40 to 85 °C
  -40 to 125 °C
- QS 9000 Quality Standard
- ESD protection > 2000 V (MIL STD 883C M3015.7)
- Latch-up immunity > 100 mA
- Packages: PDIP28 (600 mil)
  SOP28 (330 mil)

Description

The U6264B is a static RAM manufactured using a CMOS process technology with the following operating modes:

- Read - Standby
- Write - Data Retention

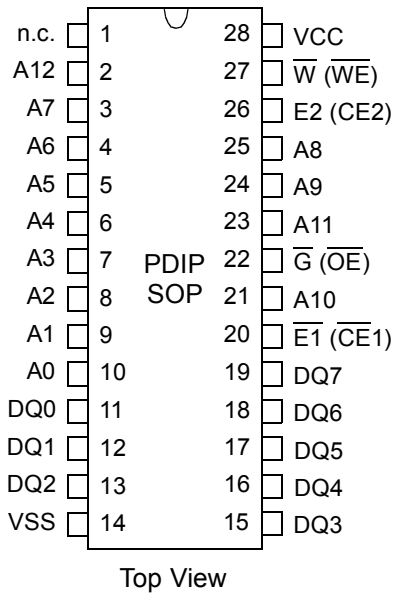
The memory array is based on a 6-transistor cell.

The circuit is activated by the rising edge of E2 (at $\overline{E1}$ = L), or the falling edge of $\overline{E1}$ (at E2 = H). The address and control inputs open simultaneously. According to the information of $\overline{W}$ and $\overline{G}$, the data inputs, or outputs, are active. In a Read cycle, the data outputs are activated by the falling edge of $\overline{G}$, afterwards the data word read will be available at the outputs DQ0 - DQ7. After the address change, the data outputs go High-Z until the new read information is available. The data outputs have no preferred state. If the memory is driven by CMOS levels in the active state, and if there is no change of the address, data input and control signals $\overline{W}$ or $\overline{G}$, the operating current (at I_O = 0 mA) drops to the value of the operating current in the Standby mode. The Read cycle is finished by the falling edge of E2 or $\overline{W}$, or by the rising edge of $\overline{E1}$, respectively.

Data retention is guaranteed down to 2 V. With the exception of E2, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required. This gate circuit allows to achieve low power standby requirements by activation with TTL-levels too.

If the circuit is inactivated by E2 = L, the standby current (TTL) drops to 150 µA typ.

Pin Configuration

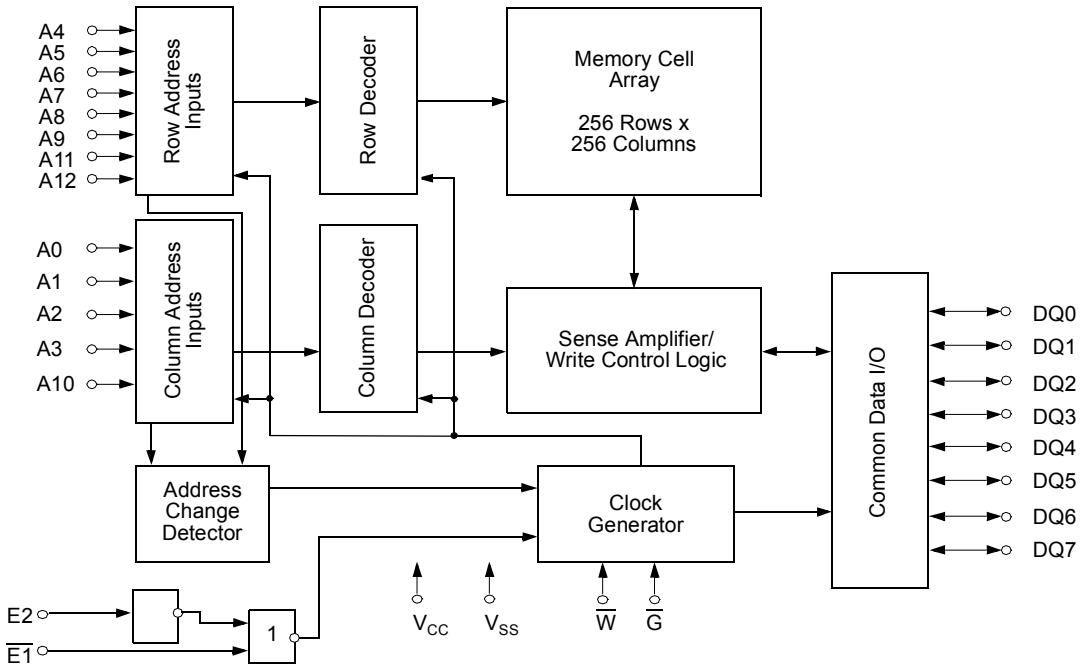


Top View

Pin Description

Signal Name	Signal Description
A0 - A12	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground
n.c.	not connected

Block Diagram



Truth Table

Operating Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0 - DQ7
Standby/not selected	*	L	*	*	High-Z
	H	*	*	*	High-Z
Internal Read	L	H	H	H	High-Z
Read	L	H	H	L	Data Outputs Low-Z
Write	L	H	L	*	Data Inputs High-Z

* H or L

Characteristics

All voltages are referenced to V_{SS} = 0 V (ground).
All characteristics are valid in the power supply voltage range and in the operating temperature range specified.
Dynamic measurements are based on a rise and fall time of ≤ 5 ns, measured between 10 % and 90 % of V_I, as well as input levels of V_{IL} = 0 V and V_{IH} = 3 V. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis}-times, in which cases transition is measured ± 200 mV from steady-state voltage.

Absolute Maximum Ratings [a]		**Symbol**	**Min.**	**Max.**	**Unit**
Power Supply Voltage		V_{CC}	-0.3	7	V
Input Voltage		V_I	-0.3	V_{CC} + 0.5 [b]	V
Output Voltage		V_O	-0.3	V_{CC} + 0.5 [b]	V
Power Dissipation		P_D	-	1	W
Operating Temperature	C-Type K-Type A-Type	T_a	0 -40 -40	70 85 125	°C °C °C
Storage Temperature	C/K-Type A-Type	T_{stg}	-55 -65	125 150	°C °C
Output Short-Circuit Current at V_{CC} = 5 V and V_O = 0 V [c]		$\lvert I_{OS} \rvert$		100	mA

[a] Stresses greater than those listed under „Absolute Maximum Ratings“ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
[b] Maximum voltage is 7 V
[c] Not more than 1 output should be shorted at the same time. Duration of the short circuit should not exceed 30 s.

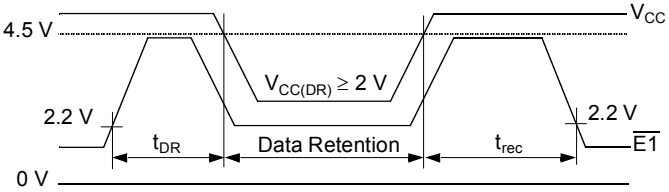
Recommended Operating Conditions	**Symbol**	**Conditions**	**Min.**	**Max.**	**Unit**
Power Supply Voltage	V_{CC}		4.5	5.5	V
Data Retention Voltage	$V_{CC(DR)}$		2.0		V
Input Low Voltage [d]	V_{IL}		-0.3	0.8	V
Input High Voltage	V_{IH}		2.2	V_{CC} + 0.3	V

[d] -2 V at Pulse Width 10 ns

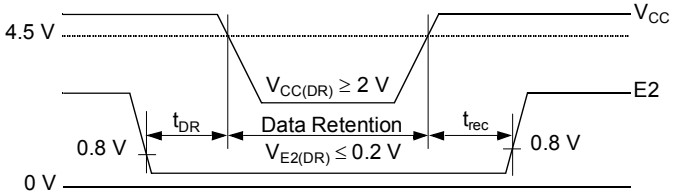
Electrical Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	V_{CC} = 5.5 V V_{IL} = 0.8 V V_{IH} = 2.2 V t_{cW} = 70 ns		55	mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	V_{CC} = 5.5 V $V_{\overline{E1}} = V_{E2}$ = V_{CC} - 0.2 V or V_{E2} = 0.2 V C-Type K-Type A-Type		 2 5 100	 µA µA µA
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)1}$	V_{CC} = 5.5 V $V_{\overline{E1}} = V_{E2}$ = 2.2 V or V_{E2} = 0.8 V		3	mA
Supply Current - Data Retention Mode	$I_{CC(DR)}$	$V_{CC(DR)}$ = 2 V $V_{\overline{E1}} = V_{E2}$ = $V_{CC(DR)}$ - 0.2 V or V_{E2} = 0.2 V C-Type K-Type A-Type		 1 3 50	 µA µA µA
Output High Voltage Output Low Voltage	V_{OH} V_{OL}	V_{CC} = 4.5 V I_{OH} = -1.0 mA V_{CC} = 4.5 V I_{OL} = 3.2 mA	2.4	 0.4	V V
Output High Current Output Low Current	I_{OH} I_{OL}	V_{CC} = 4.5 V V_{OH} = 2.4 V V_{CC} = 4.5 V V_{OL} = 0.4 V	 3.2	-1 	mA mA
Input Leakage Current High Low	 I_{IH} I_{IL}	 V_{CC} = 5.5 V V_{IH} = 5.5 V C/K-Type A-Type V_{CC} = 5.5 V V_{IL} = 0 V C/K-Type A-Type	 - - -1 -2	 1 2 - -	 µA µA µA µA
Output Leakage Current High at Three-State Outputs Low at Three-State Outputs	 I_{OHZ} I_{OLZ}	 V_{CC} = 5.5 V V_{OH} = 5.5 V C/K-Type A-Type V_{CC} = 5.5 V V_{OL} = 0 V C/K-Type A-Type	 - - -1 -2	 1 2 - -	 µA µA µA µA

Switching Characteristics	Symbol		Min.	Max.	Unit
	Alt.	IEC			
Time to Output in Low-Z	t_{LZ}	$t_{t(QX)}$	5	10	ns
Cycle Time					
Write Cycle Time	t_{WC}	t_{cW}	70		ns
Read Cycle Time	t_{RC}	t_{cR}	70		ns
Access Time					
$\overline{E1}$ LOW or E2 HIGH to Data Valid	t_{ACE}	$t_{a(E)}$	-	70	ns
$\overline{G}$ LOW to Data Valid	t_{OE}	$t_{a(G)}$	-	40	ns
Address to Data Valid	t_{AA}	$t_{a(A)}$	-	70	ns
Pulse Widths					
Write Pulse Width	t_{WP}	$t_{w(W)}$	50		ns
Chip Enable to End of Write	t_{CW}	$t_{w(E)}$	65		ns
Setup Times					
Address Setup Time	t_{AS}	$t_{su(A)}$	0		ns
Chip Enable to End of Write	t_{CW}	$t_{su(E)}$	65		ns
Write Pulse Width	t_{WP}	$t_{su(W)}$	50		ns
Data Setup Time	t_{DS}	$t_{su(D)}$	35		ns
Data Hold Time	t_{DH}	$t_{h(D)}$	0		ns
Address Hold from End of Write	t_{AH}	$t_{h(A)}$	0		ns
Output Hold Time from Address Change	t_{OH}	$t_{v(A)}$	5		ns
$\overline{E1}$ HIGH or E2 LOW to Output in High-Z	t_{HZCE}	$t_{dis(E)}$	0	25	ns
$\overline{W}$ LOW to Output in High-Z	t_{HZWE}	$t_{dis(W)}$	0	30	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$	0	25	ns

Data Retention Mode $\overline{E1}$-Controlled



Data Retention Mode E2-Controlled



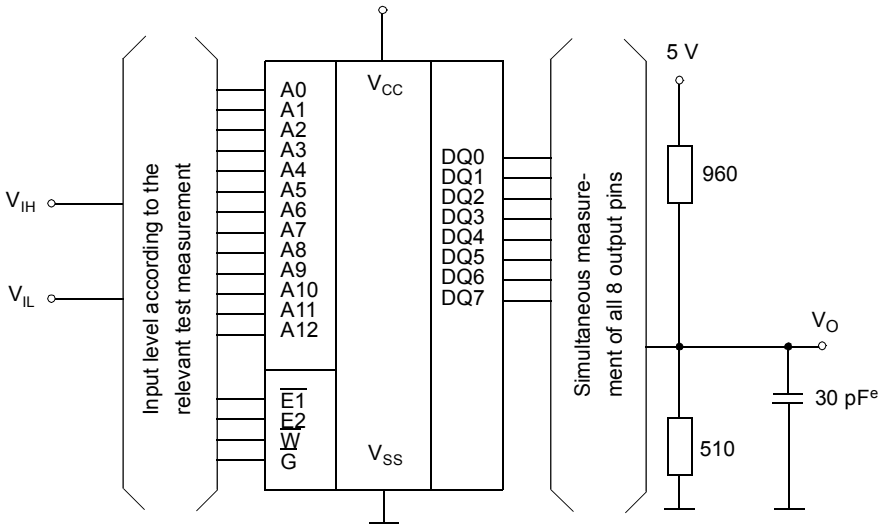
$V_{E2(DR)} \geq V_{CC(DR)}$ - 0.2 V or $V_{E2(DR)} \leq 0.2$ V

$V_{CC(DR)}$ - 0.2 V $\leq V_{E1(DR)} \leq V_{CC(DR)}$ + 0.3 V

Chip Deselect to Data Retention Time t_{DR}: min 0 ns

Operating Recovery Time t_{rec}: min t_{cR}

Test Configuration for Functional Check



[e] In measurement of $t_{dis(E)}$, $t_{dis(W)}$, $t_{dis(G)}$ the capacitance is 5 pF.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	V_{CC} = 5.0 V V_I = V_{SS} f = 1 MHz T_a = 25 °C	C_I		8	pF
Output Capacitance		C_O		10	pF

All pins not under test must be connected with ground by capacitors.

Ordering Code

Example **U6264B S2 K 07 LL**

Type

Package
D = PDIP28 (600 mil, only C/K-Type)
S = SOP28 (330 mil) Type 1
S2 = SOP28 (330 mil) Type 2

Operating Temperature Range
C = 0 to 70 °C
K = -40 to 85 °C
A = -40 to 125 °C

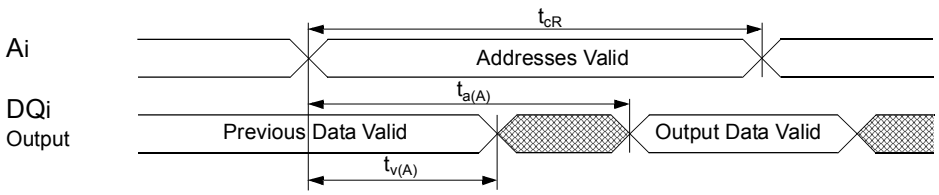
[f] on special request

Access Time
07 = 70 ns

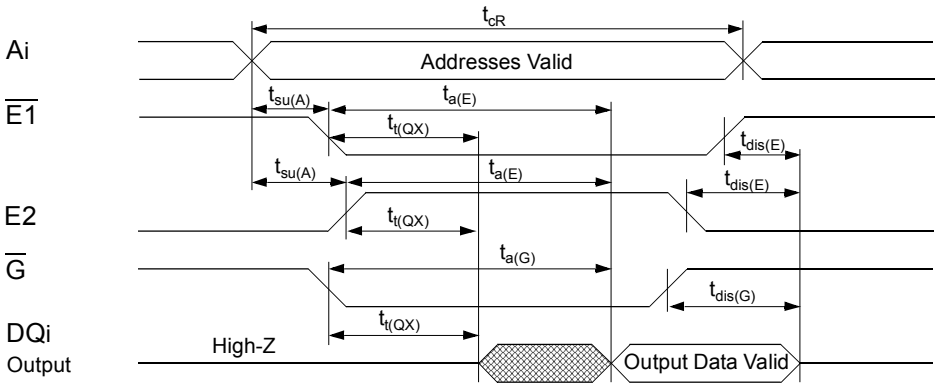
Power Consumption
blank = Standard (only A-Type)
LL = Very Low Power (C/K-Type)

Leadfree Option
blank = Standard Package
G1 = Leadfree Green Package [f]

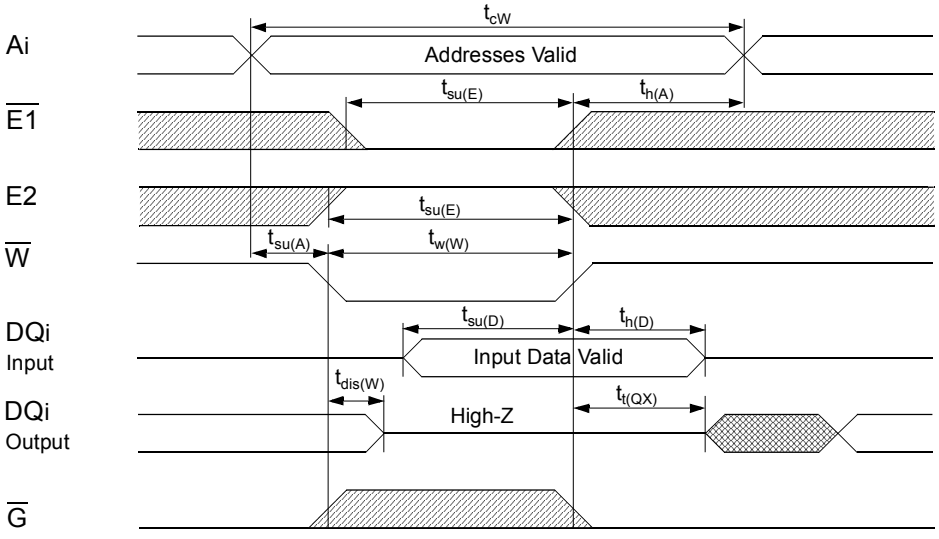
Read Cycle 1 (during Read cycle: $\overline{E1}$ = $\overline{G}$ = V_{IL}, E2 = $\overline{W}$ = V_{IH})



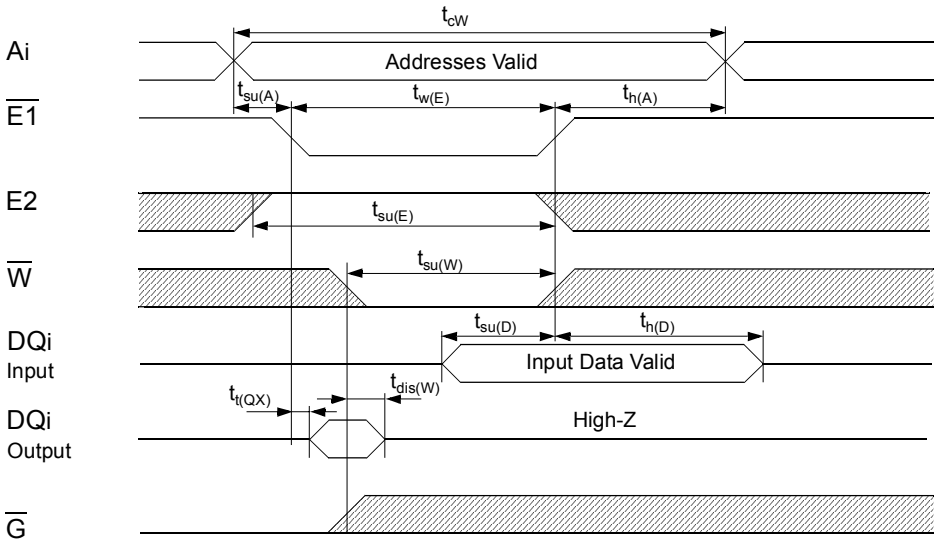
Read Cycle 2 (during Read cycle: $\overline{W}$ = V_{IH})



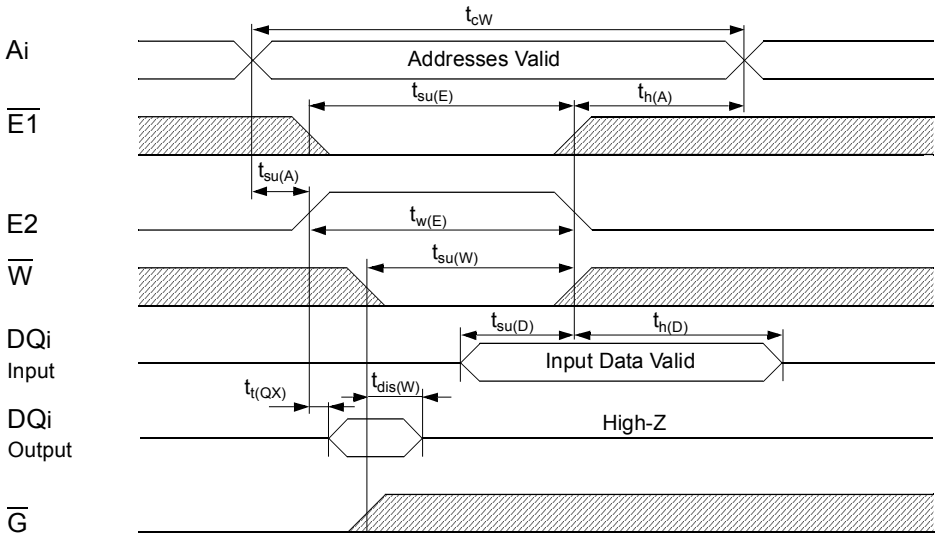
Write Cycle 1 ($\overline{W}$-controlled)

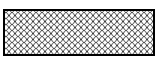


Write Cycle 2 ($\overline{E1}$-controlled)



Write Cycle 3 (E2-controlled)



undefined  L- or H-level 

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