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## Features

- Digital Self-supervising Watchdog with Hysteresis
- Three 250-mA Output Drivers
- One Relay Driver, Two Lamp Drivers
- Lamp Drivers with Auxiliary Ground
- Lamp Drivers Short-circuit Protected
- Lamp Drivers with Status Feedback
- Enable Output
- Over-/Undervoltage Detection and Reset
- All Power Outputs Protected Against Standard Transients
- All Power Outputs Protected Against 40-V Load Dump
- Automatically Activated Lamp Drivers if  $V_S$  is Disconnected
- Automatically Activated Lamp Drivers Via AUX GND if Standard Ground is Disconnected

## Description

The U6809B is designed to support the fail-safe function of safety-critical systems such as ABS. It includes a relay driver, two independent short-circuit-protected lamp drivers which are supplied by redundant ground lines, two monitoring circuits for the lamp driver output voltage and output current, a watchdog controlled by an external RC network and a reset circuit initiated by an over- and undervoltage condition of the 5-V supply providing a positive and a negative reset signal.



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## Fail-safe IC with Relay Driver and Lamp Driver

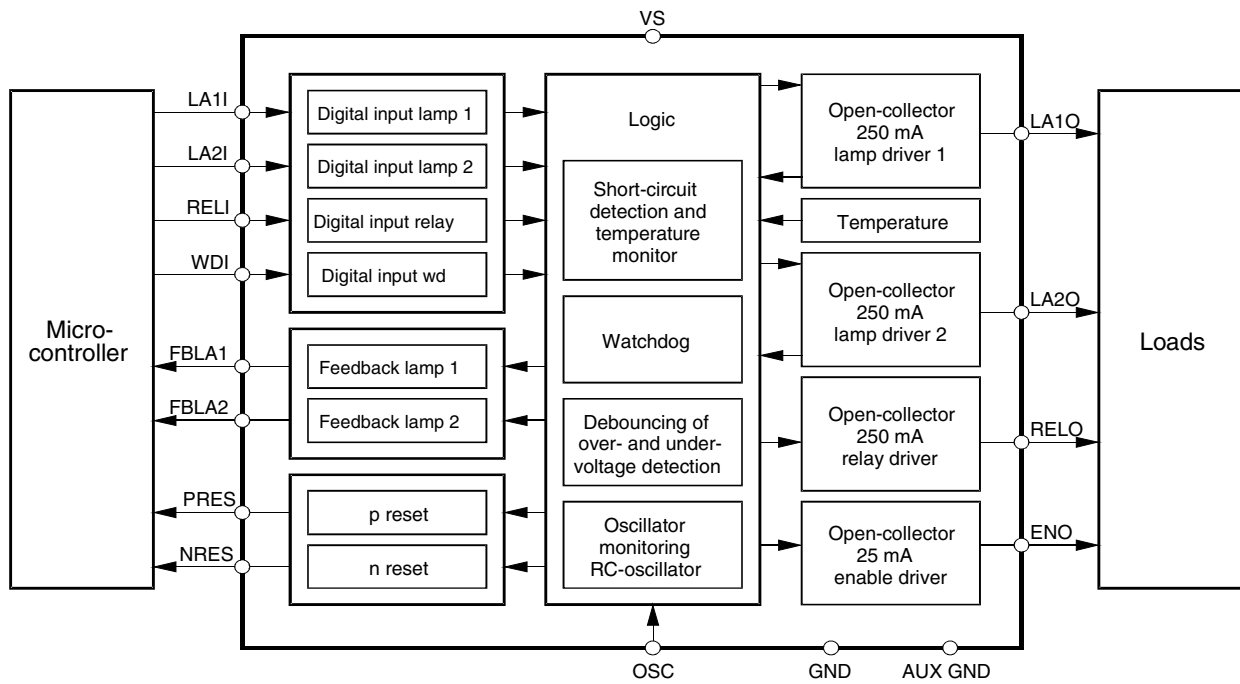
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**U6809B**

Rev. 4764A-AUTO-10/03

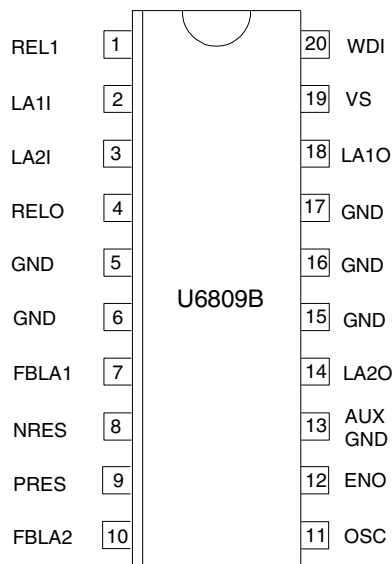


**Figure 1.** Block Diagram



## Pin Configuration

**Figure 2.** Pinning SO20

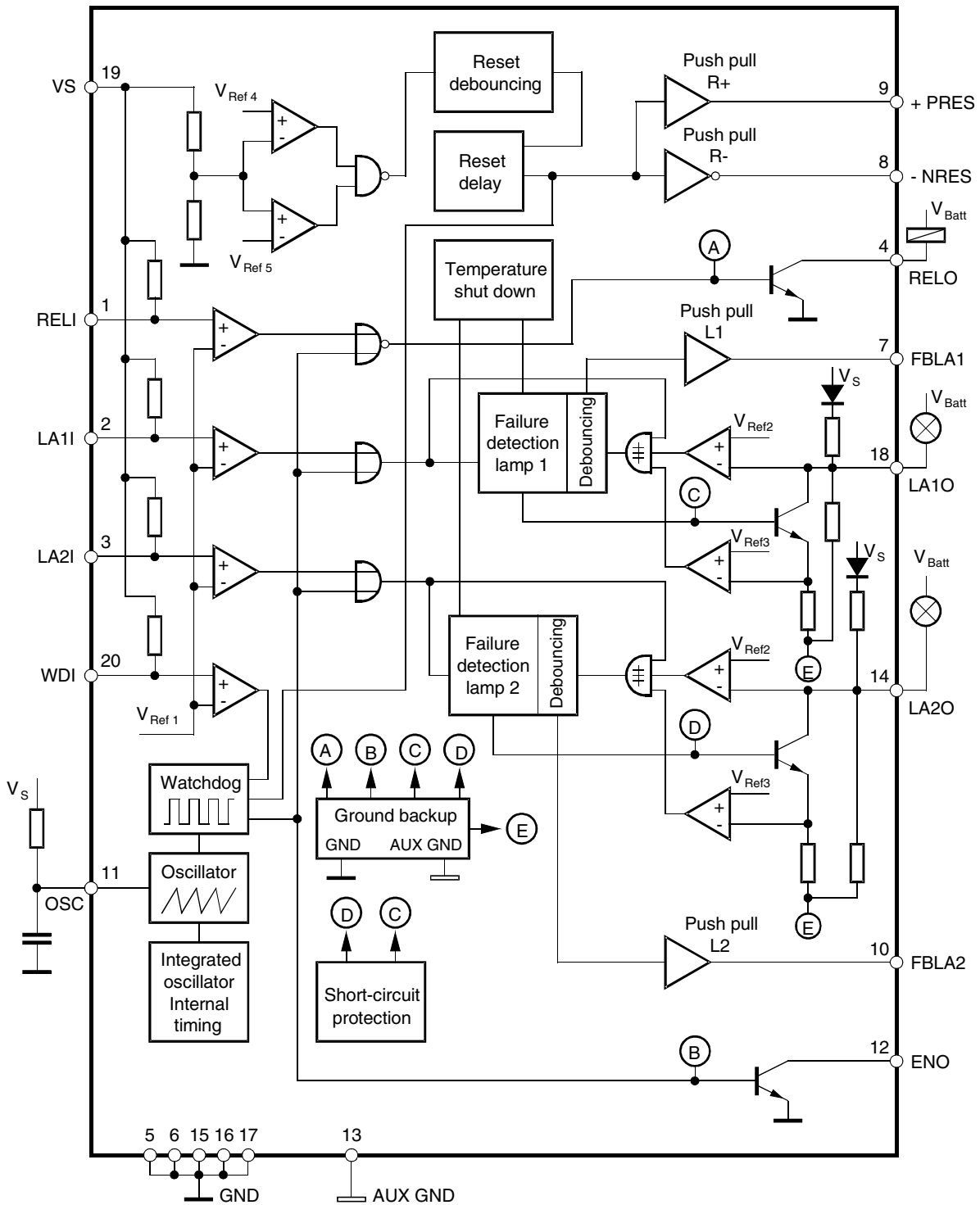


## Pin Description

Pin	Name	Type	Function	Logic
1	RELI	Digital input	Activation of relay driver	Driver on: L Driver off: H
2	LA1I	Digital input	Activation of lamp driver 1	Driver off: L Driver on: H
3	LA2I	Digital input	Activation of lamp driver 2	Driver off: L Driver on: H
4	RELO	Open-collector driver output	Fail-safe relay driver	Driver off: --- Driver on: L
5, 6	GND	Supply	Standard ground	
7	FBLA1	Digital output	Feedback lamp1	See Table 1 on page 5 and Table 2 on page 5
8	NRES	Digital output	Negative reset signal	Reset: L No reset: H
9	PRES	Digital output	Positive reset signal	Reset: H No reset: L
10	FBLA2	Digital output	Feedback lamp 2	See Table 1 on page 5 and Table 2 on page 5
11	OSC	Analog input	External RC for watchdog timer	
12	ENO	Open-collector output	Watchdog disable output	Watchdog ok: --- Watchdog n ok: L
13	AUX, GND	Supply	Auxiliary ground of lamp drivers	
14	LA2O	Open-collector driver output	Warning lamp driver	Driver off: --- Driver on: L
15, 16, 17	GND	Supply	Standard ground	
18	LA1O	Open-collector driver output	Warning lamp driver	Driver off: --- Driver on: L
19	VS	Supply	5 V supply	
20	WDI	Digital input	Watchdog trigger signal	Pulse sequence

# Detailed Block Diagram with External Components

Figure 3. Detailed Block Diagram





**Table 1.** Truth Table for Lamp Drivers and Lamp Feedback

Inputs			Outputs			Comment
Lamp (I)	Lamp Voltage	Lamp Current	Lamp Driver Current	Lamp Current	Feedback Lamp	
0	1	0	off	off	1	Output ok or open (internal pull-up) or shorted to $V_{Batt}$
0	1	1	on	off	1	Output shorted to $V_{Batt}$ and faulty input level
0	0	1	on	on	0	Internal driver activated due to internal failure
0	0	0	off	on	0	Output shorted to GND
1	0	1	on	on	0	Output ok
1	1	1	on	off	1	Output shorted to $V_{Batt}$
1	1	0	off	off	1	Internal driver deactivated due to internal failure or thermal shutdown
1	0	0	off	on/off	1	Output shorted to GND or open

**Explanation**

Lamp voltage is logic 1 if output voltage > threshold voltage detection  
 Lamp voltage is logic 0 if output voltage < threshold voltage detection  
 Lamp current is logic 1 if output current > threshold current detection  
 Lamp current is logic 0 if output current < threshold current detection

**Table 2.** Table of Fault Detection

Condition	Feedback Lamp	
	Lamp Input is 0 (Lamp off)	Lamp Input is 1 (Lamp on)
Normal operation	1	0
Lamp output shorted to GND	0 (= detection)	1 (= detection)
Lamp output shorted to $V_{Batt}$	1 (= no detection)	1 (= detection)
Lamp output open	1 (= no detection)	1 (= detection)
Feedback shorted to GND	0 (= detection)	0 (= no detection)
Feedback shorted to $V_S$	1 (= no detection)	1 (= detection)
Lamp input shorted to GND	1 (= no detection)	1 (= detection)
Lamp input shorted to $V_S$	0 (= detection)	0 (= no detection)

**Fail-safe Functions**

A fail-safe IC has to maintain its monitoring function even if there is a fault condition at one of the pins (e.g., short circuit). This ensures that a microcontroller system would not be brought into a critical status. A critical status is reached if the system is not able to actuate a warning lamp and switch off the relay. The following table shows fault conditions for different pins during which the IC still works as a fail-safe device.

**Table 3.** Table of Fault Condition

Pin	Function	Short to $V_S$	Short to $V_{Batt}$	Short to GND	Open Circuit
LA2O	Short-circuit proof driver for warning lamp	LA2O partly on	LA2O off	LA2O on	LA2O off
LA2I	Digital input to activate warning lamp	LA2O on	LA2O on	LA2O off	LA2O on
FBLA2	Digital feedback of warning lamp	Faulty feedback	Faulty feedback	Faulty feedback	Faulty feedback
LA1O	Short-circuit proof driver for warning lamp	LA1O partly on	LA1O off	LA1O on	LA1O off
LA1I	Digital input to activate warning lamp	LA1O on	LA1O on	LA1O off	LA1O on
FBLA1	Digital feedback of warning lamp	Faulty feedback	Faulty feedback	Faulty feedback	Faulty feedback
RELI	Digital input to activate the fail safe relay	Relay off	Relay off	Relay on	Relay off
WDI	Watchdog trigger input	Watchdog reset	Watchdog reset	Watchdog reset	Watchdog reset
OSC	Capacitor and resistor of watchdog	Watchdog reset	Watchdog reset	Watchdog reset	Watchdog reset

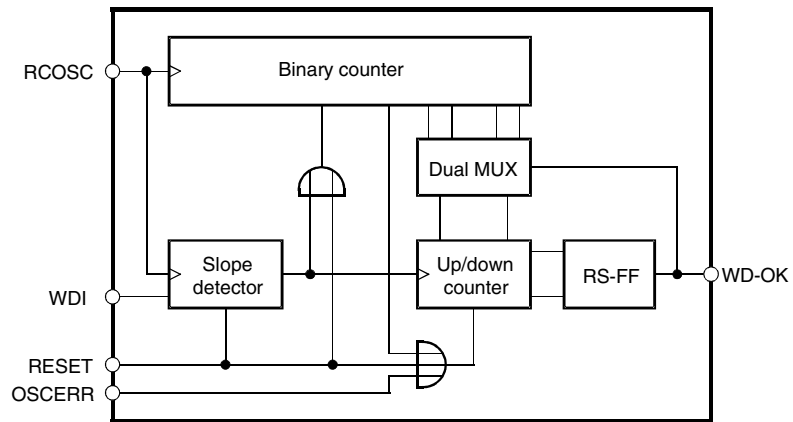
## Description of the Watchdog

### Abstract

The microcontroller is monitored by a digital window watchdog which accepts an incoming trigger signal of a constant frequency for correct operation. The frequency of the trigger signal can be varied in a broad range as the watchdog's time window is determined by external RC components.

The following description refers to Figure 1 on page 2.

**Figure 4.** Watchdog Block Diagram



**WDI Input (Pin 20)**

The microcontroller has to provide a trigger signal with the frequency  $f_{WDI}$  which is fed to the WDI input. A positive edge of  $f_{WDI}$  detected by a slope detector resets the binary and clocks the up/down counter additionally. The up/down counter only counts from 0 to 3 or reverse. Each correct trigger increments the up/down counter by 1, each wrong trigger decrements it by 1. As soon as the counter reaches the count of 3 the RS flip-flop is set (see Figure 5). A missing incoming trigger signal is detected after 250 clocks of the internal watchdog frequency  $f_{RC}$  (see WD-OK output) and resets the up/down counter directly.

**RCOSC Input**

With an external RC circuitry the IC generates a time base (frequency  $f_{RC}$ ) independent from the microcontroller. The watchdog's time window refers to a frequency of

$$RC = 100 \times f_{WDI}$$

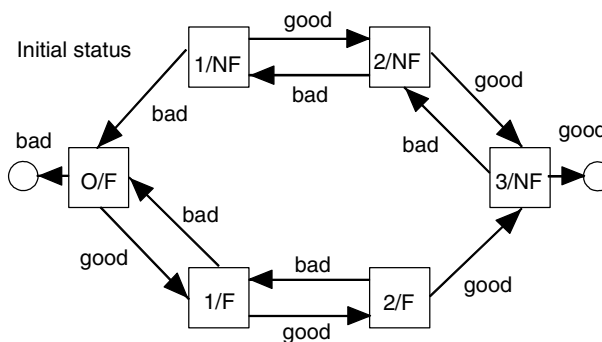
**Reset Input**

During power-on and under-/overvoltage detection a reset signal is fed to this pin. It resets the watchdog timer and sets the initial state.

**WD - OK Output**

After the up/down counter has been incremented to the count of 3 (see Figure 5, WD state diagram), the RS flip-flop is set and the WD-OK output becomes logic "1". This information is available for the microcontroller at the open-collector output ENO. If, on the other hand, the up/down counter is decremented to 0 the RS flip flop is reset, the WD OK output and the ENO output are disabled. The WD OK output also controls a dual MUX stage which shifts the time window by one clock after a successful trigger, thus forming a hysteresis to provide stable conditions for the evaluation of the trigger signal "good or false". The WD OK signal is also reset in case the watchdog counter is not reset after 250 clocks (missing trigger signal).

**Watchdog State Diagram** Figure 5. Watchdog State Diagram



**Explanation**

In each block, the first character represents the state of the counter. The second notation indicates the fault status of the counter. A fault status is indicated by an "F" and a no fault status is indicated by an "NF". When the watchdog is powered up initially, the counter starts at the 0/F block (initial state). "Good" indicates that a pulse has been received whose width resides within the timing window. "Bad" indicates that a pulse has been received whose width is either too short or too long.



## Watchdog Window Calculation

Example with recommended values

$$C_{osc} = 3.3 \text{ nF} \quad (\text{should be preferably } 10\%, \text{ NPO})$$

$$R_{osc} = 39 \text{ k}\Omega \quad (\text{may be } 5\%, \quad R_{osc} < 100 \text{ k}\Omega \text{ due to leakage current and humidity})$$

## RC Oscillator

$$t_{WDC} \text{ (s)} = 10^{-3} \times [C_{osc} \text{ (nF)} \times [(0.00078 \times R_{osc} \text{ (k}\Omega)) + 0.0005]]$$

$$f_{WDC} \text{ (Hz)} = 1/(t_{WDC})$$

## Watchdog WDI

$$f_{WDI} \text{ (Hz)} = 0.01 \times f_{WDC}$$

$$t_{WDC} = 100 \text{ }\mu\text{s} \rightarrow f_{WDC} = 10 \text{ kHz}$$

$$f_{WDI} = 100 \text{ Hz} \rightarrow t_{WDI} = 10 \text{ ms}$$

## WDI Pulse Width for Fault Detection After 3 Pulses

Upper watchdog window

$$\text{Minimum: } 169/f_{WDC} = 16.9 \text{ ms} \rightarrow f_{WDC}/169 = 59.1 \text{ Hz}$$

$$\text{Maximum: } 170/f_{WDC} = 17.0 \text{ ms} \rightarrow f_{WDC}/170 = 58.8 \text{ Hz}$$

Lower watchdog window

$$\text{Minimum: } 79/f_{WDC} = 7.9 \text{ ms} \rightarrow f_{WDC}/79 = 126.6 \text{ Hz}$$

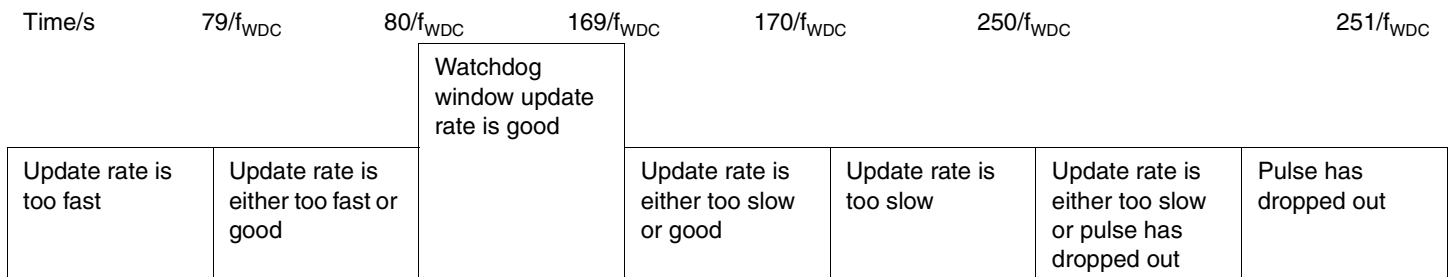
$$\text{Maximum: } 80/f_{WDC} = 8.0 \text{ ms} \rightarrow f_{WDC}/80 = 125.0 \text{ Hz}$$

## WDI Dropouts for Immediate Fault Detection

$$\text{Minimum: } 250/f_{WDC} = 25 \text{ ms}$$

$$\text{Maximum: } 251/f_{WDC} = 25.1 \text{ ms}$$

**Figure 6.** Watchdog Timing Diagram with Tolerances



## Remark to Reset Delay

The duration of the over- or undervoltage pulses determines the enable and reset output. A pulse duration shorter than the debounce time has no effect on the outputs. A pulse longer than the debounce time results in the first reset delay. If a pulse appears during this delay, a 2nd delay time is triggered. Therefore, the total reset delay time can be longer than specified in the datasheet.

## Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply voltage range	$V_S$	-0.2 to +16	V
AUX GND offset voltage to GND	$V_{AUX}$	±1.5	V
AUX GND offset current to GND	$I_{AUX}$	-600	mA
Power dissipation $V_S = 5\text{ V}$ ; $T_{amb} = 125^\circ\text{C}$	$P_{tot}$	700	mW
Thermal resistance	$R_{thjc}$	25	K/W
Junction temperature	$T_j$	150	°C
Ambient temperature range	$T_{amb}$	-40 to +125	°C
Storage temperature range	$T_{stg}$	-55 to +155	°C

## Electrical Characteristics

$V_S = 5\text{ V}$ ,  $T_{amb} = -40\text{ to }+125^\circ\text{C}$ ; reference pin is GND;  $f_{intern} = 100\text{ kHz} + 50\% - 45\%$ ,  $f_{WDC} = 10\text{ kHz} \pm 10\%$ ;  $f_{WDI} = 100\text{ Hz}$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>Supply Voltage</b>						
Operation range general		$V_S$	4.5		5.5	V
Operation range reset		$V_S$	1.5		16.0	V
<b>Supply Current</b>						
Lamp driver on, relay off	$T_{amb} = -40^\circ\text{C}$ $T_{amb} = 125^\circ\text{C}$				40 35	mA mA
Lamp driver off, relay on	$T_{amb} = -40^\circ\text{C}$ $T_{amb} = 125^\circ\text{C}$				25 20	mA mA
Lamp driver off, relay off	$T_{amb} = -40^\circ\text{C}$ $T_{amb} = 125^\circ\text{C}$				15 10	mA mA
<b>Auxiliary Ground (AUX GND)</b>						
AUX GND offset voltage operation range	$T_{amb} = -40^\circ\text{C}$ $T_{amb} = 90^\circ\text{C}$ $T_{amb} = 125^\circ\text{C}$		-1.2 -0.65 -0.5		1.2 1.0 0.8	V V V
AUX GND offset voltage to GND	$I_{AUX} = -600\text{ mA}$		-1.7		3.0	V
<b>Digital Inputs (LA1I, LA2I, REL1 and WDI)</b>						
Detection low			-0.2		$0.2 \times V_S$	V
Detection high			$0.7 \times V_S$		$V_S + 0.5\text{ V}$	V
Resistance to $V_S$			10		40	kΩ
Input current low	Input voltage = 0 V		100		550	μA
Input current high	Input voltage = $V_S$		-5		5	μA

## Electrical Characteristics (Continued)

$V_S = 5\text{ V}$ ,  $T_{\text{amb}} = -40\text{ to }+125^\circ\text{C}$ ; reference pin is GND;  $f_{\text{intern}} = 100\text{ kHz} + 50\% - 45\%$ ,  $f_{\text{WDC}} = 10\text{ kHz} \pm 10\%$ ;  $f_{\text{WDI}} = 100\text{ Hz}$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>Digital Outputs; Lamp Driver Feedbacks (FBLA1, FBLA2)</b>						
Voltage low	$I \leq 1.6\text{ mA}$		0		0.5	V
Voltage high	$I \leq 10\text{ A}$ $10\text{ A} \leq I \leq 1.6\text{ mA}$		$0.8 \times V_S$ $0.7 \times V_S + 0.1$		$V_S$	V
Threshold voltage detection			$0.4 \times V_S$		$0.5 \times V_S$	V
Threshold current detection			10		50	mA
<b>Digital Outputs (PRES and NRES)</b>						
Voltage high	$I \leq 100\text{ A}$		$0.7 \times V_S + 0.1$		$V_S$	V
Voltage low	$I \leq 1\text{ mA}$		0		0.3	V
<b>Digital Output (ENO) with Open Collector</b>						
Saturation voltage low	$I \leq 25\text{ mA}$		0		0.3	V
Clamping voltage			26		30	V
Current limit low			25			mA
Leakage current	$V_{\text{ENO}} = 5\text{ V}$ $V_{\text{ENO}} = 16\text{ V}$ $V_{\text{ENO}} = 26\text{ V}$				20 100 200	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
<b>Lamp Drivers (LA10 and LA20) with Integrated Pull-up Resistor</b>						
Saturation voltage	$I \leq 125\text{ mA}$ ; $V_S = 5\text{ V}$ $I \leq 125\text{ mA}$ ; $V_S = 0\text{ V}$				0.5 1.5	V V
Saturation voltage 250 mA requires enhanced heat sink	$I \leq 250\text{ mA}$ ; $V_S = 5\text{ V}$ $I \leq 250\text{ mA}$ ; $V_S = 0\text{ V}$ $I \leq 250\text{ mA}$ ; no GND				1.0 2.0 3.0	V V V
Maximum load current	$T_{\text{amb}} = 90^\circ\text{C}$ $T_{\text{amb}} = 125^\circ\text{C}$		250 180			mA mA
Clamping voltage			26		30	V
Leakage current	$V_{\text{LA10, LA20}} = 16\text{ V}$ $V_{\text{LA10, LA20}} = 26\text{ V}$				1 3	mA mA
Threshold current limitation			0.5		1.0	A
Pull-up resistor			2		17	k $\Omega$
<b>Relay Driver (RELO)</b>						
Saturation voltage	$I \leq 250\text{ mA}$				0.5	V
Maximum load current	$T_{\text{amb}} = 90^\circ\text{C}$ $T_{\text{amb}} = 125^\circ\text{C}$		250 200			mA mA
Clamping voltage			26		30	V
Leakage current	$V_{\text{Batt}} = 16\text{ V}$ $V_{\text{Batt}} = 26\text{ V}$				20 200	$\mu\text{A}$ $\mu\text{A}$
<b>Reset and <math>V_S</math> Control</b>						
Lower reset level		$V_S$	4.5		4.8	V
Upper reset level		$V_S$	5.2		5.5	V
Hysteresis			25			mV
Reset debounce time			120		500	$\mu\text{s}$

**Electrical Characteristics (Continued)**

$V_S = 5\text{ V}$ ,  $T_{amb} = -40\text{ to }+125^\circ\text{C}$ ; reference pin is GND;  $f_{intern} = 100\text{ kHz} + 50\% - 45\%$ ,  $f_{WDC} = 10\text{ kHz} \pm 10\%$ ;  $f_{WDI} = 100\text{ Hz}$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Reset delay			20		80	ms
<b>Watchdog Timing</b>						
Feedback reaction time (FBLA1, FBLA2)	No fault, edge at LA11, LA21	$t_{FB}$	2.56		12.8	ms
Minimum lamp input toggle time for a secure feedback reaction	No fault, pulse at LA11, LA21	$t_{P,FB}$	10.24			ms
Power-on-reset prolongation time		$t_{POR}$	34.3		103.1	ms
Detection time for RC-oscillator fault	$V_{RC} = \text{constant}$	$t_{RCerror}$	81.9		246	ms
Time interval for over-/undervoltage detection		$t_{D,OUV}$	0.16		0.64	ms
Reaction time of NRES output on over-/undervoltage		$t_{R,OUV}$	0.187		0.72	ms
Minimum toggle time for a secure broken ground detection		$t_{P,BGND}$	13.3			$\mu\text{s}$
Maximum reaction time for broken ground detection		$t_{R,BGND}$			100	$\mu\text{s}$
Nominal frequency for WDI	$f_{RC} = 100 \times f_{WDI}$	$f_{WDI}$	10		130	Hz
Nominal frequency for RC	$f_{WDI} = 1/100 \times f_{RC}$	$f_{RC}$	1		13	kHz
Minimum pulse duration for a secure WDI input pulse detection		$t_{P,WDI}$	182			$\mu\text{s}$
Frequency range for a correct WDI signal		$f_{WDI}$	64.7		112.5	Hz
Number of incorrect WDI trigger counts for locking the outputs		$n_{lock}$		3		
Number of correct WDI trigger counts for releasing the outputs		$n_{release}$		3		
Detection time for a stuck WDI signal	$V_{WDI} = \text{constant}$	$t_{WDIerror}$	24.5		25.5	ms
<b>Watchdog Timing Relative to <math>f_{RC}</math></b>						
Minimum pulse duration for a securely WDI input pulse detection				2		cycles
Frequency range for a correct WDI signal			80		170	cycles
Hysteresis range at the WDI ok margins				1		cycle
Detection time for a stuck WDI signal	$V_{WDI} = \text{constant}$		250		251	cycles

## Protection Against Transient Voltages According to ISO TR 7637-3 Level 4 (Except Pulse 5)

Pulse	Voltage	Source Resistance <sup>(1)</sup>	Rise Time	Duration	Amount
1	-110 V	10 Ω	100 V/s	2 ms	15.000
2	+110 V	10 Ω	100 V/s	0.05 ms	15.000
3a	-160 V	50 Ω	30 V/ns	0.1 s	1 h
3b	+150 V	50 Ω	20 V/ns	0.1 s	1 h
5	40 V	2 Ω	10 V/ms	250 ms	20

Notes: 1. Lamp drivers: 1.2 Ω lamps need to be added to the source resistance.  
 Relay driver: relay coil with  $R_{\min} = 70 \Omega$  need to be added to the source resistance.

### Application Hints

- The lamp output pins LA1O and LA2O may need to be protected by external protection diodes against reversed battery (e.g., BAV 202) in order to avoid a reset during negative pulses.
- If pilot lamps with a wattage of  $P > 1.2 \text{ W}$  are connected, external Zener diodes are mandatory.

## Timing Diagrams

Figure 7. Watchdog in Too Fast Condition

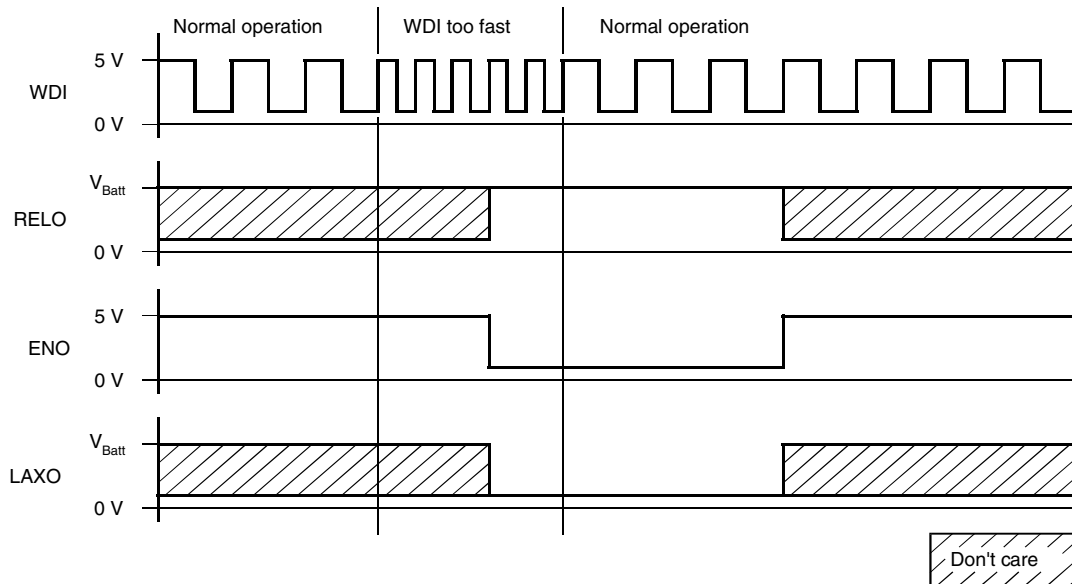


Figure 8. Watchdog in Too Slow Condition

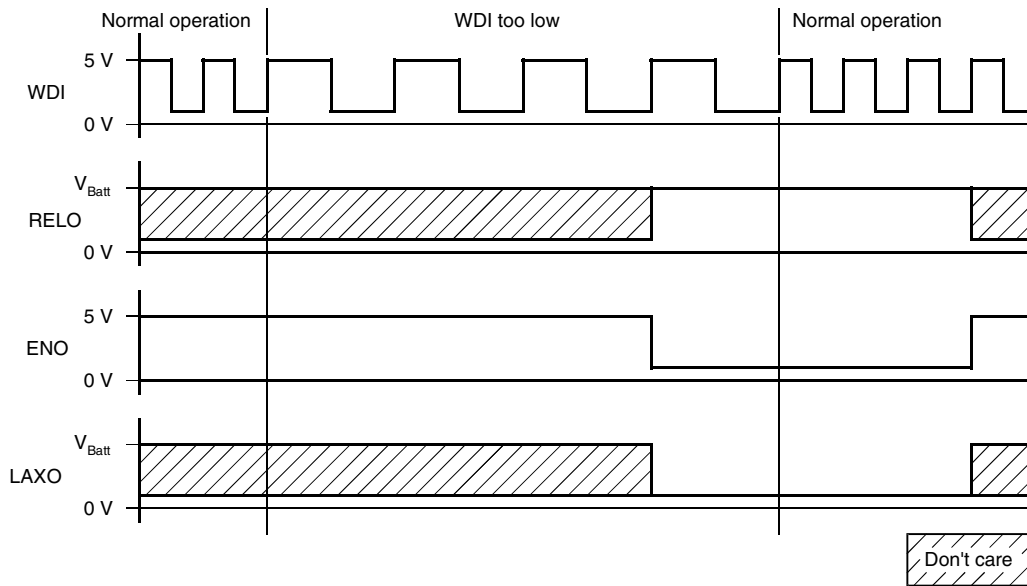
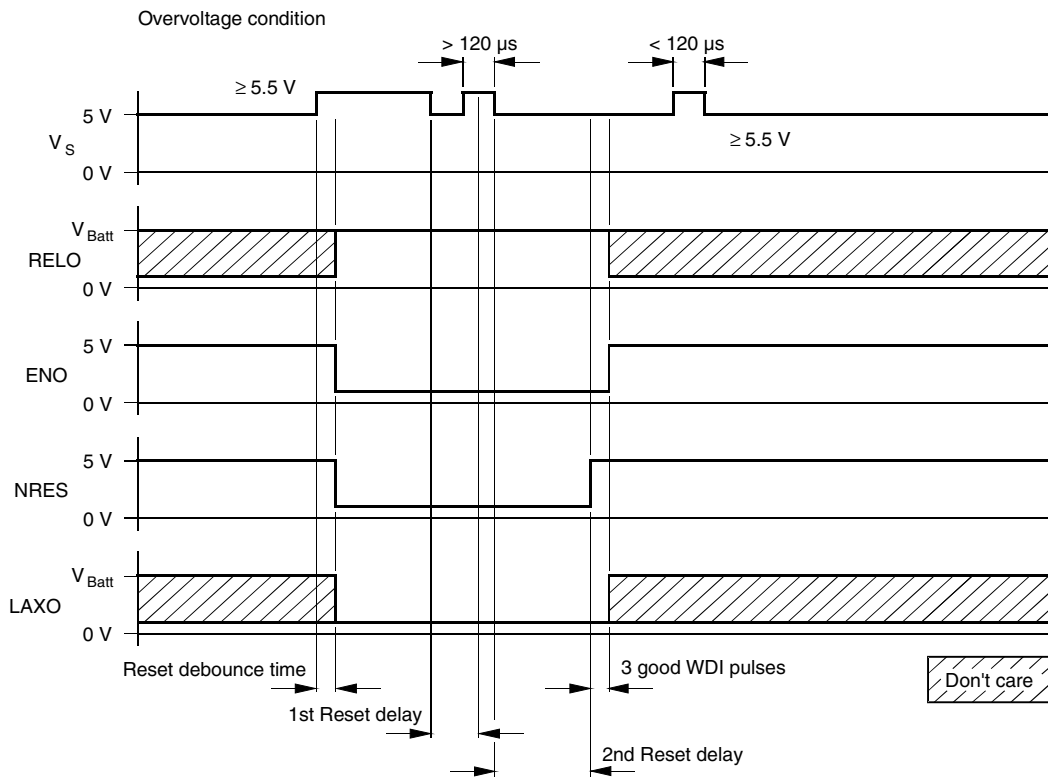
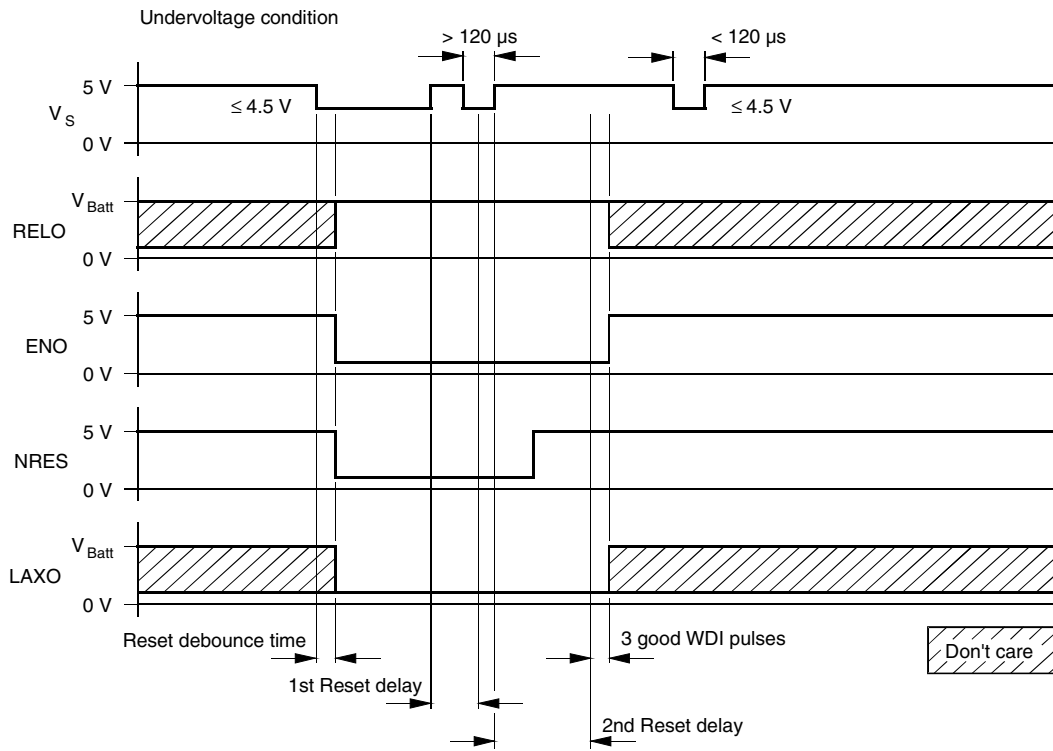


Figure 9. Overvoltage Condition





**Figure 10. Undervoltage Condition**



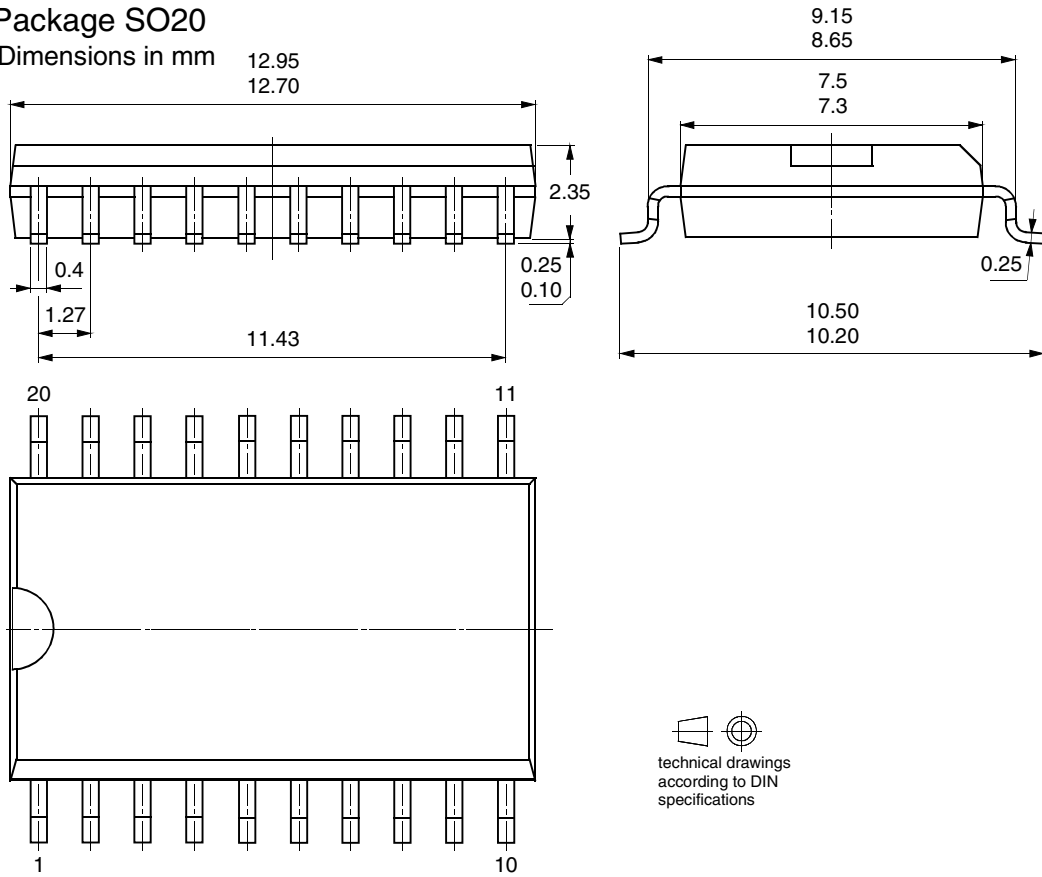
### Ordering Information


Extended Type Number	Package	Remarks
U6809B	SO20 special lead frame	–

### Package Information

Package SO20

Dimensions in mm



  
 technical drawings  
 according to DIN  
 specifications



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