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DATA SHEET

UAA3220TS
Frequency Shift Keying (FSK)/Amplitude Shift Keying (ASK) receiver

Product specification
Supersedes data of 1998 April 10
File under Integrated Circuits, IC01

1999 Jan 22

Philips Semiconductors

PHILIPS

Frequency Shift Keying (FSK)/Amplitude Shift Keying (ASK) receiver

UAA3220TS

FEATURES

- Low cost single-chip ASK or FSK receiver
- Superheterodyne architecture with high integration level
- Few external low cost components and crystal required
- Wide supply voltage range
- Low power consumption
- Wide frequency range, 250 to 920 MHz
- High sensitivity
- IF bandwidth determined by application
- High selectivity
- Automotive temperature range
- SSOP24 package.

Applications

- Keyless entry systems
- Car alarm systems
- Remote control systems
- Security systems
- Telemetry systems
- Wireless data transmission
- Domestic appliance.

GENERAL DESCRIPTION

The UAA3220TS is a fully integrated single-chip receiver, primarily intended for use in VHF and UHF systems. It supports both Amplitude Shift Keying (ASK) and Frequency Shift Keying (FSK) demodulation.
By connecting DEMO1 (pin 10) to ground during realisation of the receiver module the UAA3220TS works as an ASK receiver (see Fig.10). By connecting pin 10 as shown in Fig.9 the UAA3220TS works as an FSK receiver.
The UAA3220TS incorporates a crystal stabilized local oscillator, frequency multiplier, balanced mixer, post mixer amplifier, limiter, Received Signal Strength Indicator (RSSI), FSK demodulator, data filter, data slicer and power down circuit.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.7	–	5.5	V
I_{CC}	supply current	$f_{i(RF)}$ = 433.92 MHz; FSK mode				
		operating mode on; V_{PWD} = 0 V	2.8	4.3	5.8	mA
		operating mode off; $V_{PWD} = V_{CC}$	–	3	30	μA
ASK mode						
$P_{i(max)(ASK)}$	maximum input power	BER ≤ 3%	−22	−16	−10	dBm
$\Phi_{i(ASK)}$	sensitivity into pin MIXIN	$f_{i(RF)}$ = 433.92 MHz; BER ≤ 3%	–	−119	−113	dBm
FSK mode						
$P_{i(max)(FSK)}$	maximum input power	BER ≤ 3%	−6	0	+1	dBm
$\Phi_{i(FSK)}$	sensitivity into pin MIXIN	$f_{i(RF)}$ = 433.92 MHz; BER ≤ 3%	–	−103	−100	dBm

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA3220TS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

BLOCK DIAGRAM

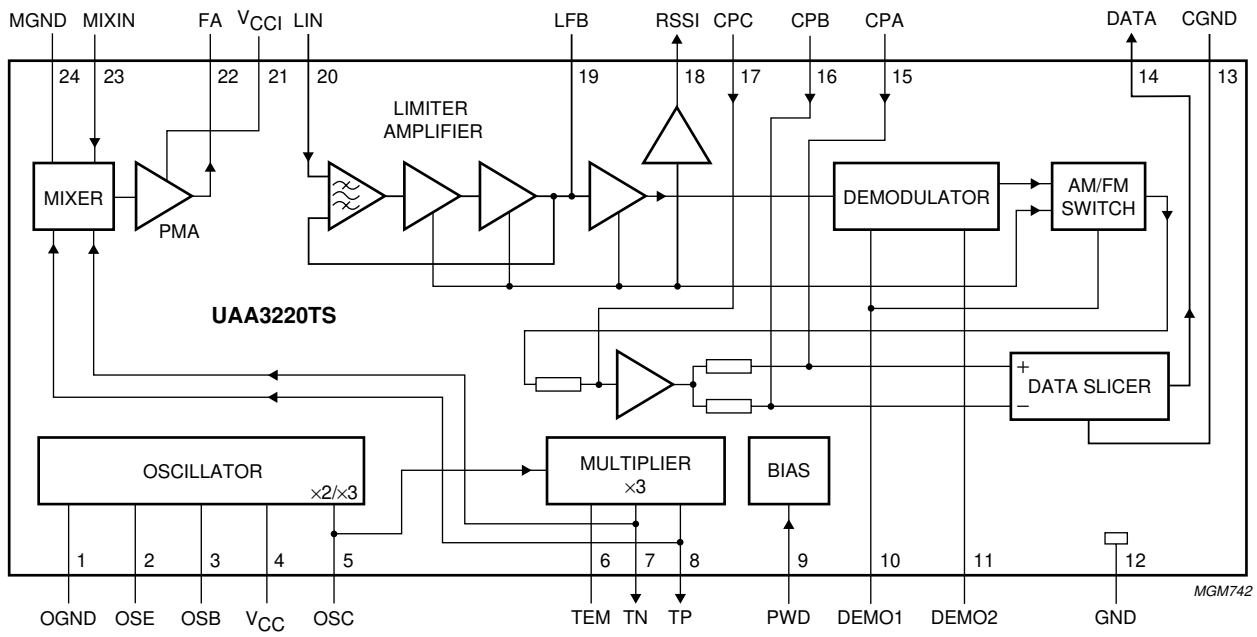


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OGND	1	oscillator ground
OSE	2	oscillator emitter
OSB	3	oscillator base
V_{CC}	4	positive supply voltage
OSC	5	oscillator collector
TEM	6	frequency multiplier emitter resistor
TN	7	frequency multiplier negative output
TP	8	frequency multiplier positive output
PWD	9	power down control input
DEMO1	10	FM demodulator 1, ASK/FSK switch
DEMO2	11	FM demodulator 2
GND	12	general ground
CGND	13	comparator ground
DATA	14	data output
CPA	15	comparator input A
CPB	16	comparator input B
CPC	17	comparator input C
RSSI	18	RSSI output
LFB	19	limiter feedback
LIN	20	limiter input
V_{CCI}	21	IF amplifier positive supply voltage
FA	22	IF amplifier output
MIXIN	23	mixer input
MGND	24	mixer ground

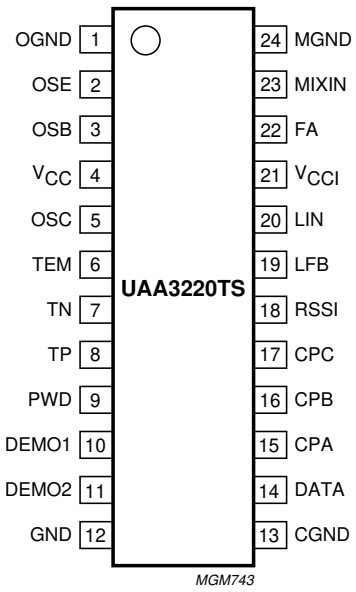


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Mixer

The mixer is a single-balanced emitter-coupled mixer with internal biasing. Matching of the RF source impedance to the mixer input requires an external matching network.

Oscillator

The oscillator is based on a transistor connected in common collector configuration followed by a cascode stage driving a tuned circuit. The voltage at this tuned circuit drives the frequency multiplier. The bias current of the oscillator is set by an off-chip resistor (R40 in the application diagram of Fig.9) to a typical value of 260 μA at 433.92 MHz (R40 = 1.8 kΩ). The oscillator frequency is controlled by an off-chip overtone crystal (X40). Off-chip capacitors between base and emitter (C42) and ground (C41) make the oscillator transistor appear as having negative resistance at small signal levels. This causes the oscillator to start. A parallel resonance circuit (L40 and C41) connected to the emitter of the oscillator transistor prevents oscillation at the fundamental frequency of the crystal. The LC tank circuit at the output of the oscillator is used to select either the fundamental, the second or the third harmonic of the oscillator frequency.

Frequency multiplier

The frequency multiplier is an emitter-coupled transistor pair driving an off-chip balanced tuned circuit. The bias current of this emitter coupled pair is set by an off-chip resistor (R50) to a typical value of 350 μA at 433.92 MHz (R50 = 1.2 kΩ). The oscillator output signal is AC-coupled to one of the inputs of the emitter-coupled pair. The other input is connected to ground via an on-chip capacitor. The output voltage of the frequency multiplier drives the switching stage of the mixer. The bias voltage at this point is set by an off-chip resistor (R51) to allow sufficient voltage swing at the mixer outputs.

Post mixer amplifier

The Post Mixer Amplifier (PMA) is a differential input, single-ended output amplifier. Amplifier gain is provided in order to reduce the influence of the limiter noise figure on the total noise figure.

Limiter

The limiter is a single-ended input multiple stage amplifier with high total gain. Amplifier stability is achieved by means of an external DC feedback capacitor (C21), which is also used to determine the lower limiter cut-off frequency. An RSSI signal proportional to the limiter input signal is provided. Figure 3 shows the DC voltage at pin 18 (RSSI) as a function of the input voltage (RMS value) at pin 20 (LIN). It also gives the typical IF of 10.7 MHz. The lower knee of the level curve (see Fig.3) is determined by the effective noise bandwidth and is, consequently, slightly higher.

IF filter

IF filtering with high selectivity is realized by means of an external ceramic filter (X20), which feeds the IF from the PMA to the limiter.

FM demodulator

Coming from the limiter the FSK signal is fed differential to the input of the FM demodulator. After buffering the signal is fed to a phase detector. The phase shift is generated by an external LC combination connected to DEMO1 (pin 10) and DEMO2 (pin 11). The baseband signal is coupled out single ended via an output buffer and is fed to the FSK input of the ASK/FSK switch.

ASK/FSK switch

The selection of either ASK or FSK reception will be done by the DEMO1 (pin 10). Grounding this pin to 0 V will switch the IC to ASK mode. Additional the FM demodulator and parts of the data slicer will be switched off. In FSK mode DEMO1 (pin 10) is connected to DEMO2 (pin 11) via a LC combination (see Fig.9).

Data filters

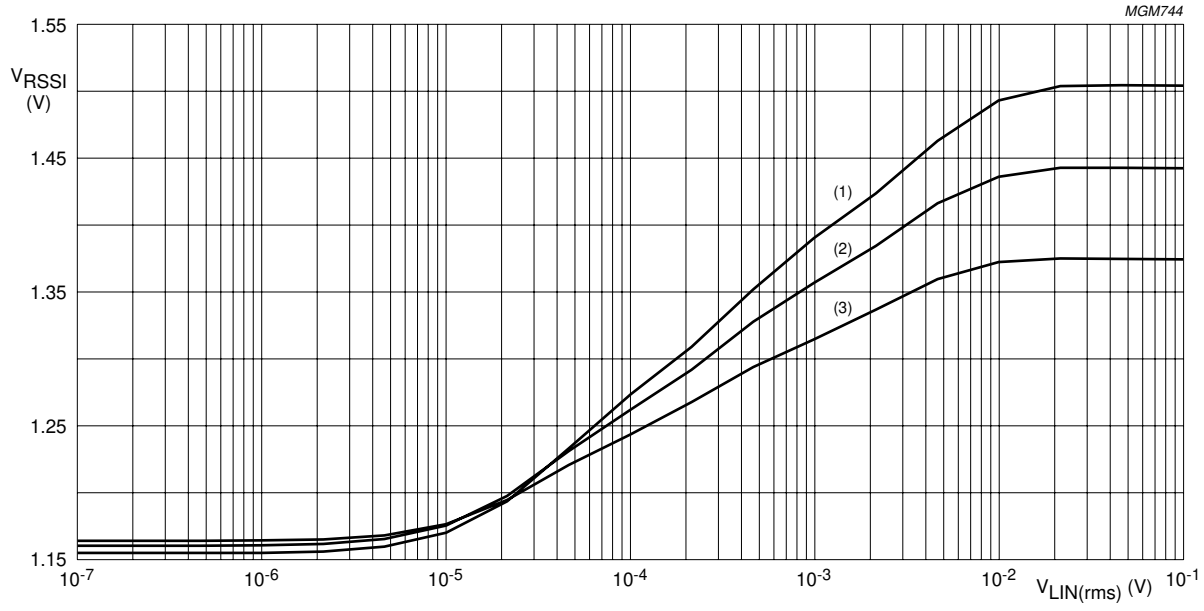
After demodulation a two-stage data filtering circuit is provided in order to suppress unwanted frequency components. Two RC low-pass filters with on-chip resistors are provided which are separated by a buffer stage.

Data slicer

Data detection is provided by means of a level comparator with adaptive slice reference. After the first data filter stage the pre-filtered data is split into two paths. One passes the second data filter stage and is fed to the positive comparator input. The other path is fed to an integration circuit with a large time constant in order to derive the average value (DC component) as an adaptive slice reference which is presented to the negative comparator input. The internal buffer provides 13 dB AC voltage gain. The adaptive reference allows to detect the received data over a large range of noise floor levels. The integration circuit consists of a simple RC low-pass filter with on-chip resistors. The data slicer output is designed with internal pull-up.

RSSI buffer

The RSSI buffer is an amplifier with a voltage gain of 0 dB. At FSK receive mode the RSSI output provides a field strength indication. It has an output impedance of 10 kΩ. Figure 3 shows the level curve (RSSI curve) as a function of the limiter input voltage (RMS value).



(1) T_{amb} = 85 °C.
(2) T_{amb} = 27 °C.
(3) T_{amb} = −40 °C.

Fig.3 Level curve V_{RSSI} as a function of $V_{LIN(rms)}$.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.3	+8.0	V
$P_{i(max)}$	absolute maximum input power		–	3	dBm
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C
V_{es}	electrostatic handling	note 1			
	pins 3 and 6		−50	+50	V
	pin 2		−100	+100	V
	pin 5		−250	+150	V
	pin 23		−200	+250	V
	all other pins		−250	+250	V

Note

1. Machine model: C = 200 pF, R = 0 Ω and L = 0.75 μH; pins are connected to GND and V_{CC}.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	125	K/W

DC CHARACTERISTICS

V_{CC} = 2.7 V; T_{amb} = 25 °C; for application diagram see Figs 9 and 10; crystal disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage		2.7	–	5.5	V
I_{CC}	supply current	operating mode on; V_{PWD} = 0 V; notes 1 and 2				
		FSK demodulation; note 3	2.8	4.3	5.8	mA
		ASK demodulation; note 4	2.5	3.7	4.9	mA
		operating mode off; $V_{PWD} = V_{CC}$	–	3	30	μA
V_{PWD}	voltage on pin PWD	operating mode on (receiving mode)	0	–	300	mV
		operating mode off (sleep mode)	V_{CC} – 0.3	–	V_{CC}	V
I_{PWD}	current into pin PWD	operating mode on (receiving mode); V_{PWD} = 0 V	–30	–10	–3	μA
		operating mode off (sleep mode); $V_{PWD} = V_{CC}$	–	2	15	μA
Oscillator						
V_{OSE}	DC voltage at pin 2	independent of oscillator	0.33	0.38	0.43	V
V_{OSB}	DC voltage at pin 3	independent of oscillator	1.05	1.15	1.25	V
Multiplier						
V_{TEM}	DC voltage at pin 6	independent of oscillator	0.33	0.39	0.45	V
$V_{TN,TP}$	DC voltage at pins 7 and 8	independent of oscillator	2.01	2.21	2.41	V
Mixer						
V_{MIXIN}	DC voltage at pin 23	independent of oscillator	0.68	0.78	0.88	V
Post mixer amplifier						
V_{FA}	DC voltage at pin 22	independent of oscillator	1.10	1.25	1.40	V
Limiter						
V_{LIN}	DC voltage at pin 20	independent of oscillator	1.85	1.95	2.05	V
V_{LFB}	DC voltage at pin 19	independent of oscillator	1.85	1.95	2.05	V
V_{RSSI}	DC voltage at pin 18	independent of oscillator	1.00	1.16	1.32	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Demodulator						
$V_{DEMO1,2}$	DC voltage at pins 10 and 11	independent of oscillator; note 5	2.00	2.24	2.48	V
$V_{DEMO1(ASK)}$	DC voltage at pin 10 to switch in ASK mode		0	–	300	mV
Data filter and slicer						
$V_{CPA,CPB,CPC}$	DC voltage at pins 15, 16 and 17	ASK mode	1.27	1.42	1.57	V
		FSK mode; note 6	1.81	2.01	2.21	V
$V_{OH(DATA)}$	HIGH-level output voltage at pin 14	I_{DATA} = −10 μA	V_{CC} − 0.5	–	V_{CC}	V
$V_{OL(DATA)}$	LOW-level output voltage at pin 14	I_{DATA} = 200 μA	0	–	0.6	V

Notes

1. For $f_{i(RF)}$ = 868.35 MHz all values + 0.6 mA.
2. Crystal connected; oscillator and multiplier active.
3. Pin DEMO1 connected to pin DEMO2 via tank circuit.
4. Pin DEMO1 short circuited to ground.
5. The given values are applicable for FSK reception mode. In ASK mode pin 10 is short circuited to ground.
6. No modulation and f_{IF} = 10.7 MHz.

AC CHARACTERISTICS

V_{CC} = 2.7 V; T_{amb} = 25 °C; for application diagram see Figs 9 and 10; $f_{i(RF)}$ = 433.92 MHz (see Table 4) and $f_{i(RF)}$ = 868.35 MHz (see Table 5); f_{mod} = 1 kHz square wave; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System performance						
$f_{i(RF)}$	RF input frequency		250	–	920	MHz
f_{IF}	IF frequency		10.56	10.7	10.84	MHz
$P_{i(max)}$	maximum input power		–	–	3	dBm
		ASK mode; BER ≤ 3%; notes 1 and 2	–22	–16	–10	dBm
		FSK mode; BER ≤ 3%; notes 2 and 3	–6	0	+1	dBm
P_{SPUR}	spurious radiation	note 4	–	–	–57	dBm
f_{DATA}	data frequency	note 5	–	1	–	kHz
$t_{on(RX)}$	receiver turn-on time	notes 6 and 7				
		$f_{i(RF)}$ = 433.92 MHz	–	6	10	ms
		$f_{i(RF)}$ = 868.35 MHz	–	3	7	ms
V_{RSSI}	RSSI voltage		1.1	–	1.6	V
ASK mode						
$\Phi_{i(ASK)}$	input sensitivity directly into pin MIXIN	BER ≤ 3%; notes 1 and 2				
		$f_{i(RF)}$ = 433.92 MHz	–	–119	–113	dBm
		$f_{i(RF)}$ = 868.35 MHz	–	–116	–110	dBm
FSK mode						
$\Phi_{i(FSK)}$	input sensitivity directly into pin MIXIN	BER ≤ 3%; notes 2 and 3	–	–103	–100	dBm
Δf	frequency deviation (peak value)		4	10	75	kHz
$\Delta\Phi_{(FSK)(max)}$	maximum sensitivity degradation	Δf = 4 kHz	–	–	3	dB
G_{dem}	demodulator gain	note 8	0.75	1.0	1.25	$\frac{mV}{kHz}$
Mixer and post mixer amplifier						
Z_i	input impedance of mixer	$f_{i(RF)}$ = 433.92 MHz	–	600	–	Ω
		$f_{i(RF)}$ = 868.35 MHz	–	300	–	Ω
$IP3_{PMA}$	interception point (mixer + PMA)		–38	–30	–	dBm
G_{PMA}	gain (mixer + PMA)	note 9	40	42	50	dB
$Z_{o(IF)}$	output impedance of IF amplifier		280	330	380	Ω

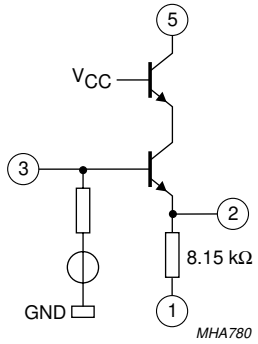
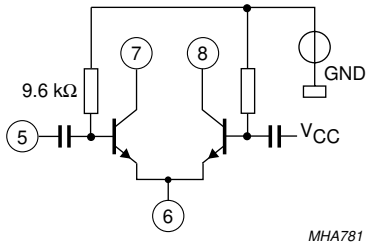
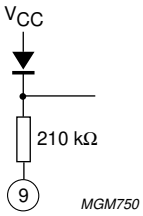
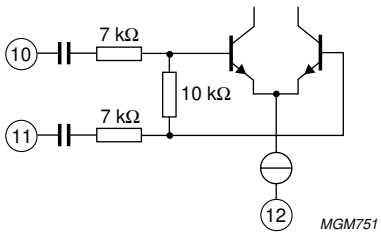
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiter						
$R_{i(LIN)}$	limiter input resistance		40	48	56	kΩ
Buffer						
R_{CPC}	data buffer output resistance at pin 17		24	30	36	kΩ
G_{buffer}	data buffer AC gain		12	13	14	dB
$R_{CPA,CPB}$	data buffer output resistance at pins 15 and 16		120	150	180	kΩ
Data slicer; see Chapter “DC characteristics”						
B_{ds}	internal data slicer bandwidth		50	–	100	kHz

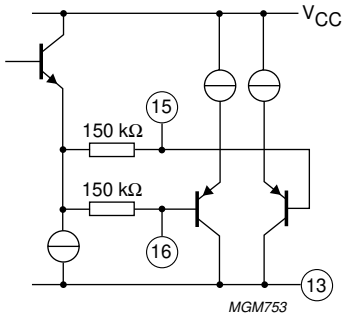
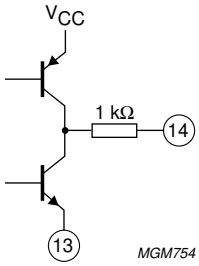
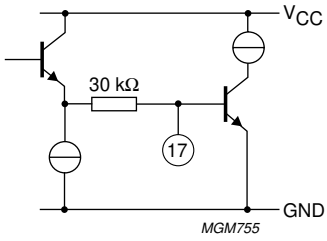
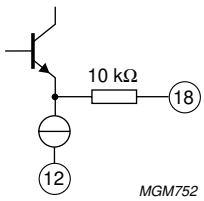
Notes

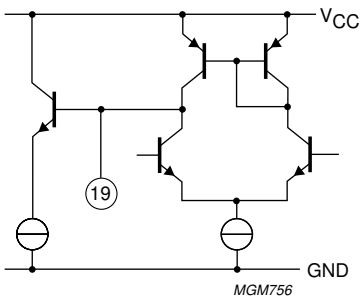
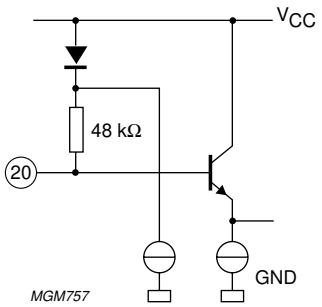
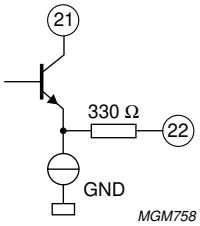
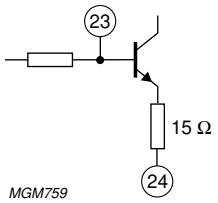
1. 100% AM modulation (ASK); available power from generator into a 50 Ω load.
2. With external matching network, to transform the impedance to 50 Ω.
3. Δf = 10 kHz; available power from generator into a 50 Ω load.
4. Measured at the RF input connector of the test board into a 50 Ω load; $f_{i(RF)}$ = 25 MHz to 1 GHz.
5. The data frequency range can be varied by changing C30 to C32 (see Figs 9 and 10) to match other bit rates. Data frequency determined by data slicer application.
6. t_{on} = 50 ms; t_{off} = 138 ms; P = P_{sens} + 3 dB.
7. The given turn-on time is only valid during strobing by pin PWD; if the IC is strobed on and off by the supply voltage the turn-on time will be longer.
8. LC tank circuit (L60, C60) tuned to maximum phase slope.
9. G_{PMA} is typically 6 dB lower when measured in the application, because of the load of the ceramic filter.

INTERNAL CIRCUITRY

Table 1 Equivalent pin circuits and pin voltages for rough test of printed-circuit board; V_{CC} = 2.7 V; no input signal

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
1	OGND	0	
2	OSE	0.38	
3	OSB	1.15	
5	OSC	2.7	
4	V_{CC}	2.7	
6	TEM	0.39	
7	TN	2.21	
8	TP	2.21	
9	PWD	–	
10	DEMO1	2.24	
11	DEMO2	2.24	
12	GND	0	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
13	CGND	0	
15	CPA	1.95	
16	CPB	1.95	
14	DATA	–	
17	CPC	1.95	
18	RSSI	1.16	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
19	LFB	1.95	
20	LIN	1.95	
21	V_{CCI}	2.7	
22	FA	1.25	
23	MIXIN	0.78	
24	MGND	0	

TEST INFORMATION

Tuning procedures

TUNING PROCEDURE FOR AC TESTS

1. Turn on the signal generator ($f_{i(RF)}$ = 433.92 or 868.35 MHz; no modulation; RF input level = −50 dBm).
2. Tune first C50 (multiplier tank circuit), second C11 (RF stage input) to obtain a peak IF voltage at pin FA.

TUNING PROCEDURE FOR ASK RECEPTION

1. Make sure that pin DEMO1 is short circuited to ground.
2. Turn on ASK modulation and check that data is appearing on the DATA output pin and proceed with the AC tests.

TUNING PROCEDURE FOR FSK RECEPTION

1. Make sure that pins DEMO1 and DEMO2 are connected by the LC tank circuit.
2. Turn on FSK modulation (Δf = 10 kHz; RF input level = −103 dBm).
3. Tune C61 (or L60) (phase shifter LC tank circuit) to obtain a peak LF voltage at pin CPC.
4. Check that data is appearing on pin DATA and proceed with the AC tests.

AC test conditions

Table 2 Test signals

The reference signal level P_{ref} for the following tests is defined as the minimum input level in dBm to give a BER $\leq 3 \times 10^{-2}$ (e.g. 60 bit errors per second for 2000 bits/s). All test signal levels refer to 50 Ω load condition.

TEST SIGNAL	FREQUENCY (MHz)	DATA SIGNAL	MODULATION	MODULATION INDEX	FREQUENCY DEVIATION
1	433.92/868.35	1000 Hz square wave	AM (ASK)	100%	–
2	433.92/868.35	1000 Hz square wave	FM (FSK)	–	10 kHz
3	433.92/868.35	–	no modulation	–	–
4	433.82/868.35	–	no modulation	–	–

Table 3 Tests and results

P_1 is the maximum available power from signal generator 1 at the input of the test board; P_2 is the maximum available power from signal generator 2 at the input of the test board.

TEST	GENERATOR		RESULT
	1	2	
ASK sensitivity into pin MIXIN (see Fig.5)	modulated test signal 1; $P_1 \leq -113$ dBm for $f_{i(RF)}$ = 433.92 MHz; $P_1 \leq -110$ dBm for $f_{i(RF)}$ = 868.35 MHz	–	BER $\leq 3 \times 10^{-2}$ (e.g. 60 bit errors per second for 2000 bits/s)
FSK sensitivity into pin MIXIN (see Fig.5)	modulated test signal 2; $P_1 \leq -100$ dBm	–	BER $\leq 3 \times 10^{-2}$ (e.g. 60 bit errors per second for 2000 bits/s)
Maximum input power for ASK (see Fig.5)	modulated test signal 1; $P_1 \geq -22$ dBm	–	BER $\leq 3 \times 10^{-2}$ (e.g. 60 bit errors per second for 2000 bits/s)
Maximum input power for FSK (see Fig.5)	modulated test signal 2; $P_1 \geq -6$ dBm	–	BER $\leq 3 \times 10^{-2}$ (e.g. 60 bit errors per second for 2000 bits/s)
Receiver turn-on time; see note 1 and Fig.4	modulated test signal 1 or 2; $P_1 = P_{ref} + 3$ dB	–	check that the first 10 bits are correct; error counting is started 10 ms after power down is switched into operating mode on
Interception point (mixer + PMA) see note 2 and Fig.6	test signal 3; $P_1 = -40$ dBm	test signal 4; $P_2 = P_1$	measure with high impedance probe at pin FA $IP3_{PMA} = P_1 + \frac{IM3}{2}$ dBm (for IM3 see Fig.6)
Spurious radiation; see note 3 and Fig.7	–	–	no spurious signals (25 MHz to 1 GHz) with level higher than maximum P_{SPUR}

Notes

1. The voltage at pin PWD of the test circuit alternates between operating mode: on (50 ms; 0 V) and off (138 ms; V_{CC}); see Fig.4.
2. Probe of spectrum analyzer connected to pin FA (pin 22).
3. Spectrum analyzer connected to the input of the test board.

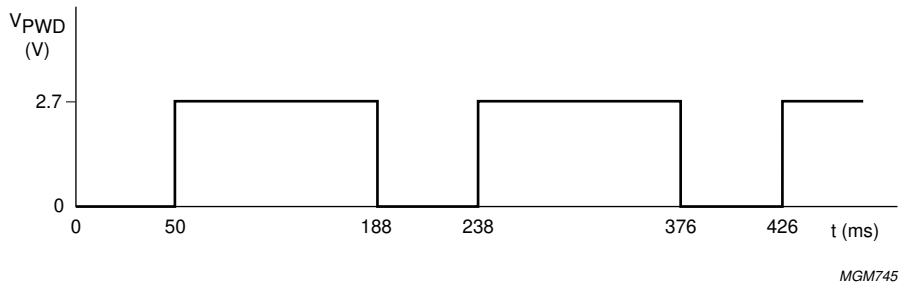
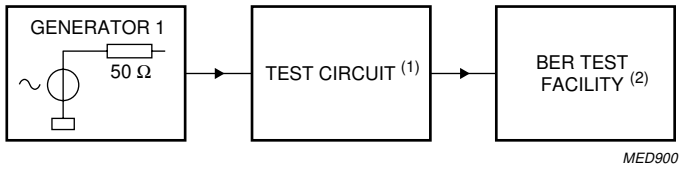
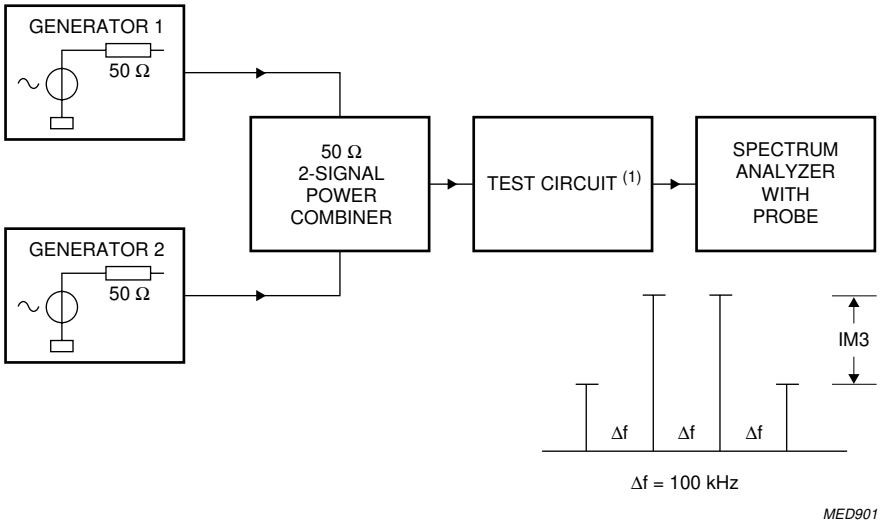


Fig.4 Timing diagram for pulsed power down voltage.



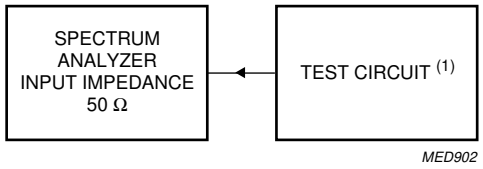
(1) For test circuit see Fig.9.
(2) For BER test facility see Fig.8.

Fig.5 Test configuration A (single generator).



(1) For test circuit see Fig.9.

Fig.6 Test configuration C (IP3).



(1) For test circuit see Fig.9.

Fig.7 Test configuration D (spurious radiation).

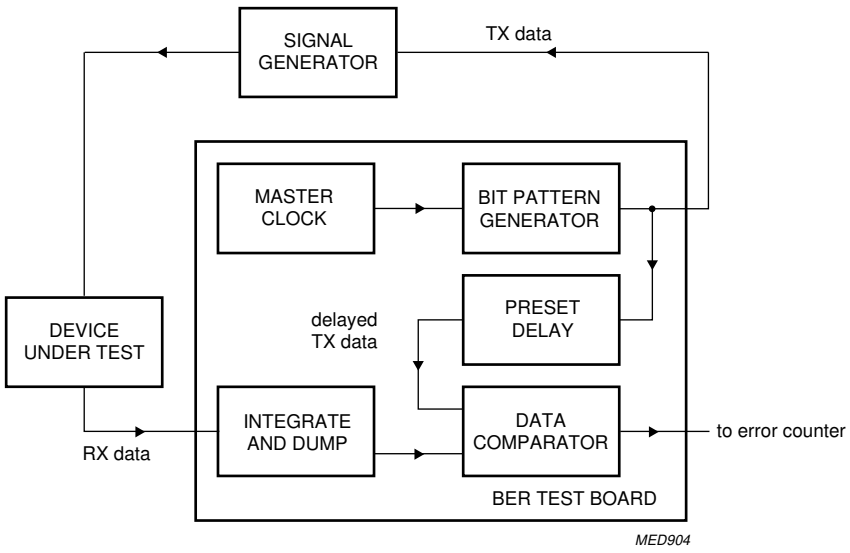


Fig.8 BER test facility.

APPLICATION INFORMATION

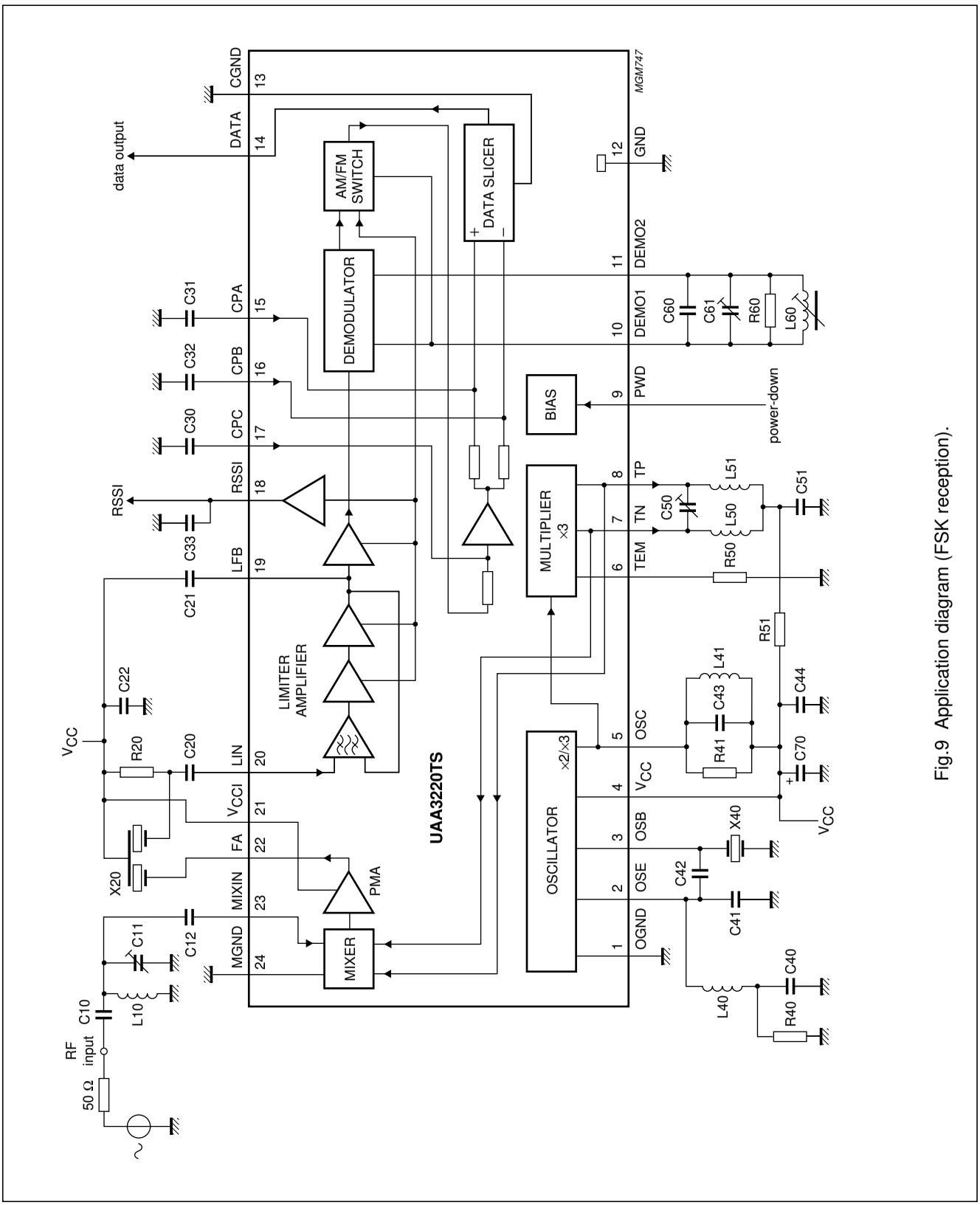


Fig.9 Application diagram (FSK reception).

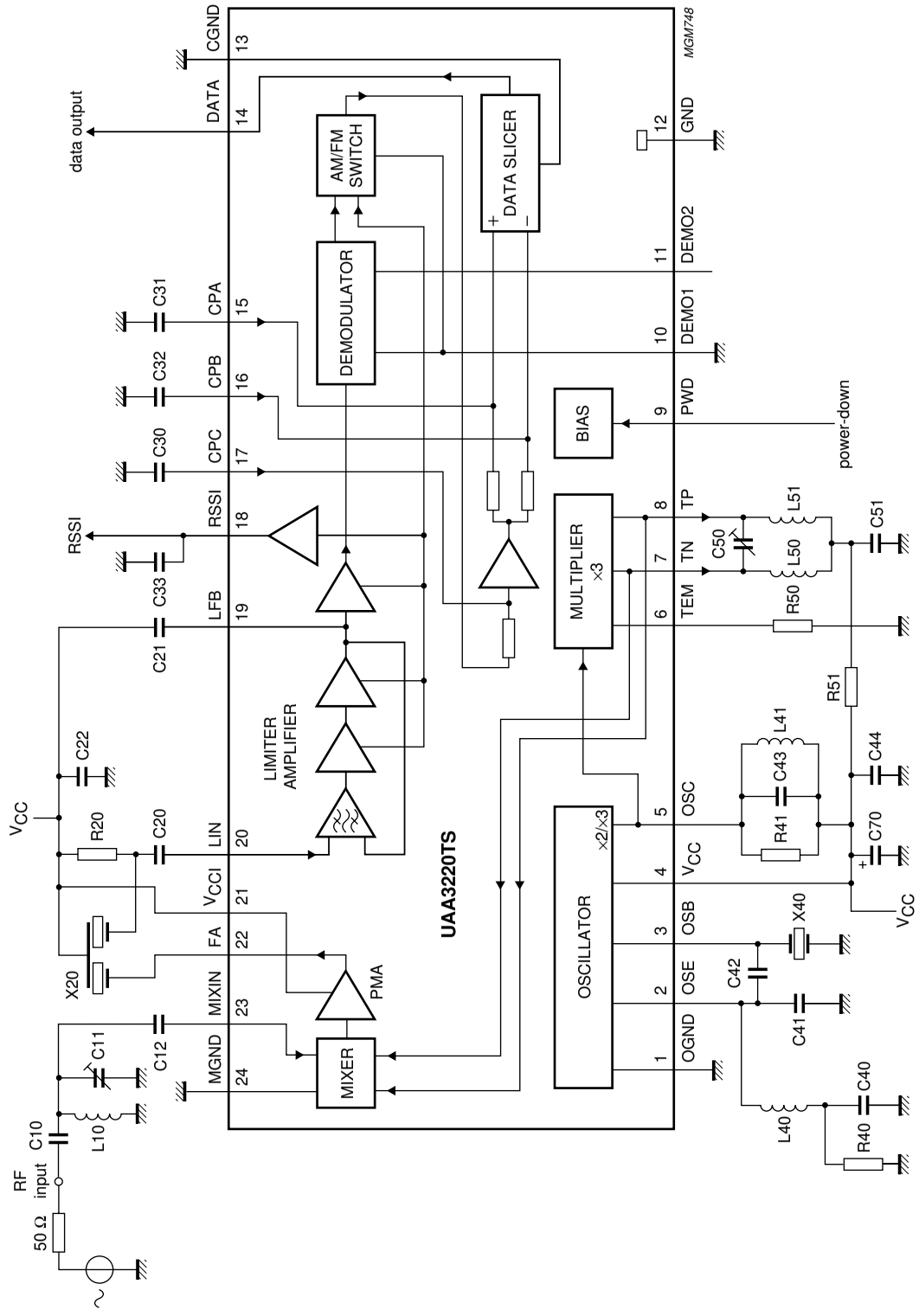


Fig.10 Application diagram (ASK reception).

Table 4 Component list for Figs 9 and 10; $f_{i(RF)}$ = 433.92 MHz

COMPONENT	COMPONENT CHARACTERISTICS					
	VALUE	TOLERANCE	TEMPERATURE COEFFICIENT (ppm/K)	LOSS FACTOR AT 1 MHz	QUALITY FACTOR	SELF RESONANCE FREQUENCY
R20	330 Ω	±2%	+50	–	–	–
R40	1.8 kΩ	±2%	+50	–	–	–
R41	not placed	–	–	–	–	–
R50	1.2 kΩ	±2%	+50	–	–	–
R51	1.5 kΩ	±2%	+50	–	–	–
R60	4.7 kΩ	±2%	+50	–	–	–
C10[1]	2.7 pF	±10%	0 ±30	$\tan\delta \leq 20 \times 10^{-4}$	–	–
C11	3 to 10 pF	–	0 ±300	$\tan\delta \leq 20 \times 10^{-4}$	–	–
C12	100 pF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C20	1 nF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C21	47 nF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C22	1 nF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C30	2.7 nF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C31	470 pF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C32	47 nF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C33	10 nF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C40	1 nF	±10%	0 ±30	$\tan\delta \leq 20 \times 10^{-4}$	–	–
C41[1]	15 pF	±10%	0 ±30	$\tan\delta \leq 20 \times 10^{-4}$	–	–
C42	15 pF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C43[1]	8.2 pF	±10%	0 ±30	$\tan\delta \leq 20 \times 10^{-4}$	–	–
C44	1 nF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C50	3 to 10 pF	–	0 ±300	$\tan\delta \leq 20 \times 10^{-4}$	–	–
C51	1 nF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C60[2]	82 pF	±10%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C61[2]	5 to 30 pF	–	0 ±300	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C70	not placed	–	–	–	–	–
L10[3]	8 nH	±5%	+25 to +125	–	≥140 at 150 MHz	≥3 GHz
L40	560 nH	±10%	+25 to +125	–	≥45 at 100 MHz	≥400 MHz
L41	100 nH	±10%	+25 to +125	–	≥60 at 350 MHz	≥1 GHz
L50[3]	8 nH	±5%	+25 to +125	–	≥140 at 150 MHz	≥3 GHz
L51[3]	8 nH	±5%	+25 to +125	–	≥140 at 150 MHz	≥3 GHz
L60[2]	2.2 μH	±10%	+25 to +125	–	≥37 at 7.9 MHz	≥150 MHz
X20	ceramic filter, Murata SFE 10.7 MA 5 A; see note 4					
X40	3rd overtone crystal, 70.5367 MHz; see note 5					

Notes

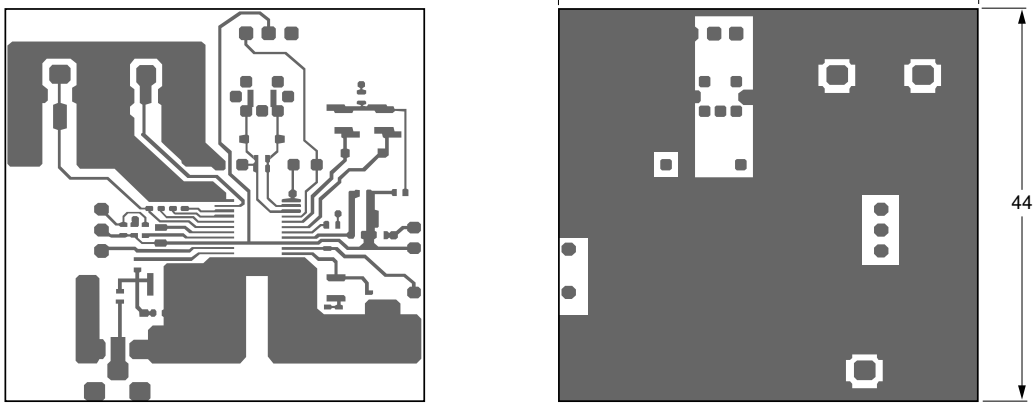
1. C10, C41 and C43 can be placed as tuning capacitors on the PCB.
2. C60, C61 and L60 can be substituted by an LC tank.
3. L10, L50 and L51 are 3 turn air coils.
4. 3 dB bandwidth: 280 ± 50 kHz; insertion loss: 4 dB typical and 6 dB maximum; spurious: 30 dB minimum at 8 to 12 MHz; input and output impedance: 330 Ω.
5. Motional resistance: $R_m \leq 20\ \Omega$; static capacitance: $C_0 \leq 6$ pF; load capacitance: $C_L = 6$ pF; loaded parallel resonance frequency: 70.5367 MHz; drive level dependency: $R_m \leq 20\ \Omega$ (1 nW ≤ P ≤ 1 mW).

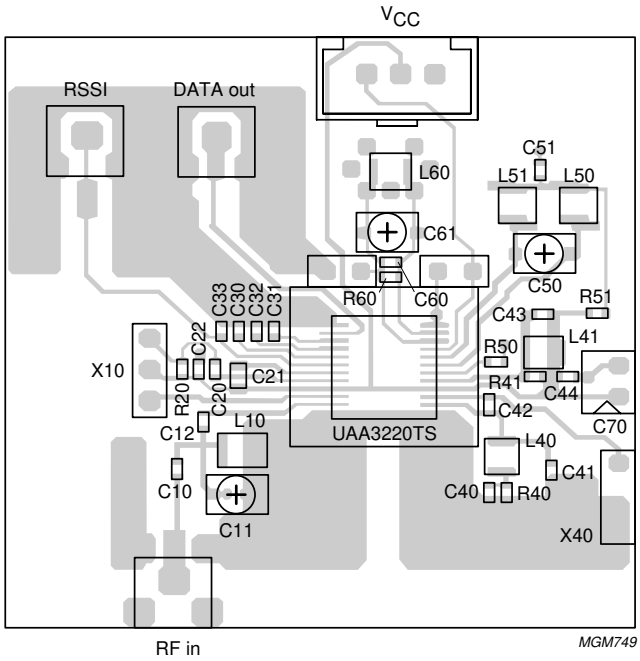
Table 5 Component list for Figs 9 and 10; $f_{i(RF)}$ = 868.35 MHz

COMPONENT	COMPONENT CHARACTERISTICS					
	VALUE	TOLERANCE	TEMPERATURE COEFFICIENT (ppm/K)	LOSS FACTOR AT 1 MHz	QUALITY FACTOR	SELF RESONANCE FREQUENCY
R20	330 Ω	±5%	≤±100	–	–	–
R40	1.5 kΩ	±5%	≤±100	–	–	–
R41	not placed	–	–	–	–	–
R50	390 Ω	±5%	≤±100	–	–	–
R51	330 Ω	±5%	≤±100	–	–	–
R60	4.7 kΩ	±5%	≤±100	–	–	–
C10	27 pF	±5%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C11	1.7 to 3 pF	–	0 ±300	$\tan\delta \leq 20 \times 10^{-4}$	–	–
C12	27 pF	±5%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C20	1 nF	±10%	±15%(1)	tan δ ≤ 2.5%	–	–
C21	47 nF	±10%	±15%(1)	tan δ ≤ 2.5%	–	–
C22	1 nF	±10%	±15%(1)	tan δ ≤ 2.5%	–	–
C30	3.3 nF	±10%	±15%(1)	tan δ ≤ 2.5%	–	–
C31	680 pF	±10%	±15%(1)	tan δ ≤ 2.5%	–	–
C32	10 nF	±10%	±15%(1)	tan δ ≤ 2.5%	–	–
C33	10 nF	±10%	±15%(1)	tan δ ≤ 2.5%	–	–
C40	1 nF	±10%	±15%(1)	tan δ ≤ 2.5%	–	–
C41	12 pF	±5%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C42	12 pF	±5%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C43	4 pF	±0.25 pF	0 ±30	$\tan\delta \leq 15 \times 10^{-4}$	–	–
C44	47 pF	±5%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C50	2.5 to 6 pF	–	0 ±300	$\tan\delta \leq 20 \times 10^{-4}$	–	–
C51	47 pF	±5%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C60(2)	82 pF	±5%	0 ±30	$\tan\delta \leq 10 \times 10^{-4}$	–	–
C61(2)	5 to 30 pF	–	0 ±300	$\tan\delta \leq 3.4 \times 10^{-4}$	–	–
C70	4.7 µF	±20%	±15%(1)	tan δ ≤ 0.06	–	–
L10(3)	–	–	–	–	–	–
L40	560 nH	±10%	+25 to +125	–	≥30 at 25 MHz	≥415 MHz
L41	39 nH	±10%	+25 to +125	–	≥50 at 50 MHz	≥1.5 GHz
L50(3)	–	–	–	–	–	–
L51(3)	–	–	–	–	–	–
L60(2)	2.2 µH	±10%	+25 to +125	–	≥20 at 7.9 MHz	≥140 MHz
X20	ceramic filter, Murata SFE 107 MA 5 A; see note 4					
X40	3rd overtone crystal, 95.2944 MHz; see note 5					

Notes

1. Temperature coefficient given as maximum $\Delta C/C$ over temperature range.
2. C60, C61 and L60 can be substituted by an LC tank.
3. Realized as microstrip line; see Fig.12.
4. 3 dB bandwidth: 280 ± 50 kHz; insertion loss: 4 dB typical and 6 dB maximum; spurious: 30 dB minimum at 8 to 12 MHz; input and output impedance: 330 Ω.
5. Motional resistance: $R_m \leq 20\ \Omega$; static capacitance: $C_0 \leq 6$ pF; load capacitance: $C_L = 6$ pF; loaded parallel resonance frequency: 95.2944 MHz; drive level dependency: $R_m \leq 20\ \Omega$ (1 nW ≤ P ≤ 1 mW).





Dimensions in mm.

Fig.11 Printed-circuit board layout for $f_{i(RF)}$ = 433.92 MHz.