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UBA2014

600 V driver IC for HF fluorescent lamps

Rev. 04 — 16 October 2008 Product data sheet

1. General description

The IC is a monolithic integrated circuit for driving electronically ballasted fluorescent lamps, with mains voltages up to 277 V (RMS) (nominal value).

The circuit is made in a 650 V Bipolar CMOS DMOS (BCD) power-logic process. It provides the drive function for the two discrete power MOSFETs.

Besides the drive function, the IC also includes the level-shift circuit, the oscillator function, a lamp voltage monitor, a current control function, a timer function and protections.

2. Features

- Adjustable preheat time
- Adjustable preheat current
- Current controlled operating
- Single ignition attempt
- Adaptive non-overlap time control
- Integrated high-voltage level-shift function
- Power-down function
- Protection against lamp failures or lamp removal
- Capacitive mode protection

3. Applications

- The circuit topology enables a broad range of ballast applications at different mains voltages for driving lamp types from T8, T5, PLC, T10, T12, PLL and PLT, for example.

4. Quick reference data

Table 1. Quick reference data

V_{DD} = 13 V; $V_{FVDD} - V_{SH}$ = 13 V; T_{amb} = 25 °C; all voltages are referenced to GND; see test circuit of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up state						
$V_{DD(stop)}$	oscillator stop supply voltage		8.6	9.1	9.6	V
$V_{DD(start)}$	oscillator start supply voltage		12.4	13.0	13.6	V
$I_{DD(start)}$	oscillator start-up supply current	$V_{DD} < V_{DD(start)}$	-	170	200	μA
High-voltage supply						
V_{HS}	high-side supply voltage	$I_{HS} < 30$ μA	-	-	570	V
Reference voltage						
V_{VREF}	reference voltage	$I_L = 10$ μA	2.86	2.95	3.04	V
Voltage controlled oscillator						
f_{max}	maximum bridge frequency		90	100	110	kHz
f_{min}	minimum bridge frequency		38.9	40.5	42.1	kHz
High-side output driver						
$I_{o(source)}$	output source current	$V_{GH} - V_{SH} = 0$ V	135	180	235	mA
$I_{o(sink)}$	output sink current	$V_{GH} - V_{SH} = 13$ V	265	330	415	mA
Preheat current sensor						
V_{ph}	preheat voltage		0.57	0.60	0.63	V
Lamp voltage sensor						
$V_{lamp(fail)}$	lamp fail voltage		0.77	0.81	0.85	V
$V_{lamp(max)}$	maximum lamp voltage		1.44	1.49	1.54	V
Average current sensor						
V_{offset}	offset voltage	$V_{CSP} = V_{CSN} = 0$ V to 2.5 V	−2	0	+2	mV
g_m	transconductance	f = 1 kHz	1900	3800	5700	μA/mV
Preheat timer						
t_{ph}	preheat time	$C_{CT} = 330$ nF; $R_{IREF} = 33$ kΩ	1.6	1.8	2.0	s
V_{OL}	LOW-level output voltage		-	1.4	-	V
V_{OH}	HIGH-level output voltage		-	3.6	-	V

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
UBA2014T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
UBA2014P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

6. Block diagram

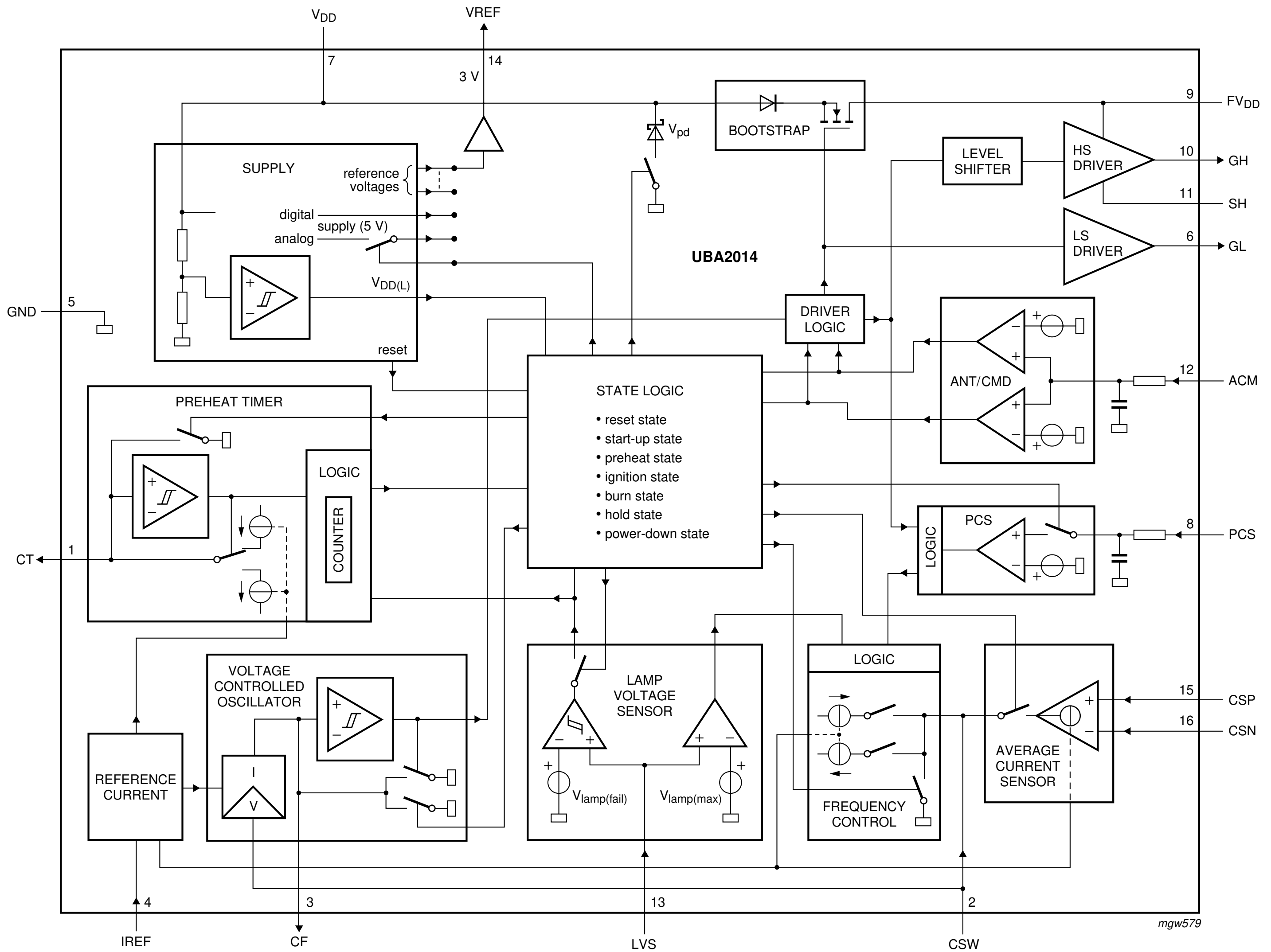


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

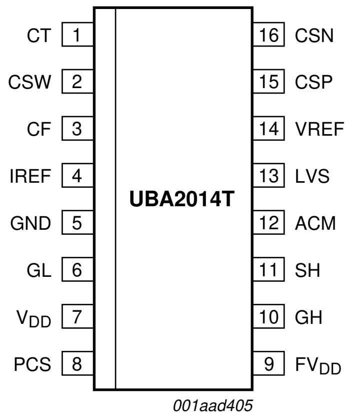


Fig 2. Pin configuration (SO16)

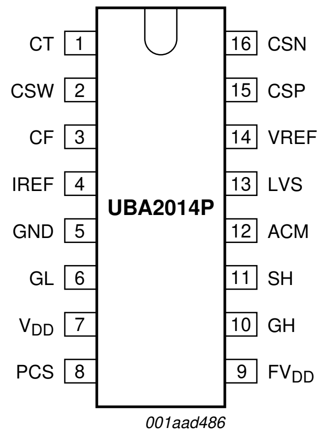


Fig 3. Pin configuration (DIP16)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CT	1	preheat timer output
CSW	2	input of voltage controlled oscillator
CF	3	voltage controlled oscillator output
IREF	4	internal reference current input
GND	5	ground
GL	6	gate output for the low-side switch
V_{DD}	7	low-voltage supply
PCS	8	preheat current sensor input
FV_{DD}	9	floating supply voltage; supply for high-side switch
GH	10	gate output for the high-side switch
SH	11	source for the high-side switch
ACM	12	capacitive mode input
LVS	13	lamp voltage sensor input
VREF	14	reference voltage output
CSP	15	positive input for the average current sensor
CSN	16	negative input for the average current sensor

8. Functional description

8.1 Start-up state

Initial start-up can be achieved by charging the low-voltage supply capacitor C7 (see Figure 8) via an external start-up resistor. Start-up of the circuit is achieved under the condition that both half bridge transistors TR1 and TR2 are non-conductive. The circuit will be reset in the start-up state. If the low-voltage supply (V_{DD}) reaches the value of $V_{DD(start)}$ the circuit will start oscillating. A DC reset circuit is incorporated in the High-Side (HS) driver. Below the lockout voltage at the FV_{DD} pin the output voltage ($V_{GH} - V_{SH}$) is zero. The voltages at pins CF and CT are zero during the start-up state.

8.2 Oscillation

The internal oscillator is a Voltage Controlled Oscillator (VCO) circuit which generates a sawtooth waveform between the $V_{CF(high)}$ level and 0 V. The frequency of the sawtooth is determined by capacitor C_{CF}, resistor R_{IREF}, and the voltage at pin CSW. The minimum and maximum switching frequencies are determined by R_{IREF} and C_{CF}; their ratio is internally fixed. The sawtooth frequency is twice the half bridge frequency. The UBA2014 brings the transistors TR1 and TR2 into conduction alternately with a duty cycle of approximately 50 %. An overview of the oscillator signal and driver signals is illustrated in Figure 4. The oscillator starts oscillating at f_{max}. During the first switching cycle the Low-Side (LS) transistor is switched on. The first conducting time is made extra long to enable the bootstrap capacitor to charge.

8.3 Adaptive non-overlap

The non-overlap time is realized with an Adaptive Non-overlap circuiT (ANT). By using an adaptive non-overlap circuit, the application can determine the duration of the non-overlap time and make it optimum for each frequency; see Figure 4. The non-overlap time is determined by the slope of the half bridge voltage, and is detected by the signal across resistor R16 which is connected directly to pin ACM. The minimum non-overlap time is internally fixed. The maximum non-overlap time is internally fixed at approximately 25 % of the bridge period time. An internal filter of 30 ns is included at the ACM pin to increase the noise immunity.

8.4 Timing circuit

A timing circuit is included to determine the preheat time and the ignition time. The circuit consists of a clock generator and a counter.

The preheat time is defined by C_{CT} and R_{IREF} and consists of 7 pulses at C_{CT}; the maximum ignition time is 1 pulse at C_{CT}. The timing circuit starts operating after the start-up state, as soon as the low supply voltage (V_{DD}) has reached $V_{DD(start)}$ or when a critical value of the lamp voltage ($V_{lamp(fail)}$) is exceeded. When the timer is not operating C_{CT} is discharged to 0 V at 1 mA.

8.5 Preheat state

After starting at f_{max}, the frequency decreases until the momentary value of the voltage across sense resistor R14 reaches the internally fixed preheat voltage level (pin PCS). At crossing the preheat voltage level, the output current of the Preheat Current Sensor (PCS) circuit discharges the capacitor C_{CSW}, thus raising the frequency. The preheat time begins at the moment that the circuit starts oscillating. During the preheat time the Average Current Sensor (ACS) circuit is disabled. An internal filter of 30 ns is included at pin PCS to increase the noise immunity.

8.6 Ignition state

After the preheat time the ignition state is entered and the frequency will sweep down due to charging of the capacitor at pin CSW with an internally fixed current; see Figure 5. During this continuous decrease in frequency, the circuit approaches the resonant frequency of the load. This will cause a high voltage across the load, which normally ignites the lamp. The ignition voltage of a lamp is designed above the $V_{lamp(fail)}$ level. If the lamp voltage exceeds the $V_{lamp(fail)}$ level the ignition timer is started.

8.7 Burn state

If the lamp voltage does not exceed the $V_{lamp(max)}$ level the voltage at pin CSW will continue to increase until the clamp level at pin CSW is reached; see Figure 5. As a consequence the frequency will decrease until the minimum frequency is reached.

When the frequency reaches its minimum level it is assumed that the lamp has ignited and the circuit will enter the burn state. The ACS circuit will be enabled. As soon as the averaged voltage across sense resistor R14, measured at pin CSN, reaches the reference level at pin CSP, the average current sensor circuit will take over the control of the lamp current. The average current through R14 is transferred to a voltage at the voltage controlled oscillator and regulates the frequency and, as a result, the lamp current.

8.8 Lamp failure mode

8.8.1 During ignition state

If the lamp does not ignite, the voltage level increases. When the lamp voltage exceeds the $V_{lamp(max)}$ level, the voltage will be regulated at the $V_{lamp(max)}$ level; see Figure 6. When the $V_{lamp(fail)}$ level is crossed the ignition timer has already started. If the voltage at pin LVS is above the $V_{lamp(fail)}$ level at the end of the ignition time the circuit stops oscillating and is forced into the Power-down mode. The circuit will be reset only when the supply voltage is powered down.

8.8.2 During burn state

If the lamp fails during normal operation, the voltage across the lamp will increase and the lamp voltage will exceed the $V_{lamp(fail)}$ level; see Figure 7. At that moment the ignition timer is started. If the lamp voltage increases further it will reach the $V_{lamp(max)}$ level. This forces the circuit to reenter the ignition state and results in an attempt to re-ignite the lamp. If during restart the lamp still fails, the voltage remains high until the end of the ignition time. At the end of the ignition time the circuit stops oscillating and the circuit will enter the Power-down mode.

8.9 Power-down mode

The Power-down mode will be entered if, at the end of the ignition time, the voltage at pin LVS is above $V_{lamp(fail)}$. In the Power-down mode the oscillator will be stopped and both TR1 and TR2 will be non-conductive. The V_{DD} supply is internally clamped. The circuit is released from the Power-down mode by lowering the low-voltage supply below $V_{DD(reset)}$.

8.10 Capacitive mode protection

The signal across R16 also gives information about the switching behavior of the half bridge. If, after the preheat state, the voltage across the ACM resistor (R16) does not exceed the V_{CMD} level during the non-overlap time, the Capacitive Mode Detection (CMD) circuit assumes that the circuit is in the capacitive mode of operation. As a consequence the frequency will directly be increased to f_{max}. The frequency behavior is decoupled from the voltage at pin CSW until C_{CSW} has been discharged to zero.

8.11 Charge coupling

Due to parasitic capacitive coupling to the high voltage circuitry all pins are burdened with a repetitive charge injection. Given the typical application the pins IREF and CF are sensitive to this charge injection. For charge coupling of approximately 8 pC, a safe functional operation of the IC is guaranteed, independent of the current level.

Charge coupling at current levels below 50 µA will not interfere with the accuracy of the V_{CS}, V_{PCS} and V_{ACM} levels.

Charge coupling at current levels below 20 µA will not interfere with the accuracy of any parameter.

8.12 Design equations

The following design equations are used to calculate the desired preheat time, the maximum ignition time, and the minimum and the maximum switching frequency.

$$t_{ph} = 1.8 \times \frac{C_{CT}}{330 \times 10^{-9}} \times \frac{R_{IREF}}{33 \times 10^{3}} \quad (1)$$

$$t_{ign} = 0.26 \times \frac{C_{CT}}{330 \times 10^{-9}} \times \frac{R_{IREF}}{33 \times 10^{3}} \quad (2)$$

$$f_{min} = 40.5 \times 10^{3} \times \frac{100 \times 10^{-12}}{C_{CF}} \times \frac{33 \times 10^{3}}{R_{IREF}} \quad (3)$$

$$f_{max} = 2.5 \times f_{min} \quad (4)$$

Start of ignition is defined as the moment at which the measured lamp voltage crosses the $V_{lamp(fail)}$ level; see Section 8.8.

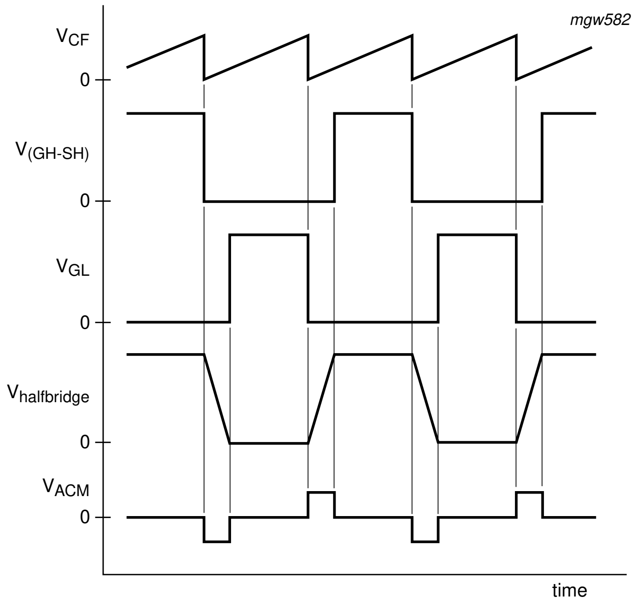


Fig 4. Oscillator and driver signals

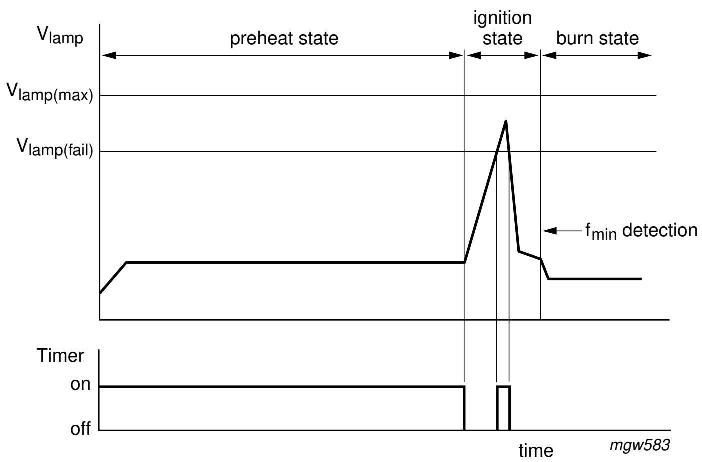


Fig 5. Normal ignition behavior

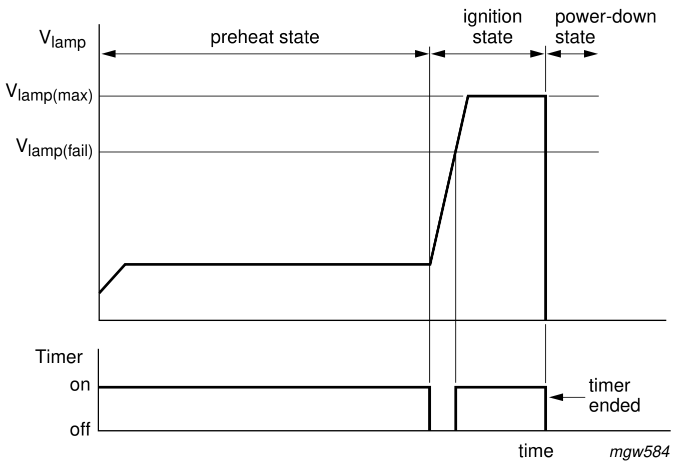


Fig 6. Failure mode during ignition

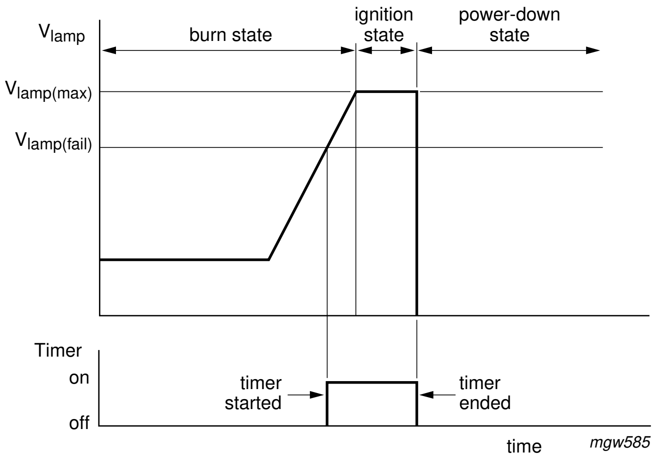


Fig 7. Failure mode during burn

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages referenced to GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{HS}	high-side supply voltage	I_{HS} < 30 μA; t < 1 s		-	600	V
		I_{HS} < 30 μA		-	570	V
V_{VDD}	voltage at pin V_{DD}			-	14	V
V_{ACM}	voltage at pin ACM			–5	+5	V
V_{PCS}	voltage at pin PCS			–5	+5	V
V_{LVS}	voltage at pin LVS			0	5	V
V_{CSP}	voltage at pin CSP			0	5	V
V_{CSN}	voltage at pin CSN			–0.3	+5	V
V_{CSW}	voltage at pin CSW			0	5	V
T_{amb}	ambient temperature			–25	+80	°C
T_j	junction temperature			–25	+150	°C
T_{stg}	storage temperature			–55	+150	°C
V_{esd}	electrostatic discharge voltage					
	pins FV_{DD}, GH and SH		[1]	–1000	+1000	V
	pins CT, CSW, CF, IREF, GL, V_{DD}, PCS, CSN, CSP, VREF, LVS and ACM		[1]	–2500	+2500	V

[1] In accordance with the human body model, i.e. equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	SO16		100	K/W
	DIP16		60	K/W
$R_{th(j-pin)}$	thermal resistance from junction to pin	in free air		
	SO16		50	K/W
	DIP16		30	K/W

11. Characteristics

Table 6. Characteristics

V_{DD} = 13 V; $V_{FVDD} - V_{SH}$ = 13 V; T_{amb} = 25 °C; all voltages referenced to GND; see test circuit of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Start-up state: pin V_{DD}							
V_{DD}	supply voltage	TR1 = off; TR2 = off		-	-	6	V
$V_{DD(reset)}$	reset supply voltage	TR1 = off; TR2 = off		4.5	5.5	7.0	V
$V_{DD(stop)}$	oscillator stop supply voltage			8.6	9.1	9.6	V
$V_{DD(start)}$	oscillator start supply voltage			12.4	13.0	13.6	V
$V_{DD(hys)}$	start-stop hysteresis supply voltage			3.5	3.9	4.4	V
$V_{DD(clamp)}$	clamp supply voltage	Power-down mode		10	11	12	V
$I_{DD(start)}$	start-up supply current	$V_{DD} < V_{DD(start)}$		-	170	200	μA
$I_{DD(pd)}$	power-down supply current	V_{DD} = 9 V		-	170	200	μA
I_{DD}	supply current	f_{bridge} = 40 kHz without gate drive		-	1.5	2.2	mA
High-voltage supply: pins GH, SH and FV_{DD}							
I_L	latching current	600 V at high-voltage pins		-	-	30	μA
Reference voltage: pin VREF							
V_{ref}	reference voltage	I_L = 10 μA		2.86	2.95	3.04	V
ΔV_{VREF}	reference voltage stability	I_L = 10 μA; T_{amb} = 25 °C to 150 °C		-	−0.64	-	%
I_{source}	source current			1	-	-	mA
I_{sink}	sink current			1	-	-	mA
Z_o	output impedance	I_L = 1 mA source		-	3.0	-	Ω
Current supply: pin IREF							
V_I	input voltage			-	2.5	-	V
I_I	input current			65	-	95	μA
Voltage controlled oscillator							
Output: pin CSW							
V_o	output control voltage			2.7	3.0	3.3	V
V_{clamp}	clamp voltage	burn state		2.8	3.1	3.4	V
Voltage controlled oscillator output: pin CF							
f_{max}	maximum frequency			90	100	110	kHz
f_{min}	minimum frequency			38.9	40.5	42.1	kHz
Δf_{stab}	frequency stability	T_{amb} = −20 °C to +80 °C		-	1.3	-	%
t_{start}	first output oscillator stroke time			-	50	-	μs
$t_{no(min)}$	minimum non-overlap time	GH to GL		0.68	0.90	1.13	μs
		GL to GH		0.75	1.00	1.25	μs
$t_{no(max)}$	maximum non-overlap time	f_{bridge} = 40 kHz	[1]	-	7.5	-	μs
$V_{CF(high)}$	high-level oscillator output voltage	$f = f_{min}$		-	2.5	-	V

Table 6. Characteristics *…continued*

V_{DD} = 13 V; V_{FVDD} – V_{SH} = 13 V; T_{amb} = 25 °C; all voltages referenced to GND; see test circuit of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{o(start)}$	oscillator output start current	V_{CF} = 1.5 V	3.8	4.5	5.2	µA
$I_{o(min)}$	minimum oscillator output current	V_{CF} = 1.5 V	-	21	-	µA
$I_{o(max)}$	maximum oscillator output current	V_{CF} = 1.5 V	-	54	-	µA
Output drivers						
High-side driver output: pin GH						
V_{OH}	HIGH-level output voltage	I_o = 10 mA	12.5	-	-	V
V_{OL}	LOW-level output voltage	I_o = 10 mA	-	-	0.5	V
$I_{o(source)}$	output source current	V_{GH} – V_{SH} = 0 V	135	180	235	mA
$I_{o(sink)}$	output sink current	V_{GH} – V_{SH} = 13 V	265	330	415	mA
R_{on}	on resistance	I_o = 10 mA	32	39	45	Ω
R_{off}	off resistance	I_o = 10 mA	16	21	26	Ω
Low-side driver output: pin GL						
V_{OH}	HIGH-level output voltage	I_o = 10 mA	12.5	-	-	V
V_{OL}	LOW-level output voltage	I_o = 10 mA	-	-	0.5	V
$I_{o(source)}$	output source current	V_{GL} = 0	135	200	235	mA
$I_{o(sink)}$	output sink current	V_{GL} = 13 V	265	330	415	mA
R_{on}	on resistance	I_o = 10 mA	32	39	45	Ω
R_{off}	off resistance	I_o = 10 mA	16	21	26	Ω
Floating supply voltage: pin FV_{DD}						
V_{FVDD}	lockout voltage		2.8	3.5	4.2	V
I_{FVDD}	floating well supply current	DC level at V_{GH} – V_{SH} = 13 V	-	35	-	µA
Bootstrap diode						
V_{boot}	bootstrap diode forward drop voltage	I = 5 mA	1.3	1.7	2.1	V
Preheat current sensor						
Input: pin PCS						
I_i	input current	V_{PCS} = 0.6 V	-	-	1	µA
V_{ph}	preheat voltage		0.57	0.60	0.63	V
Output: pin CSW						
$I_{o(source)}$	output source current	V_{CSW} = 2.0 V	9.0	10	11	µA
$I_{o(sink)}$	output sink current	V_{CSW} = 2.0 V	-	10	-	µA
Adaptive non-overlap and capacitive mode detection; pin ACM						
I_i	input current	V_{ACM} = 0.6 V	-	-	1	µA
V_{CMDP}	positive capacitive mode detection voltage		80	100	120	mV
V_{CMDN}	negative capacitive mode detection voltage		–68	–85	–102	mV

Table 6. Characteristics *…continued*

V_{DD} = 13 V; V_{FVDD} – V_{SH} = 13 V; T_{amb} = 25 °C; all voltages referenced to GND; see test circuit of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Lamp voltage sensor						
Input: pin LVS						
I_i	input current	V_{LVS} = 0.81 V	-	-	1	µA
$V_{lamp(fail)}$	lamp fail voltage		0.77	0.81	0.85	V
$V_{lamp(fail)(hys)}$	lamp fail hysteresis voltage		119	144	169	mV
$V_{lamp(max)}$	maximum lamp voltage		1.44	1.49	1.54	V
Output: pin CT						
$I_{o(sink)}$	output sink current	V_{CSW} = 2.0 V	27	30	33	µA
$I_{o(source)}$	ignition output source current	V_{CSW} = 2.0 V	9.0	10	11	µA
Average current sensor						
Input: pins CSP and CSN						
I_i	input current	V_{CS} = 0 V	-	-	1	µA
V_{offset}	offset voltage	V_{CSP} = V_{CSN} = 0 V to 2.5 V	–2	0	+2	mV
g_m	transconductance	f = 1 kHz	1900	3800	5700	µA/mV
Output: pin CSW						
I_o	output current	source and sink; V_{CSW} = 2 V	85	95	105	µA
Preheat timer; pin CT						
t_{ph}	preheat time	C_{CT} = 330 nF; R_{IREF} = 33 kΩ	1.6	1.8	2.0	s
t_{ign}	ignition time	C_{CT} = 330 nF; R_{IREF} = 33 kΩ	-	0.32	-	s
I_o	output current	V_{CT} = 2.5 V	5.5	5.9	6.3	µA
V_{OL}	LOW-level output voltage		-	1.4	-	V
V_{OH}	HIGH-level output voltage		-	3.6	-	V
V_{hys}	hysteresis voltage		2.05	2.20	2.35	V

[1] The maximum non-overlap time is determined by the level of the CF signal. If this signal exceeds a level of 1.25 V, the non-overlap will end, resulting in a maximum non-overlap time of 7.5 µs at a bridge frequency of 40 kHz.

12. Application information

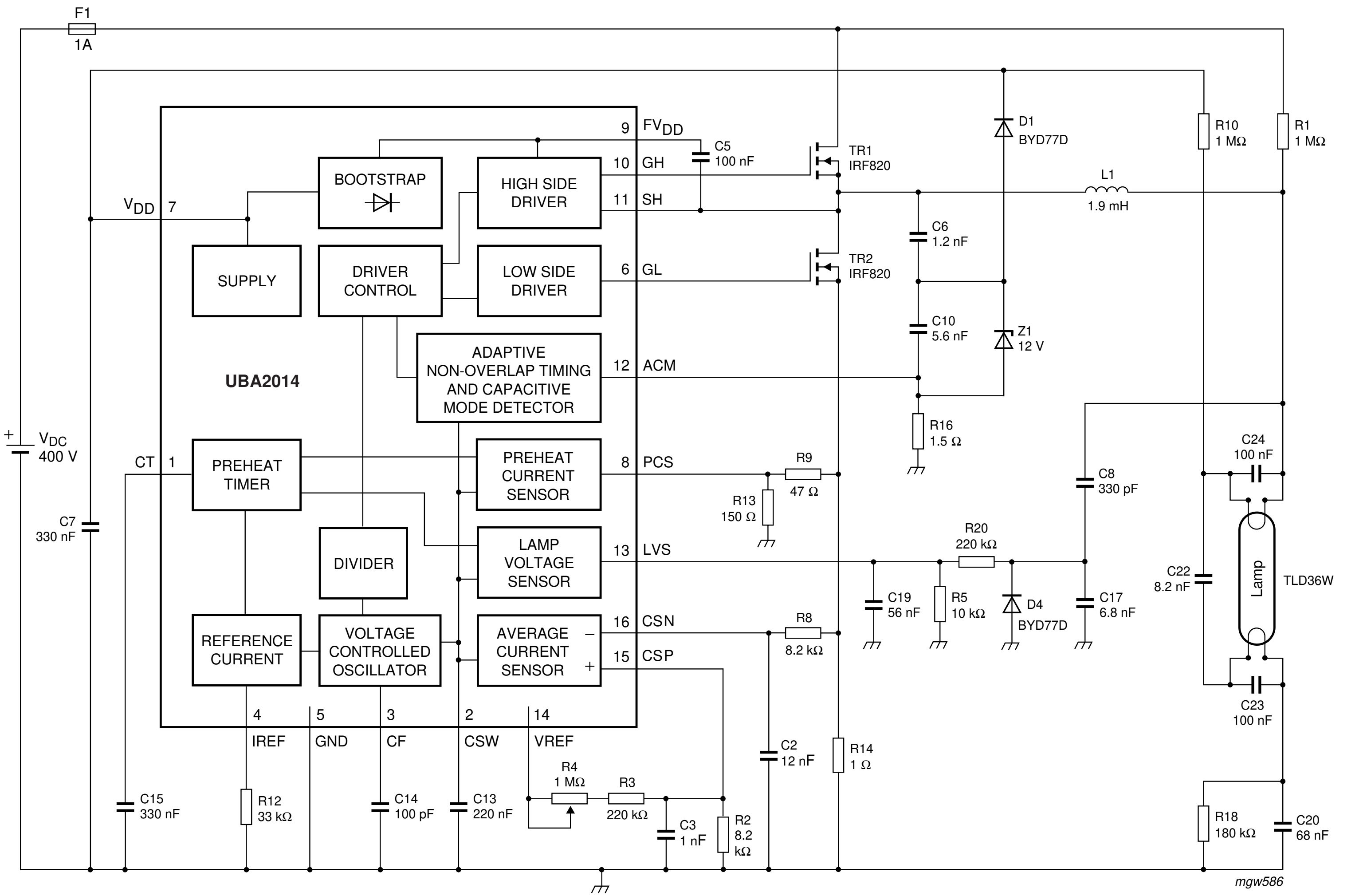
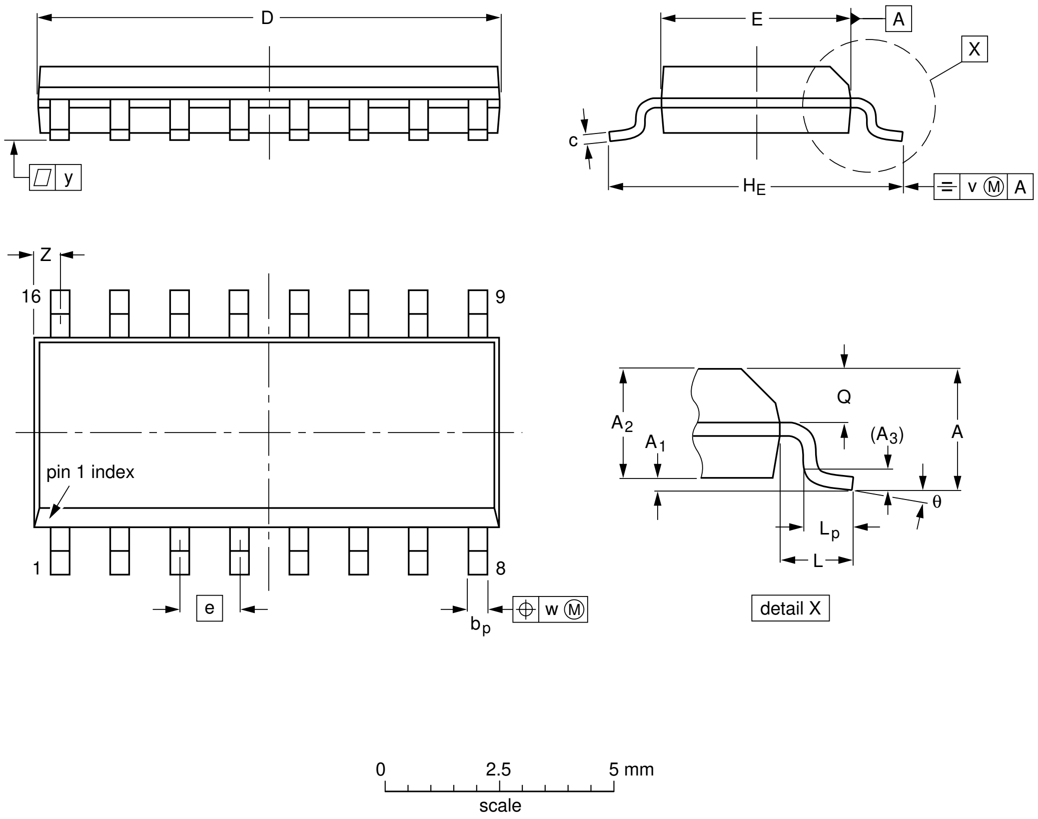


Fig 8. Test and application circuit

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D[(1)]	E[(1)]	e	H_E	L	L_p	Q	v	w	y	Z[(1)]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

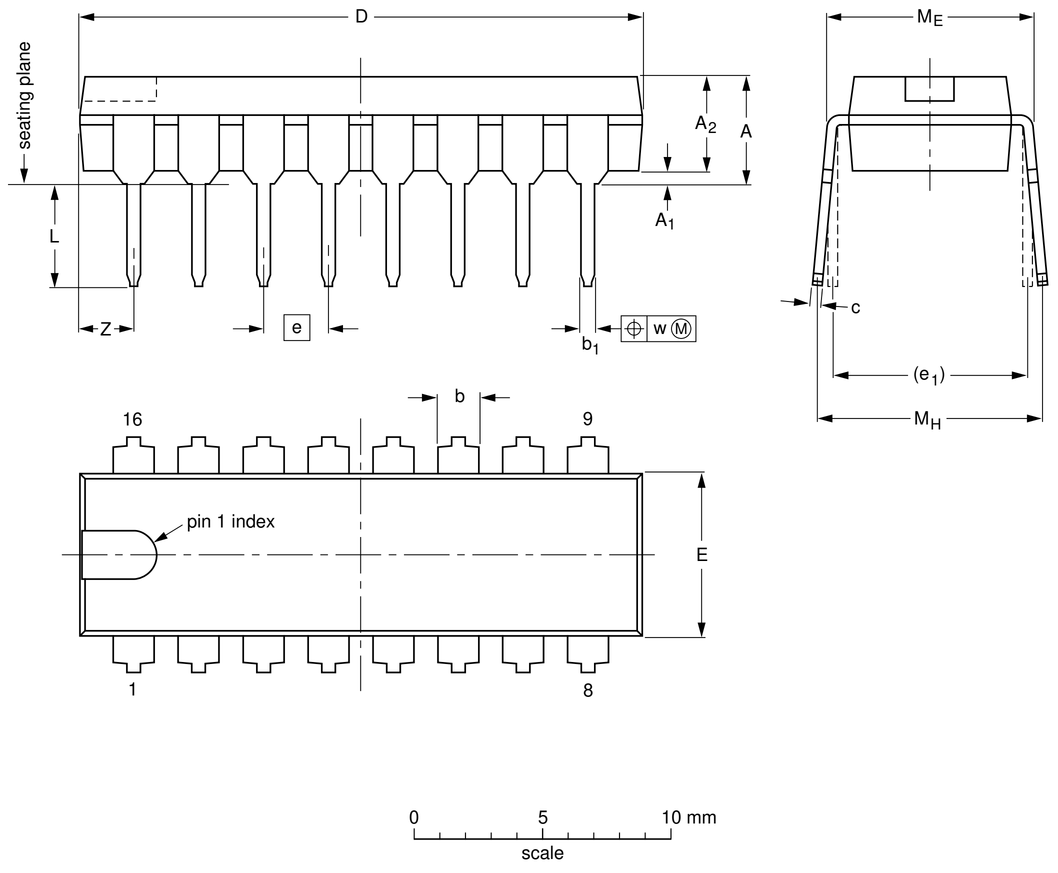
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

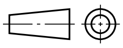
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			~~99-12-27~~ 03-02-13

Fig 10. Package outline SOT38-1 (DIP16)

14. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UBA2014_4	20081016	Product data sheet	-	UBA2014_3
Modifications:	• Max value for V_{HS} in Table 1 updated. • Max value for VHS in Table 4 updated.			
UBA2014_3	20080815	Product data sheet	-	UBA2014_2
UBA2014_2	20050912	Product data sheet	-	UBA2014_1
UBA2014_1	20020516	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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