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UBA20271/2

350 V and 600 V Power ICs for dimmable compact fluorescent lamps

Rev. 2.1 — 12 October 2011 Product data sheet

1. General description

The UBA20271/2 are high-voltage power ICs intended to drive and control higher powered self ballasted Compact Fluorescent Lamp (CFL) lighting applications. The UBA20271/2 operate from 120 V and 230 V. The module includes a half-bridge power circuit of two NMOST power FETs. In addition, a controller circuit is included that has advanced features for dimming and a lamp current controlled boost feature. The boost feature is used for boosting cold (amalgam) CFL.

The controller contains a half-bridge drive function for CFL, a high-voltage level-shift circuit with integrated bootstrap diode. In addition, the controller contains an oscillator function, a current control function both for preheat and burn, a timer function and protection circuits. The UBA20271/2 are supplied via a dV/dt current charge supply circuit from the half-bridge circuit.

Remark: Mains voltages noted are AC.

2. Features and benefits

2.1 Half-bridge features

- UBA20271: Two internal 350 V, 1.0 Ω, max 5.0 A NMOST half-bridge power FETs
- UBA20272: Two internal 600 V, 3.0 Ω, max 2.7 A NMOST half-bridge power FETs
- Integrated high-voltage level-shift function with integrated bootstrap diode

2.2 Preheat and ignition features

- Coil saturation protection during ignition
- Adjustable saturation protection level
- Adjustable preheat time
- Adjustable preheat current
- Ignition lamp current detection

2.3 Lamp boost features

- Adjustable boost timing
- Fixed boost current ratio of 1.5
- Gradually boost to burn transition timing

2.4 Dim features

- Continuously variable dimming function for standard phase cut dimmers

- Natural dimming curve by logarithmic correction
- Adjustable Minimum Dimming Level (MDL)
- Controlled lamp ON/OFF

2.5 Protection

- OverCurrent Protection (OCP) in boost and burn state
- Capacitive Mode Protection (CMP)
- OverPower Protection (OPP)
- Power-down function
- OverTemperature Protection (OTP)

2.6 Other features

- Current controlled operating in boost and burn state
- External power-down function
- Lamp flicker suppression

3. Applications

- Dimmable compact fluorescent lamps for power levels from 5 W to 20 W directly operating from 230 V (UBA20272) and 120 V (UBA20271) mains voltage.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UBA20271T/N1	SO20	Plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
UBA20272T/N1	SO20	Plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

5. Block diagram

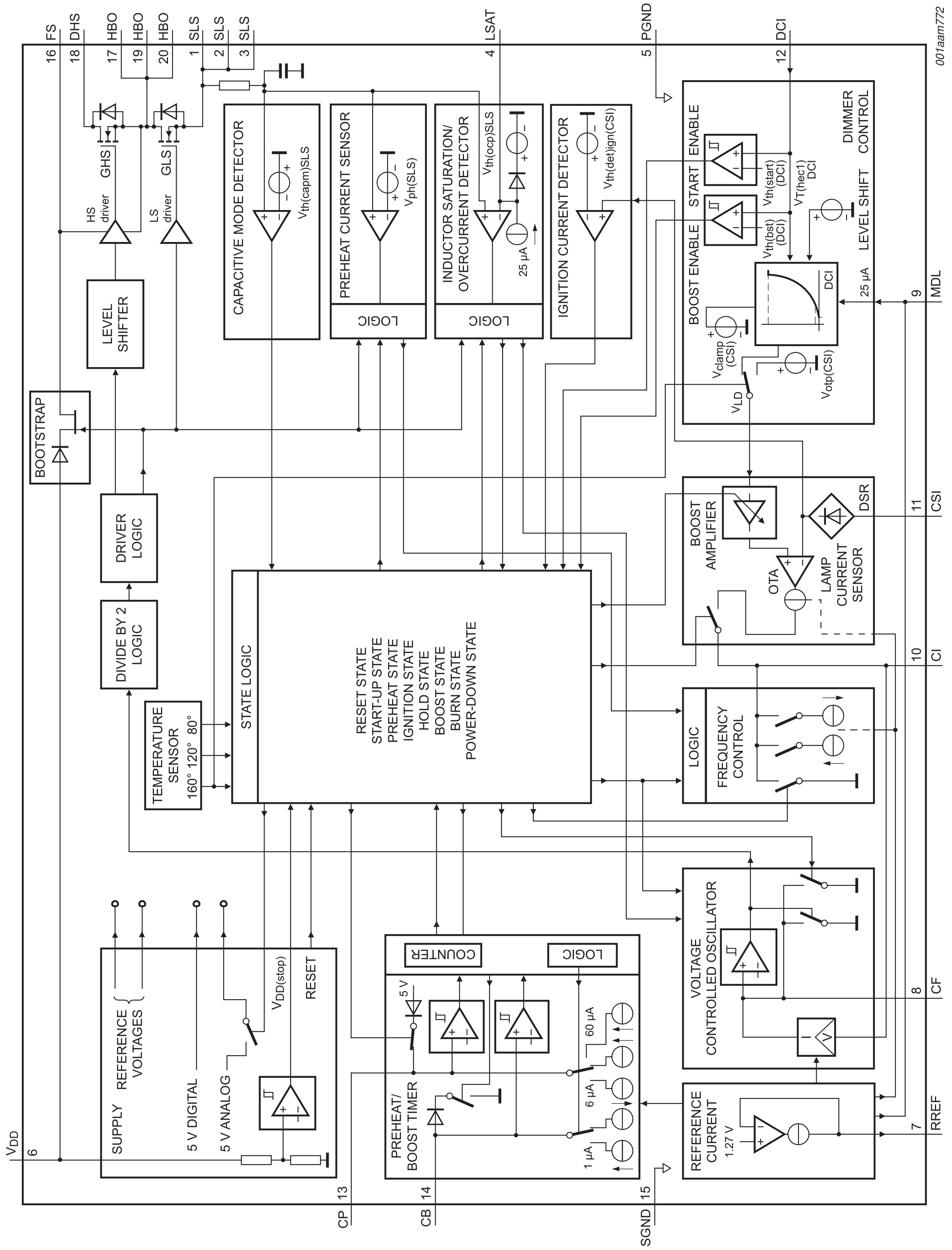


Fig 1. Block diagram UBA20271/2

6. Pinning information

6.1 Pinning

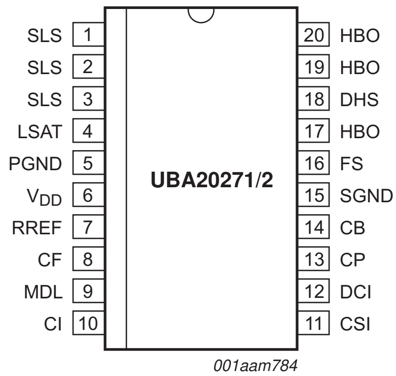


Fig 2. Pin configuration UBA20271/2 (SO20)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
SLS	1,2,3	source low-side switch[1]
LSAT	4	coil saturation level input
PGND	5	power ground[3]
V_{DD}	6	low voltage supply
RREF	7	internal reference current input
CF	8	voltage controlled oscillator capacitor
MDL	9	minimum dimming level input
CI	10	voltage controlled oscillator input integrating capacitor
CSI	11	current feedback sense input
DCI	12	dimming level input
CP	13	preheat timing capacitor
CB	14	boost timing capacitor
SGND	15	signal ground[3]
FS	16	floating supply voltage
HBO	17,19,20	half-bridge output[2]
DHS	18	high-voltage supply

[1] SLS pins are internally connected

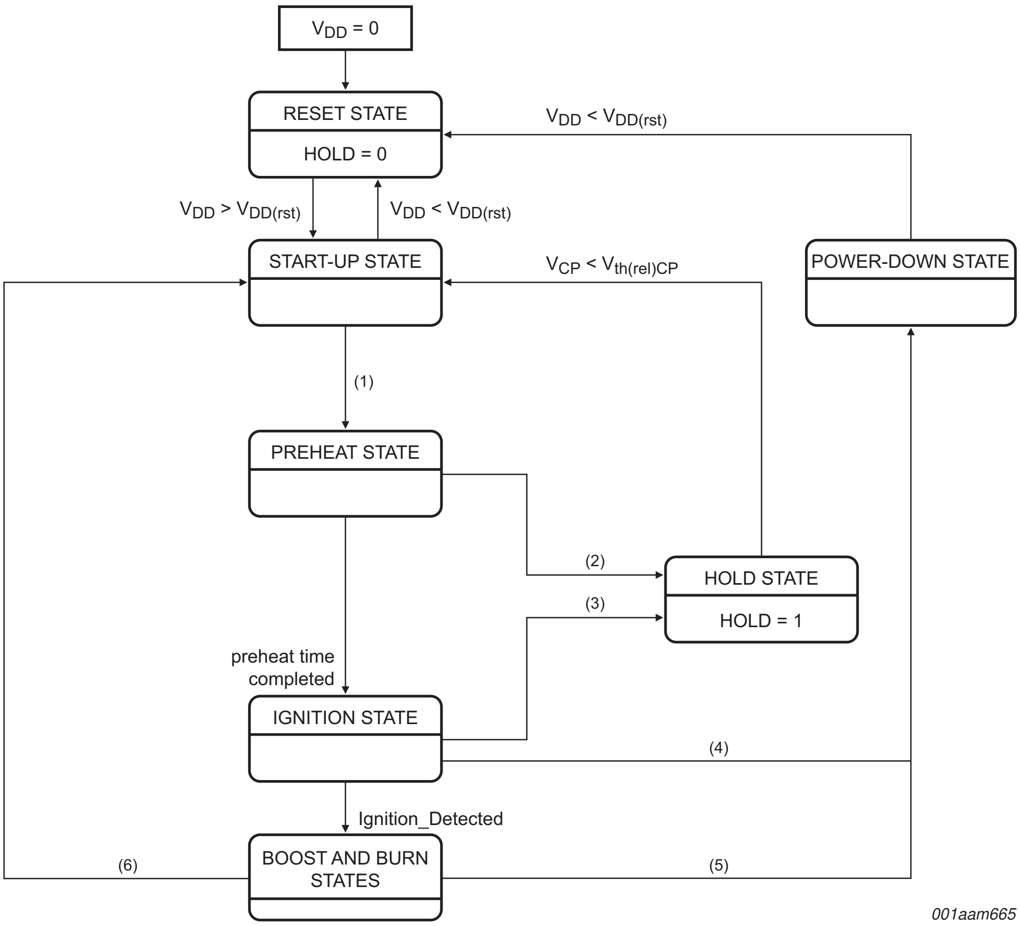
[2] HBO pins are internally connected

[3] PGND and SGND are internally connected

7. Functional description

The UBA20271/2 are ICs with integrated half-bridge MOSFETs in self ballasted high-power CFL and their derivatives. The UBA20271/2 are equipped with variable dimming functionality that has a logarithmic corrected natural dimming function. This function enables a less sensitive brightness control of the lamp at low dim levels.

The UBA20271/2 are rated up to a maximum continuous rectified mains voltage of 350 V or 500 V, respectively and lamp power-up to 20 W. The UBA20271/2 include all the necessary functions for preheat, ignition, boost, and on-state operation of the lamp and includes a linear dimming feature. In addition, several protection measures are included that safeguard the functioning of the CFL and controller. The controller states are shown in Figure 3.



(1) $V_{DD} > V_{DD(start)}$ AND $V_{i(DCI)} > V_{th(start)DCI}$ AND (HOLD = 0 OR $V_{CP} < V_{th(rel)CP}$)

(2) $V_{DD} < V_{DD(stop)}$ OR $V_{i(DCI)} < V_{th(start)DCI} - V_{th(hys)DCI}$

(3) (End of ignition time AND HOLD = 0) OR $V_{DD} < V_{DD(stop)}$ OR $V_{i(DCI)} < V_{th(start)DCI} - V_{th(hys)DCI}$

(4) End of ignition AND HOLD = 1

(5) $V_{CP} < V_{th(pd)CP}$ OR overcurrent fault time > $\frac{1}{10}$ t_{ph} OR $f_{bridge(max)}$ detected in capacitive mode

(6) $V_{DD} < V_{DD(stop)}$ OR $V_{i(DCI)} < V_{th(start)DCI} - V_{th(hys)DCI}$

Fig 3. State diagram

7.1 Lamp start-up cycle

7.1.1 Reset state

The UBA20271/2 are in a reset state while the supply voltage on the V_{DD} pin is lower than the $V_{DD(rst)}$ level. In the reset state, a part of the internal supply is turned off, all registers, counters and timers are undefined. In addition, the hold state latch is reset and both the high and low-side transistor are non-conductive. During power-up, the low voltage supply capacitor on the V_{DD} pin is charged via an external start-up resistor. When the voltage on the V_{DD} pin is higher than the $V_{DD(rst)}$ level, the start-up state is entered. The UBA20271/2 enters the reset state when the supply voltage on the V_{DD} pin drops lower than $V_{DD(rst)}$.

7.1.2 Start-up state

Start-up is achieved by charging the low voltage supply capacitor on the V_{DD} pin via an external start-up resistor. At start-up the High-Side (HS) transistor is non-conductive and the Low-Side (LS) is conductive to enable charging of the bootstrap capacitor. This capacitor supplies the HS driver and level shifter circuit connected between the FS and HBO pin. A DC reset circuit is incorporated in the ICs HS driver. This circuit ensures that lower than the lockout voltage on the FS pin the output voltage ($V_{GHS} - V_{HBO}$) is zero.

As the start-up state is entered, the circuit only starts oscillating when the low voltage supply (V_{DD}) reaches the value of $V_{DD(start)}$ AND $V_{i(DCI)} > V_{th(start)DCI}$. The circuit starts oscillating at $f_{bridge(max)}$.

The circuit enters the preheat state as soon as the capacitor on the CP pin is charged to a voltage level higher than $V_{th(CP)max}$. To remain oscillating, the V_{DD} voltage must remain higher than $V_{DD(stop)}$ and lower than the upper limit $V_{DD(clamp)}$. In addition, the typical voltage level on the DCI pin must be higher than $V_{th(start)DCI} - V_{th(hys)DCI} = 0.24$ V.

An UnderVoltage LockOut (UVLO) is implemented on the DCI pin to create a guaranteed turn-off for multiple lamps when the lamps are at low dim levels. The UVLO also guarantees that there is a preheat phase when the dim level is turned up again.

The typical turn-on level on the DCI pin is set to lower than $V_{th(start)DCI} = 0.36$ V, else it would increase the turn-on hysteresis of the lamp. This level enables the UBA20271/2 to perform a stable ignition of the lamp when there is already sufficient power from the dimmer at lower dim levels.

During the start-up state, the voltage on the CF pin is at zero and the CB pin is close to zero. The voltage on the CP pin rises to higher than $V_{th(CP)max}$ level during the start-up state. See Figure 9.

7.1.3 Preheat state

Starting at $f_{bridge(max)}$, the frequency decreases by charging capacitor C_{CI} via an output current circuit controlled by the preheat current sensor circuit. This state continues until the momentary value of the voltage across sense resistor R_{SLS} reaches the internally fixed preheat voltage level (SLS pin). At this level, the current of the preheat current sensor reaches a charge and discharge balanced state on capacitor C_{CI} to set the frequency.

The preheat time consists of eight saw-toothed pulses at the CP pin. Preheat begins as soon as the capacitor on the CP pin is charged to a voltage higher than $V_{th(CP)max}$. During the preheat time, the current feedback sensor circuit (input CSI pin) is disabled. To increase noise immunity, an internal filter of 30 ns is included at the SLS pin.

If during preheat, the level on the DCI pin drops lower than $V_{th(start)DCI} - V_{th(hys)DCI} = 0.24$ V or the V_{DD} pin drops lower than $V_{DD(stop)}$, the preheat state is immediately stopped. The circuit then enters the hold state delaying a new preheat cycle. A fixed voltage drop on the preheat capacitor C_{CP} and a fixed discharge current on the CP pin sets the delay time.

A new preheat cycle starts after the CP pin level slowly discharges. This condition continues until $V_{CP} < V_{th(rel)CP}$ and recharges higher than $V_{th(CP)max}$ provided $V_{DD} > V_{DD(start)}$ AND $V_{i(DCI)} > V_{th(start)DCI}$. See Figure 5.

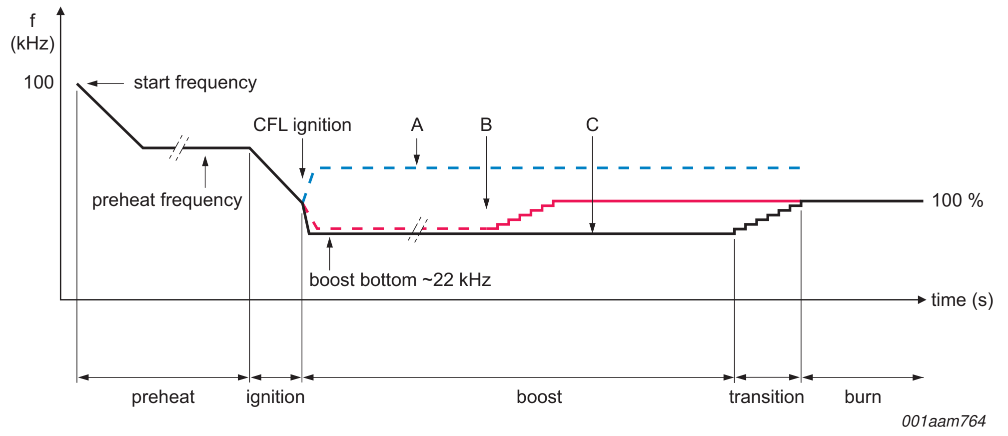


Fig 4. CFL frequency from start to burn state

7.1.4 Ignition state

Directly after the preheat state has been completed, the ignition state is entered. In the ignition state, the frequency sweeps down due to charging of the capacitor C_{CI} on the CI pin with an internally fixed current. See Figure 4. During this continuous decrease in frequency, the circuit approaches the resonant frequency of the resonant tank L2, C5. This results in a high voltage across the lamp to ignite the lamp. The current sensor circuit which monitors the voltage over resistor R_{CSI} detects lamp ignition. See Figure 11.

If the voltage on the CSI pin is above the typical ignition detection threshold voltage level of 0.6 V, lamp ignition is detected. The system then changes from ignition state to the boost or burn state. If no ignition is detected, the frequency decreases further to the minimum half-bridge frequency $f_{bridge(min)}$. To prevent continuous ignition attempts and over-heating of the application due to lamp damage, the UBA20271/2 only attempts to ignite the lamp twice after power-up. The ignition attempt counter is incremented when the lamp ignition threshold voltage on the CSI pin is not exceeded at the end of the ignition enabling time. If a second ignition attempt also exceeds the ignition time-out period, the IC enters the power-down state. See Figure 5.

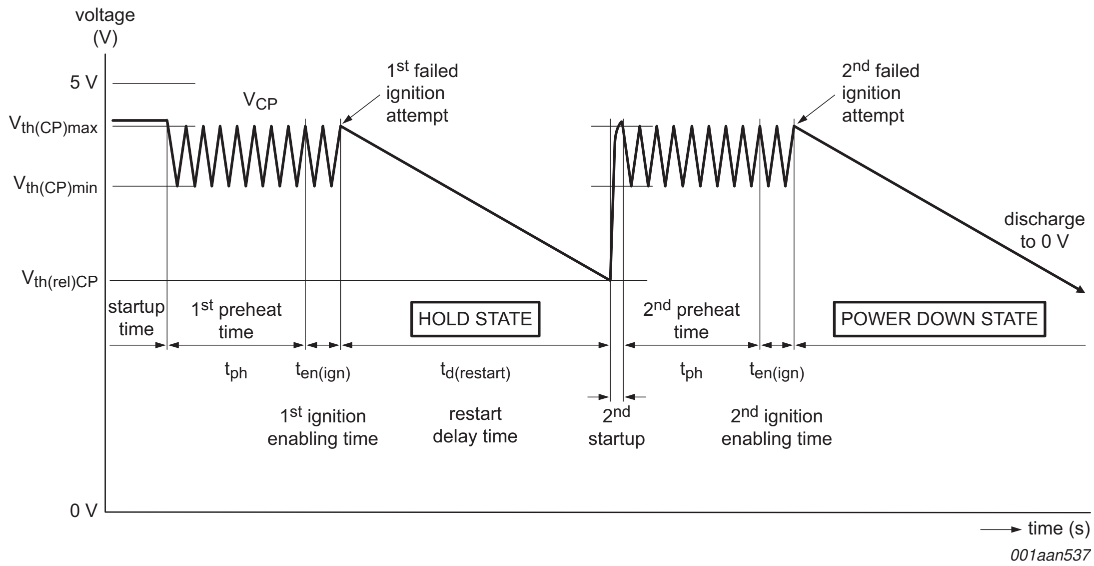


Fig 5. Retry cycle

7.1.5 Boost state and transition to burn state

When ignition is detected by measuring lamp current on the CSI pin, the circuit enters the boost state. Figure 7 shows the boost and burn state in more detail. In the boost state, the nominal burn state lamp current can be increased with a fixed boost ratio of 1.5:1. This boosts up the slow luminescence increase of a cold amalgam CFL lamp, provided $V_{DCI} > V_{th(bst)DCI}$. If the IC is at a temperature ($T_{j(bp)bst}$) before entering the boost state, the burn state is bypassed.

A boost timing circuit is included to determine the boost time and transition to burn time. The circuit consists of a clock generator comprising C_{CB}, $R_{ext(RREF)}$ and a 64-step counter. When the timer is not operating, C_{CB} is discharged to lower than the $V_{th(CB)min}$ level of 1.1 V. This voltage, about 0.6 V, is still higher than the level at which the comparator on C_{CB} detects if the CB pin is shorted to ground.

The boost time consists of 63 saw-toothed pulses at the CB pin and automatically followed by the transition time at the CP pin. The 32 saw-tooth pulses form the transition time from boost to burn enabling a smooth transition between the current controlled boost and burn state. The total transition time is approximately four times the preheat time as shown in Figure 6.

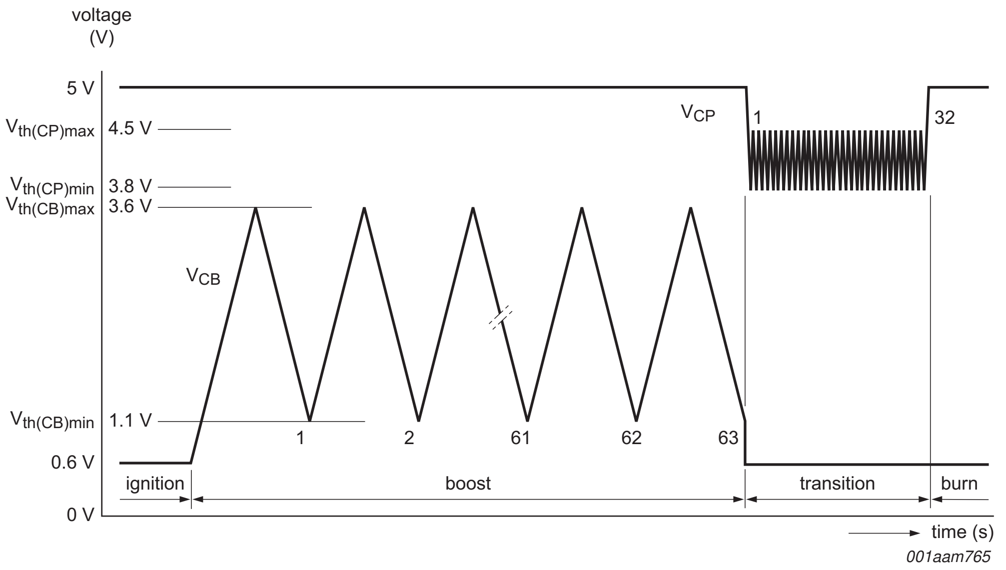


Fig 6. Boost timing

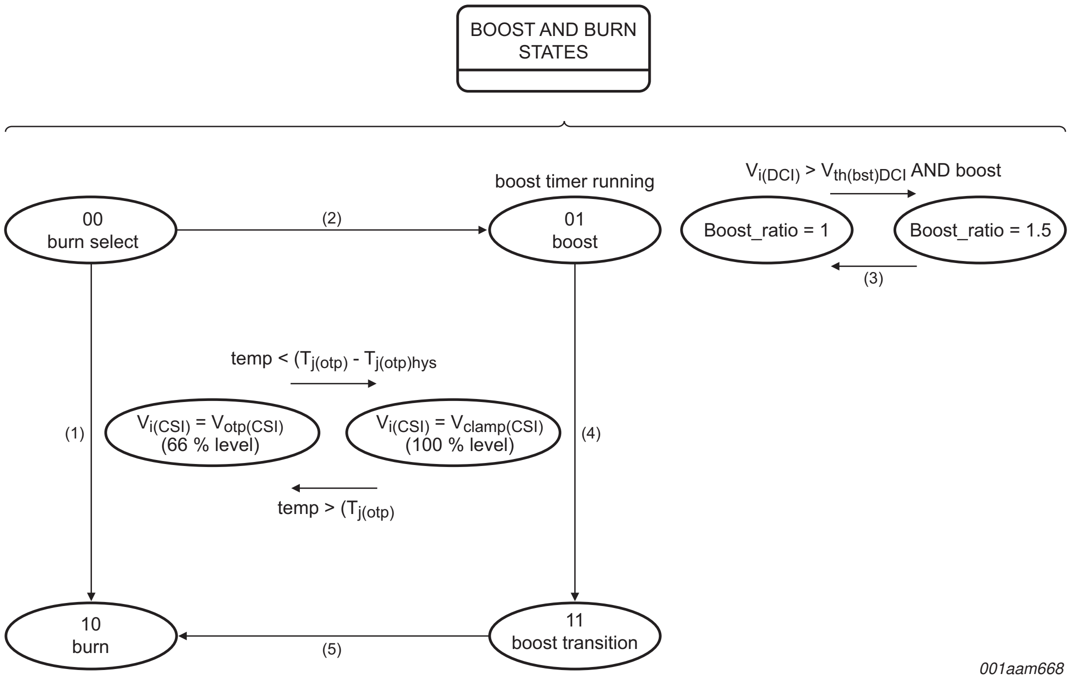
In the boost state, the lamp current feedback control circuit operates the same as in the burn state. This action is used to improve lamp stability. Lamp current boosted by a fixed ratio of 1.5 compared to the burn state, boosts up the slow luminescence increase of a cold CFL lamp. In the boost to burn transition time there is a slow 15-step ratio decrease from 1.5 to 1. For the transition to burn time, the preheat timer is reused and the boost ratio is gradually decreased in 15 steps from 1.5 to 1. The steps occur within 32 saw-toothed pulses on the CP pin. The 32 saw-toothed pulses form the transition time from boost to burn to enable a smooth transition between the current controlled boost and burn state. Given the application values of C_{CB} and $R_{ext(RREF)}$ a boost time of more than 300 s is possible. In addition to boost bypass at temperature $T_{j(bp)bst}$ (≈ 80 °C), there is a temperature protection function during the boost state of $T_{j(end)bst}$ (≈ 120 °C). If the IC temperature passes this level during boost, the transition timer is immediately started in order to enter the burn state faster. This action effectively reduces the boost time. See Figure 4 [B].

The current boost in the boost state does not start when $V_{i(DCI)}$ is lower than $V_{th(bst)DCI}$. Current boost ends when $V_{i(DCI)}$ is lower than $V_{th(bst)DCI} - V_{th(bst)hys(DCI)}$ without a boost transition. See Figure 4 [A].

Remark: If the CB pin is shorted to ground, the boost function is disabled. During such conditions, the bottom frequency $f_{bridge(min)}$ is 1.8 times higher than the boost bottom frequency $f_{bridge(bst)min}$.

7.1.6 Burn state

After the boost state, or when the boost state is bypassed burn state starts. The lamp current sensor circuit is still enabled. See Figure 4 [A]. The CSI pin (current sense input) measures the RMS voltage across sense resistor R_{CSI}. It then passes through a Double-Sided Rectifier (DSR) circuit and fed towards an Operational Transconductor Amplifier (OTA). When the RMS voltage on the CSI pin reaches the internal reference level, the lamp current sensor circuit takes over the control of the lamp current. The internal current output of the OTA is transferred via an integrator on the CI pin to the input of the Voltage Controlled Oscillator (VCO). The VCO regulates the frequency and as a result, the lamp current.



(1) Temp > $T_{j(bp)bst}$ OR Boost_Disable

(2) Temp < $T_{j(bp)bst}$ AND NOT Boost_Disable

(3) NOT (Boost OR Boost transition)

(4) Temp > $T_{j(end)bst}$ OR Boost timer ended OR (Boost_ratio = 1.5 AND $V_{DCI} < V_{th(bst)DCI} - V_{th(bst)hys(DCI)}$)

(5) Boost_Transition timer ended OR $V_{DCI} < V_{th(bst)DCI} - V_{th(bst)hys(DCI)}$ OR Temp > $T_{j(otp)}$

Fig 7. Boost and burn state machine

7.1.7 Hold state

The hold state is a special state to reduce lamp flicker at deep dim levels, on or near dim and ignition threshold level. See Figure 3.

The hold state is entered following:

- a failed ignition attempt
- or when the low supply voltage V_{DD} is lower than $V_{DD(stop)}$ in the ignition or preheat state
- or when $V_{DCI} < V_{th(start)DCI} - V_{th(hys)DCI}$ in the ignition or preheat state

A repeated aborted preheat or ignition cycle due to a drop in DCI voltage that is lower than $V_{th(start)DCI} - V_{th(hys)DCI}$ or a drop in supply voltage that is lower than $V_{DD(stop)}$ in preheat or ignition state does not increment the ignition attempt counter. The UBA20271/2 enters the hold state only delaying a new preheat cycle by the same time delay and mechanism. As shown in Figure 5 hold state retention time.

When CP is lower than $V_{th(rel)CP}$, the IC is released from the hold state and moves to the start-up state. See Figure 3. Alternatively, the hold state ends when the supply voltage is lower than $V_{DD(rst)}$ and the IC is reset.

With a 470 nF capacitor on the CP pin, the typical hold state retention delay is between 1.0 seconds and 1.7 seconds. However, it depends on where the preheat cycle is cut off on the rising or falling edge of the preheat timing. The retention time for a failed ignition always starts from the top of the rising edge on the CP pin. See Figure 5. In the hold state, a latch is set (hold state latch = 1), the oscillator is stopped, transistor HS is non-conductive and transistor LS conducting. The voltage on pin V_{DD} alternates between $V_{DD(start)}$ and $V_{DD(stop)}$ as long as the voltage on the CP pin has not reached $V_{th(rel)CP}$. See Figure 5.

The alternating supply voltage is a result of the current drawn by the IC supply pin V_{DD}. The supply current is less than 220 μA, when the supply voltage V_{DD} is increasing between $V_{DD(stop)}$ and $V_{DD(start)}$. The supply current is typically 2 mA when V_{DD} is decreasing between $V_{DD(start)}$ and $V_{DD(stop)}$. More current is drawn during the decreasing slope of V_{DD} as the internal analog supply is turned on when $V_{DD} > V_{DD(start)}$. This condition enables comparators in the IC to monitor the voltage on the CP pin and whether the supply voltage V_{DD} decreases lower than $V_{DD(stop)}$.

7.2 Oscillation and timing

7.2.1 Oscillation

The internal oscillator is a VCO circuit which generates a sawtooth waveform between the $V_{th(CF)max}$ level and 0 V. Capacitor C_{CF}, resistor $R_{ext(RREF)}$, and the voltage at the CI pin determine the frequency of the sawtooth. $R_{ext(RREF)}$ and C_{CF} determine the minimum and maximum switching frequencies. Their ratio is internally fixed. There are two ratios, the ratio between $f_{bridge(max)}$ and $f_{bridge(min)}$ is 2.5 and the ratio between $f_{bridge(max)}$ and $f_{bridge(bst)min}$ is 4.6. The sawtooth frequency is twice the half-bridge frequency.

Transistors HS (Q1) and LS (Q2) are brought into conduction with a duty cycle of approximately 50 %. Figure 8 provides an overview of the oscillator signal and driver signals. The oscillator starts oscillating at $f_{bridge(max)}$. The non-overlap time between the gate drive signals V_{GLS} and V_{GHS} is t_{no}.

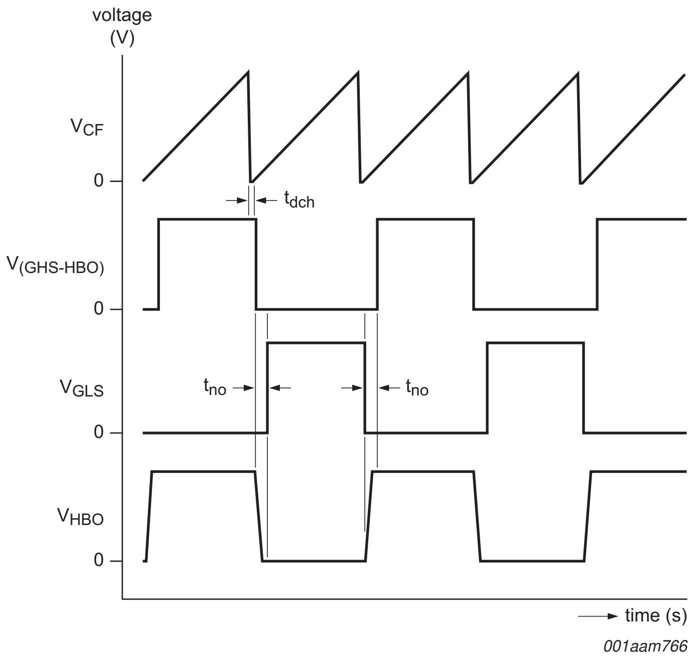


Fig 8. Sawtooth, gate driver and half-bridge output signals

7.2.2 Combined timing circuit

A combined timing circuit is included to determine the preheat time, ignition enabling time and overcurrent time, see Figure 9. The circuit consists of a clock generator defined by C_{CP} and $R_{ext(RREF)}$ and a counter. When the timer is not operating, C_{CP} is charged to 5 V. The timing circuit starts operating following the start-up state, as soon as the low supply voltage has reached $V_{DD(start)}$. Additionally the DCI input voltage is higher than $V_{th(start)DCI}$ and the voltage on pin CP must pass $V_{th(CP)max}$.The preheat time consists of eight saw-tooth pulses on the CP pin as shown in Figure 9. The maximum ignition enabling time following the preheat phase is two complete sawtooth (triangular) pulses. During the boost and burn state, part of the timer is used to generate the maximum overcurrent time (more than one half of the saw-toothed pulse). If a continuous overcurrent is detected, the timer starts.

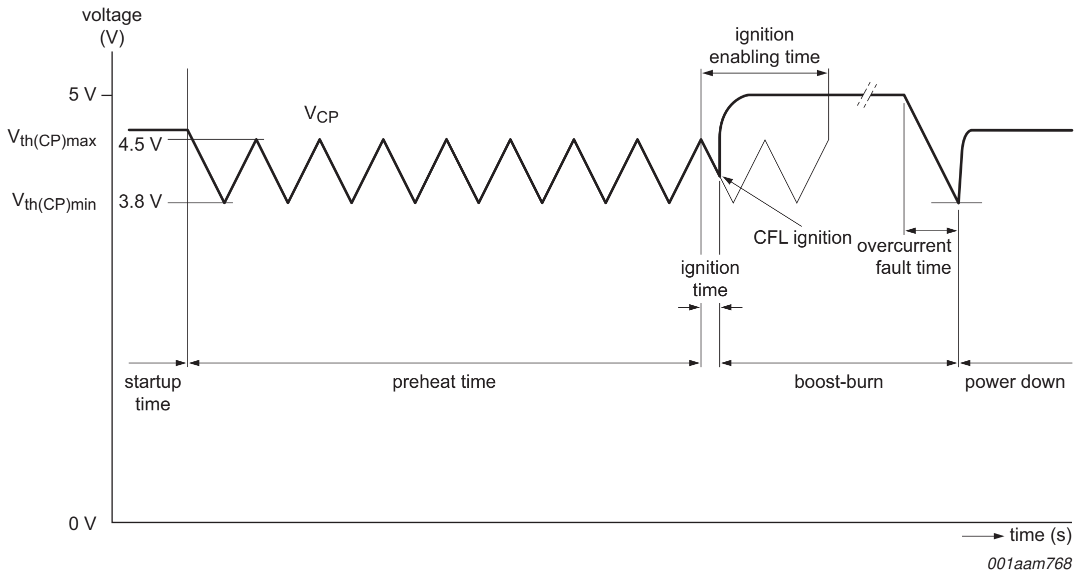


Fig 9. Timing diagram preheat, ignition and overcurrent

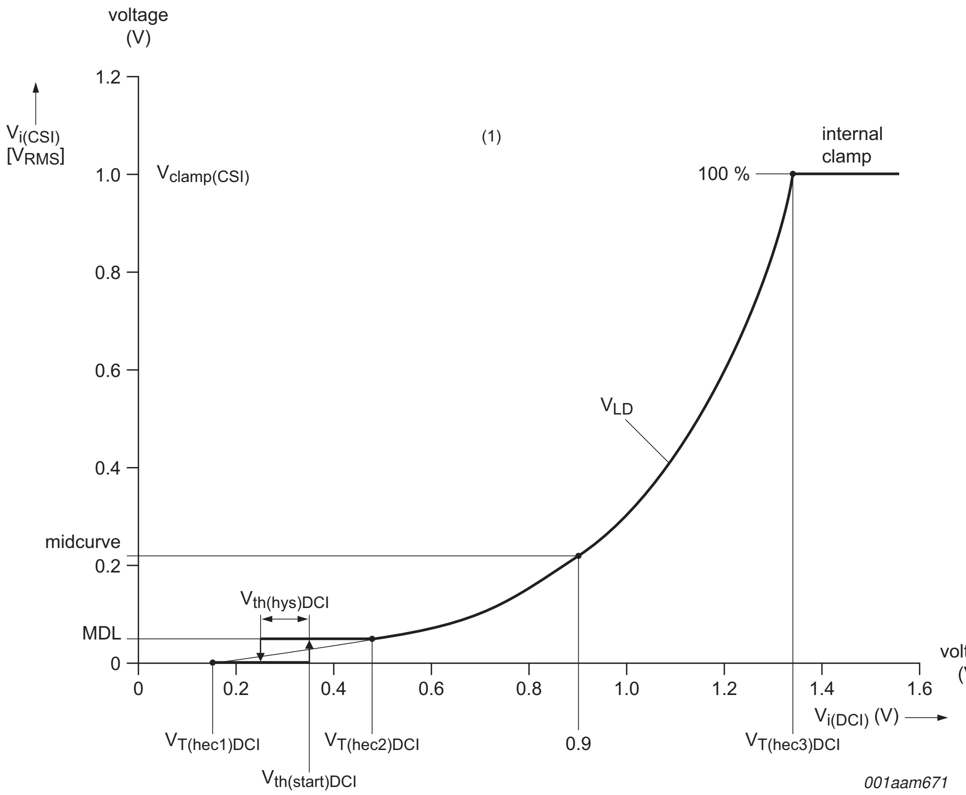
7.3 Natural linear dimming

What determines the actual internal set point level used for the current control feedback loop is an external level applied via the DCI pin for dimming. The DCI voltage is a function of the phase cut angle of the applied dimmer. To ensure that the external input for the control on the DCI pin internally stays within a certain range, this input signal passes an internal linear to logarithmic conversion circuit followed by a limiting circuit.

The linear to logarithmic conversion circuit is designed to improve dimming control by correcting for the higher sensitivity of the human eye to small changes in low light levels. See Figure 10. The conversion circuit also provides a natural perceived linear brightness adjustment of the lamp.

The limiting circuit prevents the signal falling below the MDL or rising above the 100 % reference level of $V_{clamp(CSI)}$. The output of the linear to logarithmic conversion circuit is the actual reference voltage for the lamp current control loop. See signal V_{LD} in Figure 1 (dimmer control block). When the IC is in the burn state, the voltage is equal to the RMS voltage on the CSI pin. When the control loop is regulating correctly, the upper limit is clamped at the 100 % reference level. This condition prevents lamp current values that are too high in mains overvoltage situations. See Figure 10.

The MDL level presets a minimum to which the lamp current clips at low dim levels and is adjustable via the MDL pin. An accurate minimum dimming voltage level is set by using an internal reference current (derived from the internal band gap reference circuit and resistor $R_{ext(RREF)}$) and an applied external resistor R_{MDL} on the MDL pin.



(1) $V_{i(CSI)} = V_{LD} = f(V_{i(DCI)})$

Fig 10. CSI voltage as a function of DCI voltage

7.4 Protection and power-down

7.4.1 Coil saturation protection

Coil saturation protection is integrated into the IC to allow for the use of small CFL lamps and use of small coils. Saturation of these coils is detected and excessive overcurrent due to saturation is prevented. Coil saturation protection is only enabled during the ignition state. To limit voltages and currents in the resonant circuit when there is no ignition or delayed ignition, a cycle-by-cycle control mechanism is used to prevent coil saturation. This control also limits the high peak current and dissipation in the half-bridge power transistors.

Coil saturation is detected by monitoring the voltage across the R_{SLS} resistor. A trigger is generated when this voltage exceeds the $V_{th(sat)SLS}$ level. When saturation is detected, a fixed current $\Delta I_{o(sat)CF}$ is injected into the C_{CF} capacitor to shorten the switching cycle of the half-bridge. The injected current is maintained until the end of the switching cycle. This action immediately increases the half-bridge switching frequency. Furthermore, in each successive cycle that coil saturation is detected, capacitor C_{CI} is discharged to enable an ignition time-out detection in the ignition state.

Coil saturation protection is triggered when the voltage on the SLS pin exceeds $V_{th(sat)SLS}$. The voltage V_{SLS} on the SLS pin is also used to set the preheat current. The value of external resistor R_{SLS} determines this voltage. With an internal reference source current and external resistor R_{LSAT} connected to the LSAT pin, a more secure setting of the threshold level $V_{th(sat)SLS}$ is possible. When resistor R_{LSAT} is not mounted, the $V_{th(sat)SLS}$ level is internally clamped at 2.5 V. C_{LSAT} parallel to R_{LSAT} is obligatory for stability reasons even when R_{LSAT} is not mounted.

7.4.2 OverCurrent Protection (OCP)

OCP is active in the burn and boost states (not during boost transition). When the peak absolute value of the voltage across the current sense resistor on the SLS pin exceeds the OCP reference level $V_{th(ocp)SLS}$, overcurrent is detected. A current $I_{o(CP)}$ is then sunk from the capacitor connected to the CP pin for the next full cycle. If the overcurrent is absent at the end of this cycle, this current is disabled. Instead a current, equal to $I_{o(CP)}$, is sourced to CP. If the overcurrent occurs in more than half the number of cycles, there is a net discharging of the capacitor connected to the CP pin. When the voltage, on the CP pin drops lower than $V_{th(CP)min,}$ the IC enters power-down mode. In a continuous overcurrent condition, the overcurrent time-out of $t_{fault(oc)}$ takes about $^1/_{10}$ t_{ph}. The IC then enters the power-down mode. The $V_{th(ocp)SLS}$ level corresponds with the $V_{th(sat)SLS}$ level during the ignition state.

7.4.3 OverPower Protection (OPP)

OPP is active in boost and burn state. The lamp current is limited and regulated to its nominal designed lamp current in case overvoltage situations on the mains supply occur. Overpower begins when the DCI voltage, that regulates the lamp current is exceeding the maximum DCI input range. Internally the DCI voltage is clamped to the maximum input voltage level $V_{T(hec3)DCI}$ see Figure 10. The DCI clamp level is independent of any supply voltage fluctuations.

7.4.4 Capacitive Mode Protection (CMP)

CMP is active in the ignition, burn and boost states and during boost transition. The signal across resistor R_{SLS} also provides information about the switching behavior of the half-bridge. When conditions are normal, the current flows from the source of the LS transistor to the half-bridge when the LS transistor is switched on. This results in a negative voltage on the SLS pin. As the circuit yields to capacitive mode, the voltage decreases and eventually reverses polarity. The protection prevents this condition from happening by checking if the voltage on the SLS pin is higher than $V_{th(capm)SLS}$.

If the voltage across resistor R_{SLS} is higher than the $V_{th(capm)SLS}$ threshold when the LS transistor is switched on, the circuit assumes that it is in capacitive mode. When capacitive mode is detected, the currents from the OTA are disabled and the capacitive mode sink current, $I_{o(sink)CI}$, is enabled. This sink current discharges the capacitor/resistor circuitry on the CI pin and as a result gradually increase the half-bridge frequency. Discharge continues for the remainder of the current switching cycle, so the total current on CI is equal to the sink current. If capacitive mode persists, the action is repeated until capacitive mode is not detected. If capacitive mode is no longer detected, the OTA starts regulating again.

If the conditions causing the capacitive mode persist, the OTA regulates the system back towards capacitive mode with the protection system taking control. The system operates on the edge of capacitive mode. During boost and burn state, if the load on the half-bridge continues to be capacitive at higher frequencies, CMP then eventually drives the half-bridge to the maximum frequency $f_{bridge(max)}$. From this point, the IC enters power-down mode.

7.4.5 Power-down mode

Power-down mode starts when:

- a continuous overcurrent exceeds the maximum overcurrent time-out $t_{fault(oc)}$.Or over a longer period when an overcurrent occurs in more than half the number of cycles $V_{th(CP)min}$ is reached.
- during the boost or the burn state $f_{bridge(max)}$ is reached due to capacitive mode detection
- two consecutive failed lamp ignition attempts occur

In power-down mode, the oscillator is stopped and the HS transistor is non-conductive while the LS transistor is conductive. The V_{DD} supply is internally clamped. The circuit is released from power-down mode by lowering the low voltage supply lower than $V_{DD(rst)}$ (mains switch reset).

An option exists to set the IC in power-down mode via external logic. The external power-down option is only available when the IC is in the boost or burn state. To enable the external power-down option, the CP pin is used. When pin CP, is connected via a 10 kΩ resistor to either the PGND or SGND the voltage on pin CP is pulled down lower than $V_{th(pd)CP}$. This results in the IC entering power-down mode.

Remark: Do not connect the CP pin directly to the SGND or PGND pin. Connect the SGND or PGND pin via a series 10 kΩ resistor otherwise excessive currents flow during reset and start-up. Excessive current prevent the IC from starting up.

7.4.6 OverTemperature Protection (OTP)

The OTP circuit is designed to prevent the IC from overheating in hazardous environments. The circuit is triggered when the IC temperature exceeds the maximum temperature value $T_{j(otp)}$. OTP changes the lamp current to the level that corresponds to $V_{otp(CSI)}$ level. This condition remains until the IC temperature reduces by 20 °C (=$T_{j(otp)hys}$) and returns to the DCI controlled level.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
General					
$R_{ext(RREF)}$	external resistance on pin RREF	fixed nominal value 33 kΩ	30	36	kΩ
SR	slew rate	on pins HBO with respect to GND	–4	+4	V/ns
T_{amb}	ambient temperature	P = 0.8 W	–40	85	°C
T_j	junction temperature		–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C
Currents					
I_{DM}	peak drain current	UBA20272: $T_j < T_{jmax}$; high-side; $I_{DM} = I_{DHS} = I_{HBO)}$	-	2.7	A
		low-side; $I_{DM} = I_{HBO} = I_{o(SLS)}$	-	2.7	A
	peak drain current	UBA20271: $T_j < T_{jmax}$; high-side; $I_{DM} = I_{DHS} = I_{HBO)}$	-	5.0	A
		low-side; $I_{DM} = I_{HBO} = I_{o(SLS)}$	-	5.0	A
I_D	off-state current	UBA20272: $T_j = T_{jmax;}$ high-side; P = 0.5 W; $I_D = I_{DHS} = I_{HBO}$	-	0.31	A
		low-side; $I_D = I_{HBO} = I_{o(SLS)}$	-	0.31	A
	off-state current	UBA20271: $T_j = T_{jmax;}$ P = 0.5 W; high-side; $I_D = I_{DHS} = I_{HBO}$	-	0.54	A
		low-side; $I_D = I_{HBO} = I_{o(SLS)}$	-	0.54	A
$I_{i(CF)}$	input current on pin CF		0	200	μA
Voltages					
V_{DHS}	voltage on pin DHS	UBA20272: operating	-	500	V
		during 1 second	-	600	V
	voltage on pin DHS	UBA20271: operating at T_{amb} = 25 °C	-	350	V
		operating at T_{amb} = –25 °C	-	340	V
V_{FS}	voltage on pin FS	with respect to HBO	–0.3	+14	V
V_{DD}	supply voltage		–0.3	+14	V
$V_{i(CSI)}$	input voltage on pin CSI		–5	+5	V
$V_{i(DCI)}$	input voltage on pin DCI		0	5	V
$V_{i(SLS)}$	input voltage on pin SLS		–6	+6	V

Table 3. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CI}	voltage on pin CI			0	3.5	V
V_{MDL}	voltage on pin MDL			0	5	V
ESD						
V_{ESD}	electrostatic discharge voltage	human body model:				
		all pins, except pins 16, 17, 18, 19 and 20		−2000	+2000	V
		pins 16, 17, 18, 19 and 20		−1000	+1000	V
		charged device model:				
		all pins		−400	+400	V
Latch-up			[1]	-	-	-

[1] In accordance with SNW-FQ-303: all pins.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; SO20 package on JEDEC 2S 2P board	56	K/W

10. Characteristics

Table 5. Characteristics

V_{DD} = 13 V; V_{FS} - V_{HBO} = 13 V; T_{amb} = 25 °C; settings according to default setting in Table 6, all voltages referenced to GND, positive currents flow into the IC, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Start-up state (VDD)							
$V_{DD(rst)}$	reset supply voltage	high-side switch = off; low-side switch = on		5.7	6.2	6.7	V
$V_{DD(stop)}$	stop supply voltage			9.6	10.0	10.4	V
$V_{DD(start)}$	start supply voltage			11.9	12.4	12.9	V
$V_{DD(hys)}$	hysteresis of supply voltage			2.2	2.4	2.6	V
$V_{DD(clamp)}$	clamp supply voltage	$I_{clamp(VDD)}$ = 5 mA		13.0	13.4	13.8	V
$I_{DD(clamp)}$	clamp supply current	V_{DD} = 14 V		20	30	-	mA
$I_{DD(startup)}$	start-up supply current	V_{DD} = 9 V		-	190	220	µA
$I_{DD(pd)}$	power-down supply current	V_{DD} = 9 V		-	190	220	µA
I_{DD}	supply current	default setting; V_{DCI} = 1.4 V V_{CI} = $V_{clamp(CI)}$, V_{CB} = 0 V	[1]	-	1.6	2.0	mA

Table 5. Characteristics *…continued*
V_{DD} = 13 V; V_{FS} - V_{HBO} = 13 V; T_{amb} = 25 °C; settings according to default setting in Table 6, all voltages referenced to GND, positive currents flow into the IC, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-voltage supply (DHS, HBO and FS)							
I_{leak}	leakage current	UBA20271; 300 V on high-voltage pins		-	-	30	µA
		UBA20272; 500 V on high-voltage pins		-	-	30	µA
Voltage controlled oscillator							
Output pin IC							
$V_{CI(max)}$	maximum voltage on pin CI			2.7	3.0	3.3	V
$V_{hr(CI)}$	headroom voltage on pin CI	$V_{clamp(CI)} = V_{hr(CI))} + V_{CI(max)}$; burn and boost state		-	80	-	mV
Voltage controlled oscillator							
Output pin CF							
$f_{bridge(max)}$	maximum bridge frequency	C_{CF} = 100 pF; V_{CI} = 0 V	[2]	88	100	112	kHz
$f_{bridge(bst)min}$	minimum boost bridge frequency	C_{CF} = 100 pF; $V_{CI} = V_{clamp(CI)}$	[2]	21	22	23	kHz
$f_{bridge(min)}$	minimum bridge frequency	C_{CF} = 100 pF; $V_{CI} = V_{clamp(CI)}$; V_{CB} = 0 V	[2]	38	40	42	kHz
t_{no}	non-overlap time	V_{HBO} rising edge		1.3	1.5	1.7	µs
		V_{HBO} falling edge		1.3	1.5	1.7	µs
$V_{th(CF)max}$	maximum threshold voltage on pin CF	C_{CF} = 100 pF; $V_{CI} = V_{clamp(CI)}$; V_{CB} = 0 V		2.40	2.50	2.60	V
$I_{o(bst)CF}$	boost output current on pin CF	V_{CF} = 1.5 V; $V_{CI} = V_{clamp(CI)}$		−12.3	−11.8	−11.3	µA
$I_{o(CF)min}$	minimum output current on pin CF	V_{CF} = 1.5 V; V_{CB} = 0 V; $V_{CI} = V_{clamp(CI)}$		-22.8	-21.8	-20.8	µA
$I_{o(CF)max}$	maximum output current on pin CF	V_{CF} = 1.5 V; V_{CB} = 0 V		-67.0	-60.0	-53.0	µA
Power transistors							
R_{on}	on-state resistance	UBA20272: high-side I_{DHS} = 1.1 A; T_j = 25 °C		-	3.0	3.6	Ω
	on-state resistance	UBA20271: high-side I_{DHS} = 1.1 A; T_j = 25 °C		-	1.0	1.3	Ω
R_{on}	on-state resistance	UBA20272: low-side IHBO = 1.1 A; T_j = 25 °C		-	3.0	3.6	Ω
	on-state resistance	UBA20271: low-side I_{HBO} = 1.1 A; T_j = 25 °C		-	1.0	1.3	W

Table 5. Characteristics *...continued*

V_{DD} = 13 V; V_{FS} - V_{HBO} = 13 V; T_{amb} = 25 °C; settings according to default setting in Table 6, all voltages referenced to GND, positive currents flow into the IC, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{on(150)}/R_{on(25)}$	on-state resistance ratio (150 °C to 25 °C)	R_{ON} at T_j = 150 °C / R_{ON} at T_j = 25 °C		-	1.7	-	
Bootstrap diode							
V_F	forward voltage	bootstrap diode; I_{FS} = 5 mA; ($V_F = V_{DD} - V_{FS}$)		1.3	1.7	2.1	V
Preheat current sensor							
Input: pin SLS							
$I_{I(SLS)}$	input current on pin SLS	$V_{i(SLS)}$ = 0.4 V		-	-	1	μA
$V_{ph(SLS)}$	preheat voltage on pin SLS		[3]	0.57	0.60	0.63	V
Output: pin CI							
$I_{o(source)CI}$	source output current on pin CI	V_{CI} = 2.0 V; $V_{i(SLS)}$ < 0.6 V		−10.6	−9.6	−8.6	μA
$I_{o(sink)CI}$	sink output current on pin CI	V_{CI} = 2.0 V; $V_{i(SLS)}$ > 0.6 V		26	29	32	μA
Preheat timer, ignition timer, overcurrent fault timer							
Pin CP							
t_{ph}	preheat time	C_{CP} = 470 nF; $R_{ext(RREF)}$ = 33 kΩ		-	0.93	-	s
$t_{en(ign)}$	ignition enable time	C_{CP} = 470 nF; $R_{ext(RREF)}$ = 33 kΩ		-	0.22	-	s
$t_{fault(oc)}$	overcurrent fault time	C_{CP} = 470 nF; $R_{ext(RREF)}$ = 33 kΩ; initial voltage V_{CP} = 5.0 V		-	0.10	-	s
$I_{o(CP)}$	output current on pin CP	V_{CP} = 4.1 V; source (−) and sink (+)		5.5	5.9	6.3	μA
$V_{th(CP)min}$	minimum threshold voltage on pin CP			-	3.8	-	V
$V_{th(CP)max}$	maximum threshold voltage on pin CP			-	4.5	-	V
$V_{hys(CP)}$	hysteresis voltage on pin CP			0.6	0.7	0.8	V
$I_{pu(CP)}$	pull-up current on pin CP	V_{CP} = 3.8 V		-	−60	-	μA
$V_{th(pd)CP}$	power-down threshold voltage on pin CP	burn state, pin CP connected to SGND via 10 kΩ		-	1.0	-	V
$V_{th(rel)CP}$	release threshold voltage on pin CP	hold state, V_{DCI} = 1.4 V		-	2.7	-	V
Boost timer							
Pin CB							
t_{bst}	boost time	C_{CB} = 470 nF; T_j < 80 °C		-	148	-	s
$I_{o(CB)}$	output current on pin CB	V_{CB} = 2.35 V; source (−) and sink (+)		0.8	1.0	1.2	μA

Table 5. Characteristics *...continued*

V_{DD} = 13 V; V_{FS} - V_{HBO} = 13 V; T_{amb} = 25 °C; settings according to default setting in Table 6, all voltages referenced to GND, positive currents flow into the IC, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(CB)min}$	minimum threshold voltage on pin CB		-	1.1	-	V
$V_{th(CB)max}$	maximum threshold voltage on pin CB		-	3.6	-	V
$V_{hys(CB)}$	hysteresis voltage on pin CB		2.3	2.5	2.7	V
$T_{j(bp)bst}$	boost bypass junction temperature	T_j sensed at end ignition time	65	80	95	°C
$T_{j(end)bst}$	boost end junction temperature	T_j during boost time	105	120	135	°C
$I_{det(dis)bst}$	boost disable detection current	V_{CB} = 0 V	-30	-25	-20	μA
$t_{t(bst-burn)}$	transition time from boost to burn	C_{CP} = 470 nF; T_j < 80 °C	-	3.6	-	s
Pin CSI						
N_{LCBR}	lamp current boost ratio	V_{CSI} in boost state versus V_{CSI} in burn state; V_{DCI} = 1.34 V	1.4	1.5	1.6	
Coil saturation protection and overcurrent detection						
Input: pin SLS						
$V_{th(sat)SLS}$	saturation threshold voltage on pin SLS	ignition state; R_{LSAT} = 47 kΩ	1.10	1.18	1.25	V
$V_{th(ocp)SLS}$	overcurrent protection threshold voltage on pin SLS	boost state and burn state; R_{LSAT} = 47 kΩ	1.10	1.18	1.25	V
t_{leb}	leading edge blanking time	detection disabled first part of GLS time	-	800	-	ns
$I_{o(sink)CI}$	sink output current on pin CI	V_{CI} = 2.0 V; ignition state; $V_{i(SLS)} > V_{th(sat)SLS}$; cycle clocked	26	29	32	μA
Input: pin LSAT						
$I_{source(LSAT)}$	source current on pin LSAT	V_{LSAT} = 1.2 V	−26.3	−25.0	−23.7	μA
$V_{clamp(LSAT)}$	clamp voltage on pin LSAT	$R_{LSAT} = \infty$;	2.3	2.5	2.7	V
Output: pin CF						
$\Delta I_{o(sat)CF}$	saturation output current difference on pin CF	V_{CF} = 1.5 V; ignition state; low side switch = on	-	160	-	μA

Table 5. Characteristics *...continued*

V_{DD} = 13 V; V_{FS} - V_{HBO} = 13 V; T_{amb} = 25 °C; settings according to default setting in Table 6, all voltages referenced to GND, positive currents flow into the IC, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Ignition current detection							
Input: pin CSI							
$V_{th(det)ign(CSI)}$	ignition detection threshold voltage on pin CSI			0.55	0.60	0.65	V
$t_{w(det)ign(min)}$	minimum ignition detection pulse width	$V_{th(det)ign(CSI)}$ = 0.75 V square pulse		685	885	1085	ns
Capacitive mode detection							
Input: pin SLS							
$V_{th(capm)SLS}$	capacitive mode threshold voltage on pin SLS		[4]	−15	−5	0	mV
Output: pin CI							
$I_{o(sink)CI}$	sink output current on pin CI	V_{SLS} > $V_{th(capm)SLS}$; V_{CI} = 2.0 V; ignition state or boost and burn state		26	29	32	μA
Lamp current sensor and dimming control							
Input: pin CSI							
$R_{i(CSI)}$	input resistance on pin CSI	$V_{i(CSI)}$ = 1 V		1	-	-	MΩ
		$V_{i(CSI)}$ = −1 V		40	50	60	kΩ
$V_{i(CSI)}$	input voltage on pin CSI	controlled feedback RMS voltage at minimum dim level; $V_{i(DCI)}$ = 0 V; $R_{ext(RREF)}$ = 33 kΩ; R_{MDL} = 2.0 kΩ		44	50	56	mV
		controlled feedback RMS voltage at mid scale of I_{in} log curve in burn state; $V_{i(DCI)}$ = 0.9 V; $R_{ext(RREF)}$ = 33 kΩ		-	215	-	mV
		voltage rectification range for linear operation		−2.5	-	+2.5	V
$V_{clamp(CSI)}$	clamping voltage on pin CSI	100 % light output; $V_{i(DCI)}$ ≥ 1.34 V		-	1.0	-	V
Input: pin DCI							
$V_{i(DCI)}$	input voltage on pin DCI	minimum voltage set by MDL pin resistor		$V_{T(hec2)DCI}$	-	1.34	V
$R_{i(DCI)}$	input resistance on pin DCI	$V_{i(CSI)}$ = 1 V		1	-	-	MΩ
$V_{th(bst)DCI}$	boost threshold voltage on pin DCI			1.00	1.05	1.10	V
$V_{th(bst)hys(DCI)}$	hysteresis boost threshold voltage on pin DCI			80	100	120	mV

Table 5. Characteristics *…continued*

V_{DD} = 13 V; V_{FS} - V_{HBO} = 13 V; T_{amb} = 25 °C; settings according to default setting in Table 6, all voltages referenced to GND, positive currents flow into the IC, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(start)DCI}$	start threshold voltage on pin DCI		-	0.35	-	V
$V_{th(hys)DCI}$	hysteresis threshold voltage on pin DCI		80	100	120	mV
$V_{T(hec1)DCI}$	human eye correction 1 transition voltage on pin DCI	$V_{i(CSI)}$ = 0 V; V_{MDL} = 0 V	-	0.17	-	V
$V_{T(hec2)DCI}$	human eye correction 2 transition voltage on pin DCI	$R_{ext(RREF)}$ = 33 kΩ; R_{MDL} = 2.0 kΩ; $V_{i(CSI)} = V_{clamp(CSI)}$	-	0.44	-	V
$V_{T(hec3)DCI}$	human eye correction 3 transition voltage on pin DCI	$V_{i(CSI)}$ = 1 V	-	1.34	-	V
$V_{otp(CSI)}$	overtemperature protection voltage on pin CSI	RMS voltage; $R_{ext(RREF)}$ = 33 kΩ; R_{MDL} = 2.0 kΩ; $V_{i(DCI)}$ = 1.5 V; $T_j > T_{j(otp)} - T_{j(otp)hys}$	380	400	420	mV
Output: pin CI						
$I_{o(CI)}$	output current on pin CI	burn state; source (−) and sink (+); V_{CI} = 2.0 V	85	95	105	μA
Input: pin MDL						
$I_{source(MDL)}$	source current on pin MDL		-26.3	-25.0	-23.7	μA
V_{MDL}	voltage on pin MDL	$R_{ext(RREF)}$ = 33 kΩ; R_{MDL} = 2.0 kΩ	-	50	-	mV
Temperature protection						
$T_{j(otp)}$	overtemperature protection junction temperature		145	160	175	°C
$T_{j(otp)hys}$	hysteresis overtemperature protection junction temperature		10	20	30	°C

[1] For the default setting, see Table 6.

[2] Switching frequency of the half-bridge output HBO. The sawtooth frequency on pin CF is twice as high.

[3] Data sampling of $V_{ph(SLS)}$ is performed at the end of the conduction period of the low-side power MOSFET, in preheat state.

[4] Data sampling of $V_{th(capm)SLS}$ is performed at the start of conduction of the low-side power MOSFET, in all states with oscillator active.

11. Application information

11.1 Design equations

All equations are only valid for $R_{ext(RREF)}$ = 33 kΩ

11.1.1 C_{CP} related timing equations:

- **Preheat time:**

$$t_{ph} = \frac{C_{CP}}{I_{o(CP)}} \times (16 \times V_{hys(CP)} + 5 - V_{th(CP)max}) \quad (1)$$

- **Ignition enabling time:**

$$t_{en(ign)} = \frac{C_{CP}}{I_{o(CP)}} \times 4 \times V_{hys(CP)} \quad (2)$$

- **Overcurrent fault time:**

$$t_{fault(oc)} = \frac{C_{CP}}{I_{o(CP)}} \times (5 - V_{th(CP)min}) \quad (3)$$

- **Transition to burn time:**

$$t_{t(bst-burn)} = \frac{C_{CP}}{I_{o(CP)}} \times (64 \times V_{hys(CP)} + 5 - V_{th(CP)max}) \quad (4)$$

- **Restart delay time**

$$t_{d(restart)} = \frac{C_{CP}}{I_{restart(CP)}} \times (V_{th(CP)max} - V_{th(rel)CP}) \quad (5)$$

Where: $I_{restart(CP)}$ = 0.5 μA (typical)

11.1.2 C_{CB} related timing equations:

- **Boost time:**

$$t_{bst} = \frac{C_{CB}}{I_{o(CB)}} \times (126 \times V_{hys(CB)} + V_{th(CB)min} - 0.6) \quad (6)$$

11.1.3 C_{CF} related frequency equations:

- **Maximum bridge frequency:**

$$f_{bridge(max)} = \frac{0.5}{\frac{C_{CF} + C_{par}}{I_{o(CF)max}} \times V_{th(CF)max} + t_{dch}} \quad (7)$$

- **Minimum bridge frequency with disabled boost:**

$$f_{bridge(min)} = \frac{0.5}{\frac{C_{CF} + C_{par}}{I_{o(CF)min}} \times V_{th(CF)max} + t_{dch}} \quad (8)$$

- **Minimum bridge frequency with enabled boost**

$$f_{bridge(bst)min} = \frac{0.5}{\frac{C_{CF} + C_{par}}{I_{o(bst)CF}} \times V_{th(CF)max} + t_{dch}} \quad (9)$$

Where: C_{par} = 4.7 [pF] and t_{dch} = 0.4 [μs] (typical)

11.1.4 R_{SLS} related preheat current:

$$I_{ph(M)} = \frac{V_{ph(SLS)}}{R_{SLS}} \qquad I_{ph(RMS)} \approx \frac{V_{ph(SLS)}}{R_{SLS} \times \sqrt{3}} \quad (10)$$

11.1.5 R_{MDL} related MDL:

- **MDL threshold voltage:**

$$V_{MDL} = R_{MDL} \times I_{source(MDL)} \quad (11)$$

11.1.6 R_{LSAT} related saturation and overcurrent threshold level

- **Saturation threshold voltage**

$$V_{th(sat)SLS} = V_{th(ocp)SLS} = R_{LSAT} \times I_{source(LSAT)} \quad (12)$$

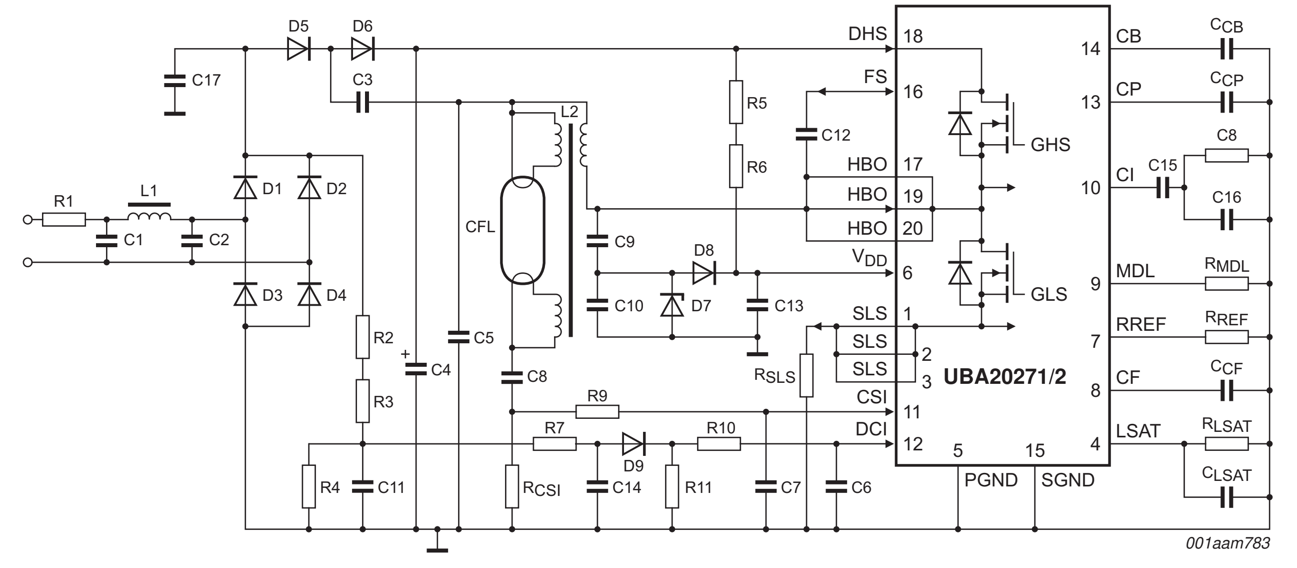


Fig 11. Application diagram

Detailed in Table 6 is a list of typical application components. See Figure 11.