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UCB1400

Audio codec with touch screen controller and power management monitor

Rev. 02 — 21 June 2002 **Product data**

1. General description

The UCB1400 is a stereo audio codec equipped with touch screen and power management interfaces. It integrates an AC ’97 Rev. 2.1 interface for communication to an AC link host controller such as the Intel Xscale™ processor. The stereo audio codec inputs connect directly to a microphone or line level sources such as a CD player. The stereo audio codec outputs at line level and can drive a headphone directly. The touch screen interface connects directly to a 4-wire resistive touch screen. A built-in 10-bit analog-to-digital converter provides readout of touch screen and power management parameters. Ten general-purpose I/O pins provide programmable inputs and/or outputs to the system.

2. Features

- 48-pin LQFP surface mount package and low external component count for minimal PCB space requirement
- Integrated AC ’97 Rev. 2.1 interface
- 20-bit stereo audio codec supporting programmable sample rates, and input/output gain control
  - Stereo line input and mono microphone input
  - Stereo line/headphone output with bass/treble control
  - Headphone driver with short circuit protection and virtual ground for DC coupling
- 4-wire resistive touch screen interface circuit supporting position, pressure and plate resistance measurements
- 10-bit successive approximation ADC with internal track-and-hold circuit and analog multiplexer for touch screen readout and monitoring of four external high voltage (7.5 V) sources
- Ten general purpose input/output pins
- 3.3 V supply voltage and built-in power saving modes for portable and battery powered applications.

3. Applications

- Smart mobile phones
- Handheld PCs
- Palm-top PCs
- Personal Intelligent Communicators (PIC)
- Personal Digital Assistants (PDA).

PHILIPS

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
UCB1400BE	LQFP48	Plastic low profile quad flat package, 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

5. Block diagram

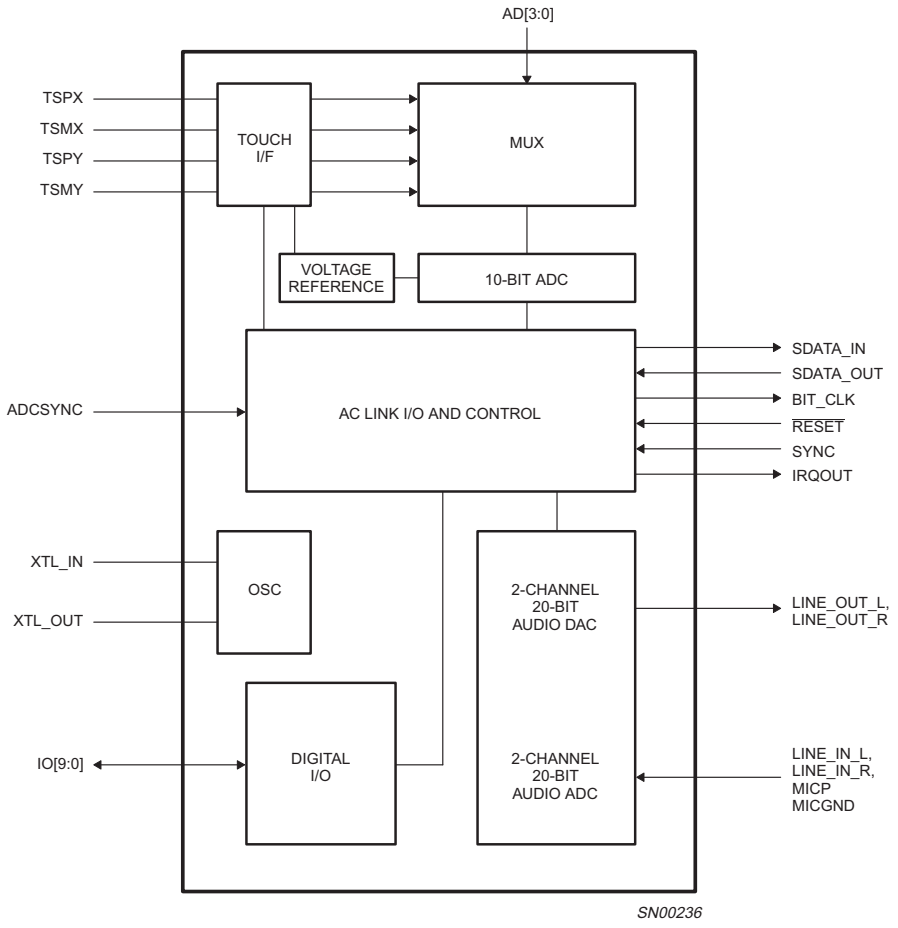


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

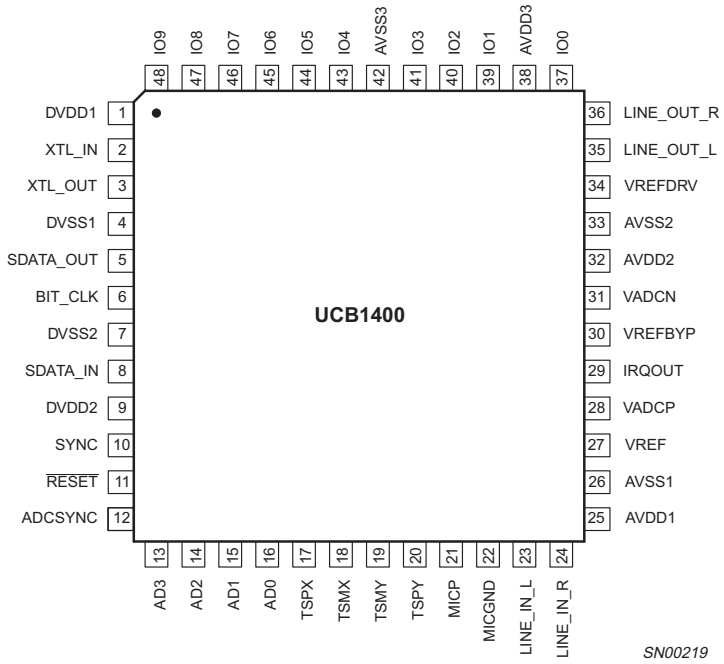


Fig 2. Pin configuration (LQFP48).

6.2 Pin description

Table 2: Pin description

Total pin count = 48

Symbol	Pin	Type	Default state	Description
AC-link, crystal and interrupt interface (pin count = 8)				
XTL_IN	2	I	–	24.576 MHz crystal / master clock input
XTL_OUT	3	O	–	24.576 MHz crystal
$\overline{\text{RESET}}$	11	I	–	AC-link master reset
SYNC	10	I	–	AC-link sample sync
BIT_CLK	6	O	0	AC-link 12.288 MHz serial data clock
SDATA_OUT	5	I	–	AC-link serial data output. UCB1400 input stream
SDATA_IN	8	O	0	AC-link serial data input. UCB1400 output stream
IRQOUT	29	O	0	Interrupt output

Table 2: Pin description…*continued*

Total pin count = 48

Symbol	Pin	Type	Default state	Description
Audio interface (pin count = 6)				
MICP	21	I	–	Microphone input
MICGND	22	I	closed	Microphone ground switch input
LINE_IN_L	23	I	–	Line in left channel
LINE_IN_R	24	I	–	Line in right channel
LINE_OUT_L	35	O	driver off	Line out left channel
LINE_OUT_R	36	O	driver off	Line out right channel
ADC and touch screen interface (pin count = 9)				
AD[3:0]	13, 14, 15, 16	I	–	Analog voltage input
TSPX	17	I/O	Hi-Z	Touch screen positive X-plate
TSMX	18	I/O	Hi-Z	Touch screen negative X-plate
TSMY	19	I/O	Hi-Z	Touch screen negative Y-plate
TSPY	20	I/O	Hi-Z	Touch screen positive Y-plate
ADCSYNC	12	I	–	ADC synchronization pulse
GPIO interface (pin count = 10)				
IO[9:0]	48, 47, 46, 45, 44, 43, 41, 40, 39, 37	I/O	Input	General purpose input/output
Power and miscellaneous (pin count = 15)				
DVDD2, DVDD1	9, 1	S	–	Digital supply
DVSS2, DVSS1	7, 4	S	–	Digital ground
AVDD3, AVDD2, AVDD1	38, 32, 25	S	–	Analog supply
AVSS3, AVSS2, AVSS1	42, 33, 26	S	–	Analog ground
VREFDRV	34	O	–	Reference voltage for headphone drivers
VREF	27	O	–	Reference voltage
VADCP	28	S	–	Audio ADC positive reference voltage
VADCN	31	S	–	Audio ADC negative reference voltage
VREFBYP	30	I/O	Hi-Z	Reference bypass output/ external reference voltage input

7. Functional description

7.1 Functional block diagram

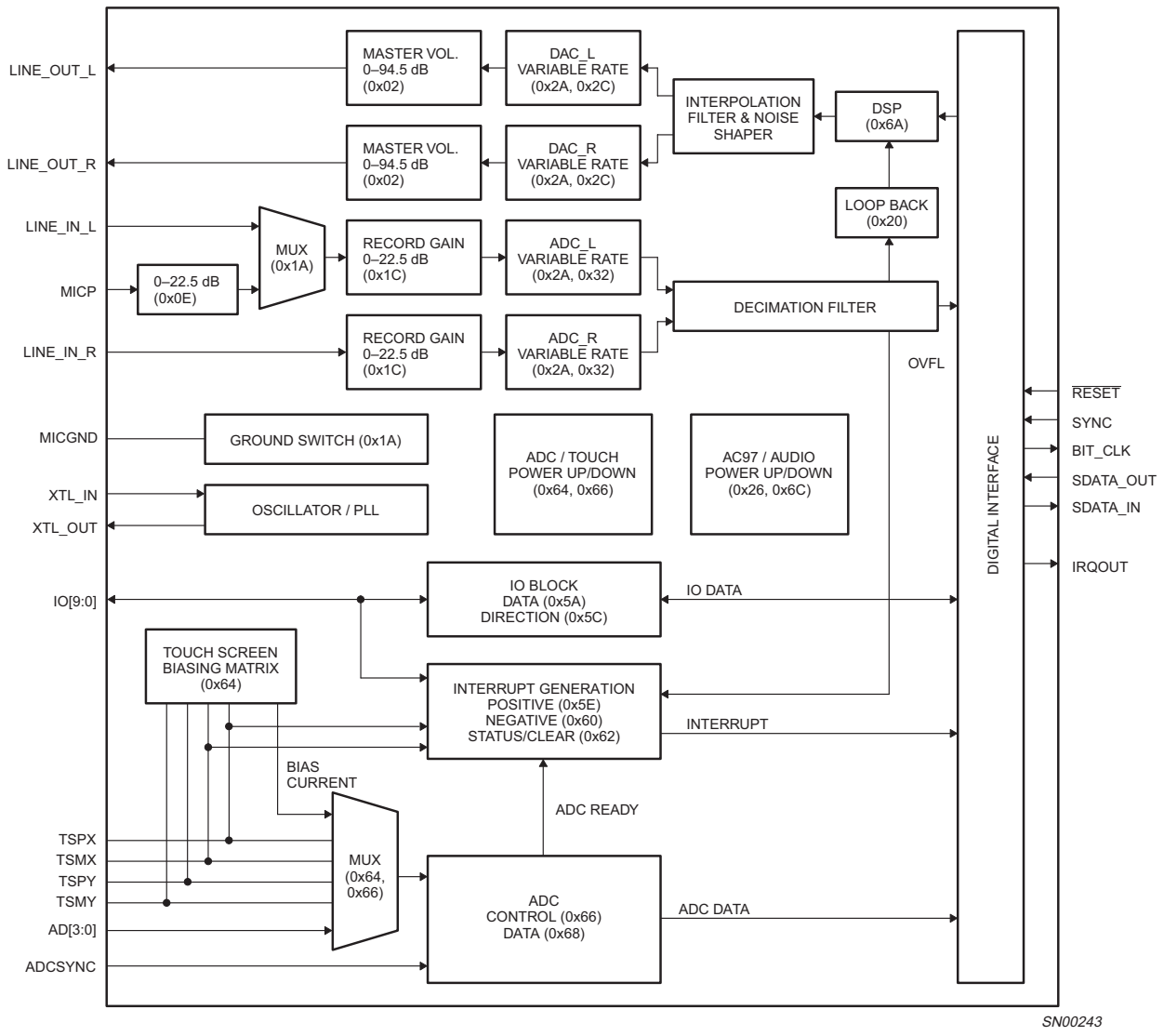


Fig 3. Functional block diagram.

8. AC ’97 interface

The UCB1400 implements an AC ’97 Revision 2.1 interface. Refer to the *Audio Codec ’97 Component Specification Revision 2.1* from Intel.

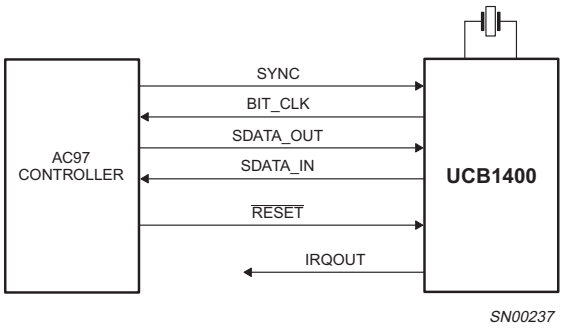


Fig 4. UCB1400 and AC ’97 controller connection diagram.

8.1 Clocking

The UCB1400 functions only as a primary codec. As such, it derives its clock internally from an externally attached 24.576 MHz crystal or clock oscillator, and drives a buffered and divided down ($1/2$) clock to its digital companion controller over AC-link under the signal name “BIT_CLK”.

The beginning of all audio sample packets, or Audio Frames, transferred over AC-link is synchronized to the rising edge of the SYNC signal. SYNC is driven by the AC ’97 Controller. The AC ’97 Controller takes BIT_CLK as an input and generates SYNC by dividing BIT_CLK by 256 and applying some conditioning to tailor its duty cycle. This yields a 48 kHz SYNC signal whose period defines an audio frame. Data is transitioned on AC-link on every rising edge of BIT_CLK, and subsequently sampled on the receiving side of AC-link on each immediately following falling edge of BIT_CLK.

8.2 Resetting UCB1400

The UCB1400 recognizes the following types of reset:

- Cold reset: where all UCB1400 logic (registers included) is initialized to its default state. Initiated by bringing $\overline{\text{RESET}}$ LOW for at least 1 µs.
- Warm reset: where the contents of the UCB1400 register set are left unaltered. Initiated by bringing SYNC HIGH for at least 1 µs without BIT_CLK.
- Register reset: which only initializes the UCB1400 registers to their default states. Initiated by a write to register 0x00.

After signaling a reset to UCB1400, the AC ’97 Controller should not attempt to play or capture audio data until it has sampled a “Codec Ready” indication from UCB1400.

8.3 Digital interface

8.3.1 AC-link digital serial interface protocol

The UCB1400 incorporates a 5-pin digital serial interface that links it to the AC ’97 Controller. AC-link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input, and output audio and modem streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. The control and data slots defined by UCB1400 include:

- SDATA_OUT TAG (output slot 0)
- SDATA_IN TAG (input slot 0)
- Control (CMD ADDR & DATA) write port (output slots 1, 2)
- Status (STATUS ADDR & DATA) read port (input slots 1, 2)
- PCM L & R DAC playback (output slots 3, 4)
- PCM L & R ADC record (input slots 3, 4)
- GPIO interrupt status (input slot 12)

The AC-link protocol provides for a special 16-bit time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data.

SYNC remains HIGH for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is HIGH is defined as the Tag Phase. The remainder of the audio frame where SYNC is LOW is defined as the “Data Phase”. Additionally, for power savings, all clock, sync, and data signals can be halted. UCB1400 is implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

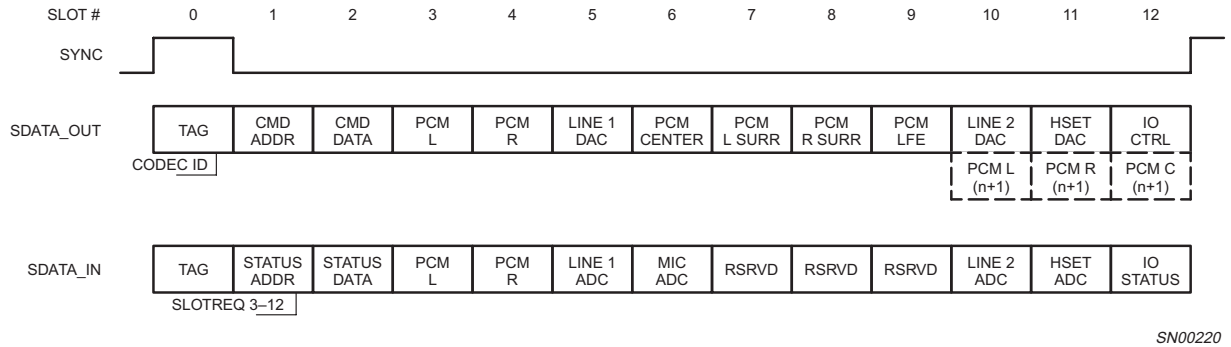


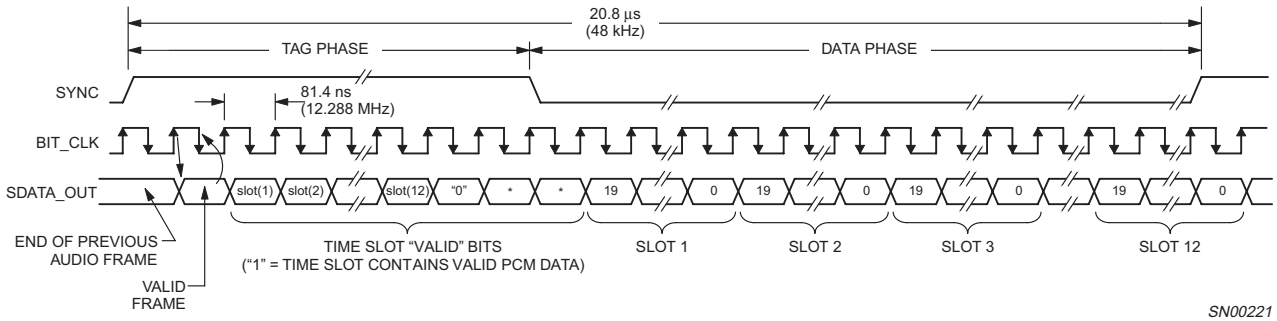
Fig 5. Standard bi-directional audio frame.

8.3.2 AC-link audio output frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting UCB1400's DAC inputs, and control registers. Each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits which are used for AC-link protocol infrastructure.

Slot 0: TAG: Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the 'Valid Frame' bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by UCB1400 indicate which of the corresponding 12 time slots contain valid data. In this way, data streams of differing sample rates can be transmitted across AC-link at its fixed 48 kHz audio frame rate.

Figure 6 illustrates the time slot based AC-link protocol. (Note that Bits 1 and 0 of slot 0 tag phase are used for primary/secondary codec addressing as described in Section 8.4.



* See Table 4.

Fig 6. AC Link audio output frame.

A new audio output frame begins with a LOW-to-HIGH transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the UCB1400 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 Controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by UCB1400 on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

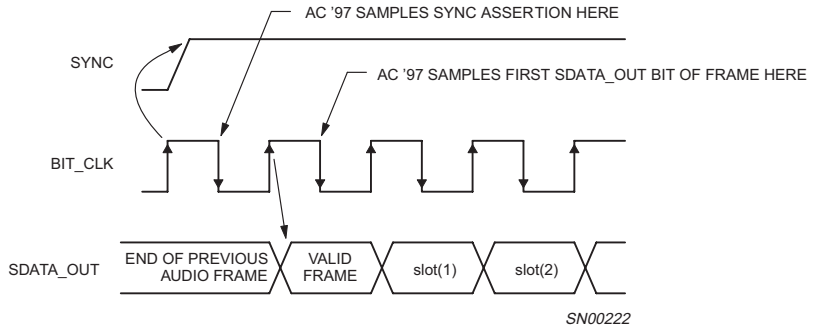


Fig 7. Start of an audio output frame.

SDAT_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions stuffed with 0s by the AC '97 Controller. If there are less than 20 valid bits within an assigned and valid time slot, the AC '97 Controller always stuffs all trailing non-valid bit positions of the 20-bit slot with 0s.

Slot 1: Command address port: The command port is used to control features, and monitor status (see Section 8.3.3 "AC-link audio input frame (SDATA_IN)", Slots 1 and 2) for AC '97 functions including, but not limited to, sample rate, codec configuration, and power management.

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries, and reserves support for 64 odd addresses, as described in *AC '97 2.1 Component Specification Appendix D*. Only the even registers (00h, 02h, etc.) are currently defined, odd register (01h, 03h, etc.) accesses are reserved.

Note that shadowing of the control register file on the AC '97 Controller is an option left open to the implementation of the AC '97 Controller. UCB1400's control register file is readable as well as writable to provide more robust testability.

Audio output frame slot 1 communicates control register address, and write/read command information to the UCB1400.

Command Address Port bit assignments are:

- Bit(19) Read/write command (1 = read, 0 = write).
- Bit(18:12) Control register index (64 16-bit locations, addressed on even byte boundaries)
- Bit(11:0) Reserved (stuffed with 0s)

The first bit (MSB) sampled by UCB1400 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate with the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0s by the AC '97 Controller.

Slot 2: Command data port: The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1, bit 19).

- Bit(19:4) Control Register Write Data (stuffed with 0s if current operation is a read).
- Bit(3:0) Reserved (stuffed with 0s)

If the current command port operation is a read, then the entire slot time must be stuffed with 0s by the AC ’97 Controller.

Slot 3: PCM playback left channel: Audio output frame slot 3 is the composite digital audio left playback stream. Typically, this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC ’97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20 bits is transferred, the AC ’97 Controller must stuff all trailing non-valid bit positions within this time slot with 0s.

Slot 4: PCM playback right channel: Audio output frame slot 4 is the composite digital audio right playback stream. Typically, this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC ’97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20 bits is transferred, the AC ’97 Controller must stuff all trailing non-valid bit positions within this time slot with 0s.

Slots 5 through 12: All other audio output frame slots are ignored by the UCB1400.

8.3.3 AC-link audio input frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC ’97 Controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits, which are used for AC-link protocol infrastructure.

Slot 0: TAG: Within slot 0, the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether UCB1400 is in the ‘Codec Ready’ state or not. If the ‘Codec Ready’ bit is a 0, this indicates that UCB1400 is not ready for normal operation. This condition is normal following the deassertion of power-on reset, for example, while UCB1400’s voltage references settle. When the AC-link ‘Codec Ready’ indicator bit is a logic 1, it indicates that the AC-link and UCB1400 control and status registers are in a fully operational state. The AC ’97 Controller must further probe the Power-down Control/Status Register (0x26) to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting UCB1400 into operation, the AC ’97 Controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that the UCB1400 has gone ‘Codec Ready’. Once the UCB1400 is sampled ‘Codec Ready’ then the next 12 bit positions sampled by the AC ’97 Controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. Figure 8 illustrates the time slot based AC-link protocol.

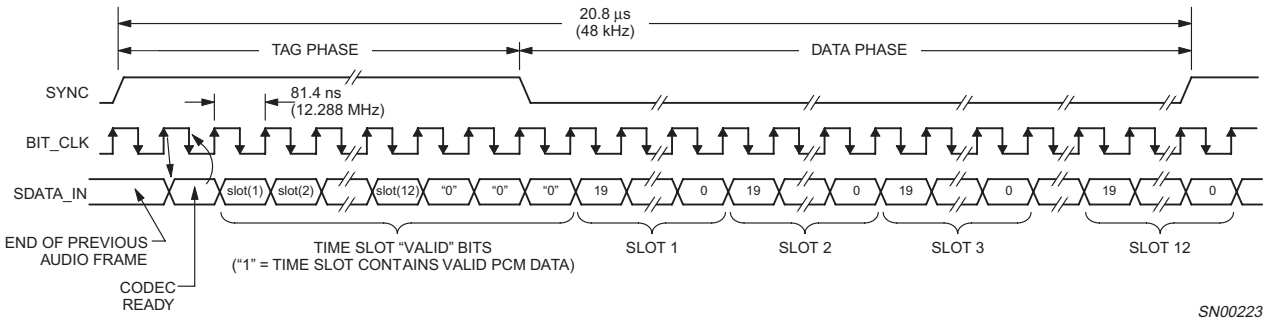


Fig 8. AC-link audio input frame.

A new audio input frame begins with a LOW-to-HIGH transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, UCB1400 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, UCB1400 transitions SDATA_IN into the first bit position of slot 0 (‘Codec Ready’ bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC ’97 Controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

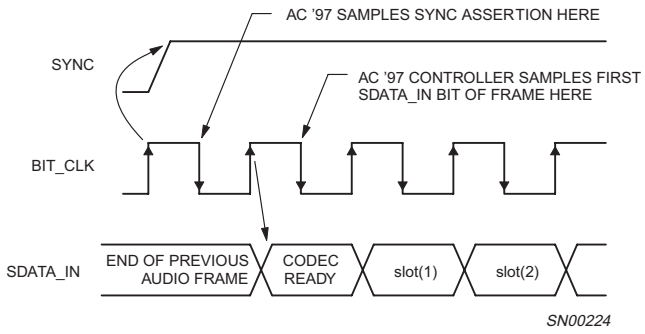


Fig 9. Start of an audio input frame.

SDATA_IN’s composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0s by the UCB1400. SDATA_IN data is sampled on the falling edges of BIT_CLK.

Slot 1: Status address port: The status port is used to monitor status for UCB1400 functions including, but not limited to, codec settings and power management.

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged 'valid' by UCB1400 during slot 0.)

Status address port bit assignments are:

- Bit(19) Reserved (stuffed with 0s)
- Bit(18:12) Control register index (echo of register index for which data is being returned)
- Bit(11:2) SLOTREQ bits: Only bits 11 and 10 (PCM L & R) shall be used by UCB1400. All unused bits shall be stuffed with 0s.
- Bit(1, 0) Reserved (stuffed with 0s)

The first bit (MSB) generated by UCB1400 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, the next 10 bits are the SLOTREQ bits, two of which (bits 11 and 10) are used by UCB1400 to request data using the variable sample rate signaling protocol as defined in the *AC '97 Component Specification*. The trailing 2 bit positions are stuffed with 0s by UCB1400.

Slot 2: Status data port: The status data port delivers 16-bit control register read data.

- Bit(19:4) Control register read data (stuffed with 0s if tagged 'invalid' by UCB1400)
- Bit(3:0) Reserved (stuffed with 0s)

If slot 2 is tagged invalid by UCB1400, then the entire slot will be stuffed with 0s by UCB1400.

Slot 3: PCM record left channel: Audio input frame slot 3 is the left channel output of UCB1400's input MUX, post-ADC. The UCB1400's ADCs are implemented to support 20-bit resolution. UCB1400 ships out its ADC output data (MSB first) to fill out its 20-bit time slot.

Slot 4: PCM record right channel: Audio input frame slot 4 is the right channel output of UCB1400's input MUX, post-ADC. The UCB1400's ADCs are implemented to support 20-bit resolution. UCB1400 ships out its ADC output data (MSB first) to fill out its 20-bit time slot.

Slot 12: GPIO status: Audio output frame slot 12 is used to carry modem GPIO input data. Table 3 shows the definition by *AC '97 Component Specification*. The UCB1400 does not make use of slot 12 to report its IO pin status. It only uses the GPIO_INT as an optional means (when the GIEN bit is set in the Feature CSR1 register) to signify an interrupt event (in addition to pin IRQOUT).

Table 3: Slot 12 definition

Bit	GPIO	Name	Sense	Description
19-4	GPIO[15:0]		in/out	Modem GPIO as defined by the *Intel AC '97 Component Specification*.
3-1		Vendor rsrvd		Vendor optional.
0		GPIO_INT	in	GPIO_INT (uses same logic as wake-up event)

Slots 5 through 11: All other audio input frame slots shall be stuffed with 0s by the UCB1400.

8.3.4 AC-link low power mode

The AC-link signals can be placed in a low power mode. When the UCB1400's PR4 bit is set to '1' in the Power-down status and control register (0x26), both BIT_CLK and SDATA_IN will be brought to, and held at, a logic LOW voltage level.

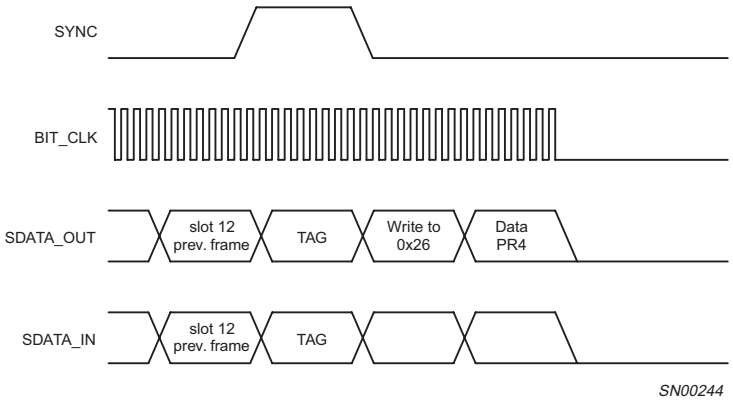


Fig 10. AC-link power-down timing.

BIT_CLK and SDATA_IN are transitioned low immediately following the decode of the write to Register 0x26 with PR4. When the AC '97 Controller driver is at the point where it is ready to program the AC-link into its low power mode, slots (1 and 2) **are assumed to be** the only valid stream in the audio output frame.

The AC '97 Controller should also drive SYNC and SDATA_OUT LOW after programming UCB1400 AC '97 to this low power, halted mode. The AC '97 Controller is required to drive and keep SYNC and SDATA_OUT LOW in this low power, halted mode.

Once the UCB1400 has been instructed to halt BIT_CLK, a special 'wake-up' protocol must be used to bring the AC-link to the active mode since normal audio output and input frames cannot be communicated in the absence of BIT_CLK.

Waking up the AC-link: There are two methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC ’97 Controller that performs the wake-up task.

AC-link protocol provides for a ‘Cold AC ’97 Reset’, and a ‘Warm AC ’97 Reset’. The current power-down state would ultimately dictate which form of AC ’97 reset is appropriate. Unless a ‘cold’ or ‘register’ reset (a write to the Reset register) is performed, wherein the UCB1400 registers are initialized to their default values, registers are required to keep state during all power-down modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of four audio frame times following the frame in which the power-down was triggered. When AC-link powers-up, it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

Cold AC ’97 reset: A cold reset is achieved by asserting $\overline{\text{RESET}}$ for the minimum specified time. By driving $\overline{\text{RESET}}$ LOW, all UCB1400 control registers will be initialized to their default power-on reset values. BIT_CLK and SDATA_OUT will be activated, or re-activated as the case may be. $\overline{\text{RESET}}$ is an asynchronous input to the UCB1400.

Warm AC ’97 reset: A warm AC ’97 reset will re-activate the AC-link without altering the current AC ’97 register values. A warm reset is signaled, in the absence of BIT_CLK, by driving SYNC HIGH for a minimum of 1 μs.

Within normal audio frames, SYNC is a synchronous input to the UCB1400. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the UCB1400.

The UCB1400 **must not** respond with the activation of BIT_CLK until SYNC has been sampled LOW again by the UCB1400. This will preclude the false detection of a new audio frame.

8.4 Accessing the UCB1400

The UCB1400 supports only primary codec configuration. Typically, the UCB1400 expects a 24.576 MHz crystal across the XTL_IN and XTL_OUT pins. Alternatively, an external 24.576 MHz clock can be applied to XTL_IN.

Table 4: AC-link audio output frame slot 0 bit allocation

Bit	Description
15	Frame valid
14	Slot 1 valid command address bit (primary codec only)
13	Slot 2 valid command data bit (primary codec only)
12-3	Slot 3-12 valid bits as defined by *AC ’97 Component Specification*
2	Reserved (set to 0)
1-0	2-bit codec ID field 00 reserved for primary 01, 10, 11 indicate secondary

In order for the AC ’97 Digital Controller to access the UCB1400, the 2-bit Codec ID field (chip select) (LSBs of Output Slot 0) must be set to ‘0’ (see Table 4). The UCB1400 shall monitor the Frame Valid, Slot 1 Valid Command Address, Slot 2 Valid Command Data and Codec ID bits, and respond only if properly accessed by the AC ’97 Digital Controller, as illustrated in Table 5. Note that although SLOTREQ bits reside in slot 1, they have validity independent of the tag bit for Valid Slot 1 Address. The UCB1400 shall only set SDATA_IN tag bits for Slot 1 (Address) and Slot 2 (Data) to ‘1’ when returning valid data from a previous register read, regardless of the validity of SLOTREQ bits (see also Section 8.5).

Table 5: UCB1400 response to AC ’97 digital controller access

Function	Slot 0, bit 15 (Valid frame)	Slot 0, bit 14 (Valid Slot 1 address)	Slot 0, bit 13 (Valid Slot 2 data)	Slot 0, bits 1-0 (codec ID)	Action
AC ’97 digital controller primary read frame N, SDATA_OUT	1	1	0	00	AC ’97 controller reads UCB1400 register
UCB1400 status frame N+1, in response to AC ’97 digital controller primary read frame N, SDATA_IN	1	1	1	00	UCB1400 returns register status
AC ’97 digital controller primary write frame N, SDATA_OUT	1	1	1	00	AC ’97 controller writes UCB1400 register
UCB1400 status frame N+1, in response to AC ’97 digital controller primary write frame N, SDATA_IN	1	0	0	00	UCB1400 writes register internally and returns nothing
AC ’97 digital controller secondary read or write frame N, SDATA_OUT	1	0	0	01, 10 or 11	AC ’97 controller reads or writes secondary codec
UCB1400 status frame N+1, in response to AC ’97 digital controller secondary read or write frame N, SDATA_IN	1	0	0	00	UCB1400 ignores commands and returns nothing

8.5 Variable sample rate signaling protocol

The AC-link is defined for a fixed transfer rate of 48 kHz. To support the diverse sample rates, UCB1400 implements the Variable Sample Rate Signaling Protocol of the *AC '97 Component Specification*:

- To control the AC '97 Controller to input a rate other than 48 kHz, the UCB1400 uses the tag bit for slot 3 and 4 (PCM L & R) to indicate whether valid data is present or not.
- To control the AC '97 Controller to output a rate other than 48 kHz, the UCB1400 uses the active-low SLOTREQ bit for slot 3 and slot 4 (PCM L & R) to indicate whether it needs data from the AC '97 Controller.

8.5.1 SLOTREQ protocol

To control the AC '97 Controller to output a rate other than 48 kHz, the UCB1400 examines its sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (LOW). SLOTREQ bits asserted during the current audio input frame signal which active output slots require data from the AC '97 Digital Controller in the next audio output frame. An active output slot is defined as any slot supported by UCB1400 that is not in a power-down state.

In case of UCB1400, the only SLOTREQ bits used are that for slot 3 and slot 4 request (bits 11 and 10 of input slot 1). SLOTREQ bits for all other slots shall be stuffed with 0s by UCB1400. Note that although SLOTREQ bits reside in slot 1, their validity does not depend on the tag bit for Valid Slot 1 Address (see also Section 8.4).

8.6 Wake-up support

Pressing the touch screen is an example of events that might need to wake-up the host CPU that has suspended into a low power state. Figure 11 shows the AC Link power-down/power-up sequence. The UCB1400 powers down the AC Link subsequent to its PR4 bit being programmed to 1. When enabled to wake on, e.g., a touch screen event, a wake event causes the UCB1400 to transition IRQOUT from LOW to HIGH. The system controller can use this information as a signal to wake up. Subsequently, the first thing that the device driver must do to reestablish communications with the UCB1400 is to command the AC '97 Digital Controller to execute a warm reset to the AC Link. Alternatively, if the GIEN bit in the Feature CSR1 register (0x6A) is set, a wake event will cause the UCB1400 to transition its SDATA_IN from LOW to HIGH. The UCB1400 shall keep SDATA_IN HIGH until it has sampled SYNC having gone HIGH, and then LOW.

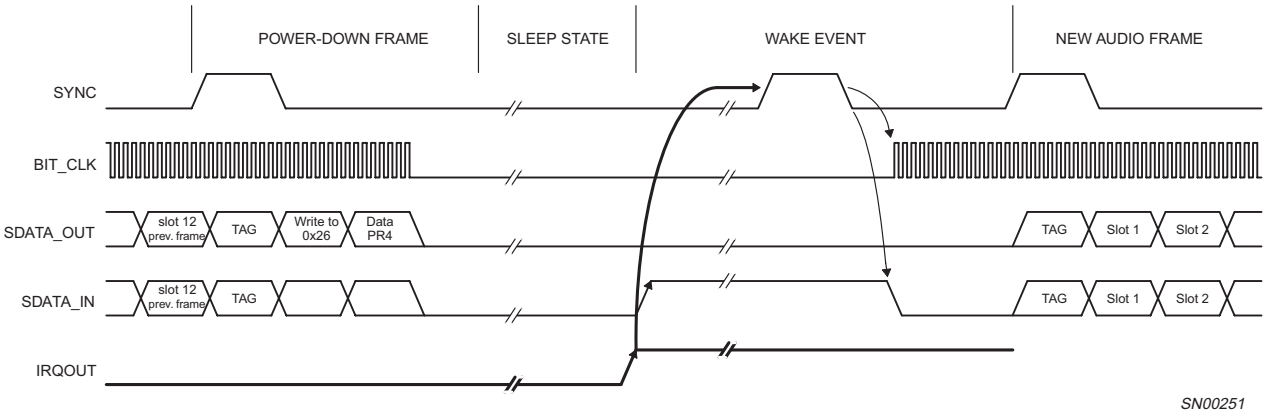


Fig 11. AC Link power-down/power-up sequence.

Before enabling wake-up via IRQOUT or GIEN bit, the UCB1400 must be enabled for interrupt by setting the appropriate bits in the Positive INT Enable register (0x5E) and Negative INT Enable register (0x60). The INT Clear/Status register (0x62) should then be cleared of any previous interrupts before going to low-power mode.

8.7 Test modes

AC '97 Component Specification defines two test modes. One is for ATE in-circuit test, and the other if for vendor-specific tests. The UCB1400 enters the ATE in-circuit test mode if SDATA_OUT is sampled HIGH at the trailing edge of $\overline{\text{RESET}}$. The UCB1400 enters the vendor-specific test mode when coming out of reset if SYNC is HIGH. These cases will never occur during standard operating conditions. Regardless of the test mode, the AC '97 Controller must issue a cold reset to resume normal operation of the UCB1400.

8.7.1 ATE in-circuit test mode

When the UCB1400 is placed in the ATE test mode, its digital AC-link outputs (i.e., BIT_CLK and SDATA_IN) shall be driven to a high impedance state. This allows ATE in-circuit testing of the AC '97 Controller.

8.7.2 Vendor-specific test mode

When the UCB1400 is placed in the vendor-specific test mode, the Test Control register (Index 0x6E) determines the kind of tests to be performed.
Refer to Section 12 "Register definition" for details.

8.8 General purpose IOs

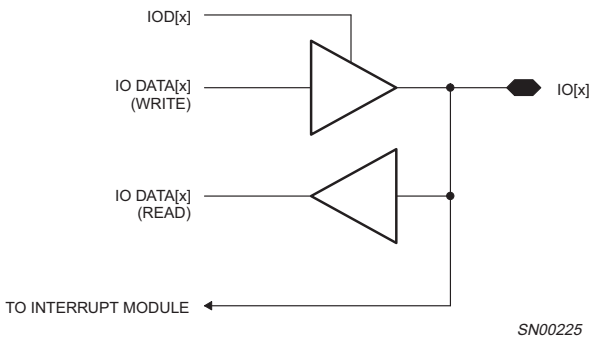


Fig 12. Block diagram of IO pin circuitry.

The UCB1400 has 10 programmable digital input/output (I/O) pins. These pins can be independently programmed as input or output using the IOD[9:0] bits in the IO Direction Register (0x5C). The output data is determined by the content of the IO[9:0] bits in the IO Data Register (0x5A), while the actual status of these pins can be read from the same register bits.

The data on the IO[9:0] pins are fed into the interrupt control block, where they can generate an interrupt on the rising and/or falling edge of these signals.

8.9 Interrupt generation

The UCB1400 contains a programmable interrupt control block, which can generate an interrupt for a 0-to-1 and/or 1-to-0 transition on one or more of the IO[9:0] pins, the audio overload detection, the ADC Ready signal, and the TSPX and TSMX signals.

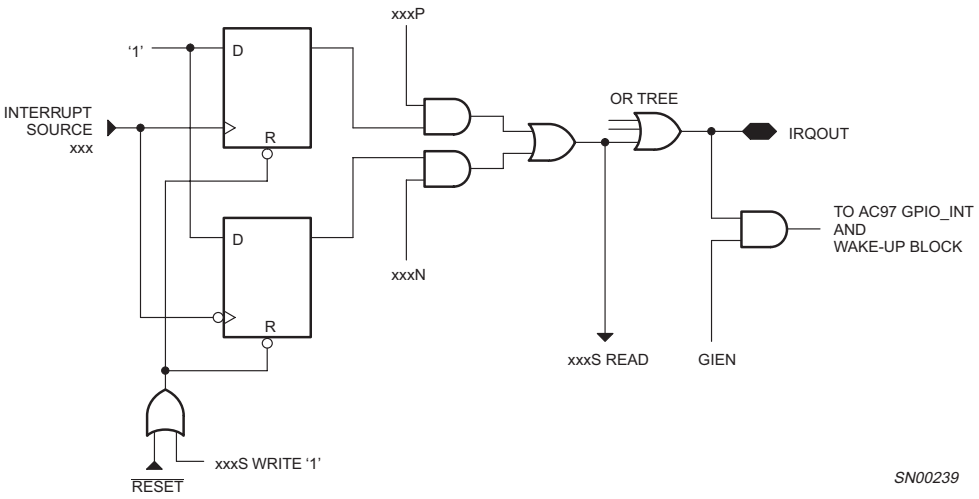


Fig 13. Block diagram of the interrupt controller.

The interrupt generation mode is set by the Positive INT Enable Register (0x5E) and Negative INT Enable Register (0x60). The actual interrupt status of each signal can be read from the INT Clear/Status Register (0x62). The interrupt status is cleared whenever a ‘1’ is written in the INT Clear/Status Register (0x62) for the corresponding bit.

The interrupt controller is implemented asynchronously. This provides the possibility to generate interrupts when the BIT_CLK is stopped, e.g., an interrupt can be generated in power-down mode when the touch screen is pressed or when the state of one of the IO pins changes.

The IRQOUT pin presents the ‘OR’ function of all interrupt status bits and can be used to give an interrupt to the system controller.

When the GIEN bit of the Feature Control/Status Register 1 (0x6A) is set, the IRQOUT signal is communicated to the AC Link by means of:

- GPIO_INT bit of input slot 12 when BIT_CLK is on.
- Rising SDATA_IN when BIT_CLK is off.

9. Audio codec

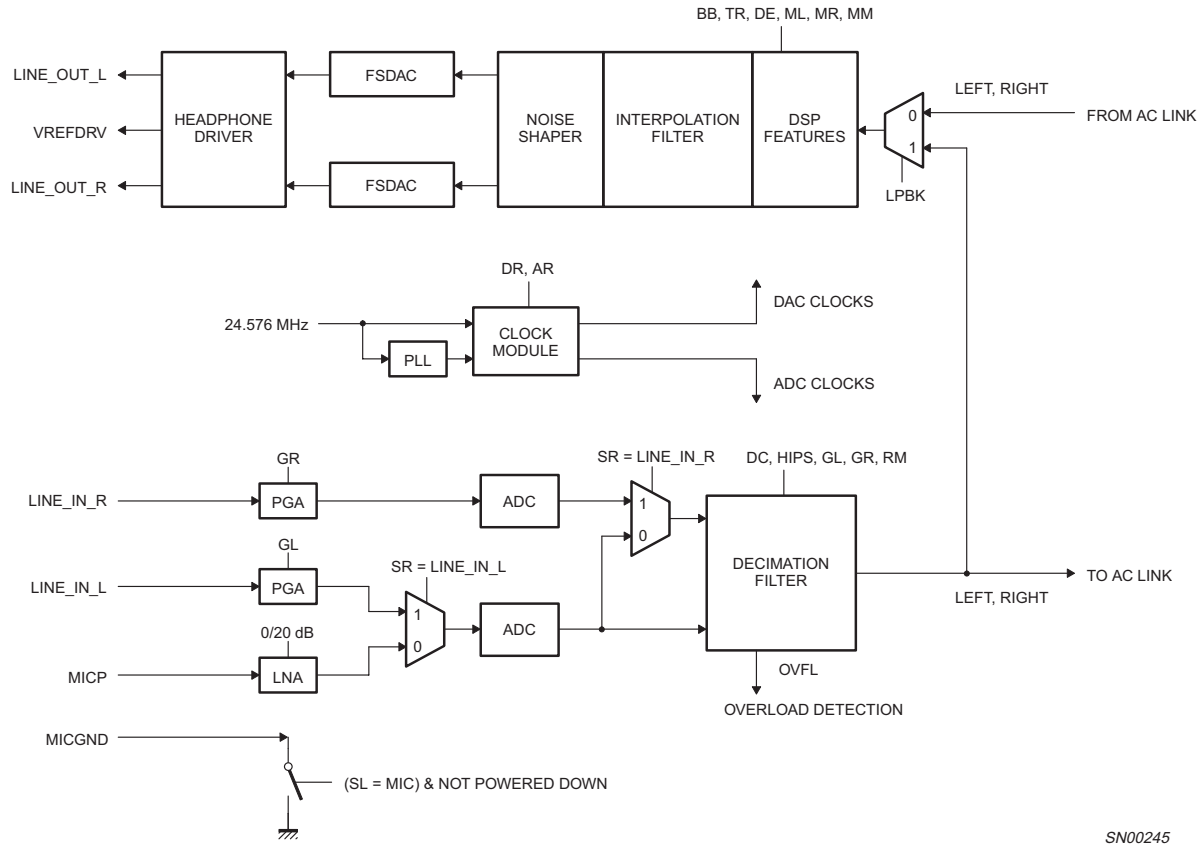


Fig 14. Audio codec block diagram.

9.1 ADC analog front-end

The analog front-end of the UCB1400 consists of one stereo ADC with a selector in front of it. Using this selector, one can either select the microphone input with a dedicated Low Noise Amplifier (LNA), or the line input with a Programmable Gain Amplifier (PGA). Via appropriate AC '97 register settings, the following modes can be supported:

- Standby mode: all PGAs, LNA and ADCs are powered down.
- Stereo line in mode: the PGAs are used, and the LNA is powered down.
- Microphone mode: the PGAs and right channel ADC are powered down, and MICGND switch is on. The mono microphone signal can be sent to both left and right input of the decimation filter via a MUX in front of the decimation input.
- One line-in and one microphone mode: the left PGA is powered down.

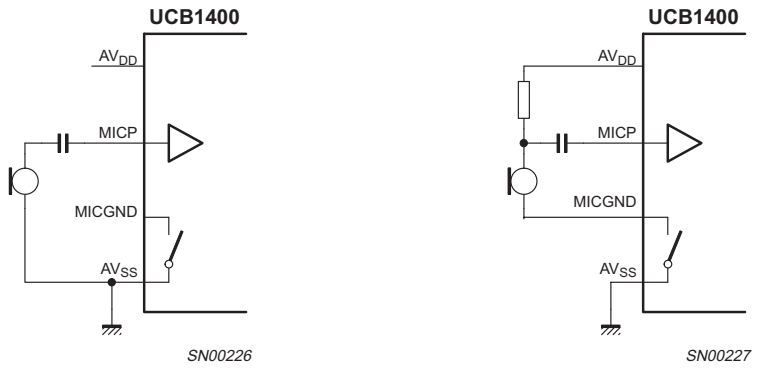
9.1.1 Line inputs

The analog front-end of the UCB1400 consists of two stereo ADCs with a programmable gain stage. The full scale input voltage of the line input path is programmable in 1.5 dB steps independently for the left and right channels by setting the GL[3:0] and GR[3:0] bits in the Record Gain Register (0x1C).

9.1.2 Microphone input

The UCB1400 audio codec input path accepts microphone signals via a DC blocking capacitor. The 'ground' side of the microphone is either connected to the analog ground (AV_{SS}) or to the MICGND pin of the UCB1400. The latter will decrease the current consumption of active microphones, since the MICGND pin is made Hi-Z when the microphone input is not selected (SL = LINE_IN_L in Record Select register (0x1A)).

The LNA gain can be set to 0 or 20 dB via the 20 dB bit in the MIC Volume register (0x0E). Additional gain in 1.5 dB steps is possible via the GL[3:0] in the Record Gain register (0x1C).



a. 'Passive' microphone.

b. 'Active' microphone.

Fig 15. Possible microphone connections.

9.1.3 Decimation filter

The decimation from 128 fs is performed in two stages. The first stage realizes sin(x)/x characteristics with decimation factor of 16. The second stage consists of 3 half-band filters, each decimating by a factor of 2. The filter characteristics are shown in Table 6.

Table 6: Decimation filter characteristics

Item	Condition	Value (dB)
Pass-band ripple	0 to 0.45 fs	±0.015
Stop band	> 0.55 fs	–60
Dynamic range	0 to 0.45 fs	> 135

Two bits in the Feature Control/Status Register 1 (0x6A) provide control over DC filtering:

- DC bit: controls the DC filter before the decimator used to compensate the DC offset is added in the ADC to remove idle tones from the audio band.
- HIPS bit: controls the DC filter at the output of the decimation filter.

9.1.4 Overload detection

An overload detection circuit will inform the user whenever the input voltage exceeds the maximum input voltage, which will lead to a high distortion. In that case, the OVFL bit in the Feature Control/Status Register 1 (0x6A) is set. In addition, an interrupt is generated on the IRQOUT pin of the UCB1400 whenever the **OVLP bit** or the **OVLN bit** is set in the Positive and/or Negative INT Enable Registers.

9.2 Interpolation filter (DAC)

The digital interpolation filter interpolates from 1 fs to 128 fs by means of a cascade of FIR filters. The filter characteristics are shown in Table 7.

Table 7: Interpolation filter characteristics

Item	Condition	Value (dB)
Pass-band ripple	0 to 0.45 fs	±0.025
Stop band	> 0.55 fs	–65
Dynamic range	0 to 0.45 fs	> 135

9.2.1 DSP features

The UCB1400 supports the following DSP (Digital Sound Processing) features through the Feature Control/Status register 1 (0x6A):

- Tone control: Bass Boost (BB[3:0]) and Treble Boost (TR[1:0])
- Flat/Minimum/Maximum setting for bass and treble boost (M[1:0])
- De-emphasis control (DE bit)

In addition, the UCB1400 supports volume control and soft muting via the Master Volume register (0x02):

- Master volume control: The output level can be attenuated in 1.5 dB steps down to –94.5 dB independently for the left and right channels via the Master Volume Register (0x02).
- Mute: The output is muted when the MM bit in the Master Volume Register is set. Muting the DAC will result in a cosine roll-off soft mute, using 128 samples in the normal mode: this results in 3 ms at fs = 44.1 kHz.

9.2.2 Noise shaper

The 3rd-order noise shaper operates at 128 fs. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream Digital-to-Analog Converter (FSDAC).

9.2.3 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way, very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output. The output voltage of the FSDAC scales proportionally with the power supply voltage.

9.2.4 Headphone driver

The headphone driver a reference output that acts as the virtual ground. This allows direct connection to a stereo headphone without the use of external DC blocking capacitors. The headphone driver is enabled when HPEN is set to ‘1’ in the Feature Control/Status Register 1 (0x6A).

The headphone driver is equipped with a short circuit protection on each of the LINE_OUT_L, LINE_OUT_R and VREFDRV output. When HPEN = 1, the short circuit protection circuit will inform the user in case the limiter is activated, e.g., in case of short circuit, by setting the corresponding bit (CLPL, CLPR or CLPG) in the Extra Interrupt register (0x70). In addition, an interrupt is generated on the IRQOUT pin of UCB1400 whenever the CLPP or CLPN bit is set in the Positive and/or Negative INT Enable Registers. In that case, the CPLS bit will be set in the INT Clear/Status register (index 0x62). The user can subsequently examine the Extra Interrupt register (0x70) to determine the source of the short circuit.

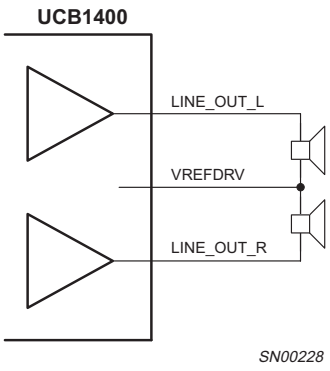


Fig 16. Headphone connections.

9.3 Loopback mode

The audio codec incorporates a loopback mode, in which codec input path and output path are connected in series. It is activated when the LPBK bit in the General Purpose register (0x20) set. The loopback internally connects the digital output from the decimator of the ADC to the digital input of the Interpolator of the DAC, allowing for codec testing without the use of the AC Link.

9.4 PLL and sample rates

The audio sample rate is derived from the 24.576 MHz crystal clock for 8, 12, 16, 24, 32, and 48 kHz sample rates, and from the built-in PLL for 11.025, 22.05 and 44.1 kHz sample rates. The ADC and DAC can run at independent sample rates and are controlled by the ADC and DAC Sample Rate registers (0x32 and 0x2C).

9.5 Power-down modes

The audio input and output paths can be powered down independently; the input path is powered down when the PR0 bit in the Power-down Control/Status register (0x26) is set. The output path is disabled when the PR1 bit of the same register is set. This provides the user the means to reduce the current consumption of UCB1400 if one part of the audio codec is not used in the application. When both the input and output paths are disabled, the PR3 bit of the same register can also be set to turn off the audio reference to further reduce power consumption.

If the Smart Low Power bits (SLP0 and SLP1) are set in the Feature Control/Status Register 2 (0x6C), the UCB1400 will power down unused blocks in the audio ADC analog front end and the PLL in a smart way, ensuring the lowest power consumption in each audio operating mode.

10. Touch screen interface

10.1 Universal touch screen matrix

The UCB1400 contains a universal touch screen interface for 4-wire resistive touch screen, capable of performing position, pressure and plate resistance measurements. In addition, the touch screen can be programmed to generate interrupts when the touch screen is pressed. The last mode is also active when the UCB1400 is set in the stand-by mode.

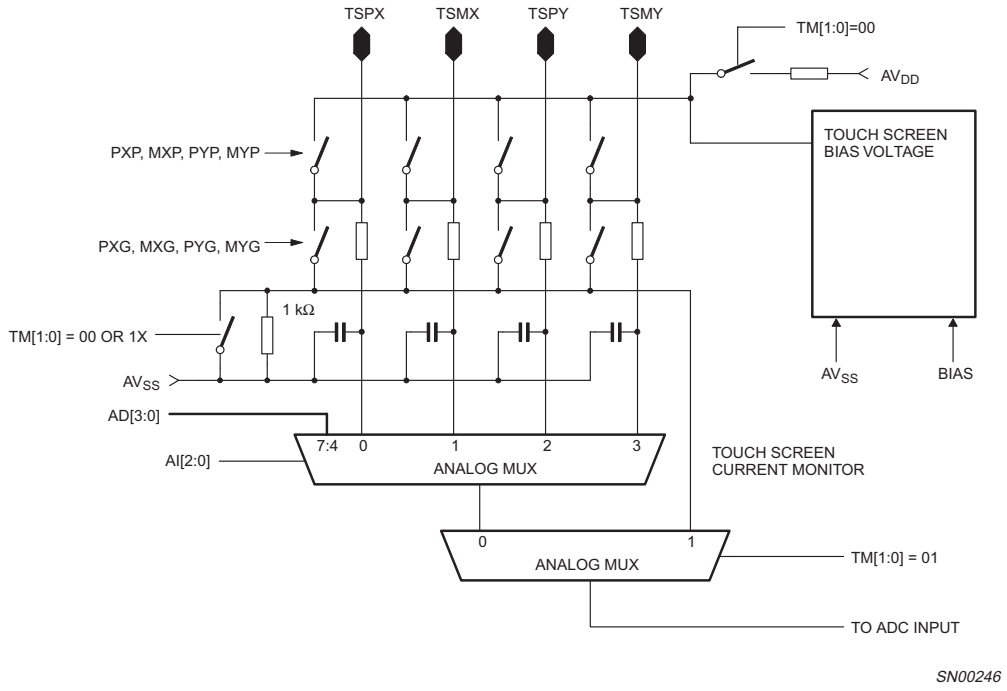


Fig 17. Block diagram of the touch screen interface.

The touch screen interface connects to the touch screen by four wires: TSPX, TSMX, TSPY and TSMY. Each of these pins can be programmed to be floating, powered or grounded in the touch screen switch matrix. The setting of each touch screen pin is programmable by the PXP, MXP, PYP, MYP and PXG, MYG, PYG, MYG bits in the touch screen control register. Possible conflicting settings (grounding and powering of a touch screen pin at the same time) are detected by the UCB1400. In that case, the UCB1400 will ground the touch screen pin.

Each of the four touch screen signals can be selected as input for the built-in 10-bit ADC, which is used to determine the voltage on the selected touch screen pin in position measurement mode. In addition, the UCB1400 can monitor touch screen current via an internal 1 kΩ resistor that can act as the input to the 10-bit ADC in pressure or plate resistance measurement mode. The flexible switch matrix and the multi-functional touch screen bias circuit enable the user of the UCB1400 to set each desired touch screen configuration.