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UCS1001-3 UCS1001-4

USB Port Power Controller with Charger Emulation

PRODUCT FEATURES

Datasheet

General Description

The UCS1001 provides a USB port power switch for precise control of up to 2.5 amperes continuous current with over-current limit (OCL), dynamic thermal management, latch or auto-recovery (low test current) fault handling, selectable active low or high enable, under- and over-voltage lockout, back-drive protection, and back-voltage protection.

Split supply support for VS and VDD is an option for low power in system standby states. This gives battery operated applications, like notebook PCs, the ability to detect attachments from a sleep or off state. After the Attach Detection is flagged, the system can decide to wake up and/or provide charging.

In addition to power switching and current limiting modes, the UCS1001 will automatically charge a wide variety of portable devices, including USB-IF BC1.2, YD/T-1591 (2009), most Apple® and RIM®, and many others. Nine preloaded charger emulation profiles maximize compatibility coverage of peripheral devices.

The UCS1001 is available in a 20-pin QFN 4 mm x 4 mm package.

Applications

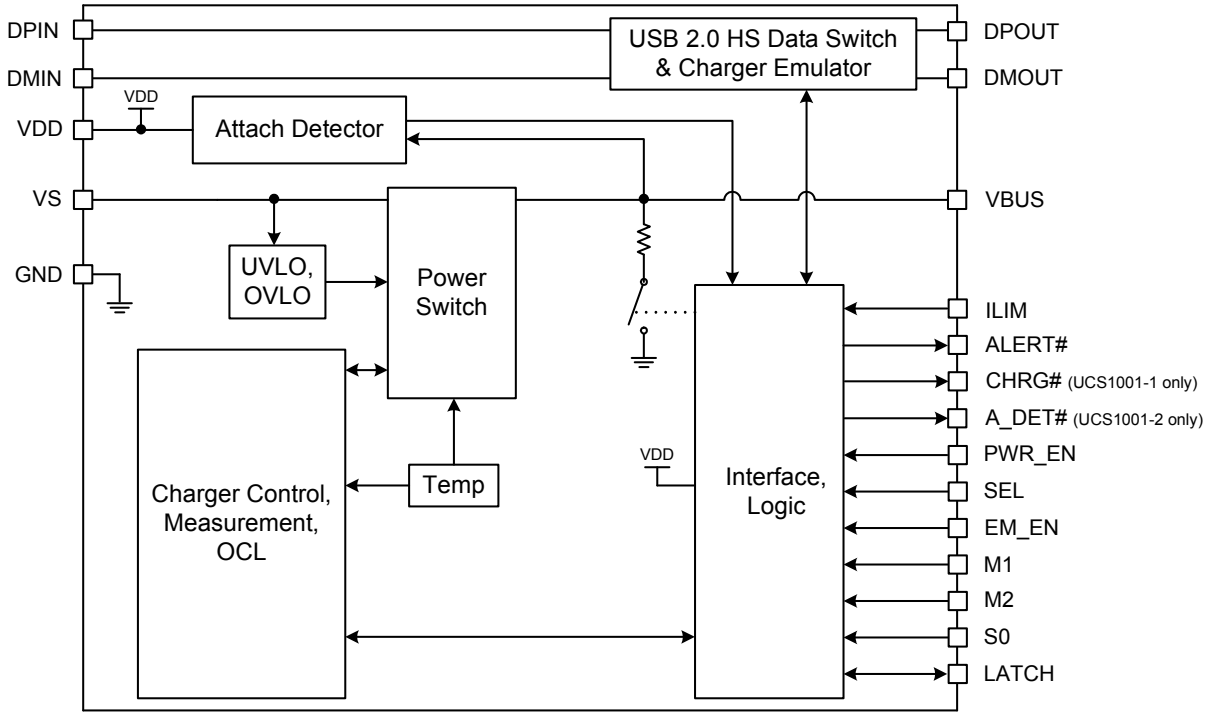
- Notebook and Netbook Computers
- Tablets and E-book readers
- Desktops and Monitors
- Docking Stations and Printers
- AC-DC wall adapters

Features

- Port power switch with two current limit behaviors
  - 2.9 V to 5.5 V source voltage range
  - Up to 2.5 A current with 55 mΩ On Resistance
  - Over-current trip or constant current limiting
  - Soft turn-on circuitry
  - Selectable current limit
  - Dynamic thermal management
  - Under- and over-voltage lockout
  - Back-drive, back-voltage protection
  - Latch or auto-recovery (low test current) fault handling
  - Selectable active high or low power switch enable
  - BC1.2 VBUS discharge port renegotiation function
- Selectable / automatic cycling of USB data line charger emulation profiles
  - Employs unique method and system for sampling multiple profiles*
  - UCS1001-3 and UCS1001-4 supports 12W charger emulation
  - Allows for active cables
  - USB-IF BC1.2 charging downstream port (CDP) & dedicated charging port (DCP) modes, YD/T-1591, and most Apple and RIM protocols standard
  - USB 2.0 compliant high-speed data switch (in Pass-through and CDP modes)
  - Nine preloaded charger emulation profiles for maximum compatibility coverage of peripheral devices
- Charging Active (UCS1001-3) or Attach Detection (UCS1001-4) open-drain output
- Ultra low power Sleep state
- Optional split supply support for VBUS and VDD for low power in system standby states
- Wake on Attach USB (UCS1001-4)
- Wide operating temperature range: -40 °C to +85 °C
- IEC61000-4-2 8 / 15 kV ESD immunity
- UL recognized and EN/IEC 60950-1 (CB) certified

* Unique technology covered under the following US patents pending: 13/109,446; 13/149,529; 13/173,287; 13/233,949; 13/157,282; 12/978,371; 13/232,965.

Block Diagram



ORDERING INFORMATION:

ORDERING NUMBER	PACKAGE	FEATURES
UCS1001-3-BP-TR	20 pin QFN 4mm x 4mm (RoHS compliant)	USB Port Power Controller with Charger Emulation, 12W Emulation support, and charging active output indicator
UCS1001-4-BP-TR	20 pin QFN 4mm x 4mm (RoHS compliant)	USB Port Power Controller with Charger Emulation, 12W Emulation support, and portable device attachment detected output indicator

REEL SIZE IS 4,000 PIECES

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Chapter 1 Terms and Abbreviations

APPLICATION NOTE: The M1, M2, PWR_EN, and EM_EN pins are referenced in text as the <pin name> control.

Table 1.1 Terms and Abbreviations

TERM / ABBREVIATION	DESCRIPTION
Active mode	Active power state operation mode: Data Pass-through, BC1.2 SDP, BC1.2 CDP, BC1.2 DCP, or Dedicated Charger Emulation Cycle.
attachment	The physical insertion of a portable device into a USB port that UCS1001 is controlling.
CC	Constant current
CDM	Charged Device Model. JEDEC model for characterizing susceptibility of a device to damage from ESD.
CDP or USB-IF BC1.2 CDP	Charging downstream port. The combination of the UCS1001 CDP handshake and an active standard USB host comprises a CDP. This enables a BC1.2 compliant portable device to simultaneously draw current up to 1.5 A while data communication is active. The USB high-speed data switch is closed in this mode.
charge enable	When a charger emulation profile has been accepted by a portable device and charging commences.
charger emulation profile	Representation of a charger comprised of DPOUT, DMOUT, and VBUS signalling which make up a defined set of signatures or handshaking protocols.
connection	USB-IF term which refers to establishing active USB communications between a USB host and a USB device.
current limiting mode	Determines the action that is performed when the IBUS current reaches the ILIM threshold. Trip opens the port power switch. Constant current (variable slope) allows VBUS to be dropped by the portable device.
DCE	Dedicated charger emulation. Charger emulation in which the UCS1001 can deliver power only. No active USB data communication is possible when charging in this mode.
DCP or USB-IF BC1.2 DCP	Dedicated Charging Port. This functions as a dedicated charger for a BC1.2 portable device. This allows the portable device to draw currents up to 1.5 A with constant current limiting (and beyond 1.5 A with trip current limiting). No USB communications are possible.
DC	Dedicated charger. A charger which inherently does not have USB communications, such as an A/C wall adapter.
disconnection	USB-IF term which refers to the loss of active USB communications between a USB host and a USB device.
dynamic thermal management	The UCS1001 automatically adjusts port power switch limits and modes to lower internal power dissipation when the thermal regulation temperature value is approached.
enumeration	A USB-specific term that indicates that a host is detecting and identifying USB devices.
handshake	Application of a charger emulation profile that requires a response. Two-way communication between the UCS1001 and the portable device.
HBM	Human Body Model.
HSW	High-speed switch.

Table 1.1 Terms and Abbreviations (continued)

TERM / ABBREVIATION	DESCRIPTION
I_{BUS_R2MIN}	Current limiter mode boundary.
ILIM	The IBUS current threshold used in current limiting. In trip mode, when ILIM is reached, the port power switch is opened. In constant current mode, when the current exceeds ILIM, operation continues at a reduced voltage and increased current; if VBUS voltage drops below V_{BUS_MIN}, the port power switch is opened.
Legacy	USB devices that require non-BC1.2 signatures be applied on the DPOUT and DMOUT pins to enable charging.
OCL	Over-current limit.
portable device	USB device attached to the USB port.
power thief	A USB device that does not follow the handshaking conventions of a BC1.2 device or Legacy devices and draws current immediately upon receiving power (i.e., a USB book light, portable fan, etc).
removal	The physical removal of a portable device from a USB port that the UCS1001 is controlling.
SDP or USB-IF SDP	Standard downstream port. The combination of the UCS1001 high-speed switch being closed with an upstream USB host present comprises a BC1.2 SDP. This enables a BC1.2 compliant portable device to simultaneously draw current up to 0.5 A while data communication is active.
signature	Application of a charger emulation profile without waiting for a response. One-way communication from the UCS1001 to the portable device.

Chapter 2 Pin Description

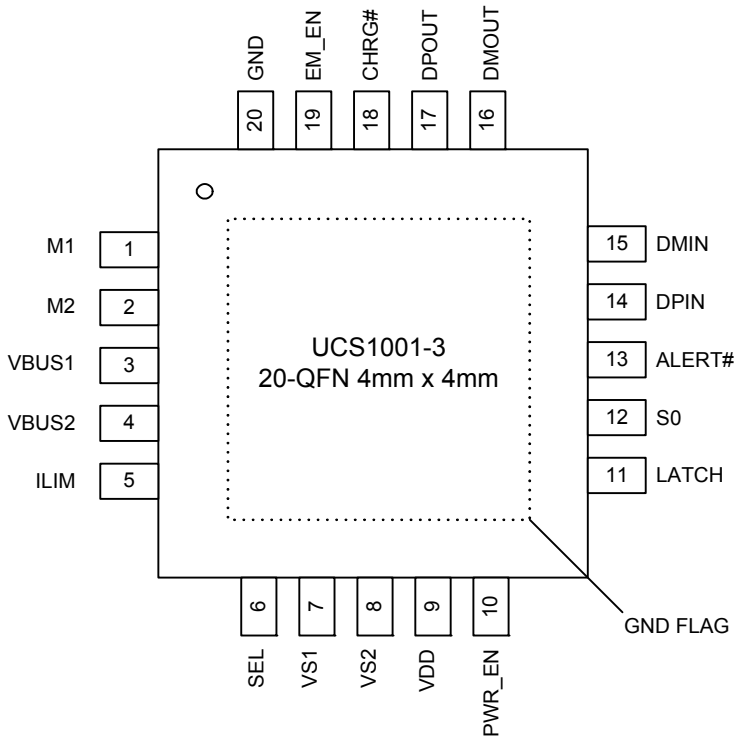


Figure 2.1 UCS1001-3 Pin Diagram

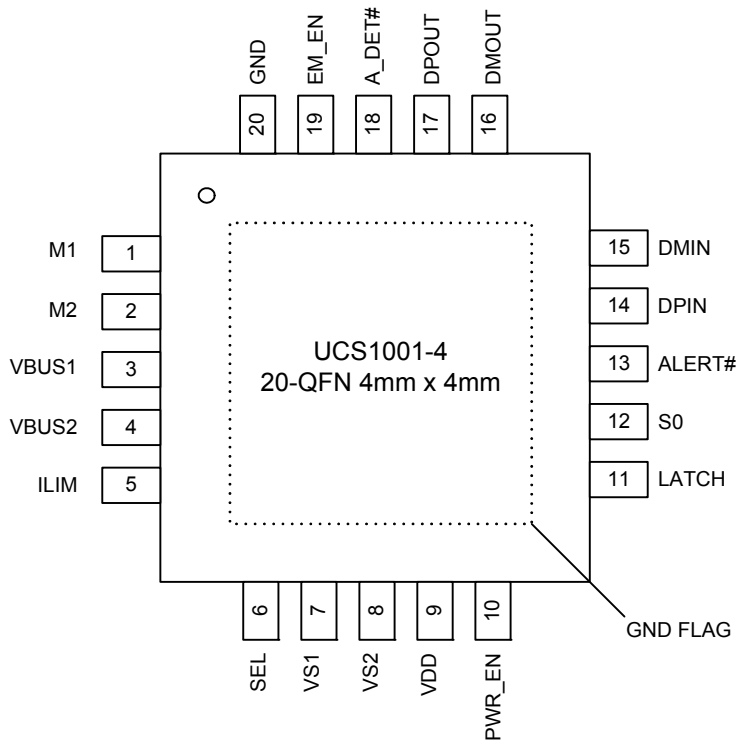


Figure 2.2 UCS1001-4 Pin Diagram

The pin types are described in Table 2.2. All pins are 5 V tolerant.

Table 2.1 UCS1001 Pin Description

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	IF PIN NOT USED CONNECTION
1	M1	Active mode selector input #1	DI	Connect to ground or VDD (see Note 2.2)
2	M2	Active mode selector input #2	DI	Connect to ground or VDD (see Note 2.2)
3	VBUS1	Voltage output from Power Switch. These pins must be tied together.	Hi-Power, AIO Note 2.1	Leave open
4	VBUS2			
5	ILIM	Selects the maximum current limit at power-up	AIO	n/a
6	SEL	Selects polarity of PWR_EN control	DI	n/a
7	VS1	Voltage input to Power Switch. These pins must be tied together.	Hi-Power, AIO	Connect to ground
8	VS2			

Table 2.1 UCS1001 Pin Description (continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	IF PIN NOT USED CONNECTION
9	VDD	Main power supply input for chip functionality	Power	n/a
10	PWR_EN	Port power switch enable input. Polarity determined by SEL pin.	DI	Connect to ground or VDD (see Note 2.2)
11	LATCH	Latch / Auto-recovery fault handling mechanism selection input	DI	n/a
12	S0	Enables Attach / Removal Detection feature	DI	n/a
13	ALERT#	Active low error event output flag (requires pull-up resistor)	OD	Connect to ground
14	DPIN	USB data input (plus)	AIO	Connect to ground or ground through a resistor
15	DMIN	USB data input (minus)	AIO	Connect to ground or ground through a resistor
16	DMOUT	USB data output (minus)	AIO	Connect to ground
17	DPOUT	USB data output (plus)	AIO	Connect to ground
18 (UCS1001-1, UCS1001-3)	CHRG#	Active low “Charging Active” output flag (requires pull-up resistor)	OD	Connect to ground
18 (UCS1001-2, UCS1001-4)	A_DET#	Active low Attach Detection output flag (requires pull-up resistor)	OD	Connect to ground
19	EM_EN	Active mode selector input	DI	Connect to ground or VDD (see Note 2.2)
20	GND	Ground	Power	n/a
Bottom Pad	GND FLAG	Thermal connection to ground plane	Thermal Pad	n/a

Note 2.1 Total leakage current from pins 3 and 4 (VBUS) to ground must be less than 100 µA for proper attach / removal detection operation.

Note 2.2 To ensure operation, the PWR_EN pin must be enabled, as determined by the SEL pin decode, when it is not driven by an external device. Furthermore, one of the M1, M2, or EM_EN pins must be connected to VDD if all three are not driven from an external device. If the PWR_EN is disabled or all of the M1, M2, and EM_EN are connected to ground, the UCS1001 will remain in the Sleep or Detect state indefinitely.

Table 2.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
Hi-Power	This pin is a high current pin.
AIO	Analog Input / Output - this pin is used as an I/O for analog signals.
DI	Digital Input - this pin is used as a digital input.
OD	Open-drain Digital Output - used as a digital output. It is open-drain and requires a pull-up resistor.

Chapter 3 Electrical Specifications

Table 3.1 Absolute Maximum Ratings

Voltage on VDD, VS, and VBUS pins	-0.3 to 6	V
Pullup voltage (V_{PULLUP})	-0.3 to VDD + 0.3	
Data switch current (I_{HSW_ON}), switch on	±50	mA
Port power switch current	Internally limited	
Data switch pin voltage to ground (DPOUT, DPIN, DMOUT, DMIN); (VDD powered or unpowered)	-0.3 to VDD + 0.3	V
Differential voltage across open data switch (DPOUT - DPIN, DMOUT - DMIN, DPIN - DPOUT, DMIN - DMOUT)	VDD	V
Voltage on any other pin to ground	-0.3 to VDD + 0.3	V
Current on any other pin	±10	mA
Package power dissipation	See Table 3.2	
Operating ambient temperature range	-40 to 125	°C
Storage temperature range	-55 to 150	°C

Note: Stresses above those listed could cause permanent damage to the UCS1001. This is a stress rating only and functional operation of the UCS1001 at any other condition above those indicated in the operation sections of this specification is not implied.

Table 3.2 Power Dissipation Summary

BOARD	PKG	θ_{JC}	θ_{JA}	DERATING FACTOR ABOVE 25 °C	TA < 25 °C POWER RATING	TA = 70 °C POWER RATING	TA = 85 °C POWER RATING
High K (see Note 3.1)	20-pin QFN 4 mm x 4 mm	6 °C / W	41 °C / W	24.4 mW / °C	2193 mW	1095 mW	729 mW
Low K (see Note 3.1)	20-pin QFN 4 mm x 4 mm	6 °C / W	60 °C / W	16.67 mW / °C	1498 mW	748 mW	498 mW

Note 3.1 A High K board uses a thermal via design with the thermal landing soldered to the PCB ground plane with 0.3 mm (12 mil) diameter vias in a 3x3 matrix (9 total) at 0.5 mm (20 mil) pitch. The board is multi-layer with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom. A Low K board is a two layer board without thermal via design with 2-ounce copper traces on the top and bottom.

Table 3.3 Electrical Specifications

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, = -40 °C to all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Power and Interrupts - DC						
Supply Voltage	VDD	4.5	5	5.5	V	See Note 3.2
Source Voltage	VS	2.9	5	5.5	V	See Note 3.2
Supply Current in Active (I_{DD_ACTIVE} + I_{VS_ACT})	I_{ACTIVE}		650	750	µA	Average current IBUS = 0 mA
Supply Current in Sleep (I_{DD_SLEEP} + I_{VS_SLEEP})	I_{SLEEP}		5	15	µA	Average current $V_{PULLUP} \leq$ VDD
Supply Current in Detect (I_{DD_DETECT} + I_{VS_DETECT})	I_{DETECT}		185	220	µA	Average current No portable device attached.
Power-on Reset						
VS Low Threshold	V_{S_UVLO}		2.5		V	VS voltage increasing
VS Low Hysteresis	$V_{S\_UVLO\_HYST}$		100		mV	VS voltage decreasing
VDD Low Threshold	V_{DD_TH}		4		V	VDD voltage increasing
VDD Low Hysteresis	$V_{DD\_TH\_HYST}$		500		mV	VDD voltage decreasing
I/O Pins - EM_EN, M1, M2, PWR_EN, ALERT#, CHRG# (UCS1001-3), A_DET# (UCS1001-4)- DC Parameters						
Output Low Voltage	V_{OL}			0.4	V	I_{SINK_IO} = 8 mA ALERT#CHRG#, A_DET#
Input High Voltage	V_{IH}	2.0			V	PWR_EN, EM_EN, M1, M2
Input Low Voltage	V_{IL}			0.8	V	PWR_EN, EM_EN, M1, M2, EM_EN
Leakage Current	I_{LEAK}			±5	µA	Powered or unpowered V_{PULLUP} <= VDD T_A < 85 °C
Interrupt Pins - AC Parameters						
ALERT#, A_DET# Pin Blanking Time	t_{BLANK}		25		ms	
ALERT# Pin Interrupt Masking Time	t_{MASK}		5		ms	
High-speed Data Switch						
High-speed Data Switch - DC Parameters						

Table 3.3 Electrical Specifications (continued)

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, = -40 °C to all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Switch Leakage Current	I_{HSW_OFF}		±0.5		µA	Switch open - DPIN to DPOUT, DMIN to DMOUT, or all four pins to ground. VDD ≤ VS.
Charger Resistance	R_{CHG}	2			MΩ	DPOUT or DMOUT to VBUS or ground, see Figure 3.2 BC1.2 DCP charger emulation active
On Resistance	R_{ON_HSW}		2		Ω	Switch closed, VDD = 5 V test current = 8 mA, test voltage = 0.4 V, see Figure 3.2
On Resistance	$R_{ON\_HSW\_1}$		5		Ω	Switch closed, VDD = 5 V, test current = 8 mA, test voltage = 3.0 V, see Figure 3.2
Delta On Resistance	ΔR_{ON_HSW}		±0.3		Ω	Switch closed, VDD = 5 V I_{TST} = 8 mA, V_{TST} = 0 to 1.5 V, see Figure 3.2
High-speed Data Switch - AC Parameters						
DP, DM Capacitance to Ground	C_{HSW_ON}		4		pF	Switch closed VDD = 5 V
DP, DM Capacitance to Ground	C_{HSW_OFF}		2		pF	Switch open VDD = 5 V
Turn Off Time	t_{HSW_OFF}		400		µs	Time from state control (EM_EN, M1, M2) switch on to switch off, R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Turn On Time	t_{HSW_ON}		400		µs	Time from state control (EM_EN, M1, M2) switch off to switch on, R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Propagation Delay	t_{PD}		0.25		ns	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Propagation Delay Skew	Δt_{PD}		25		ps	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Rise/Fall Time	$t_{F/R}$		10		ns	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
DP - DM Crosstalk	X_{TALK}		-40		dB	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Off Isolation	O_{IRR}		-30		dB	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF f = 240 MHz
-3dB Bandwidth	BW		1100		MHz	R_{TERM} = 50 Ω, C_{LOAD} = 1.5 pF V_{DPOUT} = V_{DMOUT} = 350 mV DC

Table 3.3 Electrical Specifications (continued)

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, = -40 °C to all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Total Jitter	t_J		200		ps	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF, rise time = fall time = 500 ps at 480 Mbps (PRBS = 2^{15} - 1)
Skew of Opposite Transitions of the Same Output	$t_{SK(P)}$		20		ps	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Port Power Switch						
Port Power Switch - DC Parameter						
Over-voltage Lockout	V_{S_OV}		6		V	
On Resistance	R_{ON_PSW}		55	65	mΩ	4.75 V < VS < 5.25 V
VS Leakage Current	I_{LEAK_VS}		2.2	5	µA	Sleep state into VS pin
Back-voltage Protection Threshold	V_{BV_TH}		150		mV	VBUS > VS VS > V_{S_UVLO}
Back-drive Current	I_{BD_1}		0	3	µA	VDD < V_{DD_TH}, Any powered power pin to any unpowered power pin. Current out of unpowered pin.
	I_{BD_2}		0	2	µA	VDD > V_{DD_TH}, Any powered power pin to any unpowered power pin, except for VDD to VBUS in Detect power state and VS to VBUS in Active power state. Current out of unpowered pin.

Table 3.3 Electrical Specifications (continued)

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, = -40 °C to all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Selectable Current Limits	I_{LIM1}		480	500	mA	ILIM Resistor = 47 kΩ (500 mA setting)
	I_{LIM2}		850	900	mA	ILIM Resistor = 56 kΩ (900 mA setting)
	I_{LIM3}		950	1000	mA	ILIM Resistor = 68 kΩ (1000 mA setting)
	I_{LIM4}		1130	1200	mA	ILIM Resistor = 82 kΩ (1200 mA setting)
	I_{LIM5}		1400	1500	mA	ILIM Resistor = 100 kΩ (1500 mA setting)
	I_{LIM6}		1720	1800	mA	ILIM Resistor = 120 kΩ (1800 mA setting)
	I_{LIM7}		1910	2000	mA	ILIM Resistor = 150 kΩ (2000 mA setting)
	I_{LIM8}		2370	2500	mA	ILIM Resistor = VDD (2500 mA setting)
Pin Wake Time	t_{PIN_WAKE}		3		ms	
Thermal Regulation Limit	T_{REG}		110		°C	Die Temperature at which current limit will be reduced
Thermal Regulation Hysteresis	T_{REG_HYST}		10		°C	Hysteresis for t_{REG} functionality. Temperature must drop by this value before ILIM value restored to normal operation
Thermal Shutdown Threshold	T_{TSD}		135		°C	Die Temperature at which port power switch will turn off
Thermal Shutdown Hysteresis	T_{TSD_HYST}		35		°C	After shutdown due to T_{TSD} being reached, die temperature drop required before port power switch can be turned on again
Auto-recovery Test Current	I_{TEST}		190		mA	Portable device attached, VBUS = 0 V, Die temp < T_{TSD}
Auto-recovery Test Voltage	V_{TEST}		750		mV	Portable device attached, VBUS = 0 V before application, Die temp < T_{TSD}
Discharge Impedance	$R_{DISCHARGE}$	100			Ω	

Table 3.3 Electrical Specifications (continued)

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, = -40 °C to all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Port Power Switch - AC Parameters						
Turn On Delay	t_{ON_PSW}		0.75		ms	PWR_EN active toggle to switch on time, VBUS discharge not active
Turn Off Time	$t_{OFF\_PSW\_INA}$		0.75		ms	PWR_EN inactive toggle to switch off time C_{BUS} = 120 µF
Turn Off Time	$t_{OFF\_PSW\_ERR}$		1		ms	Over-current Error, VBUS Min Error, or Discharge Error to switch off C_{BUS} = 120 µF
Turn Off Time	$t_{OFF\_PSW\_ERR}$		100		ns	TSD or Back-drive Error to switch off C_{BUS} = 120 µF
VBUS Output Rise Time	t_{R_BUS}		1.1		ms	Measured from 10% to 90% of VBUS, C_{LOAD} = 220 µF ILIM = 1.0 A
Soft Turn on Rate	$\Delta I_{BUS} / \Delta_t$		100		mA / µs	
Temperature Update Time	t_{DC_TEMP}		200		ms	
Short Circuit Response Time	t_{SHORT_LIM}		1.5		µs	Time from detection of short to current limit applied. No C_{BUS} applied
Short Circuit Detection Time	t_{SHORT}		6		ms	Time from detection of short to port power switch disconnect and ALERT# pin assertion.
Latched Mode Cycle Time	t_{UL}		7		ms	From PWR_EN edge transition from inactive to active to begin error recovery
Auto-recovery Mode Cycle Time	t_{CYCLE}		25		ms	Time delay before error condition check
Auto-recovery Delay	t_{RST}		20		ms	Portable device attached, VBUS must be $\geq$ V_{TEST} after this time
Discharge Time	$t_{DISCHARGE}$		200		ms	Amount of time discharge resistor applied

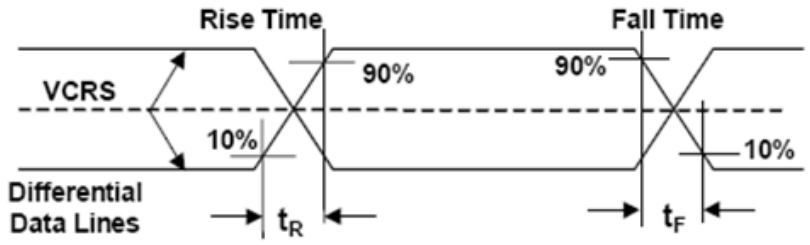
Table 3.3 Electrical Specifications (continued)

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, = -40 °C to all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Port Power Switch Operation With Trip Mode Current Limiting						
Region 2 Current Keep-out	I_{BUS_R2MIN}			0.1	A	
Minimum VBUS Allowed at Output	V_{BUS_MIN}	2.0			V	
Port Power Switch Operation With Constant Current Limiting (Variable Slope)						
Region 2 Current Keep-out	I_{BUS_R2MIN}			1.5	A	
Minimum VBUS Allowed at Output	V_{BUS_MIN}	2.0			V	
VBUS Bypass - DC						
On Resistance	R_{ON_BYP}		50		Ω	
Leakage Current	I_{LEAK_BYP}			3	µA	Switch off
Current Limit	I_{DET_CHG} / I_{BUS_BYP}		2		mA	VDD = 5 V and VBUS> 4.75 V
Attach / Removal Detection - DC						
Attach Detection Threshold	I_{DET_QUAL}		800		µA	
Primary Removal Detection Threshold	$I_{REM\_QUAL\_ACT}$		700		µA	Active power state
	$I_{REM\_QUAL\_DET}$		800		µA	Detect power state (see Section 7.4)
Attach / Removal Detection - AC						
Attach Detection Time	t_{DET_QUAL}		100		ms	Time from Attach to A_DET# assert (UCS1001-4 only).
Removal Detection Time	t_{REM_QUAL}		1000		ms	
Allowed Charge Time	t_{DET_CHARGE}		800		ms	C_{BUS} = 500 µF max
Charger Emulation Profile						
General Emulation - DC						
Charging Current Threshold	I_{BUS_CHG}		156		mA	

Table 3.3 Electrical Specifications (continued)

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, = -40 °C to all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DP-DM Shunt Resistor Value	R_{DCP_RES}			200	Ω	Connected between DPOUT and DMOUT 0 V < DPOUT = DMOUT ≤ 3 V
Voltage Output	SX_RXMAG_ VOLT_BC	0.5			V	DMOUT 250 µA load
Pull-down Current	SX_PUPD _ACC_BC	50			µA	DPOUT or DMOUT = 0.15 V Compliance voltage
General Emulation - AC						
Emulation Reset Time	t_{EM_RESET}		50		ms	

Note 3.2 For split supply systems using the Attach Detection feature, VS must not exceed VDD + 150 mV.



Data Signal Rise and Fall Time

Figure 3.1 USB Rise Time / Fall Time Measurement

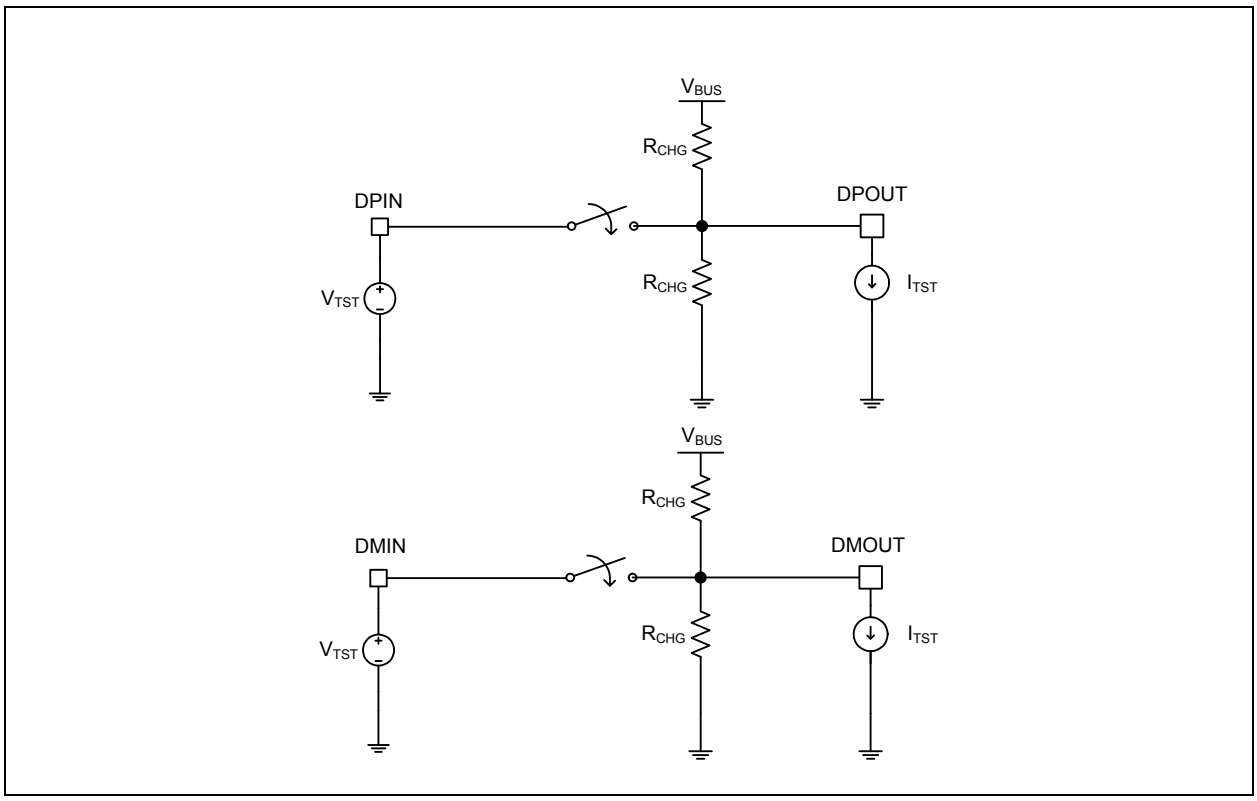


Figure 3.2 Description of DC Terms

3.1 ESD & Transient Performance

APPLICATION NOTE: Depending on the level of ESD protection required by the application, external protection devices may be required. The datasheet ESD levels were reached using external devices and standard USB-A connectors; refer to the EVB schematic and reference design for details.

Table 3.4 ESD Ratings

ESD SPEC	RATING OR VALUE
EN / IEC61000-4-2 (DPOUT, DMOUT pins) air gap, Operational Classification B (see Note 3.3)	Level4(15kV)
EN / IEC61000-4-2 (DPOUT, DMOUT pins) direct contact, Operational Classification B (see Note 3.3)	Level4(8 kV)
EN / IEC61000-4-2 (VBUS, GND pins) air gap, Operational Classification A (see Note 3.4)	Level4(15 kV)
EN / IEC61000-4-2 (VBUS, GND pins) direct contact, Operational Classification A (see Note 3.4)	Level4(8 kV)

Note 3.3 Operational Classification B indicates that during and immediately after an ESD event, anomalous behavior may occur; however, it is non-damaging and the device is self-recovering. All IEC testing is performed using an SMSC evaluation board.

Note 3.4 Operational Classification A indicates that during and immediately after an ESD event no anomalous behavior will occur. All IEC testing is performed using an SMSC evaluation board.

3.1.1 Human Body Model (HBM) Performance

HBM testing verifies the ability to withstand ESD strikes like those that occur during handling and manufacturing and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event.

3.1.2 Charged Device Model (CDM) Performance

CDM testing verifies the ability to withstand ESD strikes like those that occur during handling and assembly with pick and place style machinery and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event.

3.1.3 IEC61000-4-2 Performance

The IEC61000-4-2 ESD specification is an international standard that addresses system-level immunity to ESD strikes while the end equipment is operational. These tests are performed while the device is powered.

Chapter 4 General Description

The UCS1001 provides a single USB port power switch for precise control of up to 2.5 amperes continuous current with over-current limit (OCL), dynamic thermal management, latch or auto-recovery fault handling, selectable active low or high enable, under- and over-voltage lockout, and back-voltage protection.

Split supply support for VBUS and VDD is an option for low power in system standby states.

In addition to power switching and current limiting, the UCS1001 provides charger emulation profiles to charge a wide variety of portable devices, including USB-IF BC1.2 (CDP or DCP modes), YD/T-1591 (2009), most Apple and RIM portable devices, and many others.

Figure 4.1 shows a system configuration in which the UCS1001-3 provides a port power switch, low power Attach Detection, and charging active signaling. Figure 4.2 shows a system configuration in which the UCS1001-4 provides a port power switch, low power Attach Detection, and portable device Attach Detection signaling. These configurations are useful for applications that already provide USB BC1.2 and/or legacy data line handshaking on the USB data lines, but still require port power switching.

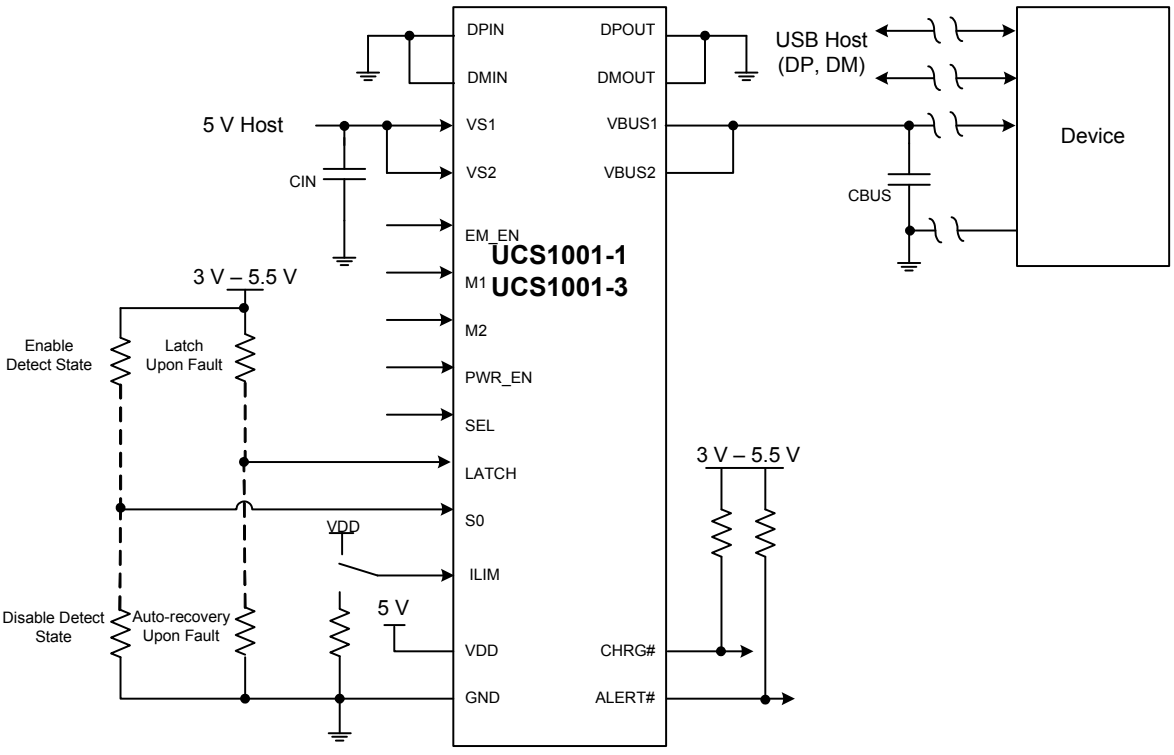


Figure 4.1 UCS1001-3 System Configuration (No Charger Emulation)

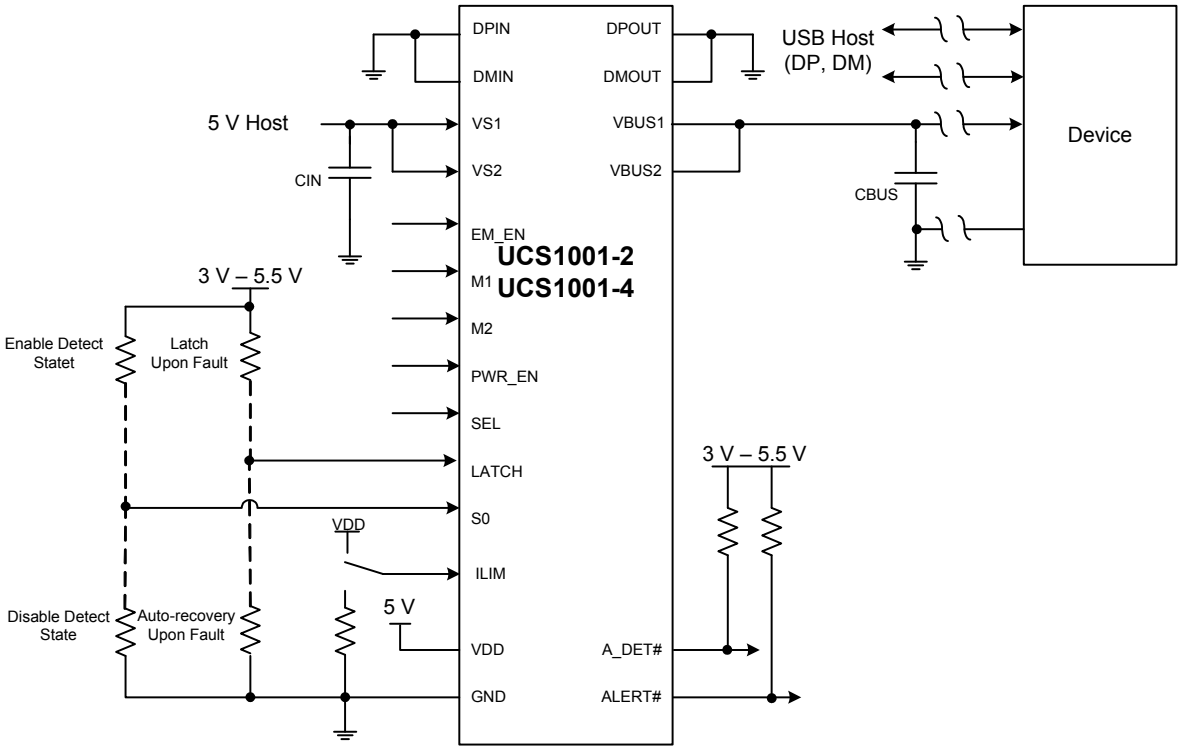


Figure 4.2 UCS1001-4 System Configuration (No Charger Emulation)

Figure 4.3 shows a system configuration in which the UCS1001-3 provides a port power switch, low power Attach Detection, charger emulation (with no USB host), and charging active signaling. Figure 4.4 shows a system configuration in which the UCS1001-4 provides a port power switch, low power Attach Detection, charger emulation (with no USB host), and portable device Attach Detection signaling. These configurations are useful for wall adapter type applications.