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## USB Dual-Port Power Switch and Current Monitor

### Features

- Dual-Port Power Switches:
  - 2.9V to 5.5V source voltage range
  - 3.0A continuous current per  $V_{BUS}$  port with 40 m $\Omega$  On resistance per switch
  - Independent port power switch enable pins
  - DUAL fault ALERT# active drain output pins
  - Constant Current or Trip mode current limiting behaviors
  - Undervoltage and overvoltage lockout
  - Back-drive, back-voltage protection
  - Auto-recovery fault handling with low test current
  - BOOST# logic output to increase DC-DC converter output under large load conditions
- SMBus 2.0/I<sup>2</sup>C Mode Features:
  - Eight programmable current limits assignable to each power switch
  - Other SMBus addresses available upon request
  - Block read and block write
- Self-Contained Current Monitoring (No External Sense Resistor Required)
- Fully Programmable Per-Port Charge Rationing and Behaviors
- Configurable Per-Port BC1.2  $V_{BUS}$  Discharge Function
- Wide Operating Temperature Range:
  - -40°C to +105°C
- UL Recognized and EN/IEC 60950-1 (CB) Certified

### Description

The UCS2113 is a dual USB port power switch configuration which can provide 3.0A continuous current (3.4A maximum) per  $V_{BUS}$  port with precision overcurrent limiting (OCL), port power switch enables, auto-recovery fault handling, undervoltage and overvoltage lockout, back-drive protection and back-voltage protection, and thermal protection.

The UCS2113 is well suited for both stand-alone and applications having SMBus/I<sup>2</sup>C communications.

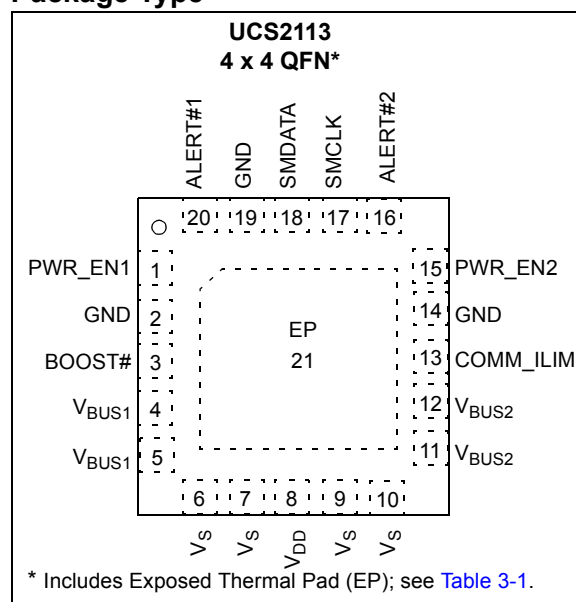
For applications with SMBus, the UCS2113 provides per-port current monitoring and eight programmable current limits per switch, ranging from 0.53A to 3.0A continuous current (3.4A maximum). Per-port charge rationing is also provided ranging from 3.8 mAh to 246.3 Ah.

In stand-alone mode, the UCS2113 provides eight current limits for both switches, ranging from 0.53A + 0.53A to 3A + 3A total continuous current (see [Table 1-1](#)).

Both power switches include an independent  $V_{BUS}$  discharge function and constant current mode current limiting for BC1.2 applications.

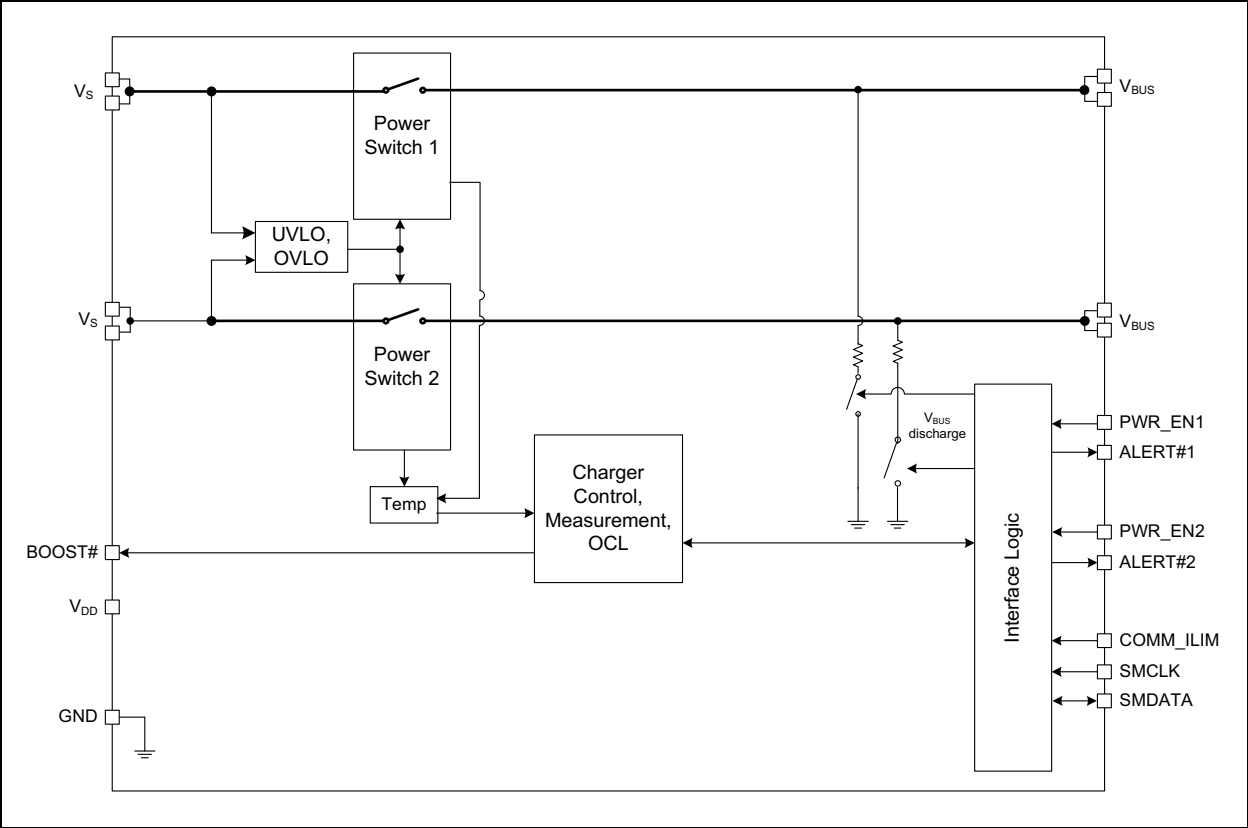
The UCS2113 is available in a 4x4 mm 20-pin QFN package.

### Package Type



# UCS2113

Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Voltage on $V_{DD}$ , $V_S$ , and $V_{BUS}$ pins .....	-0.3 to 6V
Pull-Up Voltage ( $V_{PULLUP}$ ) .....	-0.3 to $V_{DD} + 0.3$
Port Power Switch Current .....	Internally limited
Voltage on any Other Pin to Ground .....	-0.3 to $V_{DD} + 0.3V$
Current on any Other Pin .....	$\pm 10$ mA
Package Power Dissipation .....	See <a href="#">Table 1-1</a>
Operating Ambient Temperature Range .....	-40°C to +105°C
Storage Temperature Range .....	-55°C to +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: POWER DISSIPATION SUMMARY**

Board	Package	$\theta_{JC}$	$\theta_{JA}$	Derating Factor Above +25°C	$T_A < +25^\circ\text{C}$ Power Rating	$T_A = +70^\circ\text{C}$ Power Rating	$T_A = +85^\circ\text{C}$ Power Rating
High K ( <a href="#">Note</a> )	20-pin QFN 4x4 mm	6 °C/W	41 °C/W	24.4 mW/°C	2193 mW	1095 mW	729 mW
Low K ( <a href="#">Note</a> )	20-pin QFN 4x4 mm	6 °C/W	60 °C/W	16.67 mW/°C	1498 mW	748 mW	498 mW

**Note:** A High-K board uses a thermal via design with the thermal landing soldered to the PCB ground plane with 0.3 mm (12 mil) diameter vias in a 3x3 matrix (9 total) at 0.5 mm (20 mil) pitch. The board is multilayer with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom. A Low-K board is a two-layer board without thermal via design with 2-ounce copper traces on the top and bottom.

**TABLE 1-2: ELECTRICAL SPECIFICATIONS**

<b>Electrical Characteristics:</b> Unless otherwise specified, $V_{DD} = 4.5V$ to $5.5V$ , $V_S = 2.9V$ to $5.5V$ , $V_{PULLUP} = 3V$ to $5.5V$ , $T_A = -40^\circ\text{C}$ to $105^\circ\text{C}$ . All typical values at $V_{DD} = V_S = 5V$ , $T_A = 27^\circ\text{C}$ .						
Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>Power and Interrupts - DC</b>						
Supply Voltage	$V_{DD}$	4.5	5	5.5	V	
Supply Current in Active ( $I_{DD\_ACT} + I_{S1\_ACT} + I_{S2\_ACT}$ )	$I_{ACTIVE}$	—	700	—	$\mu\text{A}$	Average current $I_{BUS} = 0$ mA
Supply Current in Sleep ( $I_{DD\_SLEEP} + I_{S1\_SLEEP} + I_{S2\_SLEEP}$ )	$I_{SLEEP}$	—	6	20	$\mu\text{A}$	Average current $V_{PULLUP} \leq V_{DD}$
<b>Power-On Reset</b>						
$V_{DD}$ Low Threshold	$V_{DD\_TH}$	—	4	4.3	V	$V_{DD}$ voltage increasing ( <a href="#">Note 1</a> )
$V_{DD}$ Low Hysteresis	$V_{DD\_TH\_HYST}$	—	500	600	mV	$V_{DD}$ voltage decreasing ( <a href="#">Note 1</a> )

- Note 1:** This parameter is characterized, not 100% tested.  
**Note 2:** This parameter is ensured by design and not 100% tested.  
**Note 3:** The current measurement full scale range maximum value is 3.4A. However, the UCS2113 cannot report values above  $I_{LIM}$  (if  $I_{BUS\_R2MIN} \leq I_{LIM}$ ) or above  $I_{BUS\_R2MIN}$  (if  $I_{BUS\_R2MIN} > I_{LIM}$  and  $I_{LIM} \leq 1.6A$ ).



**TABLE 1-2: ELECTRICAL SPECIFICATIONS (CONTINUED)**

<b>Electrical Characteristics:</b> Unless otherwise specified, $V_{DD} = 4.5V$ to $5.5V$ , $V_S = 2.9V$ to $5.5V$ , $V_{PULLUP} = 3V$ to $5.5V$ , $T_A = -40^{\circ}C$ to $105^{\circ}C$ . All typical values at $V_{DD} = V_S = 5V$ , $T_A = 27^{\circ}C$ .						
Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>I/O Pins - SMCLK, SMDATA, PWR_EN, ALERT#, BOOST# - DC Parameters</b>						
Output Low Voltage	$V_{OL}$	—	—	0.4	V	$I_{SINK\_IO} = 8\text{ mA}$ SMDATA, ALERT#, BOOST#
Input High Voltage	$V_{IH}$	2.0	—	—	V	PWR_EN, SMDATA, SMCLK
Input Low Voltage	$V_{IL}$	—	—	0.8	V	PWR_EN, SMDATA, SMCLK
Leakage Current	$I_{LEAK}$	—	—	$\pm 5$	$\mu A$	Powered or unpowered $V_{PULLUP} \leq V_{DD}$ $T_A < 85^{\circ}C$ (Note 1)
<b>Interrupt Pins - AC Parameters</b>						
ALERT# Pin Blanking Time	$t_{BLANK}$	—	25	—	ms	Blanking time, coming out of reset
ALERT# Pin Interrupt Masking Time	$t_{MASK}$	—	5	—	ms	
BOOST# Pin Minimum Assertion Time	$t_{BOOST\_MAT}$	—	1	—	s	
BOOST# Pin Assertion Current	$I_{BOOST}$	—	1.9	—	A	
<b>SMBus/I<sup>2</sup>C Timing</b>						
Input Capacitance	$C_{IN}$	—	5	—	pF	
Clock Frequency	$f_{SMB}$	10	—	400	kHz	
Spike Suppression	$t_{SP}$	—	—	50	ns	
Bus Free Time Stop to Start	$t_{BUF}$	1.3	—	—	$\mu s$	
Start Setup Time	$t_{SU:STA}$	0.6	—	—	$\mu s$	
Start Hold Time	$t_{HD:STA}$	0.6	—	—	$\mu s$	
Stop Setup Time	$t_{SU:STO}$	0.6	—	—	$\mu s$	
Data Hold Time	$t_{HD:DAT}$	0	—	—	$\mu s$	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	$\mu s$	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	0.6	—	—	$\mu s$	
Clock Low Period	$t_{LOW}$	1.3	—	—	$\mu s$	
Clock High Period	$t_{HIGH}$	0.6	—	—	$\mu s$	
Clock/Data Fall Time	$t_{FALL}$	—	—	300	ns	Min. = $20+0.1C_{LOAD}$ ns (Note 1)
Clock/Data Rise Time	$t_{RISE}$	—	—	300	ns	Min. = $20+0.1C_{LOAD}$ ns (Note 1)
Capacitive Load	$C_{LOAD}$	—	—	400	pF	Per bus line (Note 1)
Timeout	$t_{TIMEOUT}$	25	—	35	ms	Disabled by default (Note 1)
Idle Reset	$t_{IDLE\_RESET}$	350	—	—	$\mu s$	Disabled by default (Note 1)

**Note 1:** This parameter is characterized, not 100% tested.

**2:** This parameter is ensured by design and not 100% tested.

**3:** The current measurement full scale range maximum value is 3.4A. However, the UCS2113 cannot report values above  $I_{LIM}$  (if  $I_{BUS\_R2MIN} \leq I_{LIM}$ ) or above  $I_{BUS\_R2MIN}$  (if  $I_{BUS\_R2MIN} > I_{LIM}$  and  $I_{LIM} \leq 1.6A$ ).

TABLE 1-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, $V_{DD} = 4.5V$ to $5.5V$ , $V_S = 2.9V$ to $5.5V$ , $V_{PULLUP} = 3V$ to $5.5V$ , $T_A = -40^{\circ}C$ to $105^{\circ}C$ . All typical values at $V_{DD} = V_S = 5V$ , $T_A = 27^{\circ}C$ .						
Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>Port Power Switch</b>						
<b>Port Power Switch - DC Parameter</b>						
Overvoltage Lockout	$V_{S\_OV}$	—	6	—	V	Note 2
$V_S$ Low Threshold	$V_{S\_UVLO}$	—	2.5	—	V	Note 2
$V_S$ Low Hysteresis	$V_{S\_UVLO\_HYST}$	—	100	—	mV	Note 2
On Resistance	$R_{ON\_PSW}$	—	40	—	$m\Omega$	$4.75V < V_S < 5.25V$
$V_S$ Leakage Current	$I_{LEAK\_VS}$	—	—	5	$\mu A$	Sleep state into $V_S$ pin on one channel (Note 1)
Back-Voltage Protection Threshold	$V_{BV\_TH}$	—	150	—	mV	$V_{BUS} > V_S$ $V_S > V_{S\_UVLO}$
Leakage Current	$I_{LKG\_1}$	—	0	3	$\mu A$	$V_{DD} < V_{DD\_TH}$ , Leakage current from $V_{BUS}$ pins to the $V_{DD}$ and the $V_S$ pins (Note 1)
	$I_{LKG\_2}$	—	0	2	$\mu A$	$V_{DD} > V_{DD\_TH}$ , Leakage current from $V_{BUS}$ pins to the $V_S$ pins, when the power switch is open
Selectable Current Limits	$I_{LIM1}$	—	530	—	mA	$I_{LIM}$ Resistor = 0 or 47 k $\Omega$ (530 mA setting)
	$I_{LIM2}$	—	960	—	mA	$I_{LIM}$ Resistor = 10 k $\Omega$ or 56 k $\Omega$ (960 mA setting)
	$I_{LIM3}$	—	1070	—	mA	$I_{LIM}$ Resistor = 12 k $\Omega$ or 68 k $\Omega$ (1070 mA setting)
	$I_{LIM4}$	—	1280	—	mA	$I_{LIM}$ Resistor = 15 k $\Omega$ or 82 k $\Omega$ (1280 mA setting)
	$I_{LIM5}$	—	1600	—	mA	$I_{LIM}$ Resistor = 18 k $\Omega$ or 100 k $\Omega$ (1600 mA setting)
	$I_{LIM6}$	—	2130	—	mA	$I_{LIM}$ Resistor = 22 k $\Omega$ or 120 k $\Omega$ (2130 mA setting)
	$I_{LIM7}$	2500	2670	2900	mA	$I_{LIM}$ Resistor = 27 k $\Omega$ or 150 k $\Omega$ (2670 mA setting)
	$I_{LIM8}$	3000	3200	3400	mA	$I_{LIM}$ Resistor = 33 k $\Omega$ or $V_{DD}$ (3200 mA setting)
Pin Wake Time	$t_{PIN\_WAKE}$	—	3	—	ms	
SMBus Wake Time	$t_{SMB\_WAKE}$	—	4	—	ms	
Idle Sleep Time	$t_{IDLE\_SLEEP}$	—	200	—	ms	
First Thermal Shutdown Stage Threshold	$T_{TSD\_LOW}$	—	120	—	$^{\circ}C$	Die Temperature at which the power switch will open if it is in constant current mode
First Thermal Shutdown Stage Hysteresis	$T_{TSD\_LOW\_HYST}$	—	10	—	$^{\circ}C$	Hysteresis for $T_{TSD\_LOW}$ functionality. Temperature must drop by this value before any of the power switches can be closed.

**Note 1:** This parameter is characterized, not 100% tested.

**Note 2:** This parameter is ensured by design and not 100% tested.

**Note 3:** The current measurement full scale range maximum value is 3.4A. However, the UCS2113 cannot report values above  $I_{LIM}$  (if  $I_{BUS\_R2MIN} \leq I_{LIM}$ ) or above  $I_{BUS\_R2MIN}$  (if  $I_{BUS\_R2MIN} > I_{LIM}$  and  $I_{LIM} \leq 1.6A$ ).

**TABLE 1-2: ELECTRICAL SPECIFICATIONS (CONTINUED)**

<b>Electrical Characteristics:</b> Unless otherwise specified, $V_{DD} = 4.5V$ to $5.5V$ , $V_S = 2.9V$ to $5.5V$ , $V_{PULLUP} = 3V$ to $5.5V$ , $T_A = -40^{\circ}C$ to $105^{\circ}C$ . All typical values at $V_{DD} = V_S = 5V$ , $T_A = 27^{\circ}C$ .						
Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Second Thermal Shutdown Stage Threshold	$T_{TSD\_HIGH}$	—	135	—	$^{\circ}C$	Die Temperature at which both power switches will open
Second Thermal Shutdown Stage Hysteresis	$T_{TSD\_HIGH\_HYST}$	—	25	—	$^{\circ}C$	Hysteresis for $T_{TSD\_HIGH}$ functionality. Temperature must drop by this value before any of the power switches can be closed.
Auto-Recovery Test Current	$I_{TEST}$	—	190	—	mA	Portable device attached, $V_{BUS} = 0V$ , Die temp $< T_{TSD}$
Auto-Recovery Test Voltage	$V_{TEST}$	—	750	—	mV	Portable device attached, $V_{BUS} = 0V$ before application, Die temp $< T_{TSD}$ Programmable, 250 - 1000 mV, default listed
Discharge Impedance	$R_{DISCHARGE}$	—	100	—	$\Omega$	
<b>Port Power Switch - AC Parameters</b>						
Turn-On Delay	$t_{ON\_PSW}$	—	0.9	—	ms	PWR_EN active toggle to switch on time, $V_{BUS}$ discharge not active
Turn-Off Time	$t_{OFF\_PSW\_INA}$	—	0.75	—	ms	PWR_EN inactive toggle to switch off time $C_{BUS} = 120 \mu F$
Turn-Off Time	$t_{OFF\_PSW\_ERR}$	—	1	—	ms	Over-current Error, $V_{BUS}$ Min Error, or Discharge Error to switch off $C_{BUS} = 120 \mu F$
Turn-Off Time	$t_{OFF\_PSW\_ERR1}$	—	100	—	ns	TSD or Back-drive Error to switch off $C_{BUS} = 120 \mu F$
$V_{BUS}$ Output Rise Time	$t_{R\_BUS}$	—	1.1	—	ms	Measured from 10% to 90% of $V_{BUS}$ , $C_{LOAD} = 220 \mu F$ $I_{LIM} = 1.0A$
Soft Turn-On Rate	$\Delta I_{BUS}/\Delta t$	—	100	—	mA/ $\mu s$	
Temperature Update Time	$t_{DC\_TEMP}$	—	200	—	ms	
Short-Circuit Response Time	$t_{SHORT\_LIM}$	—	1.5	—	$\mu s$	Time from detection of short to current limit applied. No $C_{BUS}$ applied
Short-Circuit Detection Time	$t_{SHORT}$	—	6	—	ms	Time from detection of short to port power switch disconnect and ALERT# pin assertion
Latched Mode Cycle Time	$t_{UL}$	—	7	—	ms	From PWR_EN edge transition from inactive to active to begin error recovery

- Note 1:** This parameter is characterized, not 100% tested.  
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**Note 3:** The current measurement full scale range maximum value is 3.4A. However, the UCS2113 cannot report values above  $I_{LIM}$  (if  $I_{BUS\_R2MIN} \leq I_{LIM}$ ) or above  $I_{BUS\_R2MIN}$  (if  $I_{BUS\_R2MIN} > I_{LIM}$  and  $I_{LIM} \leq 1.6A$ ).

**TABLE 1-2: ELECTRICAL SPECIFICATIONS (CONTINUED)**

<b>Electrical Characteristics:</b> Unless otherwise specified, V <sub>DD</sub> = 4.5V to 5.5V, V <sub>S</sub> = 2.9V to 5.5V, V <sub>PULLUP</sub> = 3V to 5.5V, T <sub>A</sub> = -40°C to 105°C. All typical values at V <sub>DD</sub> = V <sub>S</sub> = 5V, T <sub>A</sub> = 27°C.						
Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Auto-Recovery Mode Cycle Time	t <sub>CYCLE</sub>	—	25	—	ms	Time delay before error condition check. Programmable 15-50 ms, default listed
Auto-Recovery Delay	t <sub>TST</sub>	—	20	—	ms	Portable device attached, V <sub>BUS</sub> must be ≥ V <sub>TEST</sub> after this time. Programmable 10-25 ms, default listed
Discharge Time	t <sub>DISCHARGE</sub>	—	200	—	ms	Amount of time discharge resistor applied. Programmable 100-400 ms, default listed
<b>Port Power Switch Operation With Trip Mode Current Limiting</b>						
Region 2 Current Keep-Out	I <sub>BUS_R2MIN_1</sub>	—	—	0.1	A	<a href="#">Note 2</a>
Minimum V <sub>BUS</sub> Allowed at Output	V <sub>BUS_MIN_1</sub>	2.0	—	—	V	<a href="#">Note 2</a>
<b>Port Power Switch Operation With Constant Current Limiting (Variable Slope)</b>						
Region 2 Current Keep-Out	I <sub>BUS_R2MIN</sub>	—	—	2.13	A	<a href="#">Note 2</a>
Minimum V <sub>BUS</sub> Allowed at Output	V <sub>BUS_MIN</sub>	2.0	—	—	V	<a href="#">Note 2</a>
<b>Current Measurement - DC</b>						
Current Measurement Range	I <sub>BUS_M</sub>	0	—	3400	mA	Range ( <a href="#">Note 2</a> and <a href="#">Note 3</a> )
Reported Current Measurement Resolution	ΔI <sub>BUS_M</sub>	—	13.3	—	mA	1 LSB
Current Measurement Accuracy		—	±2	—	%	200 mA < I <sub>BUS</sub> < I <sub>LIM</sub>
		—	±2	—	LSB	I <sub>BUS</sub> < 200 mA
<b>Current Measurement - AC</b>						
Sampling Rate	—	—	1.1	—	ms	<a href="#">Note 2</a>
Conversion Time Both Channels	t <sub>CONV</sub>	—	2.2	—	ms	All registers updated in digital ( <a href="#">Note 2</a> )
<b>Charge Rationing - DC</b>						
Accumulated Current Measurement Accuracy	—	—	±4.5	—	%	
<b>Charge Rationing - AC</b>						
Current Measurement Update Time	t <sub>PCYCLE</sub>	—	1	—	s	

- Note 1:** This parameter is characterized, not 100% tested.  
**Note 2:** This parameter is ensured by design and not 100% tested.  
**Note 3:** The current measurement full scale range maximum value is 3.4A. However, the UCS2113 cannot report values above  $I_{LIM}$  (if  $I_{BUS\_R2MIN} \leq I_{LIM}$ ) or above  $I_{BUS\_R2MIN}$  (if  $I_{BUS\_R2MIN} > I_{LIM}$  and  $I_{LIM} \leq 1.6A$ ).



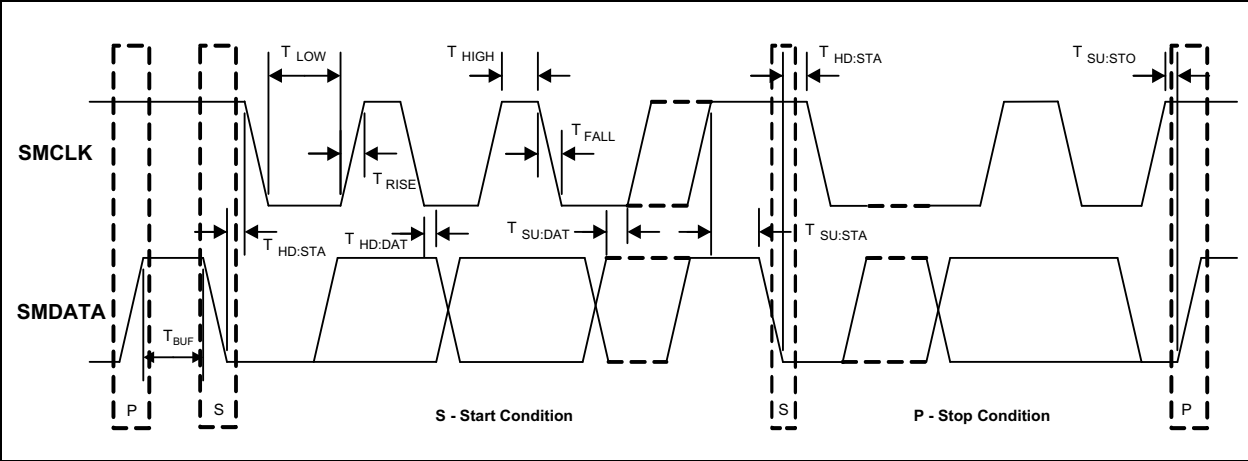


FIGURE 1-1: SMBus Timing.

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	$T_A$	-40	—	+105	°C	
Operating Junction Temperature	$T_J$	-40	—	+125	°C	
Storage Temperature Range	$T_A$	-55	—	+150	°C	
Thermal Package Resistances - see <a href="#">Table 1-1</a>						

## 1.1 ESD and Transient Performance

**TABLE 1-4: ESD RATINGS**

ESD Specification	Rating or Value
Human Body Model (JEDEC JESD22-A114) - All pins	8 kV
Charged Device Model (JEDEC JESD22-C101) - All pins	500V

### 1.1.1 HUMAN BODY MODEL (HBM) PERFORMANCE

HBM testing verifies the ability to withstand ESD strikes, like those that occur during handling and manufacturing, and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event.

### 1.1.2 CHARGED DEVICE MODEL (CDM) PERFORMANCE

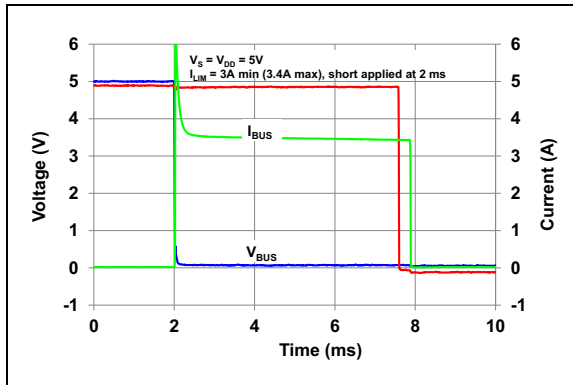
CDM testing verifies the ability to withstand ESD strikes, like those that occur during handling and assembly, with pick-and-place-style machinery and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event.

NOTES:

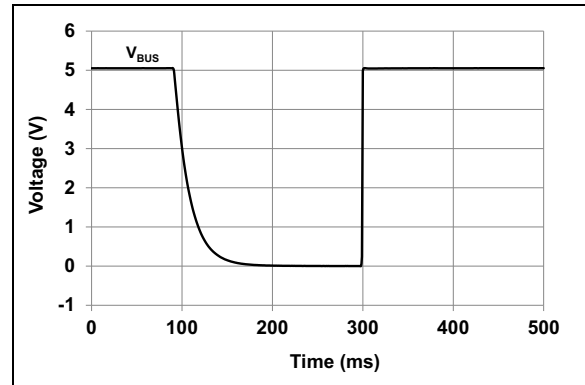
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

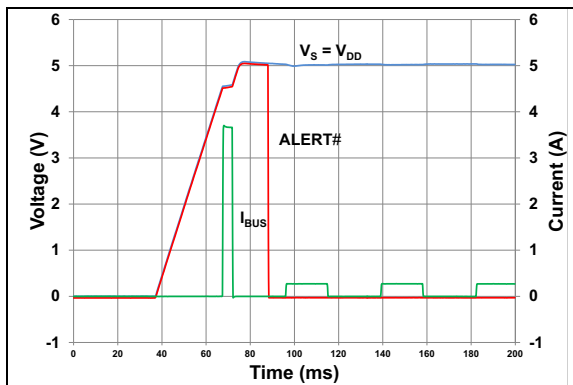
**Note:** Unless otherwise indicated,  $V_{DD} = V_S = 5V$ ,  $T_A = +27^\circ C$ .



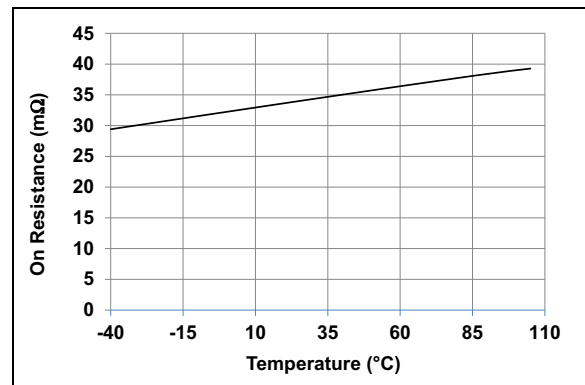
**FIGURE 2-1:** Short Applied After Power-Up.



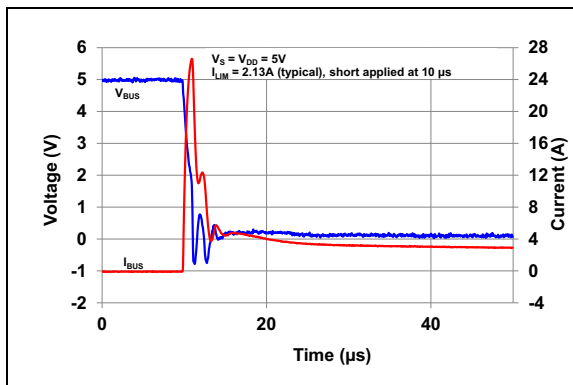
**FIGURE 2-4:**  $V_{BUS}$  Discharge Behavior.



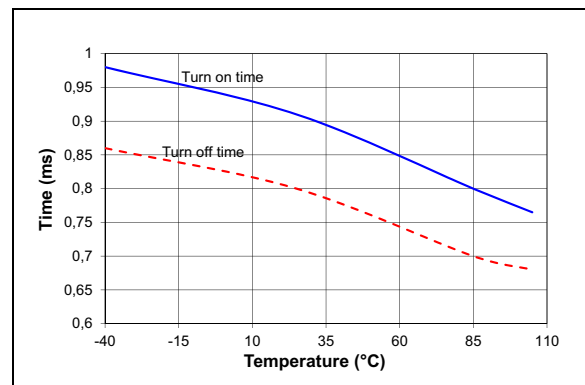
**FIGURE 2-2:** Power-Up Into a Short.



**FIGURE 2-5:** Power Switch On Resistance vs. Temperature.



**FIGURE 2-3:** Internal Power Switch Short Response.



**FIGURE 2-6:** Power Switch On/Off Time vs. Temperature.

Note: Unless otherwise indicated,  $V_{DD} = V_S = 5V$ ,  $T_A = +27^{\circ}C$ .

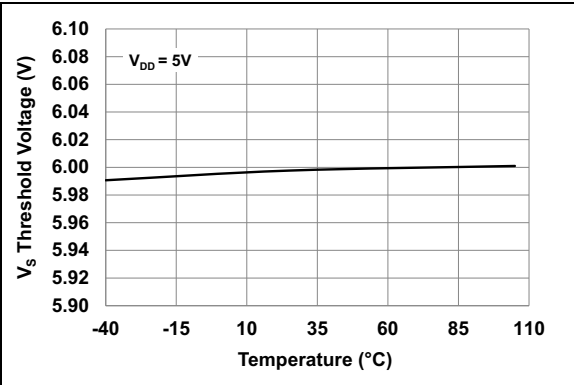


FIGURE 2-7:  $V_S$  Overvoltage Threshold vs. Temperature.

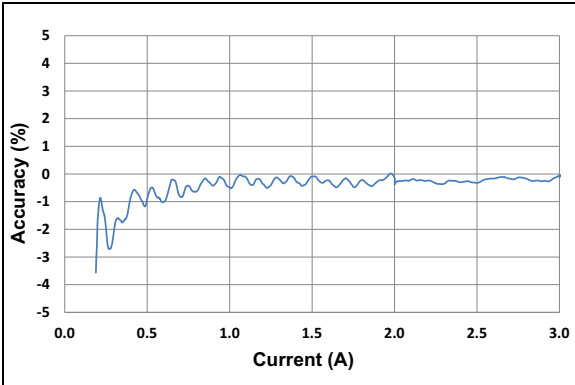


FIGURE 2-10:  $I_{BUS}$  Measurement Accuracy.

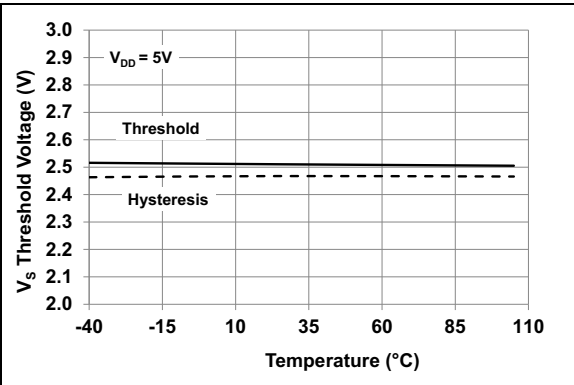


FIGURE 2-8:  $V_S$  Undervoltage Threshold vs. Temperature.

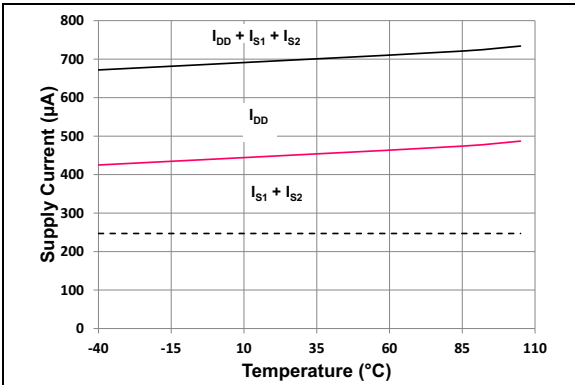


FIGURE 2-11: Active State Current vs. Temperature (both channels on,  $PWR\_EN1 = PWR\_EN2 = 1$ ).

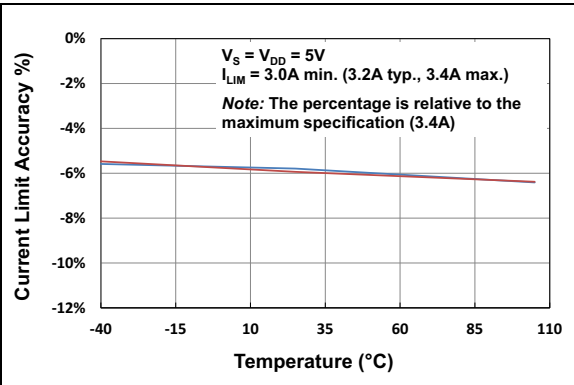
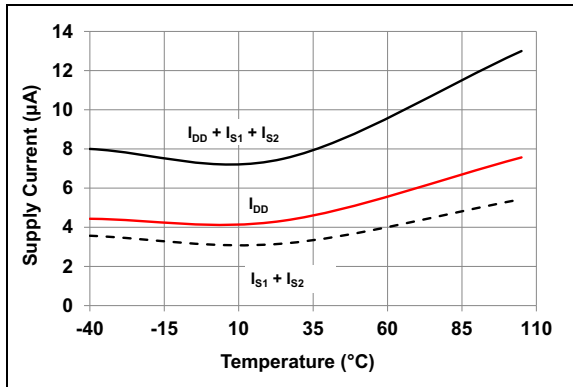


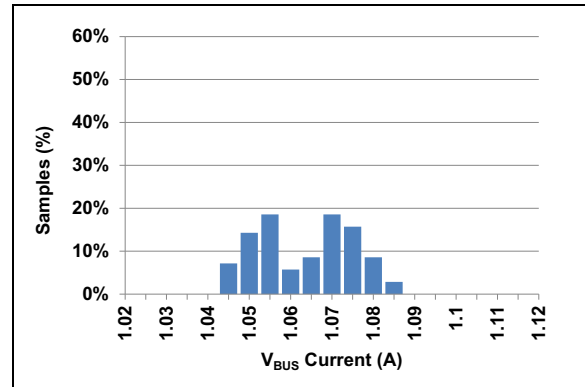
FIGURE 2-9: Trip Current Limit Operation vs. Temperature.



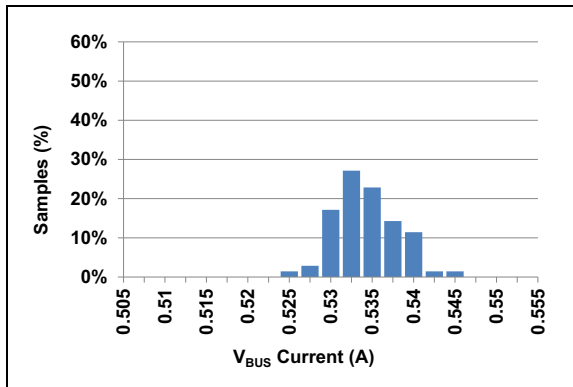
**Note:** Unless otherwise indicated,  $V_{DD} = V_S = 5V$ ,  $T_A = +27^\circ C$ .



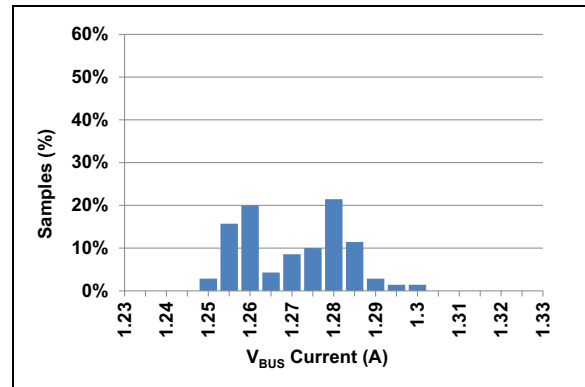
**FIGURE 2-12:** Sleep State Current vs. Temperature.



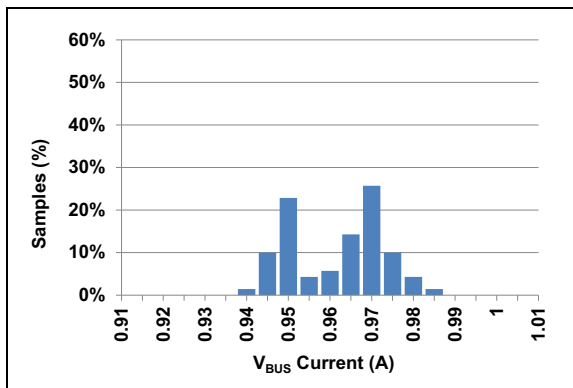
**FIGURE 2-15:** ILIM3 Trip Current Distribution<sup>(1)</sup>.



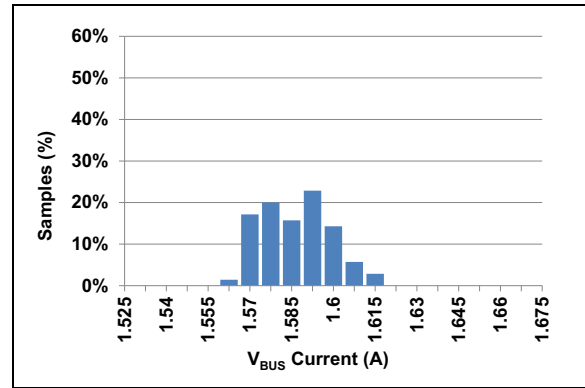
**FIGURE 2-13:** ILIM1 Trip Current Distribution.



**FIGURE 2-16:** ILIM4 Trip Current Distribution<sup>(1)</sup>.



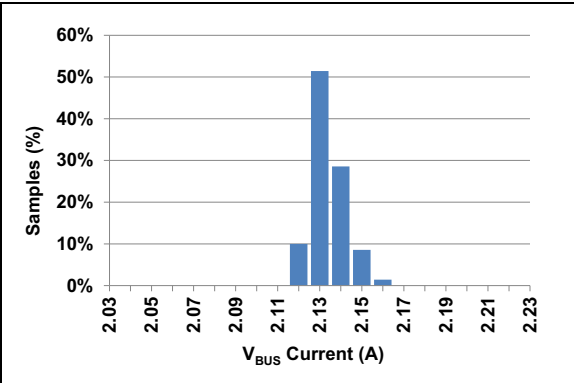
**FIGURE 2-14:** ILIM2 Trip Current Distribution<sup>(1)</sup>.



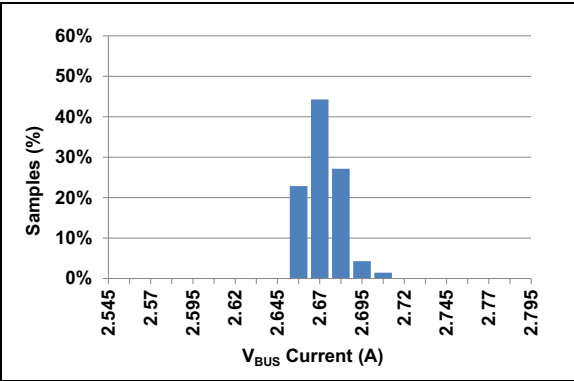
**FIGURE 2-17:** ILIM5 Trip Current Distribution<sup>(1)</sup>.

**Note 1:** The histogram aspect is caused by a mixture of two normal distributions, corresponding to the two  $V_{BUS}$  channels.

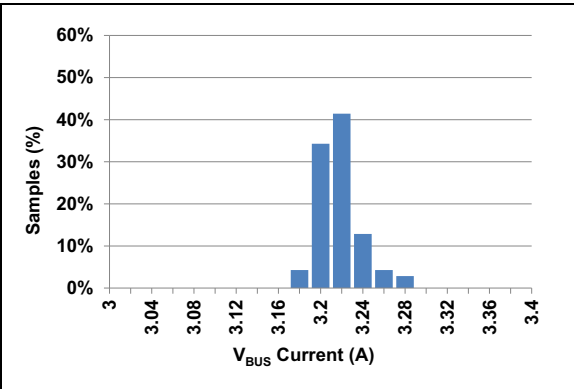
**Note:** Unless otherwise indicated,  $V_{DD} = V_S = 5V$ ,  $T_A = +27^{\circ}C$ .



**FIGURE 2-18:** ILIM6 Trip Current Distribution.



**FIGURE 2-19:** ILIM7 Trip Current Distribution.



**FIGURE 2-20:** ILIM8 Trip Current Distribution.

**Note 1:** The histogram aspect is caused by a mixture of two normal distributions, corresponding to the two  $V_{BUS}$  channels.

### 3.0 PIN DESCRIPTION

Descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

UCS2113 4x4 QFN	Symbol	Function	Pin Type	Connection Type if Pin Not Used
1	PWR_EN1	Port power switch enable #1	DI	Connect to ground or $V_{DD}$ (depending on the polarity decoded via COMM_ILIM pin)
2	GND	Ground	Power	N/A
3	BOOST#	Logic output for DC-DC converter voltage increase (requires pull-up resistor)	OD	Connect to ground
4, 5	$V_{BUS1}$	Port power switch #1 output (requires both pins tied together)	High Power, AIO	Leave open
6, 7	$V_S$	Voltage input to port power switch $V_{BUS1}$ (requires both pins tied together)	High Power, AIO	Connect to ground
8	$V_{DD}$	Common supply voltage	Power	N/A
9, 10	$V_S$	Voltage input to port power switch $V_{BUS2}$ (requires both pins tied together)	High Power, AIO	Connect to ground
11, 12	$V_{BUS2}$	Port power switch #2 output (requires both pins tied together)	High Power, AIO	Leave open
13	COMM_ILIM	Enables SMBus or Stand-Alone mode at power-up. Hardware strap for maximum current limit.	AIO	N/A
14	GND	Ground	Power	N/A
15	PWR_EN2	Port power switch enable #2	DI	Connect to ground or $V_{DD}$ (depending on the polarity decoded via COMM_ILIM pin)
16	ALERT#2	Output fault ALERT for $V_{BUS2}$ (requires pull-up resistor)	OD	Connect to ground
17	SMCLK	SMCLK - SMBus clock input (requires pull-up resistor)	DI	Connect to $V_{PULLUP}$ (or to ground in Stand-Alone mode)
18	SMDATA	SMDATA - SMBus data input/output (requires pull-up resistor)	DIOD	Connect to $V_{PULLUP}$ (or to ground in Stand-Alone mode)
19	GND	Ground	Power	N/A
20	ALERT#1	Output fault ALERT for $V_{BUS1}$ (requires pull-up resistor)	OD	Connect to ground
21	EP	Exposed thermal pad. Must be connected to electrical ground.	EP	N/A

**TABLE 3-2: PIN TYPES**

Pin Type	Description
<b>Power</b>	This pin is used to supply power or ground to the device
<b>Hi-Power</b>	This pin is a high-current pin
<b>AIO</b>	Analog Input/Output - this pin is used as an I/O for analog signals
<b>DI</b>	Digital Input - this pin is used as a digital input
<b>DIOD</b>	Open-Drain Digital Input/Output - this pin is bidirectional. It is open-drain and requires a pull-up resistor.
<b>OD</b>	Open-Drain Digital Output - used as a digital output. It is open-drain and requires a pull-up resistor.
EP	Exposed thermal pad

## 4.0 TERMS AND ABBREVIATIONS

**Note:** The PWR\_EN1 and PWR\_EN2 pins each have configuration bits ("**<pin name>\_S**" in [General Configuration 1 register \(Address 11h\)](#) and [General Configuration 2 register \(Address 12h\)](#)) that may be used to perform the same function as the external pin state. These bits are accessed via the SMBus/I<sup>2</sup>C and are OR'd with the respective pin. This OR'd combination of pin state and register bit is referenced as the **<pin name> control**.

**TABLE 4-1: TERMS AND ABBREVIATIONS**

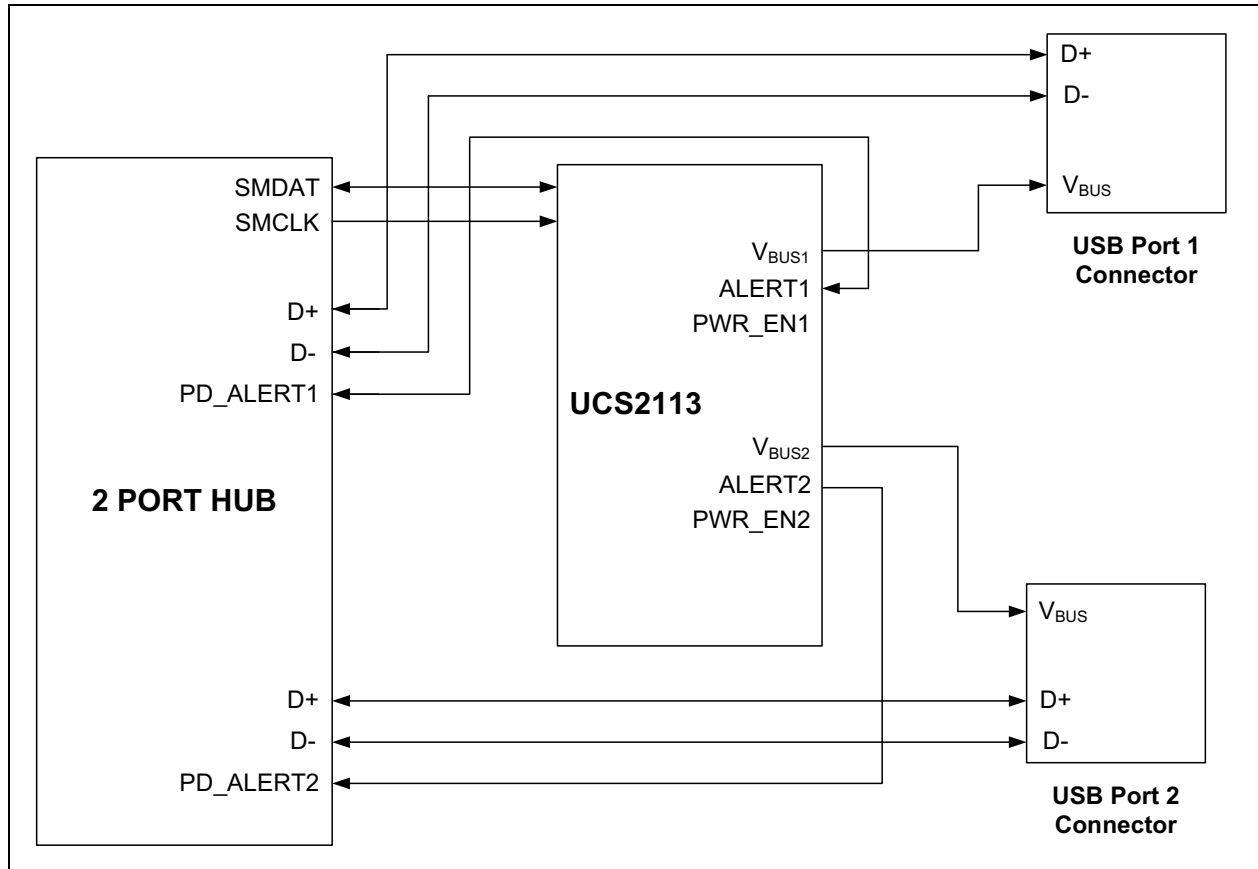
Term/Abbreviation	Description
CC	Constant Current
Current Limiting Mode	Determines the action that is performed when the $I_{BUS}$ current reaches the $I_{LIM}$ threshold. Trip opens the port power switch. Constant Current (variable slope) allows $V_{BUS}$ to be dropped by the portable device.
$I_{BUS\_R2MIN}$	Current limiter mode boundary
$I_{LIM}$	The $I_{BUS}$ current threshold used in current limiting. In Trip mode, when $I_{LIM}$ is reached, the port power switch is opened. In Constant Current mode, when the current exceeds $I_{LIM}$ , operation continues at a reduced voltage and increased current; if $V_{BUS}$ voltage drops below $V_{BUS\_MIN}$ , the port power switch is opened.
OCL	Overcurrent limit
POR	Power-on Reset
Portable Device	USB device attached to the USB port
Stand-Alone Mode	Indicates that the communications protocol is not active and all communications between the UCS2113 and a controller are done via the external pins only (PWR_EN1 and PWR_EN2 as inputs, and ALERT1# and ALERT2# as outputs)



NOTES:

## 5.0 GENERAL DESCRIPTION

The UCS2113 is a dual-port power switch. Two USB power ports are supported with current limits up to 3.0A continuous current (3.4A maximum) each. Selectable and programmable current limiting configurations are also available to the application. A typical block diagram is shown in [Figure 5-1](#).



**FIGURE 5-1:** Typical USB Application.

# UCS2113

## 5.1 UCS2113 Power States

Power states are indicators of the device's current consumption in the system and the functionality of the digital logic. Table 5-1 details the UCS2113 power states.

TABLE 5-1: POWER STATES DESCRIPTION

State	Description
Off	This power state is entered when the voltage at the $V_{DD}$ pin voltage is $< V_{DD\_TH}$ . In this state, the device is considered "off". The UCS2113 will not retain its digital states and register contents nor respond to SMBus/I <sup>2</sup> C communications. The port power switch will be off. See Section 5.1.1 "Off State Operation".
Sleep	This is the lowest power state available. While in this state, the UCS2113 will retain digital functionality and wake to respond to SMBus/I <sup>2</sup> C communications. See Section 5.1.2 "Sleep State Operation".
Error	This power state is entered when a fault condition exists. Error power state is one or both channels in Fault Handling. This state is updated as Priority One. The Interrupt Status Registers for each channel will update the fault detected per channel. Only the channel that has detected a Fault will be affected since the other channel can remain active if no fault is detected. See Section 5.1.4 "Error State Operation".
Active	Active power State is one, or both channels active and sourcing current to the $V_{BUS}$ Port. This state is updated as Priority Two. None of the channels have detected Fault. This power state provides full functionality. While in this state, operations include activation of the port power switch, current limiting, and charge rationing. See Section 5.1.3 "Active State Operation".

Table 5-2 shows the settings for the various power states, except Off and Error. If  $V_{DD} < V_{DD\_TH}$ , the UCS2113 is in the Off state.

TABLE 5-2: POWER STATES CONTROL SETTINGS

Power State	PWR_EN1	PWR_EN2	Behavior
Sleep	disabled	disabled	<ul style="list-style-type: none"><li>All switches disabled</li><li><math>V_{BUS}</math> will be near ground potential</li><li>The UCS2113 wakes to respond to SMBus communications</li></ul>
Active	enabled	disabled	<ul style="list-style-type: none"><li>Port power switch is on for <math>V_{BUS1}</math></li><li><math>V_{BUS2}</math> pins are near ground potential or floating (Note 1)</li></ul>
	disabled	enabled	<ul style="list-style-type: none"><li>Port power switch is on for <math>V_{BUS2}</math></li><li><math>V_{BUS1}</math> pins are near ground potential or floating (Note 1)</li></ul>
	enabled	enabled	<ul style="list-style-type: none"><li>Port power switch is on for <math>V_{BUS1}</math> and <math>V_{BUS2}</math></li></ul>

**Note 1:** If the bit EN\_VBUS\_DISCHG is '1', the  $V_{BUS}$  is discharged automatically and  $V_{BUS}$  is near ground potential. If the bit EN\_VBUS\_DISCHG is '0' then the corresponding VBUS pins are floating ( $V_{BUS}$  discharge is controlled by the SMBus master).

### 5.1.1 OFF STATE OPERATION

The device will be in the Off state if  $V_{DD}$  is less than  $V_{DD\_TH}$ . When the UCS2113 is in the Off state, it will do nothing and all circuitry will be disabled. Digital register values are not stored and the device will not respond to SMBus commands.

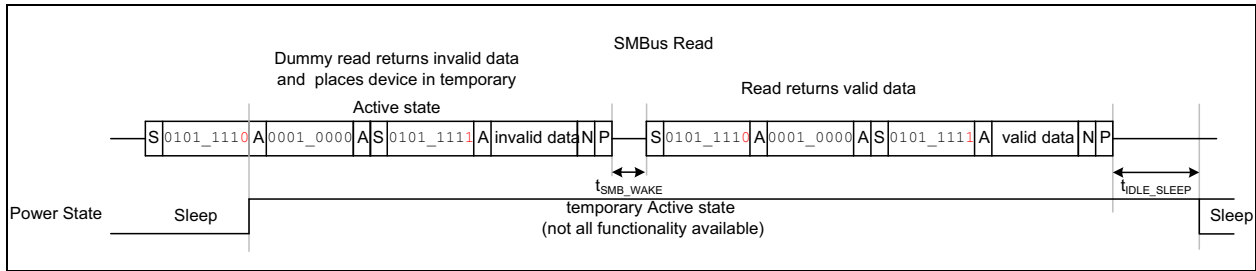
### 5.1.2 SLEEP STATE OPERATION

The PWR\_EN1 and PWR\_EN2 pins may be used to cause the UCS2113 to enter/exit Sleep. These pins are AND'ed for Sleep mode.

When the UCS2113 is in the Sleep state, the device will be in its lowest power state. The port power switch will be disabled.  $V_{BUS1}$  and  $V_{BUS2}$  will be near ground

potential. The ALERT#1 and ALERT#2 pins will not be asserted. If asserted prior to entering the Sleep state, the ALERT# pin will be released. SMBus activity is limited to single byte read or write.

The first data byte read from the UCS2113 when it is in the Sleep state will wake it; however, the data to be read will return all 0's and should be considered invalid. This is a "dummy" read byte meant to wake the UCS2113. Subsequent read or write bytes will be accepted normally. After the dummy read, the UCS2113 will be in a higher power state (see Figure 5-2). After communication has not occurred for  $t_{IDLE\_SLEEP}$ , the UCS2113 will return to Sleep.



**FIGURE 5-2:** Wake from Sleep using SMBus Read.

## 5.1.3 ACTIVE STATE OPERATION

Every time the UCS2113 enters the Active state, the port power switches are closed. The UCS2113 cannot be in the Active state (and therefore, the port power switch cannot be turned on) if any of the following conditions exist:

- $V_S < V_{S\_UVLO}$
- PWR\_EN1 and PWR\_EN2 are disabled.

## 5.1.4 ERROR STATE OPERATION

The UCS2113 will enter the Error state from the Active state when any of the following events are detected:

- The maximum allowable internal die temperature ( $T_{TSD\_HIGH}$ ) has been exceeded.
- The  $T_{TSD\_LOW}$  die temperature has been exceeded and any of the following conditions is met:
  - a power switch operates in constant current mode
  - PWR\_EN1 and/or PWR\_EN2 controls transition from inactive to active.
  - it is a power up situation and PWR\_EN1 and/or PWR\_EN2 pins are active.
- An overcurrent condition has been detected.
- An undervoltage condition on either  $V_{BUS}$  pin has been detected (see [Section 5.3.4 “Undervoltage Lockout on VS”](#)).
- A back-voltage condition has been detected (see [Section 5.3.2 “Back-voltage Detection”](#)).
- A discharge error has been detected.
- An overvoltage condition on the  $V_S$  pin.

When the UCS2113 enters the Error state, the port power switch will be disabled while the ALERT# pin is asserted. It will remain off while in this power state. The UCS2113 will leave this state as determined by the fault handling selection.

With the Auto-recovery fault handler, after the  $t_{CYCLE}$  time period, the UCS2113 will check that all of the error conditions have been removed.

If all of the error conditions have been removed, the UCS2113 will return to the Active state.

If both PWR\_EN1 and PWR\_EN2 controls transition from active to inactive while the UCS2113 is in the Error state, the device will not enter the Sleep state. After the fault has been removed, the UCS2113 will not automatically enter the Sleep state if the EN\_VBUS\_DISCHG bit from the General Configuration 2 Register is not set (default setting). To enter the Sleep state, the PWR\_EN pins must be toggled or an SMBus read register command must be sent.

## 5.2 Communication

The UCS2113 can operate in SMBus mode (see [Section 7.0 “System Management Bus Protocol”](#)) or Stand-Alone mode. The resistor connected to the COMM\_ILIM pin determines the operating mode and the hardware-set  $I_{LIM}$  setting, as shown in [Table 5-3](#). Unless connected to GND or  $V_{DD}$ , the resistors in [Table 5-3](#) are external pull-down resistors.

The SMBus address is specified in [Section 7.2 “SMBus Address and RD/WR Bit”](#).

**TABLE 5-3: COMMUNICATION DECODE**

COMM_ILIM Pull Down Resistor ( $\pm 1\%$ )	PWR_EN1 and PWR_EN2 Polarity	$I_{LIM}$ (A)	Total $I_{LIM}$ (A) (Note 1)	Communication Mode
GND	Active-High	0.53	0.53 + 0.53	SMBUS
10 k $\Omega$	Active-High	0.96	0.96 + 0.96	SMBUS
12 k $\Omega$	Active-High	1.07	1.07 + 1.07	SMBUS
15 k $\Omega$	Active-High	1.28	1.28 + 1.28	SMBUS
18 k $\Omega$	Active-High	1.6	1.6 + 1.6	SMBUS

**TABLE 5-3: COMMUNICATION DECODE (CONTINUED)**

COMM_ILIM Pull Down Resistor ( $\pm 1\%$ )	PWR_EN1 and PWR_EN2 Polarity	$I_{LIM}$ (A)	Total $I_{LIM}$ (A) (Note 1)	Communication Mode
22 k $\Omega$	Active-High	2.13	2.13 + 2.13	SMBUS
27 k $\Omega$	Active-High	2.67	2.67 + 2.67	SMBUS
33 k $\Omega$	Active-High	3.2	3.2 + 3.2	SMBUS
47 k $\Omega$	Active-Low	0.53	0.53 + 0.53	Stand-Alone
56 k $\Omega$	Active-Low	0.96	0.96 + 0.96	Stand-Alone
68 k $\Omega$	Active-Low	1.07	1.07 + 1.07	Stand-Alone
82 k $\Omega$	Active-Low	1.28	1.28 + 1.28	Stand-Alone
100 k $\Omega$	Active-Low	1.6	1.6 + 1.6	Stand-Alone
120 k $\Omega$	Active-Low	2.13	2.13 + 2.13	Stand-Alone
150 k $\Omega$	Active-Low	2.67	2.67 + 2.67	Stand-Alone
$V_{DD}$	Active-Low	3.2	3.2 + 3.2	Stand-Alone

**Note 1:** The total maximum current depends on power dissipation characteristics of the design (see [Table 1-1](#)).

## 5.3 Supply Voltages

### 5.3.1 $V_{DD}$ SUPPLY VOLTAGE

The UCS2113 requires 4.5V to 5.5V to be present on the  $V_{DD}$  pin for core device functionality. Core device functionality consists of maintaining register states and wake-up upon SMBus/I<sup>2</sup>C query.

### 5.3.2 BACK-VOLTAGE DETECTION

The back-voltage detector is functional in all power states (Sleep and Active).

When in Sleep, the UCS2113 will enter the Error state from Sleep if a back-voltage condition was detected.

Whenever the following condition is true for either port, the port power switch will be disabled and a back-voltage event will be flagged. This will cause the UCS2113 to enter the Error power state (see [Section 5.1.4 “Error State Operation”](#)).

**Note:** The  $V_{BUS}$  voltage exceeds the  $V_S$  and/or the  $V_{DD}$  pin voltage by  $V_{BV\_TH}$  and the port power switch is closed. The port power switch will be opened immediately. If the condition lasts for longer than  $t_{MASK}$ , then the UCS2113 will enter the Error state. Otherwise, the port power switch will be turned on as soon as the condition is removed.

### 5.3.3 BACK-DRIVE CURRENT PROTECTION

If a portable device is attached that is self-powered, it may drive the  $V_{BUS}$  port to its power supply voltage level; however, the UCS2113 is designed such that leakage current from the  $V_{BUS}$  pins to the  $V_{DD}$  and/or the  $V_S$  pin shall not exceed  $I_{LKG\_1}$  (if the  $V_{DD}$  and/or  $V_S$  voltage is zero) or  $I_{LKG\_2}$  (if the  $V_{DD}$  and/or  $V_S$  voltage exceeds  $V_{DD\_TH}$  and the power switch is open).

### 5.3.4 UNDERVOLTAGE LOCKOUT ON $V_S$

The UCS2113 requires a minimum voltage ( $V_{S\_UVLO}$ ) be present on the  $V_S$  pin for Active power state.

### 5.3.5 OVERVOLTAGE DETECTION AND LOCKOUT ON $V_S$

Both power switches will be disabled if the voltage on any  $V_S$  pin exceeds a voltage ( $V_{S\_OV}$ ) for longer than the specified time ( $t_{MASK}$ ). This will cause the device to enter the Error state and both ALERT#1 and ALERT#2 pins will be asserted.

### 5.3.6 PWR\_EN1 AND PWR\_EN2 INPUT

The PWR\_EN control affects the power state and enables the port power switch to be turned on if conditions are met (see [Table 5-2](#)). The port power switch cannot be closed if PWR\_EN is disabled. However, if PWR\_EN is enabled, the port power switch is not necessarily closed (see [Section 5.1.3 “Active State Operation”](#)). In SMBus mode, the PWR\_EN1 and PWR\_EN2 pins states will be ignored by the UCS2113 if the PIN\_IGN configuration bit is set; otherwise, the PWR\_EN1S and PWR\_EN2S configuration bits are checked along with the pins.



## 5.4 Discrete Output Pins

### 5.4.1 ALERT#1 AND ALERT#2 OUTPUT PINS

The UCS2113 has two independent ALERT# out pins. ALERT#1 is tied to the status of the V<sub>BUS1</sub> pin. ALERT#2 is tied to the status of the V<sub>BUS2</sub> pin.

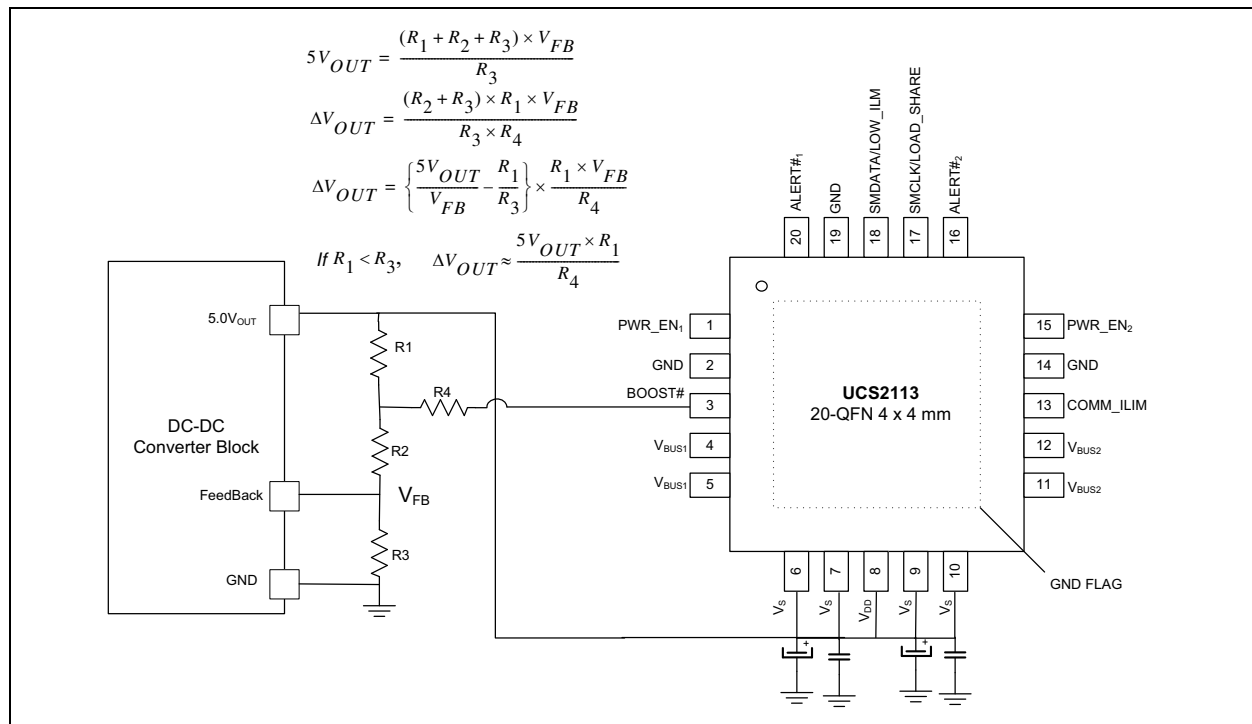
The ALERT# pin is an active-low open-drain interrupt to the host controller. The ALERT# pin is asserted when an error occurs. Also, when charge rationing is enabled, the ALERT# pin is asserted by default when the current rationing threshold is reached (as determined by RATION\_BEH<1:0>). The ALERT# pin is released when all error conditions that may assert the ALERT# pin (such as an error condition and charge rationing) have been removed or reset as necessary.

The UCS2113 is compatible with the Microchip hub devices supporting single pin power control feature. These hub devices have a single connection to the PWR\_EN and ALERT# pins of the UCS2113, which are tied together in the application.

### 5.4.2 BOOST# OUTPUT PIN

The UCS2113 provides a BOOST# output pin to compensate for voltage drops during high loads. The BOOST# pin is an active-low, open-drain output that would be connected to a resistor in the DC-DC converter's feedback error voltage loop (see [Figure 5-3](#)).

The BOOST# pin is asserted when V<sub>BUS</sub> Current > I<sub>BOOST</sub>. I<sub>BOOST</sub> typical value is 1.9A. The BOOST# is OR'ed for both V<sub>BUS1</sub> and V<sub>BUS2</sub> ports. When the BOOST# pin is asserted, it will remain in this state for at least t<sub>BOOST\_MAT</sub> (minimum assertion time).



**FIGURE 5-3:** Boost# Pin Usage.

## 5.5 Discrete Input Pins

### 5.5.1 COMM\_ILIM INPUT

The COMM\_ILIM input determines the communications mode, as shown in [Table 6-1](#). This is also the hardware strap for MAX Current Limit.

### 5.5.2 SMCLK

When operated in Stand-Alone mode, this pin should be tied to ground. When the UCS2113 is configured for SMBus communications, the SMCLK is the clock input.

### 5.5.3 SMDATA

When used in Stand-Alone, this pin should be tied to ground.

When the UCS2113 is configured for SMBus communications, the SMDATA is the data input/output.

NOTES:

## 6.0 USB PORT POWER SWITCH

To assure compliance to various charging specifications, the UCS2113 contains a USB port power switch that supports two current-limiting modes: Trip and Constant current (variable slope). The current limit ( $I_{LIM}$ ) is pin selectable (and may be updated via the register set). The switch also includes soft start circuitry and a separate short circuit current limit.

The port power switch is on in the Active state (except when  $V_{BUS}$  is discharging).

### 6.1 Current Limiting

#### 6.1.1 CURRENT LIMIT SETTING

The UCS2113 hardware set current limit,  $I_{LIM}$ , can be one of eight values. This resistor value is read once upon UCS2113 power-up. The current limit can be changed via the SMBus/I<sup>2</sup>C after power-up; however, the programmed current limit cannot exceed the hardware set current limit. Unless connected to  $V_{DD}$ , the resistors in [Table 6-1](#) are pull-down resistors.

At power-up, the communication mode (Stand-Alone or SMBus/I<sup>2</sup>C) and hardware current limit ( $I_{LIM}$ ) are determined via the pull-down resistor (or pull-up resistor if connected to  $V_{DD}$ ) on the COMM\_ILIM pin, as shown in [Table 6-1](#).

#### 6.1.2 SHORT CIRCUIT OUTPUT CURRENT LIMITING

Short circuit current limiting occurs when the output current is above the selectable current limit ( $I_{LIMx}$ ). This event will be detected and the current will immediately be limited (within  $t_{SHORT\_LIM}$  time). If the condition remains, the port power switch will flag an Error condition and enter the Error state.

#### 6.1.3 SOFT START

When the PWR\_EN control changes states to enable the port power switch, the UCS2113 invokes a soft start routine for the duration of the  $V_{BUS}$  rise time ( $t_{R\_BUS}$ ). This soft start routine will limit current flow from  $V_S$  into  $V_{BUS}$  while it is active. This circuitry will prevent current spikes due to a step in the portable device current draw.

In the case when a portable device is attached while the PWR\_EN pin is already enabled, if the bus current exceeds  $I_{LIM}$ , the UCS2113 current limiter will respond within a specified time ( $t_{SHORT\_LIM}$ ) and will operate normally at this point. The  $C_{BUS}$  capacitor will deliver the extra current, if any, as required by the load change.

TABLE 6-1:  $I_{LIM}$  DECODE

COMM_ILIM Pull-down Resistor ( $\pm 1\%$ )	PWR_EN1 and PWR_EN2 Polarity	$I_{LIM}$ (A)	Total $I_{LIM}$ (A) (Note 1)
GND	Active-High	0.53	0.53+0.53
10 k $\Omega$	Active-High	0.96	0.96+0.96
12 k $\Omega$	Active-High	1.07	1.07+1.07
15 k $\Omega$	Active-High	1.28	1.28+1.28
18 k $\Omega$	Active-High	1.6	1.6+1.6
22 k $\Omega$	Active-High	2.13	2.13+2.13
27 k $\Omega$	Active-High	2.67	2.67+2.67
33 k $\Omega$	Active-High	3.2	3.2+3.2
47 k $\Omega$	Active-Low	0.53	0.53+0.53
56 k $\Omega$	Active-Low	0.96	0.96+0.96
68 k $\Omega$	Active-Low	1.07	1.07+1.07
82 k $\Omega$	Active-Low	1.28	1.28+1.28
100 k $\Omega$	Active-Low	1.6	1.6+1.6
120 k $\Omega$	Active-Low	2.13	2.13+2.13
150 k $\Omega$	Active-Low	2.67	2.67+2.67
$V_{DD}$	Active-Low	3.2	3.2+3.2

**Note 1:** The total maximum current depends on power dissipation characteristics of the design (see [Table 1-1](#)).

#### 6.1.4 CURRENT LIMITING MODES

The UCS2113 current limiting has two modes: Trip and Constant Current (variable slope). Either mode functions at all times when the port power switch is closed.

##### 6.1.4.1 Trip Mode

When using Trip current limiting, the UCS2113 USB port power switch functions as a low-resistance switch and rapidly turns off if the current limit is exceeded. While operating using Trip current limiting, the  $V_{BUS}$  output voltage will be held relatively constant (equal to the  $V_S$  voltage minus the  $R_{ON} \times I_{BUS}$  current) for all current values up to the  $I_{LIM}$ .

If the current drawn by a portable device exceeds  $I_{LIM}$ , the following occurs:

1. The port power switch will be turned off (Trip action).
2. The UCS2113 will enter the Error state and assert the ALERT# pin.
3. The fault handling circuitry will then determine subsequent actions.