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UCS81003

Automotive USB Port Power Controller with Charger Emulation

Features:

- Port Power Switch with Two Current Limit Behaviors
  - 2.9V to 5.5V source voltage range
  - Up to 3.0A current (2.85A typical) with 55 mΩ on resistance
  - Overcurrent trip or constant current limiting
  - Soft turn-on circuitry
  - Programmable current limit
  - Dynamic thermal management
  - Under and overvoltage lockout
  - Back-Drive, back-voltage protection
  - Latch or auto-recovery (low test current) fault handling
  - Selectable active-high or -low power switch enable
  - BC1.2 V_{BUS} discharge port renegotiation function
- Selectable/Automatic Cycling of Universal Serial Bus (USB) Data Line Charger Emulation Profiles
  - USB-IF BC1.2 Charging Downstream Port (CDP) and Dedicated Charging Port (DCP) modes, Chinese Telecommunications Industry Standard YD/T 1591-2009 and most Apple® Inc. and RIM® protocols standard; others as defined via the SMBus 2.0/I^2C™ protocol
  - Supports 12W charging emulation
  - USB 2.0 compliant high-speed data switch (in data pass-through, SDP and CDP modes)
  - Nine preloaded charger emulation profiles for maximum compatibility coverage of the peripheral devices
  - One custom-programmable charger emulation profile for portable device support for fully host-controlled charger emulation
- Supports Active Cables
- Self-Contained Current Monitoring and Rationing for Power-Allocation Applications
- Low-Power Attach Detection and Open-Drain (A_DET#) Pin
- Ultra-Low Power Sleep State
- Optional Split Supply Support for V_S and V_{DD} for Low-Power in System Standby States
- Wake on Attach USB
- SMBus 2.0/I^2C Communications
  - Supports block write and read
  - Multiple SMBus addresses
- Wide Operating Temperature Range: -40°C to +85°C
- IEC61000-4-2 8/15 kV Electrostatic Discharge (ESD) Immunity

Description:

The UCS81003 provides a USB port power switch for precise control of up to 3.0A continuous current (2.85A typical) with Overcurrent Limit (OCL), dynamic thermal management, latch or auto-recovery (low-test current) fault handling, selectable active-low or -high enable, under and overvoltage lockout, back-drive protection and back-voltage protection.

Split supply support for V_S and V_{DD} is an option for low power in system standby states. This gives battery-operated applications (such as on-board computers) the ability to detect attachments from a Sleep or Off state. After the Attach Detection is flagged, the system can decide to wake up and/or provide charging.

In addition to Power Switching and Current Limiting modes, the UCS81003 will automatically charge a wide variety of portable devices, including USB-IF BC1.2, YD/T-1591 (2009), most Apple Inc. and RIM, and many others. Nine preloaded charger emulation profiles maximize the compatibility coverage of the peripheral devices. Additionally, a customizable charger emulation profile is available to accommodate unique existing and future portable device handshaking/signature requirements.

The UCS81003 also provides current monitoring to allow intelligent management of system power and charge rationing for controlled delivery of current, regardless of the host power state. This is especially important for battery-operated applications that want to provide power and do not want to drain the battery excessively.

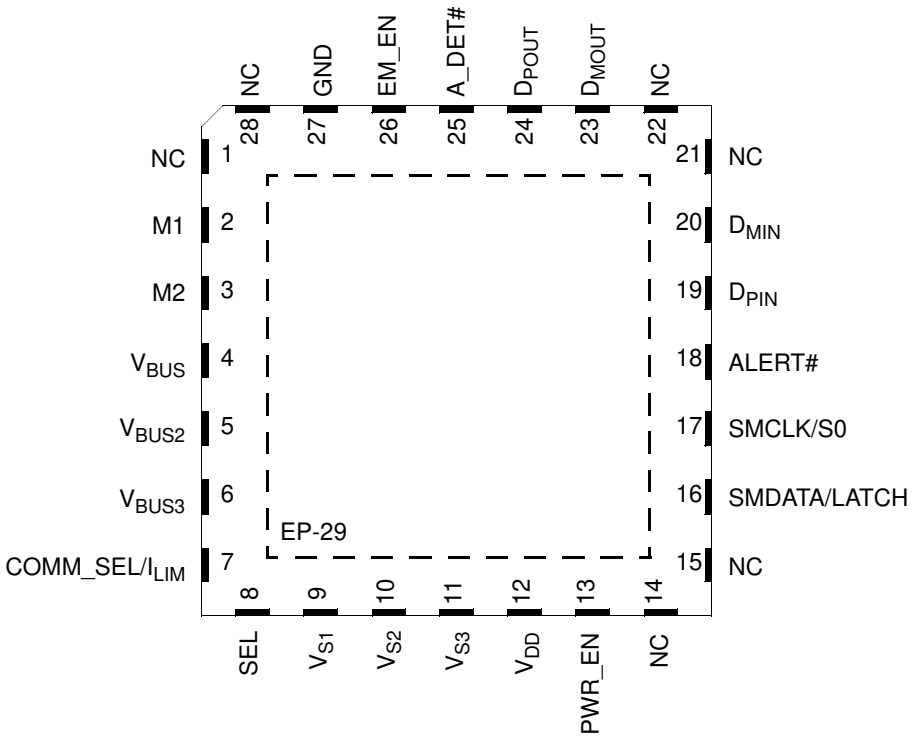
The UCS81003 is available in a 5 mm x 5 mm 28-pin VQFN package.

Applications:

- DC Power Socket Replacement
- Consumer USB Port Protection
- Consumer Device Charging Port
- Auxiliary Box Charging Feature
- Rear Seat Entertainment Consumer Access Point

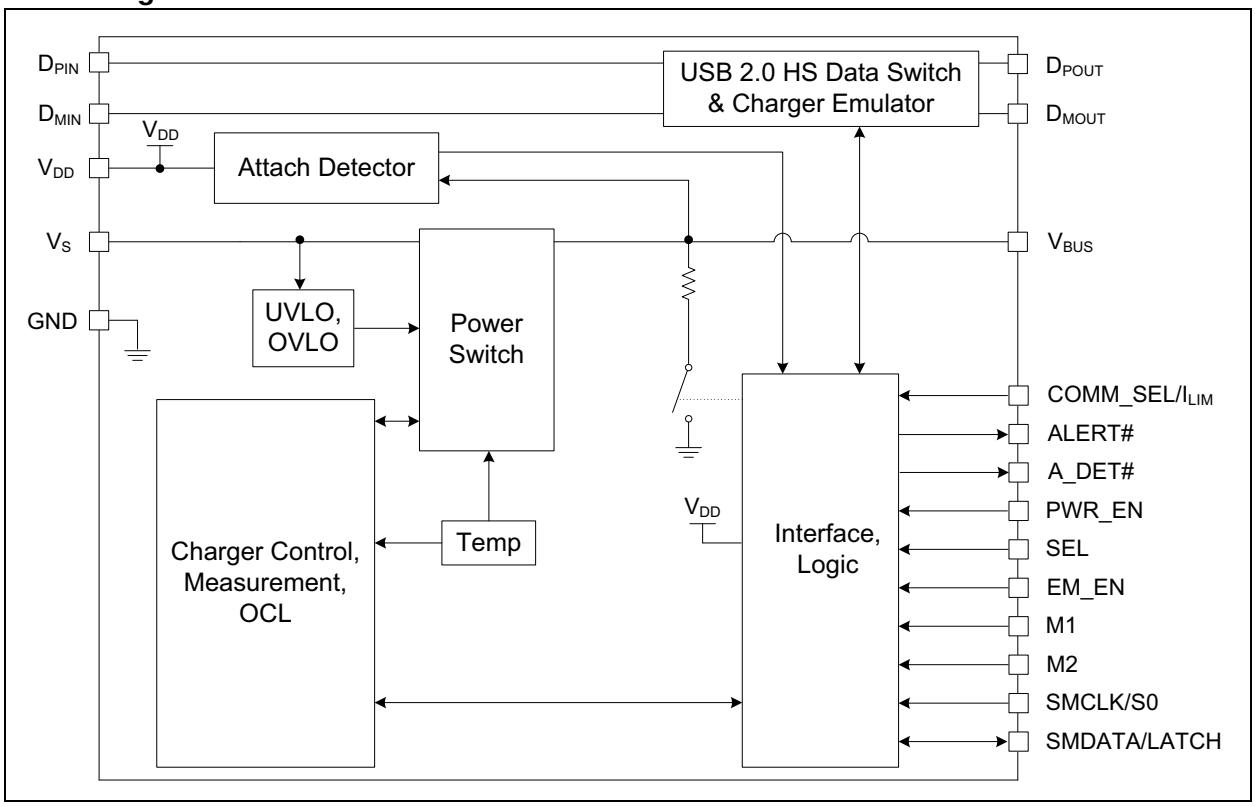
Package Type

UCS81003
5 x 5 VQFN*



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD}, V_S and V_{BUS} pins ..... -0.3 to 6V

Pull-Up Voltage (V_{PULLUP}) ..... -0.3 to V_{DD} + 0.3V

Data Switch Current (I_{HSW_ON}), Switch On ..... ±50 mA

Port Power Switch Current ..... Internally limited

Data Switch Pin Voltage To Ground (D_{POUT}, D_{PIN}, D_{MOUT}, D_{MIN}); (V_{DD} powered or unpowered) ..... -0.3 to V_{DD} + 0.3V

Differential Voltage Across Open Data Switch (D_{POUT} -D_{PIN}, D_{MOUT} - D_{MIN}, D_{PIN} - D_{POUT}, D_{MIN} - D_{MOUT}) ..... V_{DD}

Voltage on any Other Pin to Ground ..... -0.3 to V_{DD} + 0.3V

Current on any Other Pin ..... ±10 mA

Package Power Dissipation ..... Table 1-1

Maximum Junction Temperature Under Bias ..... +125°C

Storage Temperature Range ..... -55°C to +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: POWER DISSIPATION SUMMARY

Board	Package	θ_{JC}	θ_{JA}	De-rating Factor Above +25°C	T_A < +25°C Power Rating	T_A < +70°C Power Rating	T_A < +85°C Power Rating
High K (see Note 1)	28-pin VQFN 5 x 5 mm	4°C/W	32°C/W	31.3 mW°/C	2470 mW	1220 mW	800 mW
Low K (see Note 1)	28-pin VQFN 5 x 5 mm	4°C/W	51°C/W	19.6 mW°/C	1620 mW	800 mW	530 mW

Note 1: Junction to ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 77°C/W, including localized PCB temperature increase. This θ_{JA} value is an estimate for a JEDEC® compliant 2S2P PCB with thermal vias.

TABLE 1-2: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_J = -40°C to +125°C; all Typical values at V_{DD} = V_S = 5V, T_J = +27°C.

Characteristic	Sym.	Min.	Typ.	Max.	Unit	Conditions
Power Supply						
Supply Voltage	V_{DD}	4.5	5	5.5	V	Note 1
Source Voltage	V_S	2.9	5	5.5	V	Note 1
Supply Current in Active (I_{DD_ACTIVE} + I_{VS_ACT})	I_{ACTIVE}	—	650	750	µA	Average current I_{BUS} = 0 mA, T_J < +85°C

Note 1: For split supply systems using the Attach Detection feature, V_S must not exceed V_{DD} + 150 mV.

2: This parameter is ensured by design and is not 100% tested.

3: This parameter is characterized, but not 100% production tested.

4: The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \le I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \le 1.68A$).

5: The Minimum and Maximum values represent the boundaries of a programmable range. Each value in the range is typical.

TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_J = -40°C to +125°C; all Typical values at V_{DD} = V_S = 5V, T_J = +27°C.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Supply Current in Sleep (I_{DD_SLEEP} + I_{VS_SLEEP})	I_{SLEEP}	—	5	15	µA	Average current $V_{PULLUP} \le V_{DD}$, T_J < +85°C
Supply Current in Detect (I_{DD_DETECT} + I_{VS_DETECT})	I_{DETECT}	—	175	—	µA	Average current, no portable device attached
Power-On Reset						
V_S Low Threshold	V_{S_UVLO}	—	2.5	—	V	V_S voltage increasing
V_S Low Hysteresis	$V_{S\_UVLO\_HYST}$	—	100	—	mV	V_S voltage decreasing
V_{DD} Low Threshold	V_{DD_TH}	—	4	—	V	V_{DD} voltage increasing
V_{DD} Low Hysteresis	$V_{DD\_TH\_HYST}$	—	500	—	mV	V_{DD} voltage decreasing
I/O Pins - SMCLK, SMDATA, EM_EN, M1, M2, PWR_EN, S0, LATCH, ALERT#, A_DET# – DC Parameters						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{SINK_IO} = 8 mA SMDATA, ALERT#, A_DET#
Input High Voltage	V_{IH}	2.1	—	—	V	PWR_EN, EM_EN, M1, M2, LATCH, S0, SMDATA, SMCLK
Input Low Voltage	V_{IL}	—	—	0.8	V	PWR_EN, EM_EN, M1, M2, LATCH, S0, SMDATA, SMCLK
Leakage Current	I_{LEAK}	—	—	±5	µA	Powered or unpowered, $V_{PULLUP} \le V_{DD}$, T_J < +85°C
Interrupt Pins - AC Parameters						
ALERT#, A_DET# Pin Blanking Time	t_{BLANK}	—	25	—	ms	
ALERT# Pin Interrupt Masking Time	t_{MASK}	—	5	—	ms	
SMBus/I²C™ Timing						
Input Capacitance	C_{IN}	—	5	—	pF	
Clock Frequency	f_{SMB}	10	—	400	kHz	
Spike Suppression	t_{SP}		—	50	ns	Note 2
Bus Free Time Stop to Start	t_{BUF}	1.3	—	—	µs	
Start Setup Time	$t_{SU:STA}$	0.6	—	—	µs	
Start Hold Time	$t_{HD:STA}$	0.6	—	—	µs	
Stop Setup Time	$t_{SU:STO}$	0.6	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	0.6	—	—	µs	
Clock Low Period	t_{LOW}	1.3	—	—	µs	
Clock High Period	t_{HIGH}	0.6	—	—	µs	

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TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_J = -40°C to +125°C; all Typical values at V_{DD} = V_S = 5V, T_J = +27°C.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Clock/Data Fall Time	t_{FALL}	—	—	300	ns	Min = 20 + 0.1 C_{LOAD} ns, Note 3
Clock/Data Rise Time	t_{RISE}	—	—	300	ns	Min = 20 + 0.1 C_{LOAD} ns, Note 3
Capacitive Load	C_{LOAD}	—	—	400	pF	Per bus line, Note 2
Timeout	$t_{TIMEOUT}$	25	—	35	ms	Disabled by default, Note 2
Idle Reset	t_{IDLE_RESET}	350	—	—	µs	Disabled by default, Note 2
High-Speed Data Switch						
High-Speed Data Switch - DC Parameters						
Switch Leakage Current	I_{HSW_OFF}	—	±0.5	—	µA	Switch open - D_{PIN} to D_{POUT}, D_{MIN} to D_{MOUT}, or all four pins to ground. $V_{DD} \leq V_S$
Charger Resistance	R_{CHG}	—	2	—	MΩ	D_{POUT} or D_{MOUT} to V_{BUS} or ground (see Figure 1-2), BC1.2 DCP charger emulation active
On Resistance	R_{ON_HSW}	—	2	—	Ω	Switch closed, V_{DD} = 5V test current = 8 mA, test voltage = 0.4V, see Figure 1-2
On Resistance	$R_{ON\_HSW\_1}$	—	5	—	Ω	Switch closed, V_{DD} = 5V, test current = 8 mA, test voltage = 3.0V, see Figure 1-2
Delta-On Resistance	ΔR_{ON_HSW}	—	±0.3	—	Ω	Switch closed, V_{DD} = 5V, I_{TST} = 8 mA, V_{TST} = 0 to 1.5V, see Figure 1-2
High-Speed Data Switch - AC Parameters						
D_P, D_M Capacitance to Ground	C_{HSW_ON}	—	4	—	pF	Switch closed, V_{DD} = 5V
D_P, D_M Capacitance to Ground	C_{HSW_OFF}	—	2	—	pF	Switch open, V_{DD} = 5V
Turn Off Time	t_{HSW_OFF}	—	400	—	µs	Time from state control (EM_EN, M1, M2) switch on to switch off, R_{TERM} = 50Ω, C_{LOAD} = 5 pF
Turn-On Time	t_{HSW_ON}	—	400	—	µs	Time from state control (EM_EN, M1, M2) switch off to switch on, R_{TERM} = 50Ω, C_{LOAD} = 5 pF
Propagation Delay	t_{PD}	—	0.25	—	ns	R_{TERM} = 50Ω, C_{LOAD} = 5 pF

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3: This parameter is characterized, but not 100% production tested.

4: The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \leq I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \leq 1.68A$).

5: The Minimum and Maximum values represent the boundaries of a programmable range. Each value in the range is typical.

TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_J = -40°C to +125°C; all Typical values at V_{DD} = V_S = 5V, T_J = +27°C.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Propagation Delay Skew	Δt_{PD}	—	25	—	ps	R_{TERM} = 50Ω, C_{LOAD} = 5 pF
Rise/Fall Time	$t_{F/R}$	—	10	—	ns	R_{TERM} = 50Ω, C_{LOAD} = 5 pF
D_P – D_M Crosstalk	X_{TALK}	—	-40	—	dB	R_{TERM} = 50Ω, C_{LOAD} = 5 pF
Off Isolation	O_{IRR}	—	-30	—	dB	R_{TERM} = 50Ω, C_{LOAD} = 5 pF, f = 240 MHz
-3 dB Bandwidth	BW	—	1100	—	MHz	R_{TERM} = 50Ω, C_{LOAD} = 5 pF, V_{DPOUT} = V_{DMOUT} = 350 mV DC
Total Jitter	t_J	—	200	—	ps	R_{TERM} = 50Ω, C_{LOAD} = 5 pF, Rise Time = Fall Time = 500 ps at 480 Mbps (PRBS = 2^{15} – 1)
Skew of Opposite Transitions of the Same Output	$t_{SK(P)}$	—	20	—	ps	R_{TERM} = 50Ω, C_{LOAD} = 5 pF
Port Power Switch						
Port Power Switch - DC Parameter						
Overvoltage Lockout	V_{S_OV}	—	6	—	V	
On Resistance	R_{ON_PSW}	—	55	—	mΩ	4.75V < V_S < 5.25V
V_S Leakage Current	I_{LEAK_VS}	—	2.22	—	µA	Sleep state into V_S pin
Back-Voltage Protection Threshold	V_{BV_TH}	—	150	—	mV	V_{BUS} > V_S, V_S > V_{S_UVLO}
Back-Drive Current	I_{BD_1}	—	0	3	µA	V_{DD} < V_{DD_TH}, Any powered power pin to any unpowered power pin. Current out of unpowered pin (Note 3).
	I_{BD_2}	—	0	2	µA	V_{DD} < V_{DD_TH}, Any powered power pin to any unpowered power pin, except for V_{DD} to V_{BUS} in Detect power state and V_S to V_{BUS} in Active Power state. Current out of unpowered pin (Note 3).

Note 1: For split supply systems using the Attach Detection feature, V_S must not exceed V_{DD} + 150 mV.

2: This parameter is ensured by design and is not 100% tested.

3: This parameter is characterized, but not 100% production tested.

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TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_J = -40°C to +125°C; all Typical values at V_{DD} = V_S = 5V, T_J = +27°C.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Selectable Current Limits	I_{LIM1}	—	570	—	mA	I_{LIM} Resistor = 0 or 47 kΩ (minimum mA setting)
	I_{LIM2}	—	1000	—		I_{LIM} Resistor = 10 kΩ or 56 kΩ
	I_{LIM3}	—	1130	—		I_{LIM} Resistor = 12 kΩ or 68 kΩ
	I_{LIM4}	—	1350	—		I_{LIM} Resistor = 15 kΩ or 82 kΩ
	I_{LIM5}	—	1680	—		I_{LIM} Resistor = 18 kΩ or 100 kΩ
	I_{LIM6}	—	2050	—		I_{LIM} Resistor = 22 kΩ or 120 kΩ
	I_{LIM7}	—	2280	—		I_{LIM} Resistor = 27 kΩ or 150 kΩ
	I_{LIM8}	—	2850	3000		I_{LIM} Resistor = 33 kΩ or V_{DD}
Pin Wake Time	t_{PIN_WAKE}	—	3	—	ms	
SMBus Wake Time	t_{SMB_WAKE}	—	4	—	ms	
Idle Sleep Time	t_{IDLE_SLEEP}	—	200	—	ms	
Thermal Regulation Limit	T_{REG}	—	110	—	°C	Die Temperature at which current limit will be reduced.
Thermal Regulation Hysteresis	T_{REG_HYST}	—	10	—	°C	Hysteresis for t_{REG} functionality. Temperature must drop by this value before I_{LIM} value restored to normal operation.
Thermal Shutdown Threshold	T_{TSD}	—	135	—	°C	Die Temperature at which port power switch will turn off.
Thermal Shutdown Hysteresis	T_{TSD_HYST}	—	35	—	°C	After Shutdown due to T_{TSD} being reached, a die temperature drop is required before port power switch can be turned on again.
Auto-Recovery Test Current	I_{TEST}	—	190	—	mA	Portable device attached, V_{BUS} = 0V, Die Temp < T_{TSD}
Auto-Recovery Test Voltage	V_{TEST}	—	750	—	mV	Portable device attached, V_{BUS} = 0V before application, Die Temp < T_{TSD} Programmable, 250 - 1000 mV, default listed
Discharge Impedance	$R_{DISCHARGE}$	—	100	—	Ω	

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TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

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Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Port Power Switch - AC Parameters						
Turn-On Delay	t_{ON_PSW}	—	0.75	—	ms	PWR_EN active toggle to switch on time, V_{BUS} discharge not active.
Turn-Off Time	$t_{OFF\_PSW\_INA}$	—	0.75	—	ms	PWR_EN inactive toggle to switch off time C_{BUS} = 120 µF
Turn-Off Time	$t_{OFF\_PSW\_ERR}$	—	1	—	ms	Overcurrent Error, V_{BUS} Min Error, or Discharge Error to switch off, C_{BUS} = 120 µF
Turn-Off Time	$t_{OFF\_PSW\_ERR}$	—	100	—	ns	TSD or back-drive error to switch off, C_{BUS} = 120 µF
V_{BUS} Output Rise Time	t_{R_BUS}	—	1.1	—	ms	Measured from 10% to 90% of V_{BUS}, C_{LOAD} = 220 µF, I_{LIM} = 1.0A
Soft Turn-On Rate	$\Delta I_{BUS}/\Delta_t$	—	100	—	mA/µs	
Temperature Update Time	t_{DC_TEMP}	—	200	—	ms	Programmable 200 - 1600 ms, default listed
Short-Circuit Response Time	t_{SHORT_LIM}	—	1.5	—	µs	Time from detection of short to current limit applied. No C_{BUS} applied.
Short-Circuit Detection Time	t_{SHORT}	—	6	—	ms	Time from detection of short to port power switch disconnect and ALERT# pin assertion.
Latched Mode Cycle Time	t_{UL}	—	7	—	ms	From PWR_EN edge transition from inactive to active to begin error recovery.
Auto-Recovery Mode Cycle Time	t_{CYCLE}	—	25	—	ms	Time delay before error condition check. Programmable 10-25 ms, default listed.
Auto-Recovery Delay	t_{RST}	—	20	—	ms	Portable device attached, V_{BUS} must be ≥ V_{TEST} after this time. Programmable 10-25 ms, default listed.
Discharge Time	$t_{DISCHARGE}$	—	200	—	ms	Amount of time discharge resistor applied. Programmable 100-400 ms, default listed.

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Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Port Power Switch Operation With Trip Mode Current Limiting						
Region 2 Current Keep-Out	I_{BUS_R2MIN}	—	0.12	—	A	
Minimum V_{BUS} Allowed at Output	V_{BUS_MIN}	1.5	2.0	2.25	V	Note 5
Port Power Switch Operation with Constant Current Limiting (Variable Slope)						
Region 2 Current Keep-Out	I_{BUS_R2MIN}	—	1.68	—	A	
Minimum V_{BUS} Allowed at Output	V_{BUS_MIN}	1.5	2.0	2.25	V	Note 5
Current Measurement - DC						
Current Measurement Range	I_{BUS_M}	0	—	2988.6	mA	Range 0 – 255 LSB (see Note 4)
Reported Current Measurement Resolution	D_{IBUS_M}	—	11.72	—	mA	1 LSB
Current Measurement Accuracy		—	±2	—	%	180 mA < I_{BUS} < I_{LIM}
		—	±2	—	LSB	I_{BUS} < 180 mA
Current Measurement - AC						
Sampling Rate		—	500	—	µs	
Charge Rationing - DC						
Accumulated Current Measurement Accuracy		—	±4.5	—	%	
Charge Rationing - AC						
Current Measurement Update Time	t_{PCYCLE}	—	1	—	s	
Attach/Removal Detection						
V_{BUS} Bypass - DC						
On Resistance	R_{ON_BYP}	—	50	—	Ω	
Leakage Current	I_{LEAK_BYP}	—	—	3	µA	Switch off, T_A < +85°C, Note 2
Current Limit	I_{DET_CHG}/I_{BUS_BYP}	—	2	—	mA	V_{DD} = 5V and V_{BUS} > 4.75V
Attach/Removal Detection - DC						
Attach Detection Threshold	I_{DET_QUAL}	—	800	—	µA	Programmable 200 – 1000 µA, default listed.

Note 1: For split supply systems using the Attach Detection feature, V_S must not exceed V_{DD} + 150 mV.

2: This parameter is ensured by design and is not 100% tested.

3: This parameter is characterized, but not 100% production tested.

4: The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \leq I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \leq 1.68A$).

5: The Minimum and Maximum values represent the boundaries of a programmable range. Each value in the range is typical.

TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_J = -40°C to +125°C; all Typical values at V_{DD} = V_S = 5V, T_J = +27°C.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Primary Removal Detection Threshold	$I_{REM\_QUAL\_ACT}$	—	700	—	µA	Programmable 100 – 900 µA, default listed, Active Power state
		—	800	—	µA	Programmable 200 – 1000 µA, default listed, Detect power state (see **Section 8.4 "Removal Detection"**).
Attach/Removal Detection - AC						
Attach Detection Time	t_{DET_QUAL}	—	100	—	ms	Time from Attach to A_DET# assert
Removal Detection Time	t_{REM_QUAL}	—	1000	—	ms	
Allowed Charge Time	t_{DET_CHARGE}	—	800	—	ms	C_{BUS} = 500 µF maximum, Programmable 200 – 2000 ms, default listed.
Charger Emulation Profile						
General Emulation - DC						
Charging Current Threshold	I_{BUS_CHG}	—	175.8	—	mA	Default
Charging Current Threshold Range	$I_{BUS\_CHG\_RNG}$	11.72	—	175.8	mA	Note 5
DP-DM Shunt Resistor Value	R_{DCP_RES}		—	200	Ω	Connected between D_{POUT} and D_{MOUT}, 0V < D_{POUT} = D_{MOUT} < 3V
Response Magnitude (voltage divider option resistance range)	SX_RXMAG_DVDR	93	—	200	kΩ	Note 5
Resistor Ratio Range (voltage divider option)	SX_RATIO	0.25	—	0.66	V/V	Note 5
Resistor Ratio Accuracy (voltage divider option)	SX_RATIO_ ACC	—	±0.5	—	%	Average over range
Response Magnitude (resistor option range)	SX_RXMAG_RES	1.8	—	150	kΩ	Note 5
Internal Resistor Tolerance (resistor option)	SX_RXMAG_RES _ACC	—	±10	—	%	Average over range
Response Magnitude (voltage option range)	SX_RXMAG_VOLT	0.4	—	2.2	V	Note 5
Voltage Option Accuracy	SX_RXMAG_VOLT _ACC	—	±1	—	%	No load, average over range
Voltage Option Accuracy	SX_RXMAG_VOLT _ACC_ 150	—	-6	—	%	150 µA load, average over range
Voltage Option Accuracy	SX_RXMAG_VOLT _ACC_ 250	—	-10	—	%	250 µA load, average over range

Note 1: For split supply systems using the Attach Detection feature, V_S must not exceed V_{DD} + 150 mV.

2: This parameter is ensured by design and is not 100% tested.

3: This parameter is characterized, but not 100% production tested.

4: The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \leq I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \leq 1.68A$).

5: The Minimum and Maximum values represent the boundaries of a programmable range. Each value in the range is typical.

TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_J = -40°C to +125°C; all Typical values at V_{DD} = V_S = 5V, T_J = +27°C.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Voltage Option Output	SX_RXMAG_VOLT _BC	0.5	—	—	V	D_{MOUT} = 0.6V, 250 µA load, Note 3
Response Magnitude (Zero Volt Option Range)	SX_PUPD	10	—	150	µA	SX_RXMAG_VOLT = 0 Note 5
Pull-Down Current Accuracy	SX_PUPD _ACC_3p6	—	±5	—	%	D_{POUT} or D_{MOUT} = 3.6V Compliance voltage
Pull-Down Current	SX_PUPD _ACC_BC	50	—	—	µA	Setting = 100 µA D_{POUT} or D_{MOUT} = 0.15V Compliance voltage, Note 3
Stimulus Voltage Threshold Range	SX_TH	0.3	—	2.2	V	Note 5
Stimulus Voltage Accuracy	SX_TH_ ACC	—	±2	—	%	Average over range
Stimulus Voltage Accuracy	SX_TH_ACC_BC	0.25	—	—	V	At SX_TH = 0.3V, Note 3
General Emulation - AC						
Emulation Reset Time	t_{EM_RESET}	—	50	—	ms	Default
Emulation Reset Time Range	$t_{EM\_RESET\_RNG}$	50	—	175	ms	Note 5
Emulation Timeout Range	$t_{EM\_TIMEOUT}$	0.8	—	12.8	s	Note 5
Stimulus Delay, SX_TD Range	t_{STIM_DEL}	0	—	100	ms	Note 5
Emulation Delay	t_{RES_EM}	—	—	0.5	s	Time from set impedance to impedance appears on D_P/D_M, Note 3.

Note 1: For split supply systems using the Attach Detection feature, V_S must not exceed V_{DD} + 150 mV.

2: This parameter is ensured by design and is not 100% tested.

3: This parameter is characterized, but not 100% production tested.

4: The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \le I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \le 1.68A$).

5: The Minimum and Maximum values represent the boundaries of a programmable range. Each value in the range is typical.

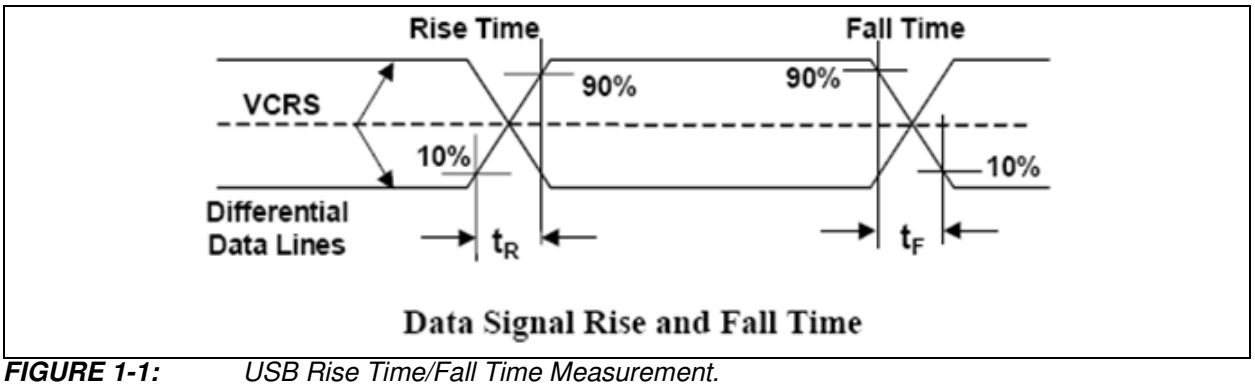

FIGURE 1-1: *USB Rise Time/Fall Time Measurement.*

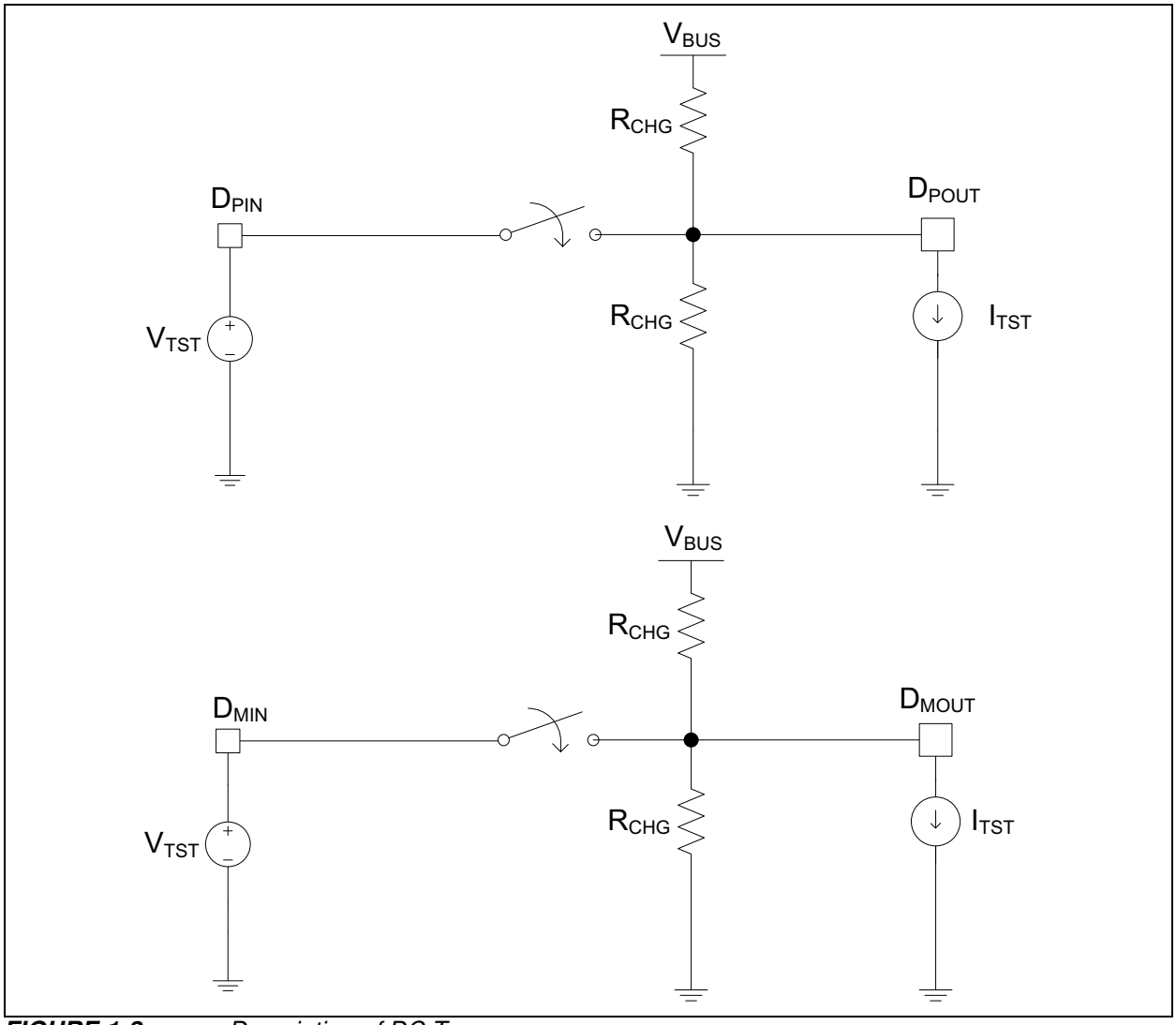

FIGURE 1-2: *Description of DC Terms.*

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+85	°C	
Storage Temperature Range	T_A	-55	—	+150	°C	
Thermal Package Resistances - see Table 1-1						

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_J = +27°C$.

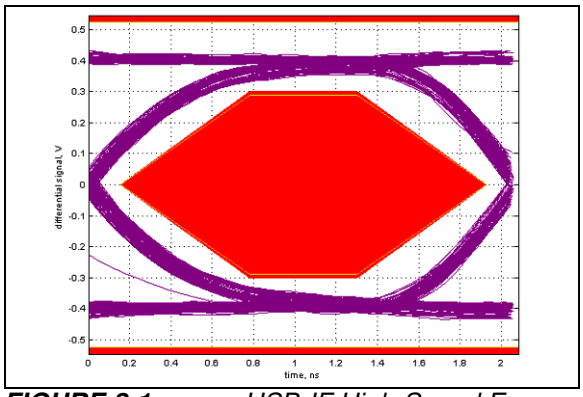

FIGURE 2-1: *USB-IF High-Speed Eye Diagram (Without Data Switch).*

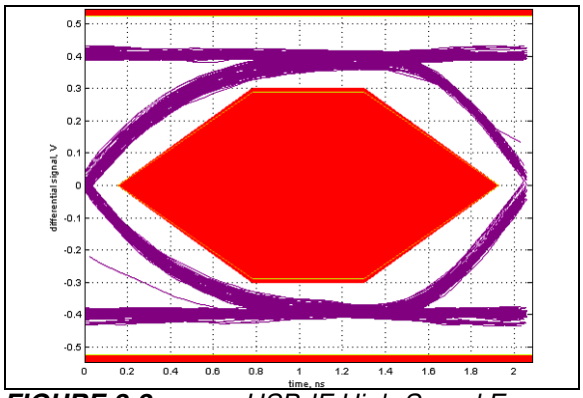

FIGURE 2-2: *USB-IF High-Speed Eye Diagram (With Data Switch).*

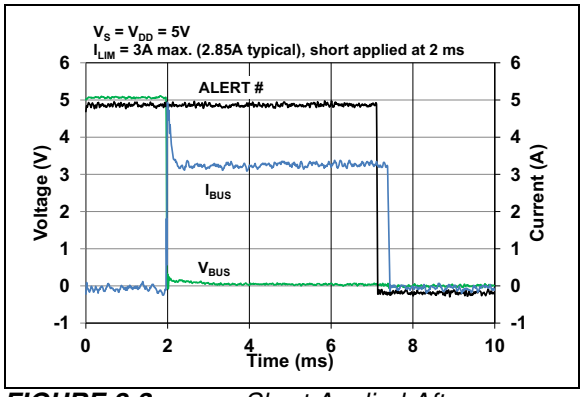

FIGURE 2-3: *Short Applied After Power-Up.*

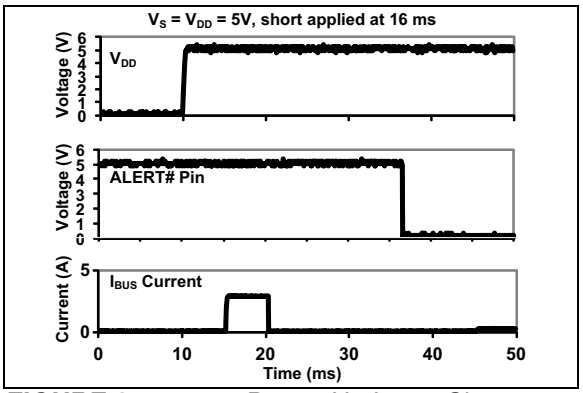

FIGURE 2-4: *Power-Up Into a Short.*

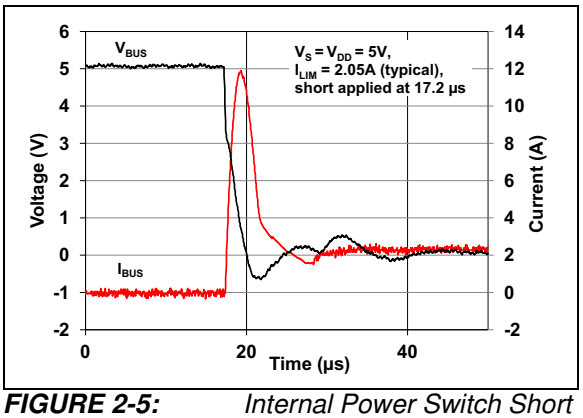

FIGURE 2-5: *Internal Power Switch Short Response.*

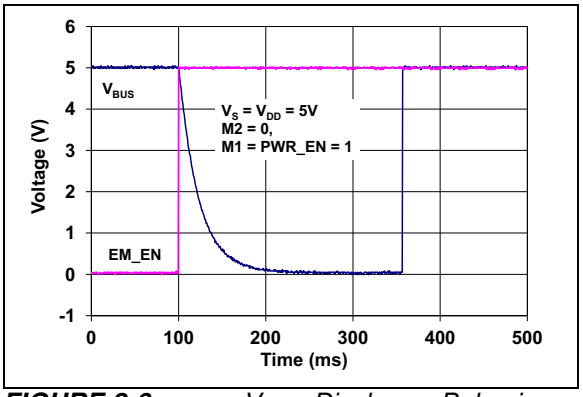

FIGURE 2-6: *V_{BUS} Discharge Behavior.*

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_J = +27°C$.

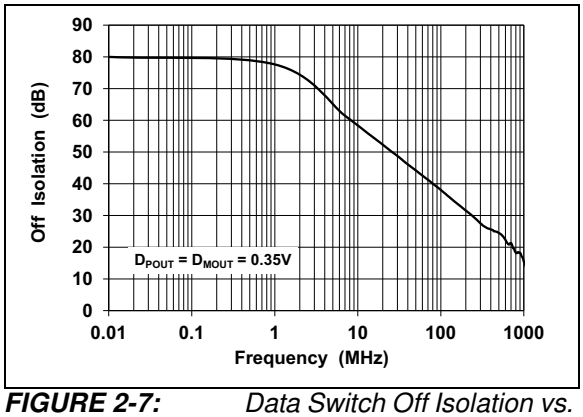

FIGURE 2-7: *Data Switch Off Isolation vs. Frequency.*

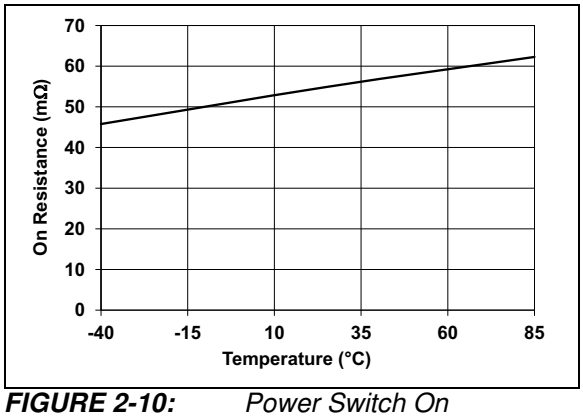

FIGURE 2-10: *Power Switch On Resistance vs. Temperature.*

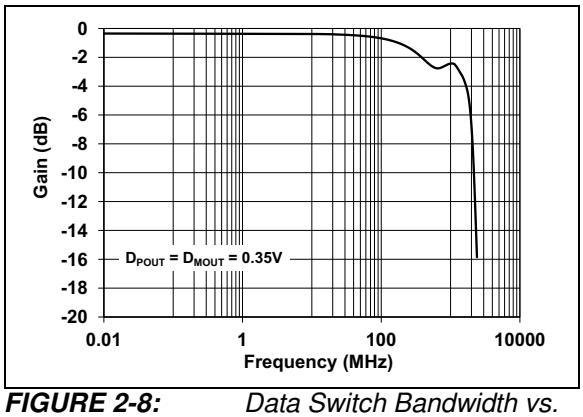

FIGURE 2-8: *Data Switch Bandwidth vs. Frequency.*

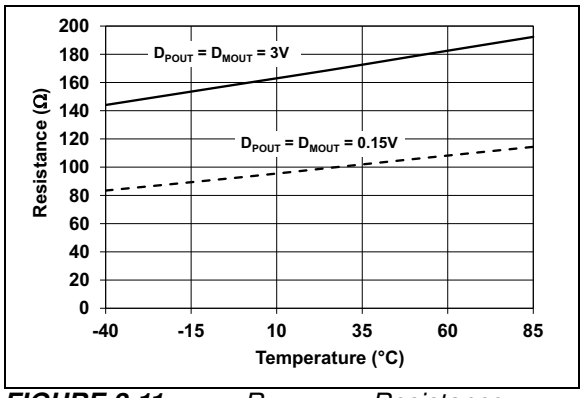

FIGURE 2-11: *R_{DCP_RES} Resistance vs.Temperature.*

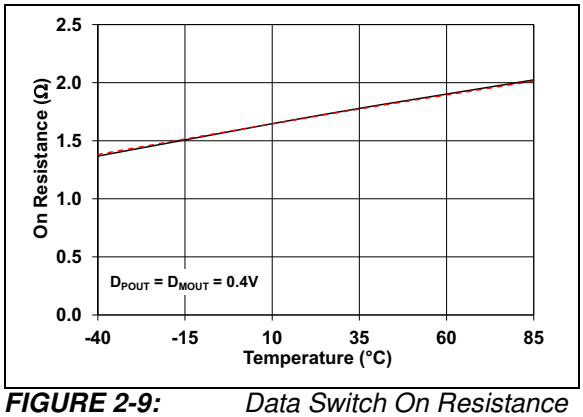

FIGURE 2-9: *Data Switch On Resistance vs. Temperature.*

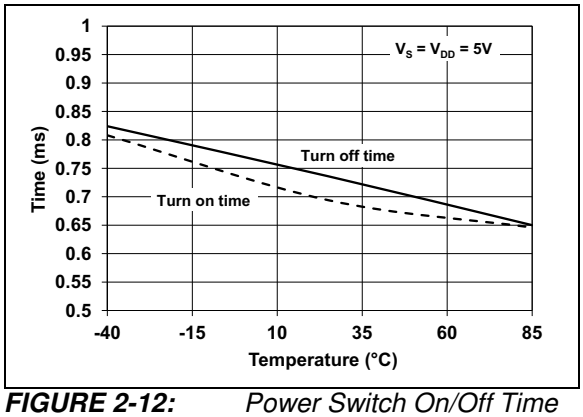

FIGURE 2-12: *Power Switch On/Off Time vs. Temperature.*

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_J = +27°C$.

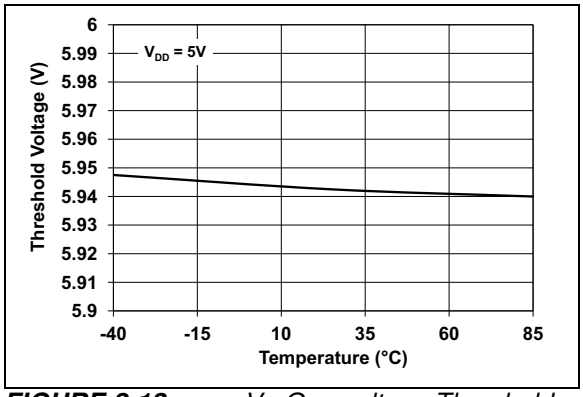

FIGURE 2-13: *V_S Overvoltage Threshold vs. Temperature.*

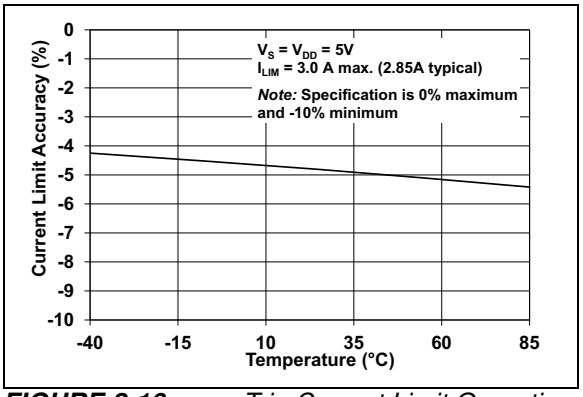

FIGURE 2-16: *Trip Current Limit Operation vs. Temperature.*

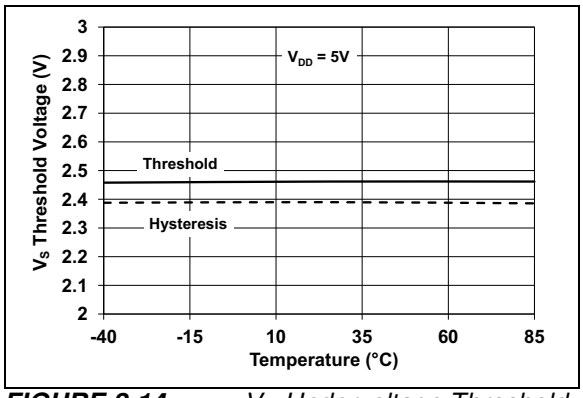

FIGURE 2-14: *V_S Undervoltage Threshold vs. Temperature.*

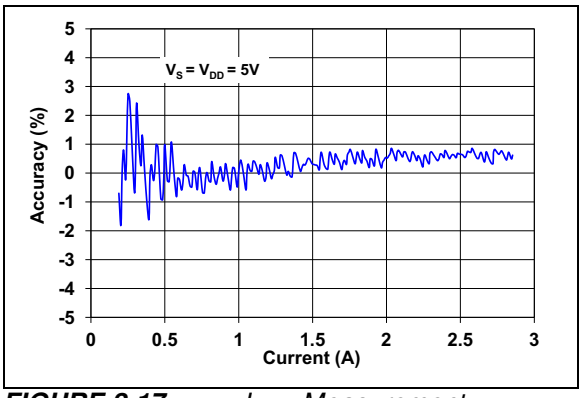

FIGURE 2-17: *I_{BUS} Measurement Accuracy.*

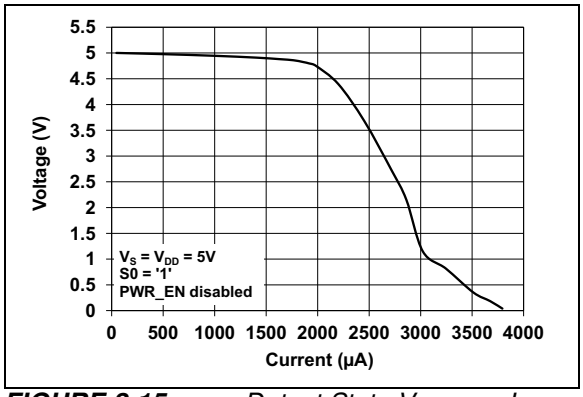

FIGURE 2-15: *Detect State V_{BUS} vs. I_{BUS}.*

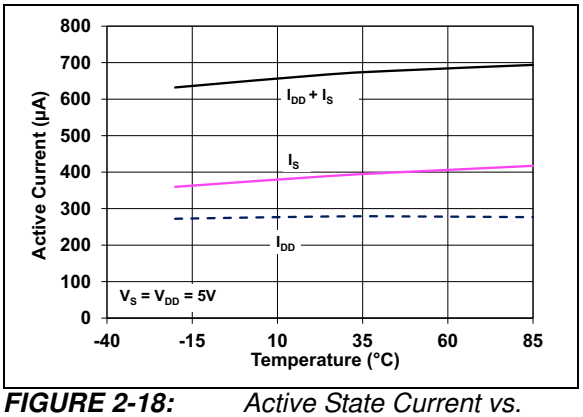

FIGURE 2-18: *Active State Current vs. Temperature.*

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_J = +27°C$.

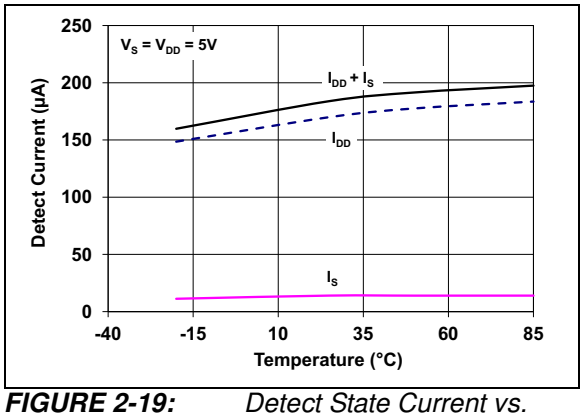

FIGURE 2-19: *Detect State Current vs. Temperature.*

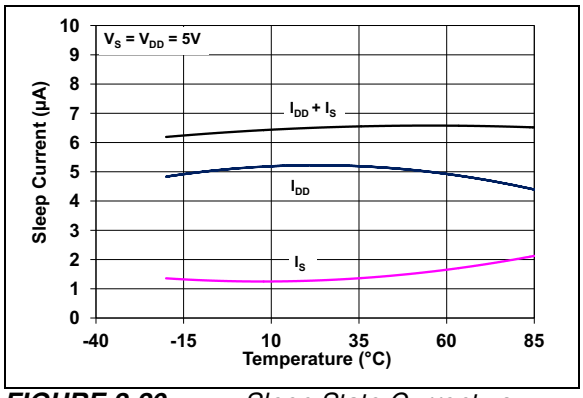

FIGURE 2-20: *Sleep State Current vs. Temperature.*

3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

UCS81003 5x5 VQFN	Symbol	Function	Pin Type	Connection Type if Pin Not Used
1	NC	Not internally connected	n/a	Leave open
2	M1	Active mode selector input #1	DI	Connect to ground or V_{DD} (see Note 3)
3	M2	Active mode selector input #2	DI	Connect to ground or V_{DD} (see Note 3)
4	V_{BUS1}	Voltage output from Power Switch. These pins are internally connected and must be tied together.	Hi-Power Note 1	Leave open
5	V_{BUS2}			
6	V_{BUS3}			
7	COMM_SEL/I_{LIM}	COMM_SEL - Selects SMBus or Stand-alone mode of operation (see Table 11-1).	AIO	n/a
		I_{LIM} - Selects the hardware current limit at power-up.		
8	SEL	Selects polarity of PWR_EN control and SMBus address (see Table 11-2).	AIO	n/a
9	V_{S1}	Voltage input to Power Switch. These pins are internally connected and must be tied together.	Hi-Power	Connect to ground
10	V_{S2}			
11	V_{S3}			
12	V_{DD}	Main power supply input for chip functionality	Power	n/a
13	PWR_EN	Port power switch enable input. Polarity determined by SEL pin.	DI	Connect to ground or V_{DD} (see Note 3)
14	NC	Not internally connected	n/a	Leave open
15	NC	Not internally connected	n/a	Leave open

Note 1: Total leakage current from pins 4, 5 and 6 (V_{BUS}) to ground must be less than 100 µA for proper attach/removal detection operation.

2: It is recommended to use 2 MΩ pull-down resistors on the D_{POUT} and/or D_{MOUT} pin if a portable device stimulus is expected when using the Customer Charger Emulation profile with the high-speed data switch open. The 2 MΩ value is based on BC1.1 impedance characteristics for Dedicated Charging Ports.

3: To ensure operation, the PWR_EN pin must be enabled, as determined by the SEL pin decode, when it is not driven by an external device. Furthermore, one of the M1, M2 or EM_EN pins must be connected to V_{DD} if all three are not driven from an external device. If the PWR_EN pin is disabled or all of the M1, M2 and EM_EN pins are connected to ground, the UCS81003 will remain in the Sleep or Detect state unless activated via the SMBus.

TABLE 3-1: PIN FUNCTION TABLE

UCS81003 5x5 VQFN	Symbol	Function	Pin Type	Connection Type if Pin Not Used
16	SMDATA/LATCH	**SMDATA** - SMBus data input/output (requires pull-up resistor)	DIOD	n/a
		LATCH - In Stand-Alone mode, Latch/Auto-recovery fault handling mechanism selection input (see **Section 7.5 "Fault Handling Mechanism"**)	DI	
17	SMCLK/S0	**SMCLK** - SMBus Clock Input (requires pull-up resistor)	DI	n/a
		S0 - In Stand-Alone mode, enables Attach/Removal Detection feature (see **Section 5.3.6 "S0 Input"**)		
18	ALERT#	Active low error event output flag (requires pull-up resistor)	OD	Connect to ground
19	D_{PIN}	USB data input (plus)	AIO	Connect to ground or ground through a resistor
20	D_{MIN}	USB data input (minus)	AIO	Connect to ground or ground through a resistor
21	NC	Not internally connected	n/a	Leave open
22	NC	Not internally connected	n/a	Leave open
23	D_{MOUT}	USB data output (minus)	AIO (see Note 2)	Connect to ground
24	D_{POUT}	USB data output (plus)	AIO (see Note 2)	Connect to ground
25	A_DET#	Active low device Attach Detection output flag (requires pull-up resistor)	OD	Connect to ground
26	EM_EN	Active mode selector input	DI	Connect to ground or V_{DD} (see Note 3)
27	GND	Ground	Power	n/a
28	NC	Not internally connected	n/a	Leave open
29	EP	Exposed Thermal Pad. Must be connected to the electrical ground.	EP	n/a

Note 1: Total leakage current from pins 4, 5 and 6 (V_{BUS}) to ground must be less than 100 µA for proper attach/removal detection operation.

2: It is recommended to use 2 MΩ pull-down resistors on the D_{POUT} and/or D_{MOUT} pin if a portable device stimulus is expected when using the Customer Charger Emulation profile with the high-speed data switch open. The 2 MΩ value is based on BC1.1 impedance characteristics for Dedicated Charging Ports.

3: To ensure operation, the PWR_EN pin must be enabled, as determined by the SEL pin decode, when it is not driven by an external device. Furthermore, one of the M1, M2 or EM_EN pins must be connected to V_{DD} if all three are not driven from an external device. If the PWR_EN pin is disabled or all of the M1, M2 and EM_EN pins are connected to ground, the UCS81003 will remain in the Sleep or Detect state unless activated via the SMBus.

TABLE 3-2: PIN TYPES DESCRIPTION

Pin Type	Description
Power	This pin is used to supply power or ground to the device
Hi-Power	This pin is a high-current pin
AIO	Analog Input/Output - this pin is used as an I/O for analog signals.
DI	Digital Input - this pin is used as a digital input. This pin will be glitch-free.
DIOD	Open-Drain Digital Input/Output - this pin is bidirectional. It is open-drain and requires a pull-up resistor. This pin will be glitch-free.
OD	Open-Drain Digital Output - used as a digital output. It is open-drain and requires a pull-up resistor. This pin will be glitch-free.
EP	Exposed Thermal Pad

4.0 TERMS AND ABBREVIATIONS

Note: The M1, M2, PWR_EN and EM_EN pins each have configuration bits (<pin name>_SET in **Section 10.4.3 "Switch Configuration Register"**) that may be used to perform the same function as the external pin state. These bits are accessed via the SMBus/I^2C and are OR'd with the respective pin. This OR'd combination of pin state and register bit is referenced as the <pin name> control.

TABLE 4-1: TERMS AND ABBREVIATIONS

Term/Abbreviation	Description
Active mode	Active power state operation mode: Data Pass-through, BC1.2 SDP, BC1.2 CDP, BC1.2 DCP or Dedicated Charger Emulation Cycle.
Attach Detection	An Attach Detection event occurs when the current drawn by a portable device is greater than I_{DET_QUAL} for longer than t_{DET_QUAL}.
Attachment	The physical insertion of a portable device into a USB port that UCS81003 is controlling.
CC	Constant Current
CDM	Charged Device Model. JEDEC® model for characterizing susceptibility of a device to damage from ESD.
CDP or USB-IF BC1.2 CDP	Charging Downstream Port. The combination of the UCS81003 CDP handshake and an active standard USB host comprises a CDP. This enables a BC1.2 compliant portable device to simultaneously draw current up to 1.5A while data communication is active. The USB high-speed data switch is closed in this mode.
Charge Enable	When a charger emulation profile has been accepted by a portable device and charging commences.
Charger Emulation Profile	Representation of a charger comprised of D_{POUT}, D_{MOUT} and V_{BUS} signaling, which make up a defined set of signatures or handshaking protocols.
Connection	USB-IF term which refers to establishing active USB communications between a USB host and a USB device.
Current Limiting Mode	Determines the action that is performed when the I_{BUS} current reaches the I_{LIM} threshold. Trip opens the port power switch. Constant Current (variable slope) allows V_{BUS} to be dropped by the portable device.
DCE	Dedicated Charger Emulation. Charger emulation in which the UCS81003 can deliver power only (by default). No active USB data communication is possible when charging in this mode (by default).
DCP or USB-IF BC1.2 DCP	Dedicated Charging Port. This functions as a dedicated charger for a BC1.2 portable device. This allows the portable device to draw currents up to 1.5A with Constant Current Limiting (and beyond 1.5A with Trip Current Limiting). No USB communications are possible (by default).
DC	Dedicated Charger. A charger which inherently does not have USB communications, such as an A/C wall adapter.
Disconnection	USB-IF term which refers to the loss of active USB communications between a USB host and a USB device.
Dynamic Thermal Management	The UCS81003 automatically adjusts port power switch limits and modes to lower internal power dissipation when the thermal regulation temperature value is approached.
Enumeration	A USB-specific term indicating that a host is detecting and identifying USB devices.
Handshake	Application of a charger emulation profile that requires a response. Two-way communication between the UCS81003 and the portable device.
HBM	Human Body Model
HSW	High-Speed switch
I_{BUS_R2MIN}	Current limiter mode boundary

TABLE 4-1: TERMS AND ABBREVIATIONS (CONTINUED)

Term/Abbreviation	Description
I_{LIM}	The I_{BUS} current threshold used in current limiting. In Trip mode, when I_{LIM} is reached, the port power switch is opened. In Constant Current mode, when the current exceeds I_{LIM}, operation continues at a reduced voltage and increased current; if V_{BUS} voltage drops below V_{BUS_MIN}, the port power switch is opened.
Legacy	USB devices that require non-BC1.2 signatures be applied on the D_{POUT} and D_{MOUT} pins to enable charging.
OCL	Overcurrent limit
POR	Power-on Reset
Portable Device	USB device attached to the USB port.
Power Thief	A USB device that does not follow the handshaking conventions of a BC1.2 device or Legacy devices and draws current immediately upon receiving power (i.e., a USB book light, portable fan, etc).
Removal Detection	A Removal Detection event occurs when the current load on the V_{BUS} pin drops to less than I_{REM_QUAL} for longer than t_{REM_QUAL}.
Removal	The physical removal of a portable device from a USB port that the UCS81003 is controlling.
Response	An action, usually in response to a stimulus, in charger emulation performed by the UCS81003 device via the USB data lines.
SDP or USB-IF SDP	Standard downstream port. The combination of the UCS81003 high-speed switch being closed with an upstream USB host present comprises a BC1.2 SDP. This enables a BC1.2 compliant portable device to simultaneously draw current up to 0.5A while data communication is active.
Signature	Application of a charger emulation profile without waiting for a response. One-way communication from the UCS81003 to the portable device.
Stand-Alone Mode	Indicates that the communications protocol is not active and all communications between the UCS81003 and a controller are done via the external pins only (M1, M2, EM_EN, PWR_EN, S0 and LATCH as inputs, and ALERT# and A_DET# as outputs).
Stimulus	An event in charger emulation detected by the UCS81003 device via the USB data lines.

5.0 GENERAL DESCRIPTION

The UCS81003 provides a single USB port power switch for precise control of up to 3.0A continuous current with overcurrent limit (OCL), dynamic thermal management, latch or auto-recovery fault handling, selectable active-low or -high enable, under and overvoltage lockout, and back-voltage protection.

Split supply support for V_{BUS} and V_{DD} is an option for low power in system standby states.

In addition to power switching and current limiting, the UCS81003 provides automatic and configurable charger emulation profiles to charge a wide variety of portable devices, including USB-IF BC1.2 (CDP or DCP modes), YD/T-1591 (2009), 12W charging, most Apple and RIM portable devices and many others.

The UCS81003 also provides current monitoring to allow intelligent management of system power and charge rationing for controlled delivery of current regardless of the host power state. This is especially important for battery-operated applications that need to provide power without excessively draining the battery, or that require power allocation depending on application activities.

Figure 5-1 shows a UCS81003 full-featured system configuration in which the UCS81003 provides a port power switch and low-power Attach Detection with wake-up signaling (wake on USB). The current limit is established at power-up. It can be lowered if required after power-up via the SMBus/I^{2}C. This configuration also provides configurable USB data line-charger emulation, programmable current limiting (as determined by the accepted charger emulation profile), active current monitoring and port charge rationing.

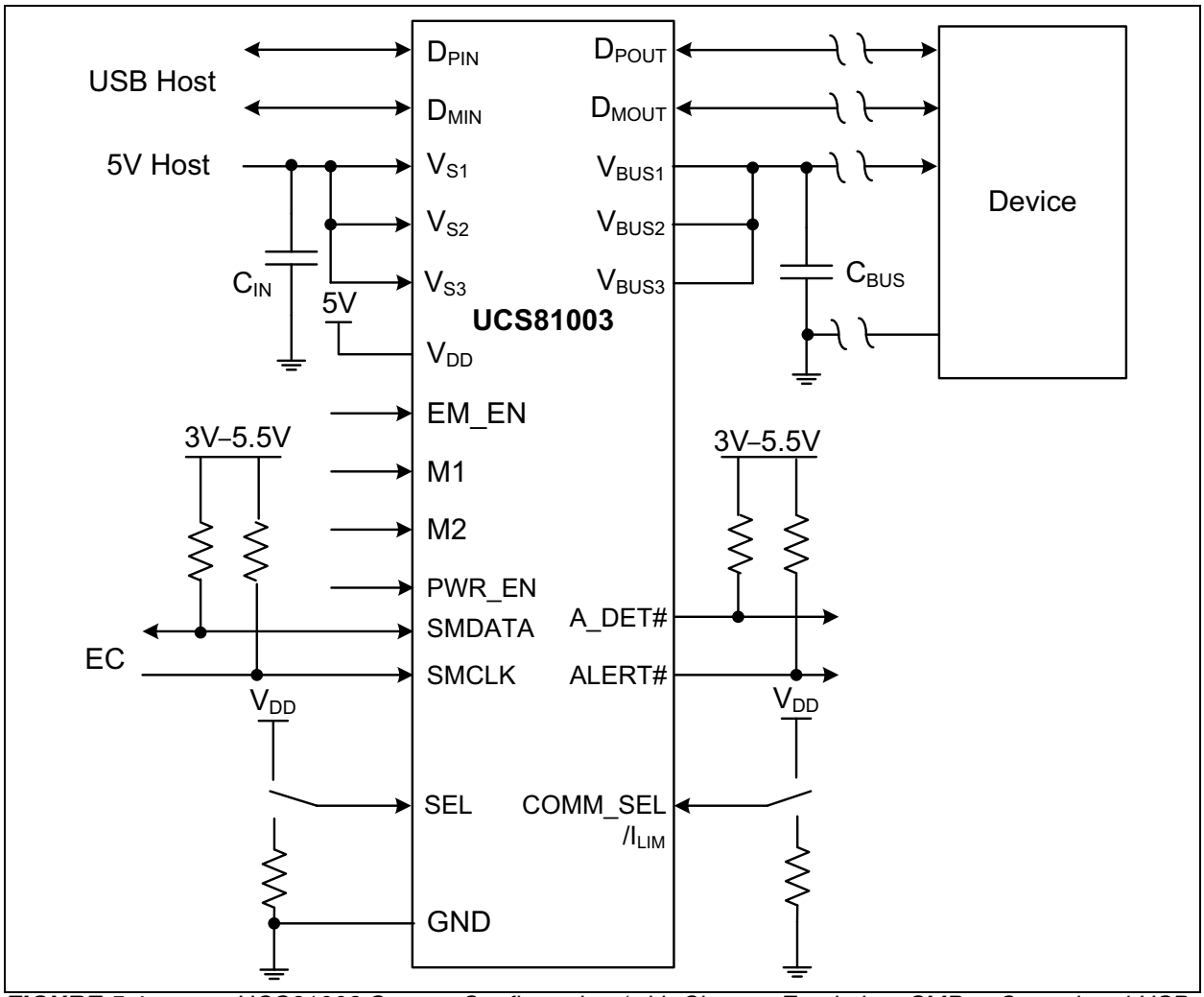

FIGURE 5-1: *UCS81003 System Configuration (with Charger Emulation, SMBus Control and USB Host).*

Figure 5-2 shows a system configuration in which the UCS81003 provides a USB data switch, port power switch, low-power Attach Detection and portable device Attach/Removal Detection signaling. This configuration does not include configurable data line charger emulation, programmable current limiting or current monitoring and rationing.

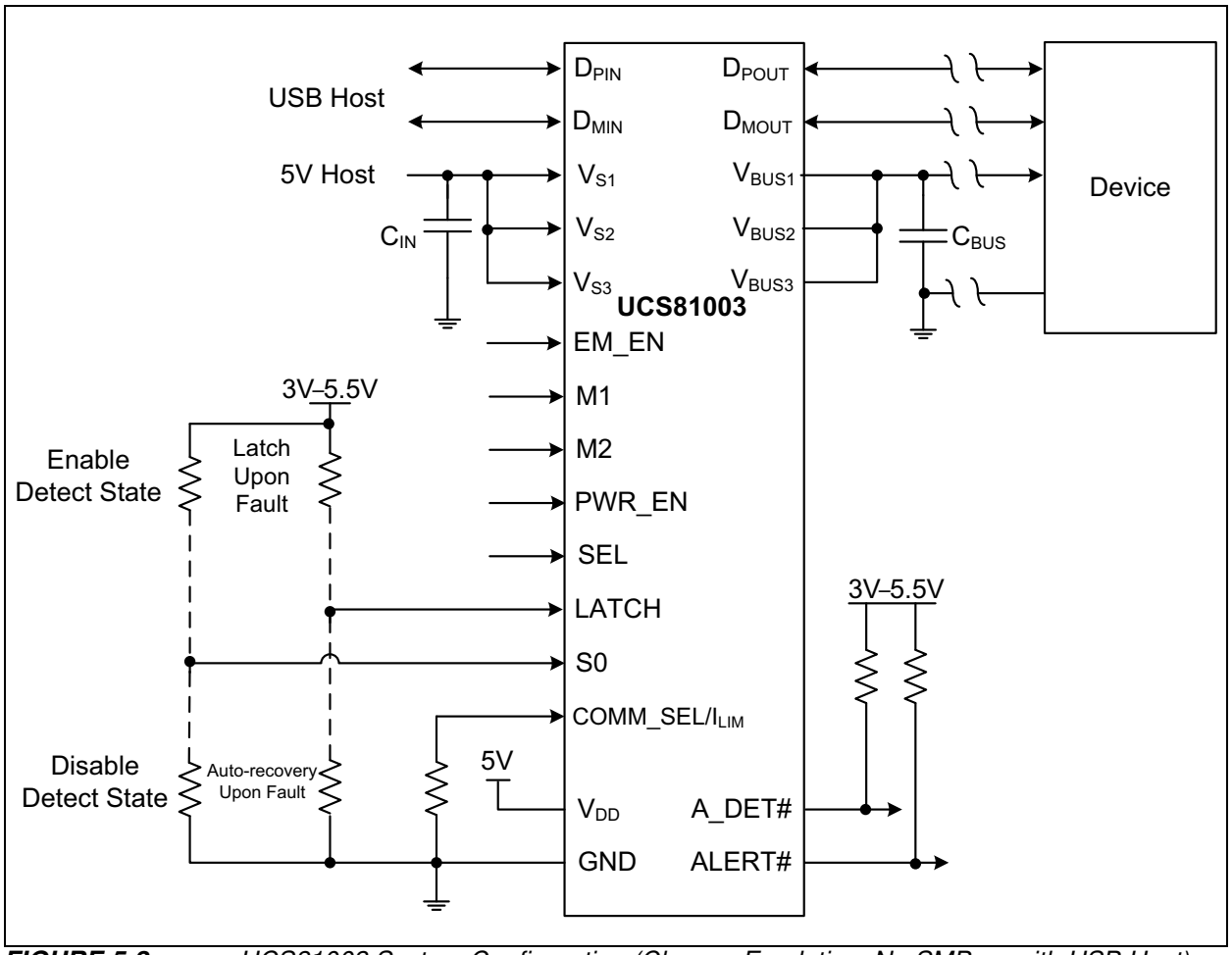

FIGURE 5-2: *UCS81003 System Configuration (Charger Emulation, No SMBus, with USB Host).*

Figure 5-3 shows a system configuration in which the UCS81003 provides a port power switch, low-power Attach Detection and portable device attachment detected signaling. This configuration is useful for applications that already provide USB BC1.2 and/or legacy data line handshaking on the USB data lines, but still require port power switching and current limiting.

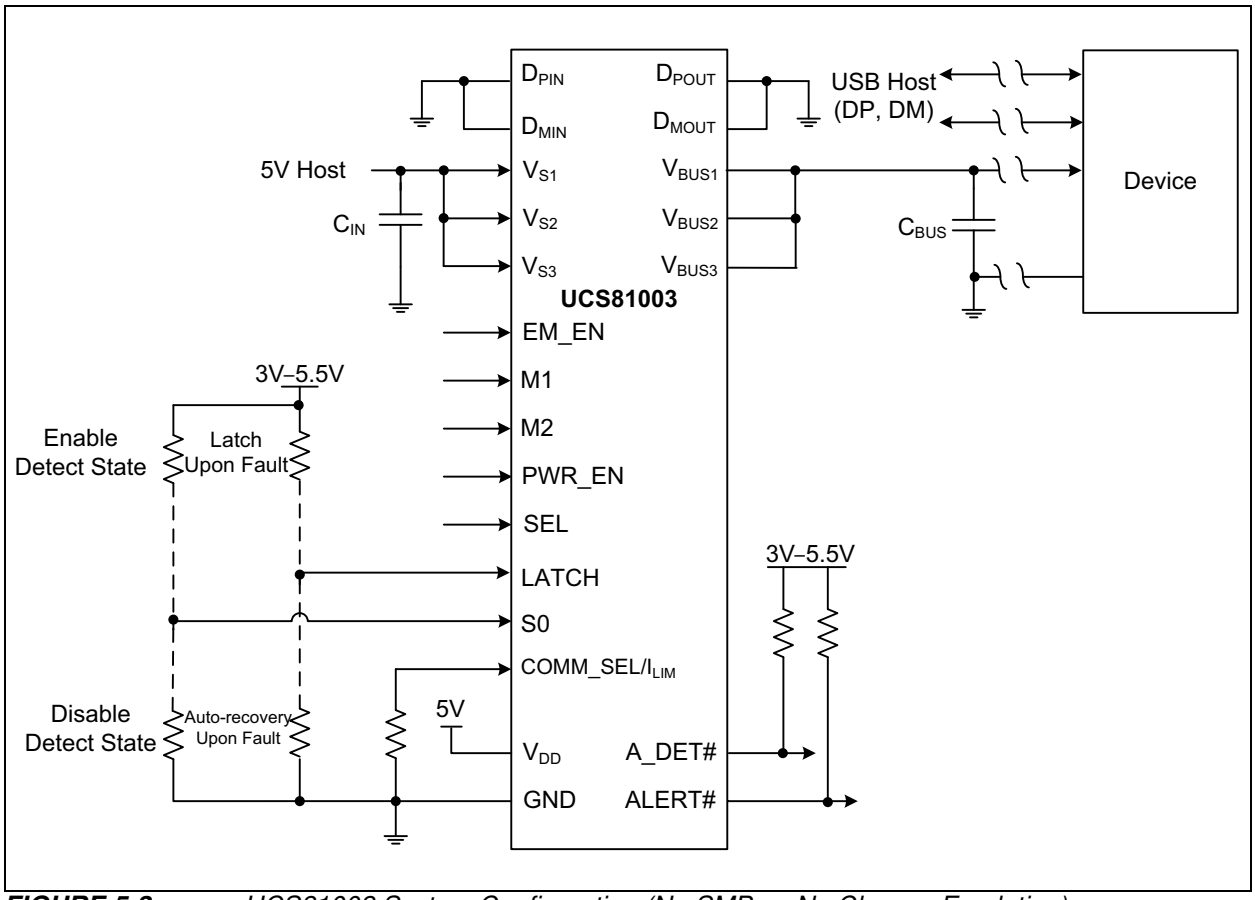

FIGURE 5-3: *UCS81003 System Configuration (No SMBus, No Charger Emulation).*