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BITSTREAM CONVERSION

UDA1338H

Multichannel audio coder-decoder

Rev. 04 — 18 May 2010 Product data sheet

1. General description

The UDA1338H is a single-chip consisting of 4 plus 1 analog-to-digital converters and 6 digital-to-analog converters with signal processing features employing bitstream conversion techniques. The multichannel configuration makes the device eminently suitable for use in digital audio equipment which incorporates surround feature.

The UDA1338H supports conventional 2 channels per line data transfer conformable to the I^2S-bus format with word lengths of up to 24 bits, the MSB-justified format with word lengths of up to 24 bits and the LSB-justified format with word lengths of 16 bits, 20 bits and 24 bits, as well as 4 to 6 channels per line transfer mode. The device also supports a combination of the MSB-justified output format and the LSB-justified input format. The UDA1338H has special sound processing features in the Direct Stream Digital (DSD) playback mode, de-emphasis, volume and mute which can be controlled via the L3-bus or I^2C-bus interface.

2. Features and benefits

2.1 General

- 2.7 V to 3.6 V power supply
- 5 V tolerant digital inputs
- 24-bit data path
- Selectable control: via L3-bus or I^2C-bus microcontroller interface
- Supports sample frequency ranges for:
  - Audio ADC: f_s = 16 kHz to 100 kHz
  - Voice ADC: f_s = 7 kHz to 50 kHz
  - Audio DAC: f_s = 16 kHz to 200 kHz
- Separate power control for ADC and DAC
- ADC plus integrated high-pass filter to cancel DC offset
- Integrated digital filter plus DAC
- Slave mode only applications
- Easy application

2.2 Multiple format data interface

- Audio interface supports standard I²S-bus, MSB-justified, LSB-justified and two multichannel formats
- Voice interface supports I²S-bus and mono channel formats

2.3 Digital sound processing

- Control via L3-bus or I²C-bus:
  - Channel independent digital logarithmic volume
  - Digital de-emphasis for f_s = 32 kHz, 44.1 kHz, 48 kHz or 96 kHz
  - Soft or quick mute
  - Output signal polarity control

2.4 Advanced audio configuration

- Inputs:
  - 4 single-ended audio inputs (2 × stereo) with programmable gain amplifiers
  - 1 single-ended voice input
- Outputs:
  - 6 differential audio outputs (3 × stereo)
- DSD mode to support stereo DSD playback
- High linearity, wide dynamic range and low distortion
- DAC digital filter with selectable sharp or soft roll-off

3. Applications

- Excellently suitable for multichannel home audio-video application

4. Quick reference data

Table 1: Quick reference data

V_{DDD} = $V_{DDA(AD)}$ = $V_{DDA(DA)}$ = 3.3 V; T_{amb} = 25 °C; R_L = 22 kΩ; all voltages referenced to ground (pins V_{SS}); unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supplies						
$V_{DDA(AD)}$	ADC analog supply voltage		2.7	3.3	3.6	V
$V_{DDA(DA)}$	DAC analog supply voltage		2.7	3.3	3.6	V
V_{DDD}	digital supply voltage		2.7	3.3	3.6	V
$I_{DDA(AD)}$	ADC analog supply current	f_{ADC} = 48 kHz	-	30	-	mA
$I_{DDA(DA)}$	DAC analog supply current	f_{DAC} = 48 kHz	-	20	-	mA
I_{DDD}	digital supply current	f_{ADC} = f_{DAC} = 48 kHz; f_{VOICE} = 48 kHz	-	31	-	mA

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Table 1: Quick reference data *...continued*

V_{DDD} = $V_{DDA(AD)}$ = $V_{DDA(DA)}$ = 3.3 V; T_{amb} = 25 °C; R_L = 22 kΩ; all voltages referenced to ground (pins V_{SS}); unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
$I_{DDD(pd)}$	digital supply current in Power-down mode	audio and voice ADCs power-down		-	18	-	mA
		DAC power-down		-	14	-	mA
T_{amb}	ambient temperature			−20	-	+85	°C
Audio analog-to-digital converter							
D_0	digital output level	at 0 dB setting; 900 mV (RMS) input	[1][2]	−2.5	−1.2	−0.7	dB
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	at −1 dBFS		-	−90	−83	dB
		at −60 dBFS; A-weighted		-	−40	−34	dB
S/N	signal-to-noise ratio	code = 0; A-weighted		94	100	-	dB
α_{cs}	channel separation			-	100	-	dB
Digital-to-analog converter							
Differential mode							
$V_{o(rms)}$	output voltage (RMS value)	at 0 dBFS digital input		1.9	2.0	2.1	V
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dBFS		-	−100	−93	dB
		at −60 dBFS; A-weighted		-	−50	−45	dB
S/N	signal-to-noise ratio	code = 0; A-weighted		107	114	-	dB
α_{cs}	channel separation			-	117	-	dB
Single-ended mode							
$V_{o(rms)}$	output voltage (RMS value)	at 0 dBFS digital input		-	1.0	-	V
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dBFS		-	−90	-	dB
		at −60 dBFS; A-weighted		-	−45	-	dB
S/N	signal-to-noise ratio	code = 0; A-weighted		-	110	-	dB
α_{cs}	channel separation			-	114	-	dB

[1] The input voltage can be up to 2 V (RMS) when the current through the ADC input pin is limited to approximately 1 mA by using a series resistor.

[2] The input voltage to the ADC scales proportionally with the power supply voltage.

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
UDA1338H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

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6. Block diagram

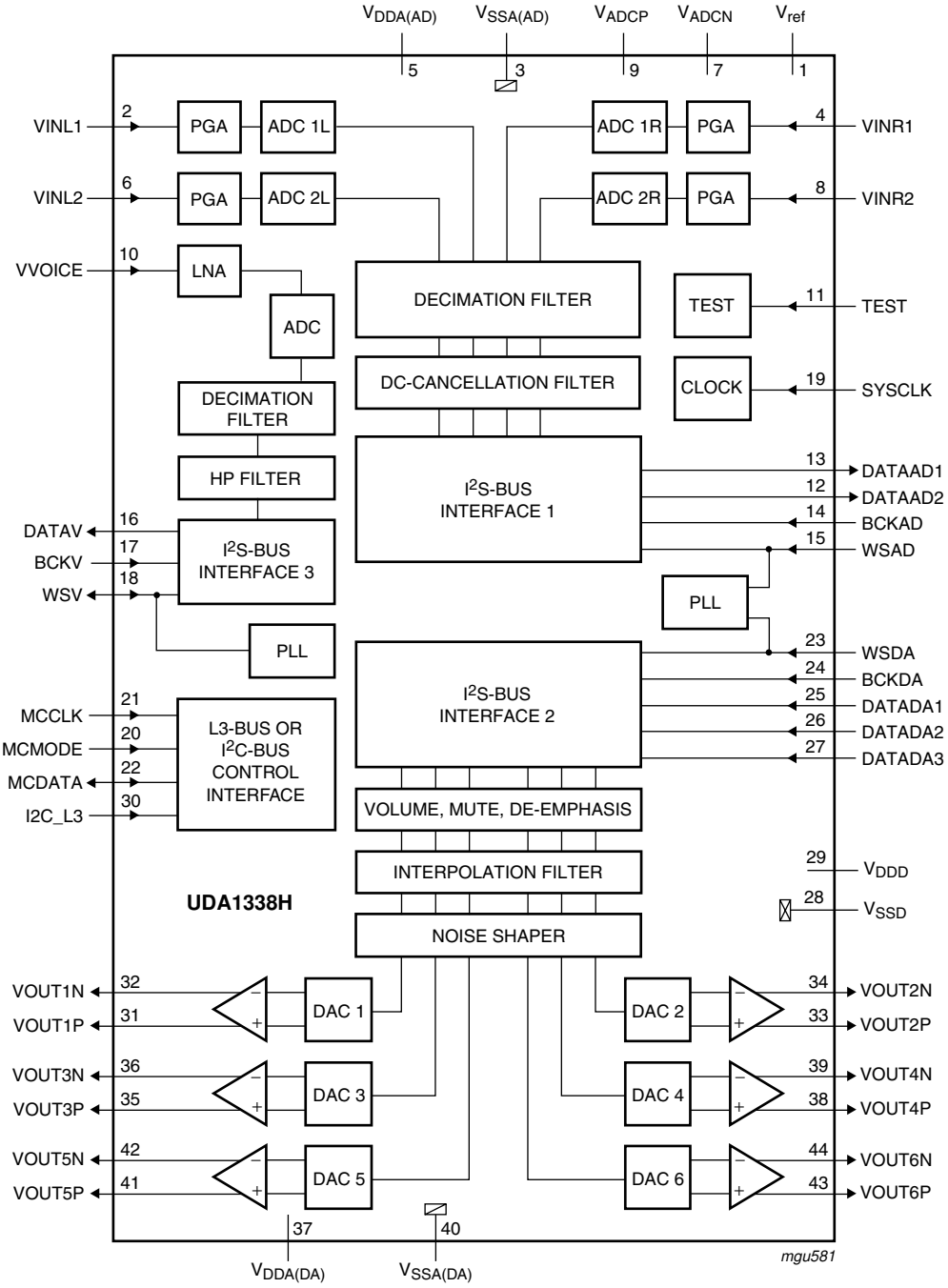

Fig 1. Block diagram

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7. Pinning information

7.1 Pinning

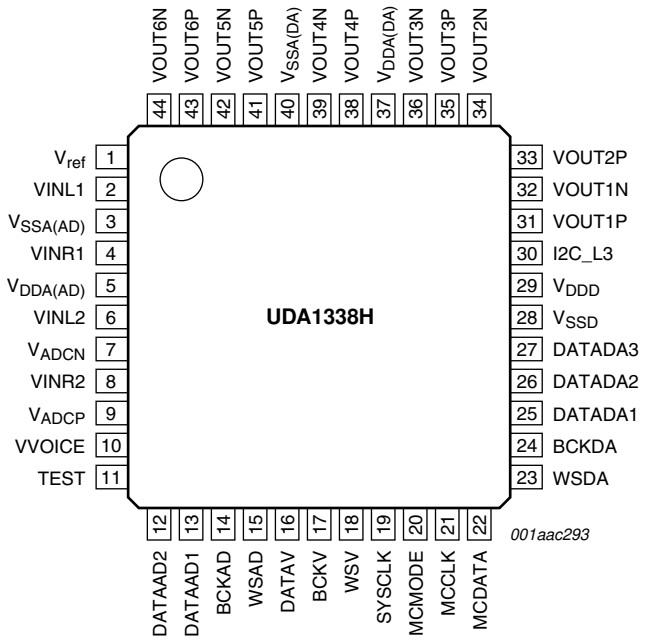

Fig 2. Pin configuration

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Type[1]	Description
V_{ref}	1	AIO	ADC reference voltage
VINL1	2	AIO	ADC 1 input left
$V_{SSA(AD)}$	3	AGND	ADC analog ground
VINR1	4	AIO	ADC 1 input right
$V_{DDA(AD)}$	5	AS	ADC analog supply voltage
VINL2	6	AIO	ADC 2 input left
V_{ADCN}	7	AIO	ADC reference voltage N
VINR2	8	AIO	ADC 2 input right
V_{ADCP}	9	AIO	ADC reference voltage P
VVOICE	10	AIO	voice ADC input
TEST	11	DID	test input; must be connected to digital ground (V_{SSD}) in application
DATAAD2	12	DO	ADC 2 data output
DATAAD1	13	DO	ADC 1 data output
BCKAD	14	DIS	ADC bit clock input
WSAD	15	DI	ADC word select input

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Table 3: Pin description *...continued*

Symbol	Pin	Type[1]	Description
DATAV	16	DO	voice data output
BCKV	17	DIS	voice bit clock input
WSV	18	DIO	voice word select input or output
SYSCLK	19	DIS	system clock input: $256f_s$, $384f_s$, $512f_s$ or $768f_s$
MCMODE	20	DI	L3-bus L3MODE input or I^2C-bus DAC mute control input
MCCLK	21	DIS	L3-bus L3CLOCK input or I^2C-bus SCL input
MCDATA	22	IIC	L3-bus L3DATA input and output or I^2C-bus SDA input and output
WSDA	23	DI	DAC word select input
BCKDA	24	DIS	DAC bit clock input
DATADA1	25	DI	DAC channel 1 and channel 2 data input
DATADA2	26	DI	DAC channel 3 and channel 4 data input
DATADA3	27	DI	DAC channel 5 and channel 6 data input
V_{SSD}	28	DGND	digital ground
V_{DDD}	29	DS	digital supply voltage
I2C_L3	30	DI	selection input for L3-bus or I^2C-bus control
VOUT1P	31	AIO	DAC 1 positive output
VOUT1N	32	AIO	DAC 1 negative output
VOUT2P	33	AIO	DAC 2 positive output
VOUT2N	34	AIO	DAC 2 negative output
VOUT3P	35	AIO	DAC 3 positive output
VOUT3N	36	AIO	DAC 3 negative output
$V_{DDA(DA)}$	37	AS	DAC analog supply voltage
VOUT4P	38	AIO	DAC 4 positive output
VOUT4N	39	AIO	DAC 4 negative output
$V_{SSA(DA)}$	40	AGND	DAC analog ground
VOUT5P	41	AIO	DAC 5 positive output
VOUT5N	42	AIO	DAC 5 negative output
VOUT6P	43	AIO	DAC 6 positive output
VOUT6N	44	AIO	DAC 6 negative output

[1] See Table 4.

Table 4: Pin types

Type	Description
AGND	analog ground
AIO	analog input and output
AS	analog supply
DGND	digital ground
DI	digital input
DID	digital input with internal pull-down resistor
DIO	digital input and output

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Table 4: Pin types *...continued*

Type	Description
DIS	digital Schmitt-triggered input
DO	digital output
DS	digital supply
IIC	input and open-drain output for I^2C-bus

8. Functional description

8.1 System clock

The UDA1338H operates in slave mode only; this means that in all applications the system must provide either the system clock (the bit clock for the voice ADC) or the word clock.

The audio ADC part, the voice ADC part and the DAC part can operate at different sampling frequencies (DAC-WS and ADC-WS modes) as well as a common frequency (SYSCLK, WSDA and DSD modes).

The voice ADC part supports a sampling frequency up to 50 kHz and the audio ADC supports a sampling frequency up to 100 kHz. The DAC sampling frequency range is extended up to 200 kHz with the range above 100 kHz being supported through 192 kHz sampling mode, which halves the oversampling ratio of SYSCLK and internal clocks.

The mode of operation of the audio and voice channels can be set via the L3-bus or I^2C-bus microcontroller interface and are summarized in and Table 6.

When applied, the system clock must be locked in frequency to the corresponding digital interface clocks.

The voice ADC part can either receive or generate the WSV signal as shown in Table 6.

Table 5: Audio ADC and DAC operating clock mode

Mode	Audio ADC		Audio DAC	
	Clock	Frequency	Clock	Frequency
SYSCLK	SYSCLK	$256f_s$, $384f_s$, $512f_s$ or $768f_s$	SYSCLK	$256f_s$, $384f_s$, $512f_s$ or $768f_s$
			SYSCLK	$128f_s$, $192f_s$, $256f_s$ or $384f_s$; 192 kHz sampling mode
DAC-WS	SYSCLK	$256f_s$, $384f_s$, $512f_s$ or $768f_s$	WSDA	$1f_s$
ADC-WS	WSAD	$1f_s$	SYSCLK	$256f_s$, $384f_s$, $512f_s$ or $768f_s$
			SYSCLK	$128f_s$, $192f_s$, $256f_s$ or $384f_s$; 192 kHz sampling mode
WSDA	WSDA	$1f_s$	WSDA	$1f_s$
DSD	SYSCLK	44.1 kHz × 512	SYSCLK	44.1 kHz × 512

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Table 6: Voice ADC operating clock mode

Mode	Voice ADC	
	Bit clock frequency (BCKV)	Word select (WSV)
WSV-in	input: $32f_s$, $64f_s$, $128f_s$ or $256f_s$	input
WSV-out	input: $32f_s$, $64f_s$, $128f_s$ or $256f_s$	output

8.2 Audio analog-to-digital converter (audio ADC)

The audio analog-to-digital front-end of the UDA1338H consists of 4-channel single-ended Adds with programmable gain stage (from 0 dB to 24 dB with 3 dB steps), controlled via the microcontroller interface. Using the PGA feature, it is possible to accept an input signal of 900 mV (RMS) or 1.8 V (RMS) if an external resistor of 10 kΩ is used in series. The schematic of audio ADC front-end is shown in Figure 3.

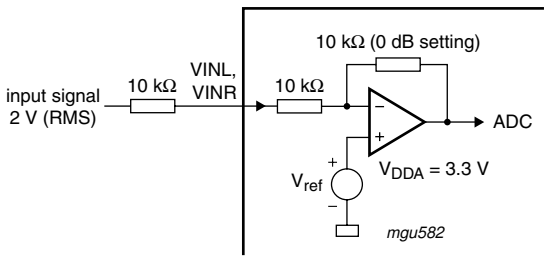

Fig 3. Schematic of audio ADC front-end

8.3 Voice analog-to-digital converter (voice ADC)

The voice analog-to-digital front-end of the UDA1338H consists of a single-channel single-ended ADC with a fixed gain (26 dB) Low Noise Amplifier (LNA). Together with the digital variable gain amplification stage, the voice ADC provides optimal processing and reproduction of the microphone signal. The supported sampling frequency range is from 7 kHz to 50 kHz. Power-down of the LNA and the ADC can be controlled separately.

8.4 Decimation filter of audio ADC

The decimation from $64f_s$ is performed in two stages. The first stage realizes $\left(\frac{\sin x}{x}\right)^4$ characteristics with a decimation factor of 8. The second stage consists of three half-band filters, each decimating by a factor of 2. The filter characteristics are shown in Table 7.

Table 7: Decimation filter characteristics (audio ADC)

Item	Condition	Value (dB)
Pass-band ripple	0 to $0.45f_s$	±0.01
Pass-band droop	$0.45f_s$	−0.2
Stop band	$>0.55f_s$	−70
Dynamic range	0 to $0.45f_s$	>135

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8.5 Decimation filter of voice ADC

The voice ADC decimation filter is realized with the combination of a Finite Impulse Response (FIR) filter and Infinite Impulse Response (IIR) filter for shorter group delay. The filter characteristics are shown in Table 8. During the power-on sequence, the output of the ADC is hard muted for a certain period. This hard-mute time can be chosen between 1024 and 2048 samples.

Table 8: Decimation filter characteristics (voice ADC)

Item	Condition	Value (dB)
Pass-band ripple	0 to 0.45f_s	±0.05
Pass-band droop	0.45f_s	−0.2
Stop band	>0.55f_s	−65
Dynamic range	0 to 0.45f_s	>110

8.6 Interpolation filter of DAC

The digital interpolation filter interpolates from 1f_s to 128f_s (or to 64f_s in the 192 kHz sampling mode) by cascading FIR filters, and has two sets of filter coefficients for sharp and slow roll-off as given in Table 9 and Table 10.

Table 9: Interpolation filter characteristics (sharp roll-off)

Item	Condition	Value (dB)
Pass-band ripple	0 to 0.45f_s	±0.002
Stop band	> 0.55f_s	−75
Dynamic range	0 to 0.45f_s	> 135

Table 10: Interpolation filter characteristics (slow roll-off)

Item	Condition	Value (dB)
Pass-band ripple	0 to 0.22f_s	±0.002
Pass-band droop	0.45f_s	−3.1
Stop band	> 0.78f_s	−94
Dynamic range	0 to 0.22f_s	> 135

8.7 Noise shaper of DAC

The 3rd-order noise shaper operates at either 128f_s or 64f_s (in the 192 kHz sampling mode), and converts the 24-bit input signal into a 5-bit signal stream. The noise shaper shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved.

8.8 Digital mixer

The UDA1338H has 6 digital mixers inside the interpolator; see Figure 4. The ADC signals can be mixed with the I^2S-bus input signals. The mixing of the ADC signals can be selected by the bits MIX[1:0].

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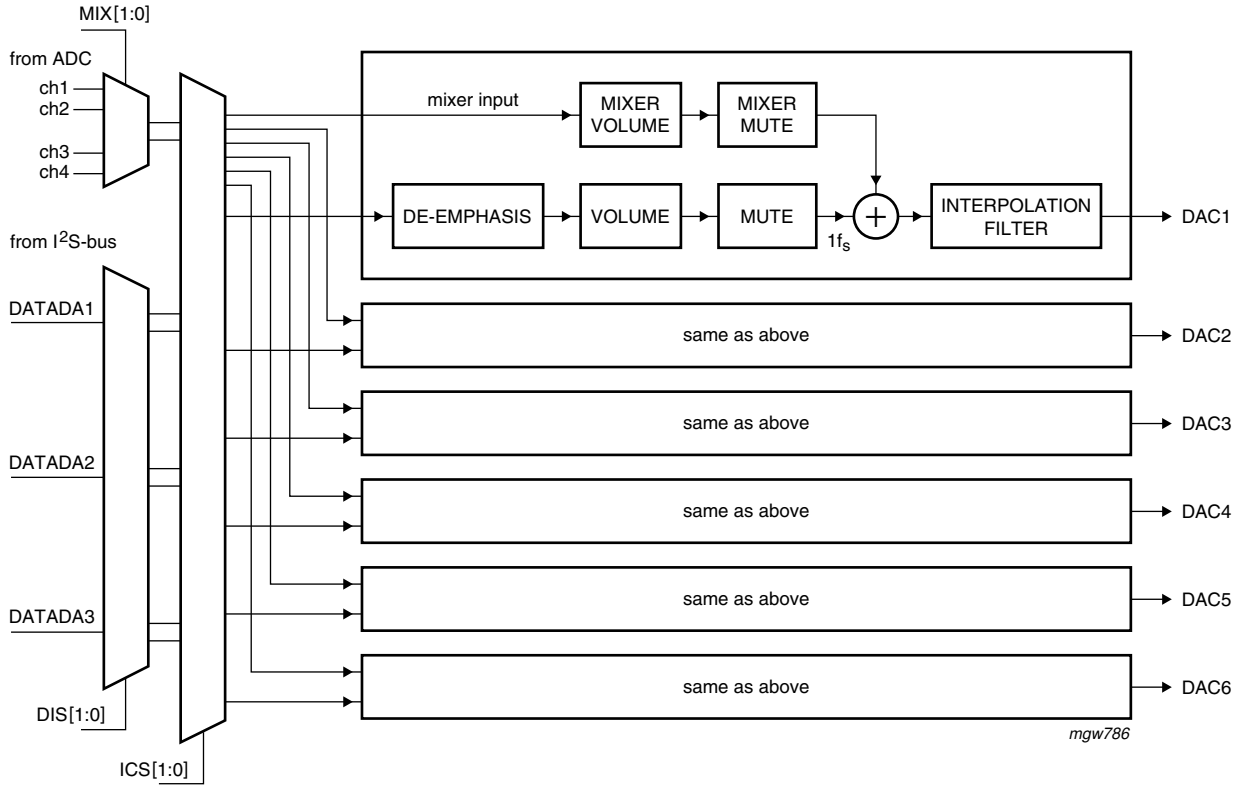

Fig 4. Block diagram of DAC mixer

8.9 Audio digital-to-analog converters

The audio digital-to-analog front-end of the UDA1338H consists of 6-channel differential SDACs: an SDAC is a multi-bit DAC based upon switched resistors. To minimize data dependent modulation effects, a Dynamic Element Matching (DEM) algorithm scrambler circuit and DC current compensation circuit are implemented with the SDAC.

8.10 Power-on reset

The UDA1338H has an internal power-on reset circuit which initializes the device; see Figure 5. All the digital sound processing features and the system controlling features are set to their default values in the L3-bus and the I²C-bus modes.

The reset time (see Figure 6) is determined by an external capacitor which is connected between pin V_{ref} and ground. The reset time should be at least 250 μs for $V_{ref} < 1.25$ V. When $V_{DDA(AD)}$ is switched off, the device will be reset again for $V_{ref} < 0.75$ V.

During the reset time, the system clock should be running.

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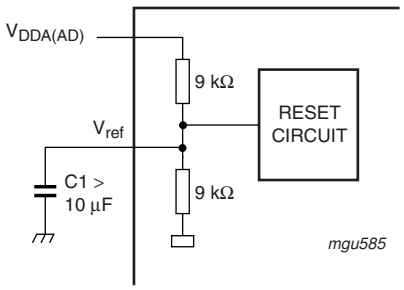

Fig 5. Power-on reset circuit

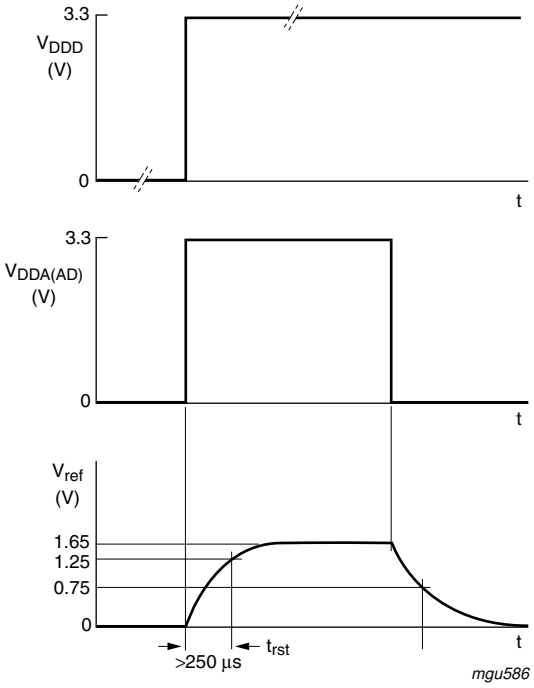

Fig 6. Power-on reset timing

8.11 Audio digital interface

The following audio formats can be selected via the microcontroller interface:

- I²S-bus format with data word length of up to 24 bits
- MSB-justified format with data word length of up to 24 bits
- LSB-justified format with data word length of 16 bits, 20 bits or 24 bits
- Multichannel formats with data word length of 20 bits or 24 bits. The used data lines are DATAAD1 and DATADA1 and the sampling frequency must be below 50 kHz

The formats are illustrated in Figure 7 and Figure 8.

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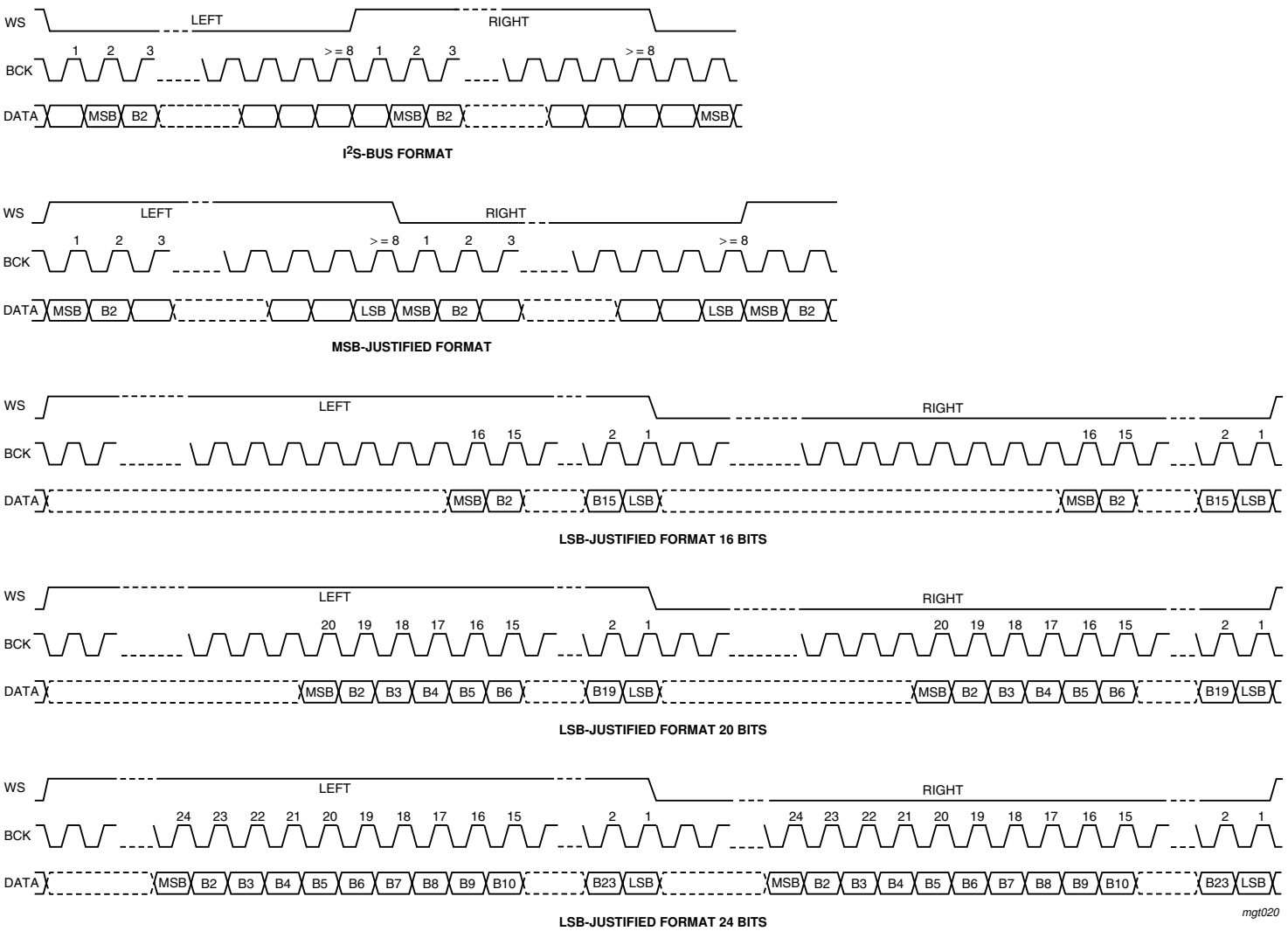

Fig 7. Formats of input and output data (single-channel)

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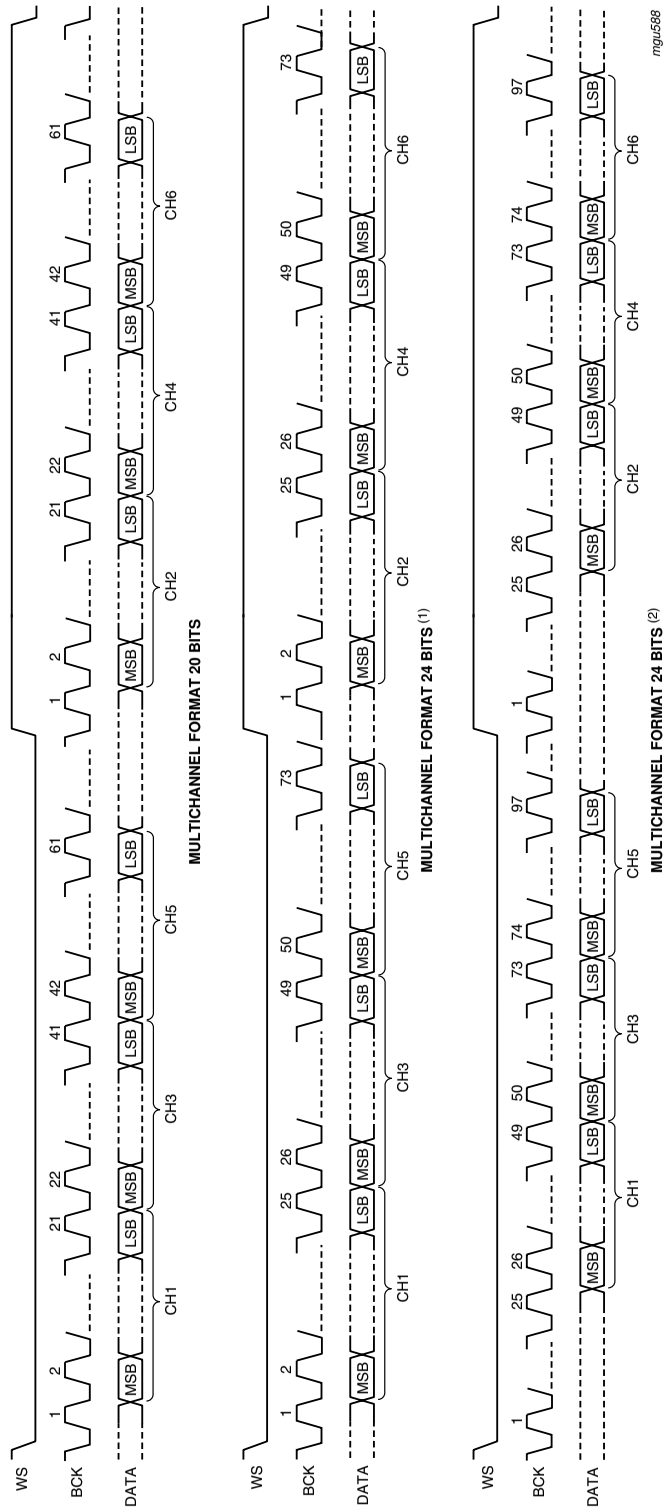

(1) Format 1.
(2) Format 2.

Fig 8. Formats of input and output data (multichannel)

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8.12 Voice digital interface

The following voice formats can be selected via the microcontroller interface:

- I²S-bus format with data word length of up to 20 bits. The left and the right channels contain the same data.
- Mono channel format with data word length of up to 20 bits

The formats are illustrated in Figure 9.

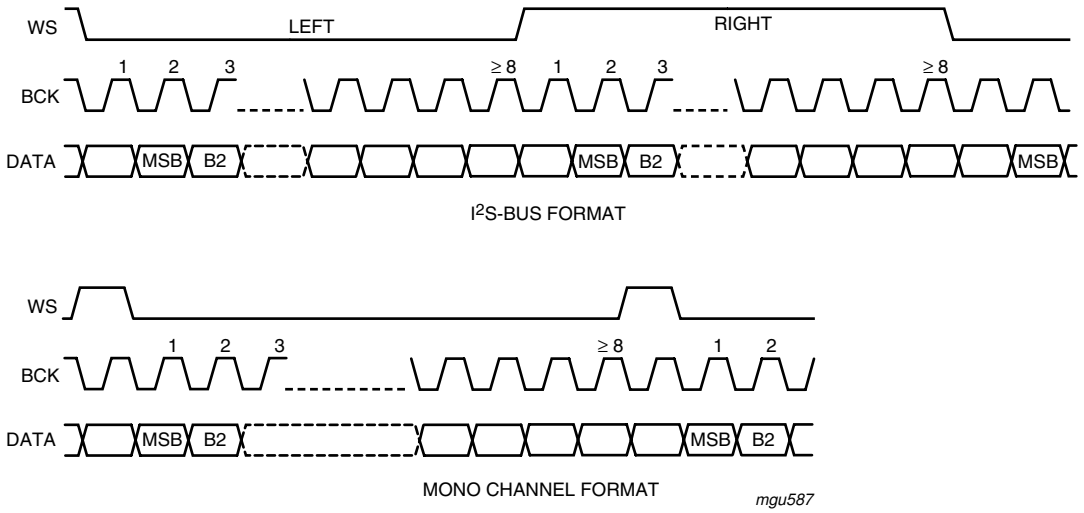

Fig 9. Voice digital interface formats

8.13 DSD mode

The UDA1338H can receive 2.8224 MHz DSD signals and generate 88.2 kHz multibit PCM signals as well as analog signal outputs. The configuration of the UDA1338H in the DSD mode is shown in Figure 10.

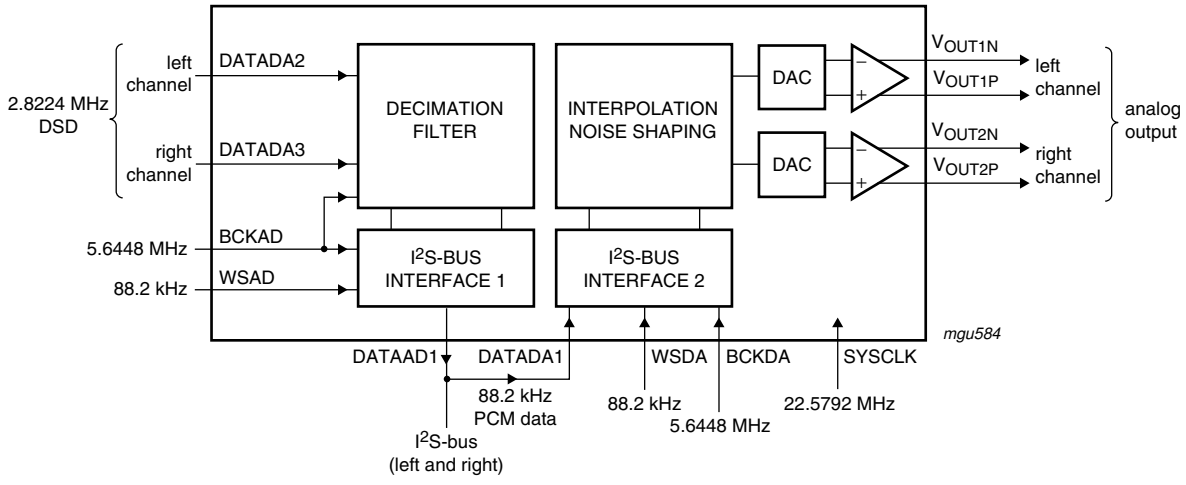

Fig 10. DSD mode

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8.14 Microcontroller interface mode

The microcontroller interface mode can be selected as shown in Table 11:

- L3-bus mode when pin I2C_L3 = LOW
- I²C-bus mode when pin I2C_L3 = HIGH

Table 11. Pin function in the L3-bus or I²C-bus mode

Pin	Level on pin I2C_L3	
	LOW	HIGH
	L3-bus mode signal	I²C-bus mode signal
MCCLK	L3CLOCK	SCL
MCDATA	L3DATA	SDA
MCMODE	L3MODE	QMUTE

Table 12: QMUTE

Signal QMUTE	Function
LOW	no muting
HIGH	muting

All the features are accessible with the I²C-bus interface protocol as with the L3-bus interface protocol.

The detailed description of the device operation in the L3-bus mode and I²C-bus mode is given in Section 9 and Section 10, respectively.

9. L3-bus interface

9.1 General

The UDA1338H has an L3-bus microcontroller interface and all the digital sound processing features and various system settings can be controlled by a microcontroller.

The exchange of data and control information between the microcontroller and the UDA1338H is LSB first and is accomplished through a serial hardware L3-bus interface comprising the following pins:

- MCCLK: clock line with signal L3CLOCK
- MCDATA: data line with signal L3DATA
- MCMODE: mode line with signal L3MODE.

The L3-bus format has two modes of operation:

- Address mode
- Data transfer mode.

The address mode is used to select a device for a subsequent data transfer. The address mode is characterized by signal L3MODE = LOW and a burst of 8 pulses for signal L3CLOCK, accompanied by 8 bits; see Figure 11.

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The data transfer mode is characterized by signal L3MODE = HIGH and is used to transfer one or more bytes representing a register address, instruction or data.

Basically, two types of data transfers can be defined:

- Write action: data transfer **to** the device
- Read action: data transfer **from** the device.

9.2 Device addressing

The device address consists of one byte with:

- Data Operating Mode (DOM) bits 0 and 1 representing the type of data transfer; see Table 11.
- Address bit 2 to bit 7 representing a 6-bit device address. The address of the UDA1338H is 01 0100 (bit 2 to bit 7).

Table 13: Selection of data transfer

DOM		Transfer
Bit 0	**Bit 1**	
0	0	not used
1	0	not used
0	1	write data or prepare read
1	1	read data

9.3 Register addressing

After sending the device address (including DOM bits), indicating whether the information is to be read or written, one data byte is sent using bit 0 to indicate whether the information will be read or written and bit 1 to bit 7 for the destination register address.

Basically, there are 3 methods for register addressing:

1. Addressing for write data: bit 0 is logic 0 indicating a write action to the destination register, followed by bit 1 to bit 7 indicating the register address; see Figure 11.
2. Addressing for prepare read: bit is logic 1, indicating that data will be read from the register; see Figure 12.
3. Addressing for data read action. Here, the device returns a register address prior to sending data from that register. When bit 0 is logic 0, the register address is valid; when bit 0 is logic 1, the register address is invalid; see Figure 12.

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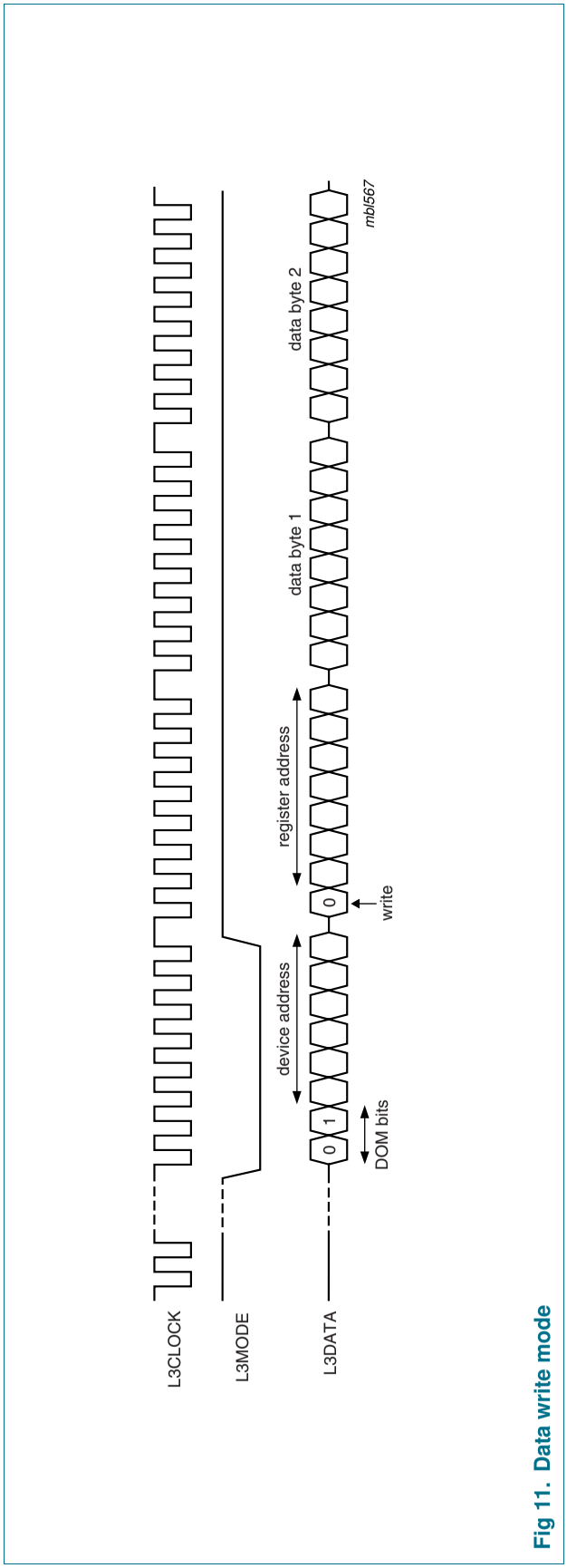

Fig 11. Data write mode

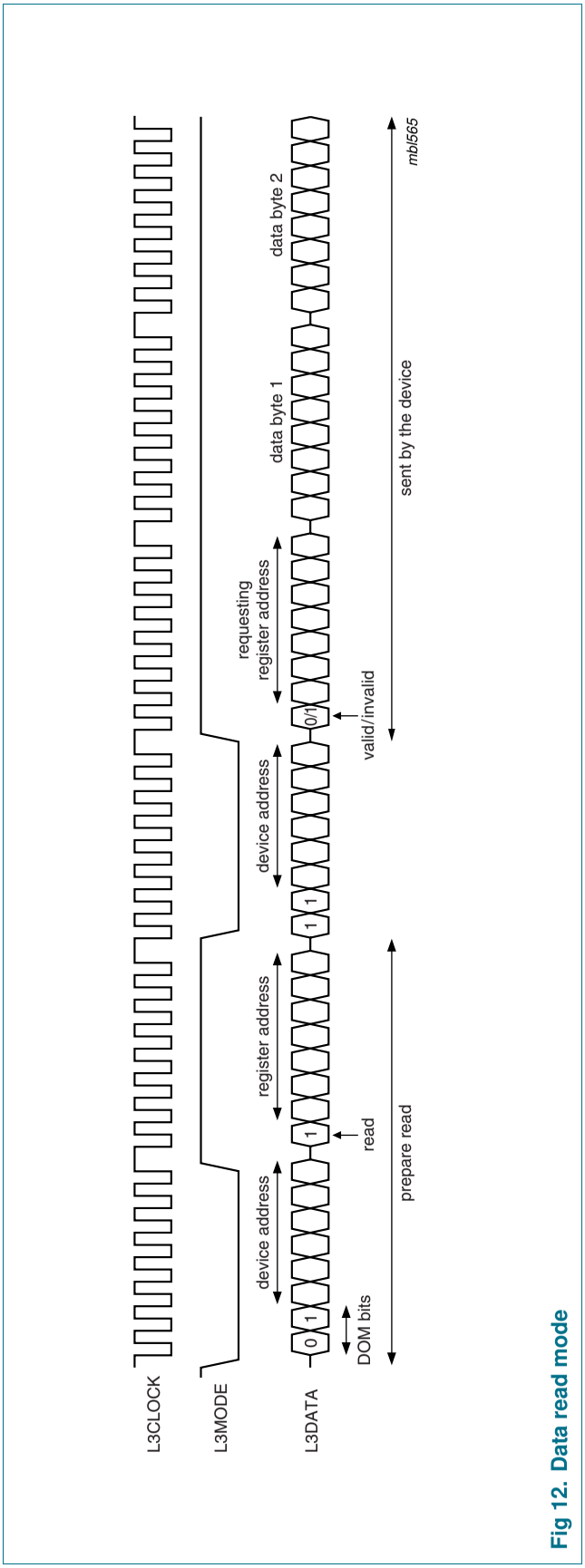

Fig 12. Data read mode

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9.4 Data write mode

The data write mode is explained in the signal diagram of Figure 11. For writing data to a device, 4 bytes must be sent (see Table 14):

1. Byte 1 starting with '01' for signalling the write action to the device, followed by the device address '01 0100'.
2. Byte 2 starting with a '0' for signalling the write action, followed by 7 bits indicating the destination address in binary format with bit A6 being the MSB and bit A0 being the LSB.
3. Byte 3 with bit D15 being the MSB.
4. Byte 4 with bit D0 being the LSB.

It should be noted that each time a new destination register address needs to be written, the device address must be sent again.

9.5 Data read mode

To read data from the device, a prepare read must first be done and then data read. The data read mode is explained in the signal diagram of Figure 12.

For reading data from a device, the following 6 bytes are involved (see Table 15):

1. Byte 1 with the device address, including '01' for signalling the write action to the device.
2. Byte 2 is sent with the register address from which data needs to be read. This byte starts with a '1', which indicates that there will be a read action from the register, followed by 7 bits for the destination address in binary format, with bit A6 being the MSB and bit A0 being the LSB.
3. Byte 3 with the device address, including '11' is sent to the device. The '11' indicates that the device must write data to the microcontroller.
4. Byte 4 sent by the device to the bus, with the (requested) register address and a flag bit indicating whether the requested register was valid (bit is logic 0) or invalid (bit is logic 1).
5. Byte 5 sent by the device to the bus, with the data information in binary format, with bit D15 being the MSB.
6. Byte 6 sent by the device to the bus, with the data information in binary format, with bit D0 being the LSB.

Table 14: L3-bus write data

Byte	L3-bus mode	Action	First in time					Latest in time		
			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1	address	device address	0	1	0	1	0	1	0	0
2	data transfer	register address	0	A6	A5	A4	A3	A2	A1	A0
3	data transfer	data byte 1	D15	D14	D13	D12	D11	D10	D9	D8
4	data transfer	data byte 2	D7	D6	D5	D4	D3	D2	D1	D0

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Table 15: L3-bus read data

Byte	L3-bus mode	Action	First in time					Latest in time		
			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1	address	device address	0	1	0	1	0	1	0	0
2	data transfer	register address	1	A6	A5	A4	A3	A2	A1	A0
3	address	device address	1	1	0	1	0	1	0	0
4	data transfer	register address	0 or 1	A6	A5	A4	A3	A2	A1	A0
5	data transfer	data byte 1	D15	D14	D13	D12	D11	D10	D9	D8
6	data transfer	data byte 2	D7	D6	D5	D4	D3	D2	D1	D0

10. I²C-bus interface

10.1 General

The UDA1338H has an I²C-bus microcontroller interface. All the features are accessible with the I²C-bus interface protocol. In the I²C-bus mode, the DAC mute function is accessible via pin MCMODE with signal QMUTE.

The exchange of data and control information between the microcontroller and the UDA1338H is accomplished through a serial hardware interface comprising the following pins as shown in Table 11:

- MCCLK: clock line with signal SCL
- MCDATA: data line with signal SDA.

10.2 Characteristics of the I²C-bus

The bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to the supply voltage V_{DD} via a pull-up resistor when connected to the output stages of a microcontroller. For a 400 kHz IC, the recommendation for this type of bus from Philips Semiconductors must be followed (e.g. up to loads of 200 pF on the bus a pull-up resistor can be used, between 200 pF and 400 pF a current source or switched resistor must be used). Data transfer can only be initiated when the bus is not busy.

10.3 Bit transfer

One data bit is transferred during each clock pulse; see Figure 13. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals. The maximum clock frequency is 400 kHz.

To be able to run on this high frequency, all the inputs and outputs connected to this bus must be designed for this high-speed I²C-bus according to the Philips specification.

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10.4 Byte transfer

Each byte (8 bits) is transferred with the MSB first; see Table 16.

Table 16: Byte transfer

MSB	Bit number						LSB
7	6	5	4	3	2	1	0

10.5 Data transfer

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves.

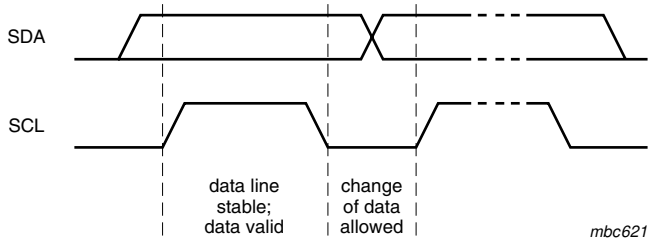

Fig 13. Bit transfer on the I²C-bus

10.6 Start and stop conditions

Both data and clock line will remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as a start condition (S); see Figure 14. A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a stop condition (P).

10.7 Acknowledgment

The number of data bits transferred between the start and stop conditions from the transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit; see Figure 15. At the acknowledge bit the data line is released by the master and the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed, must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

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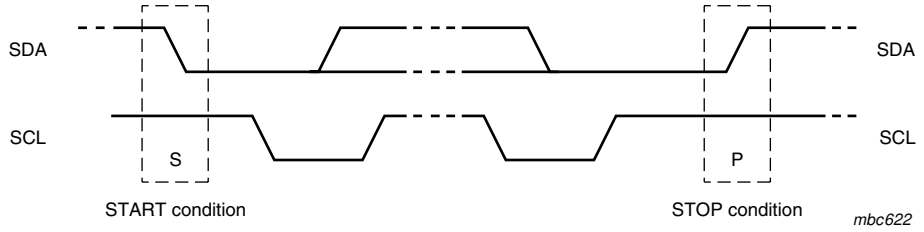

Fig 14. START and STOP conditions on the I²C-bus

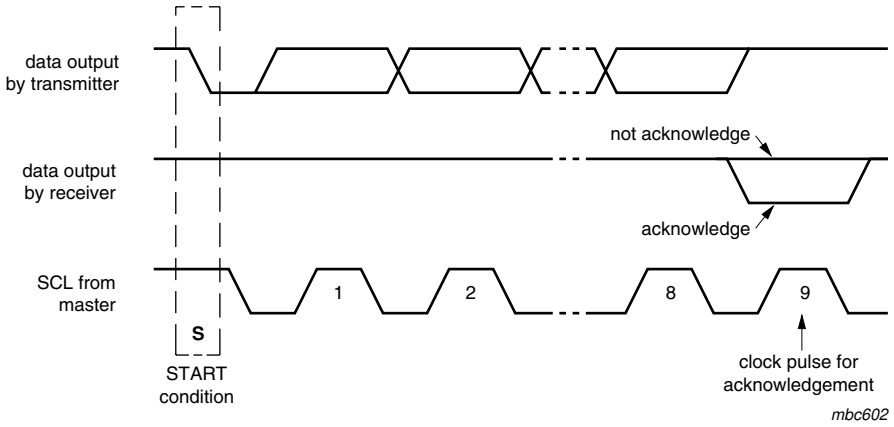

Fig 15. Acknowledge on the I²C-bus

10.8 Device address

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with byte 1 transmitted after the start procedure. The UDA1338H acts as a slave receiver or a slave transmitter.

Therefore, the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The UDA1338H device address is shown in Table 17.

Table 17. I²C-bus device address of UDA1338H

Device address							R/$\overline{W}$
A6	A5	A4	A3	A2	A1	A0	
0	0	1	1	0	0	0	0/1

10.9 Register address

The register addresses in the I²C-bus mode are the same as in the L3-bus mode. The register addresses are defined in Section 11.

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10.10 Write and read data

The I²C-bus configurations for a write and read cycle are shown in Table 18 and Table 19, respectively.

The write cycle is used to write groups of two bytes to the internal registers for the settings. It is also possible to read the registers for the device status information.

10.11 Write cycle

The I²C-bus configuration for a write cycle is shown in Table 18. The write cycle is used to write the data to the internal registers. The device and register addresses are one byte each, the setting data is always a pair of two bytes.

The format of the write cycle is as follows:

1. The microcontroller starts with a start condition (S).
2. The first byte (8 bits) contains the device address '0011 000' and a logic 0 (write) for the R/$\overline{W}$ bit.
3. This is followed by an acknowledge (A) from the UDA1338H.
4. After this the microcontroller writes the 8-bit register address (ADDR) where the writing of the register content of the UDA1338H must start.
5. The UDA1338H acknowledges this register address (A).
6. The microcontroller sends 2 bytes data with the Most Significant (MS) byte first and then the Least Significant (LS) byte. After each byte an acknowledge is followed from the UDA1338H.
7. If repeated groups of 2 bytes data are transmitted, then the register address is auto incremented. After each byte an acknowledge is followed from the UDA1338H.
8. Finally, the UDA1338H frees the I²C-bus and the microcontroller can generate a stop condition (P).

Table 18. Master transmitter writes to UDA1338H registers in the I²C-bus mode

	Device address	R/$\overline{W}$		Register address		data 1				DATA 2[1]				DATA n[1]				
S	0011 000	0	A	ADDR	A	MS1	A	LS1	A	MS2	A	LS2	A	MSn	A	LSn	A	P
	acknowledge from UDA1338H																	

[1] Auto increment of register address.

10.12 Read cycle

The read cycle is used to read the data values from the internal registers. The I²C-bus configuration for a read cycle is shown in Table 19.

The format of the read cycle is as follows:

1. The microcontroller starts with a start condition (S).
2. The first byte (8 bits) contains the device address '0011 000' and a logic 0 (write) for the R/$\overline{W}$ bit.
3. This is followed by an acknowledge (A) from the UDA1338H.

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4. After this the microcontroller writes the 8-bit register address (ADDR) where the reading of the register content of the UDA1338H must start.
5. The UDA1338H acknowledges this register address.
6. Then the microcontroller generates a repeated start (Sr).
7. Then the microcontroller generates the device address '0011 000' again, but this time followed by a logic 1 (read) of the R/$\overline{W}$ bit. An acknowledge is followed from the UDA1338H.
8. The UDA1338H sends 2 bytes data with the Most Significant (MS) byte first and then the Least Significant (LS) byte. After each byte an acknowledge is followed from the microcontroller (master).
9. If repeated groups of 2 bytes are transmitted, then the register address is auto incremented. After each byte an acknowledge is followed from the microcontroller.
10. The microcontroller stops this cycle by generating a negative acknowledge (NA).
11. Finally, the UDA1338H frees the I^{2}C-bus and the microcontroller can generate a stop condition (P).

Table 19. Master transmitter reads from the UDA1338H registers in the I^{2}C-bus mode

	Device address	R/$\overline{W}$		Register address			Device address	R/$\overline{W}$		data 1			DATA 2[1]			DATA n[1]				
S	0011 000	0	A	ADDR	A	Sr	0011 000	1	A	MS1	A	LS1	A	MS2	A	LS2	A	MSn	A	LSn	NA	P
	acknowledge from UDA1338H									acknowledge from master												

[1] Auto increment of register address.

11. Register mapping

In this chapter the register addressing and mapping of the microcontroller interface of the UDA1338H is given.

In Table 20 an overview of the register mapping is given.

In Table 21 the actual register mapping is given and the register definitions are explained in Section 11.3 to Section 11.14.

11.1 Address mapping

Table 20: Overview of register mapping

Address	Function
System settings	
00h	system
01h	audio ADC and DAC subsystem
02h	voice ADC system
Status (read out registers)	
0Fh	status outputs
Interpolator settings	
10h	DAC channel and feature selection
11h	DAC feature control

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Table 20: Overview of register mapping *…continued*

Address	Function
12h	DAC channel 1
13h	DAC channel 2
14h	DAC channel 3
15h	DAC channel 4
16h	DAC channel 5
17h	DAC channel 6
18h	DAC mixing channel 1
19h	DAC mixing channel 2
1Ah	DAC mixing channel 3
1Bh	DAC mixing channel 4
1Ch	DAC mixing channel 5
1Dh	DAC mixing channel 6
ADC input amplifier gain settings	
20h	audio ADC input amplifier gain
21h	voice ADC input amplifier gain
Supplemental settings	
30h	supplemental settings 1
31h	supplemental settings 2

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11.2 Register mapping

Table 21: UDA1338H register mapping[1]

Add	Function	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
System settings																	
00h	system	RST[2]	VFS1	VFS0	VCE	VAP	DSD	SC1	SC0	OP1	OP0	FS1	FS0	ACE	ADP	DCE	DAP
		-	0	0	1	0	0	0	0	0	0	0	1	1	0	1	0
01h	audio ADC and DAC subsystem	DC	PAB	PAA	MTB	MTA	AIF2	AIF1	AIF0	DAG	FIL	DVD	DIS1	DIS0	DIF2	DIF1	DIF0
		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02h	voice ADC system	-	-	-	-	-	-	-	-	BCK1	BCK0	WSM	VH1	VH0	PVA	MTV	VIF
		0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0
Status (read out only)																	
0Fh	status outputs	-	-	-	-	-	-	-	-	-	-	VS	AS1	AS0	DS2	DS1	DS0
Interpolator settings																	
10h	DAC channel and feature selection	MIX1	MIX0	MC5	MC4	MC3	MC2	MC1	MC0	SEL1	SEL0	CS5	CS4	CS3	CS2	CS1	CS0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11h	DAC feature control	ICS1	ICS0	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12h	DAC channel 1	ICS1	ICS0	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13h	DAC channel 2	-	-	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14h	DAC channel 3	ICS1	ICS0	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15h	DAC channel 4	-	-	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16h	DAC channel 5	ICS1	ICS0	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17h	DAC channel 6	-	-	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18h	DAC mixing channel 1	ICS1	ICS0	-	-	-	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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