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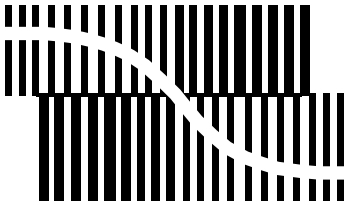
DATA SHEET



UDA1352TS
48 kHz IEC 60958 audio DAC

Preliminary specification
Supersedes data of 2002 May 22

2002 Nov 22

CONTENTS

1 FEATURES

1.1 General

- 2.7 to 3.6 V power supply
- Integrated digital filter and Digital-to-Analog Converter (DAC)
- $256f_s$ system clock output
- 20-bit data path in interpolator
- High performance
- No analog post filtering required for DAC
- Supporting sampling frequencies from 28 up to 55 kHz.

1.2 Control

- Controlled either by means of static pins, I²C-bus or L3-bus microcontroller interface.

1.3 IEC 60958 input

- On-chip amplifier for converting IEC 60958 input to CMOS levels
- Lock indication signal available on pin LOCK
- Information of the Pulse Code Modulation (PCM) status bit and the non-PCM data detection is available on pin PCMDET
- For left and right 40 key channel-status bits available via L3-bus or I²C-bus interface.

1.4 Digital sound processing and DAC

- Automatic de-emphasis when using IEC 60958 input with 32.0, 44.1 and 48.0 kHz audio sample frequencies
- Soft mute by means of a cosine roll-off circuit selectable via pin MUTE, L3-bus or I²C-bus interface
- Left and right independent dB linear volume control with 0.25 dB steps from 0 to −50 dB, 1 dB steps to −60, −66 and −∞ dB

I²C BUS

BITSTREAM CONVERSION

- Bass boost and treble control in L3-bus or I²C-bus mode
- Interpolating filter (f_s to $64f_s$) by means of a cascade of a recursive filter and a FIR filter
- Fifth-order noise shaper (operating at $64f_s$) generates the bitstream for the DAC
- Filter Stream DAC (FSDAC).

2 APPLICATIONS

- Digital audio systems.

3 GENERAL DESCRIPTION

The UDA1352TS is a single-chip IEC 60958 audio decoder with an integrated stereo DAC employing bitstream conversion techniques.

A lock indication signal is available on pin LOCK, indicating that the IEC 60958 decoder is locked. A separate pin PCMDET is available to indicate whether or not the PCM data is applied to the input.

By default, the DAC output is muted when the decoder is out-of-lock. However, this setting can be overruled in the L3-bus or I²C-bus mode.

The UDA1352TS has IEC 60958 input to the DAC only and is in SSOP28 package.

Besides the UDA1352TS, the UDA1352HL is also available. The UDA1352HL is the full featured version in LQFP48 package.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1352TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

5 QUICK REFERENCE DATA

$V_{DDD} = V_{DDA} = 3.0$ V; IEC 60958 input with $f_s = 48.0$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages measured with respect to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		2.7	3.0	3.6	V
V_{DDA}	analog supply voltage		2.7	3.0	3.6	V
$I_{DDA(DAC)}$	analog supply current of DAC	power-on	–	3.3	–	mA
		power-down; clock off	–	35	–	μA
$I_{DDA(PLL)}$	analog supply current of PLL		–	0.3	–	mA
$I_{DDD(C)}$	digital supply current of core		–	9	–	mA
I_{DDD}	digital supply current		–	0.3	–	mA
P	power dissipation	DAC in playback mode	–	38	–	mW
		DAC in Power-down mode	–	tbf	–	mW
General						
t_{rst}	reset active time		–	250	–	μs
T_{amb}	ambient temperature		−40	–	+85	°C
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)	f_i = 1.0 kHz tone at 0 dBFS; note 1	850	900	950	mV
ΔV_o	unbalance of output voltages	f_i = 1.0 kHz tone	–	0.1	0.4	dB
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	f_i = 1.0 kHz tone				
		at 0 dBFS	–	−82	−77	dB
		at −40 dBFS; A-weighted	–	−60	−52	dB
S/N	signal-to-noise ratio	f_i = 1.0 kHz tone; code = 0; A-weighted	95	100	–	dB
α_{cs}	channel separation	f_i = 1.0 kHz tone	–	110	–	dB

Note

1. The output voltage of the DAC is proportional to the DAC power supply voltage.

6 BLOCK DIAGRAM

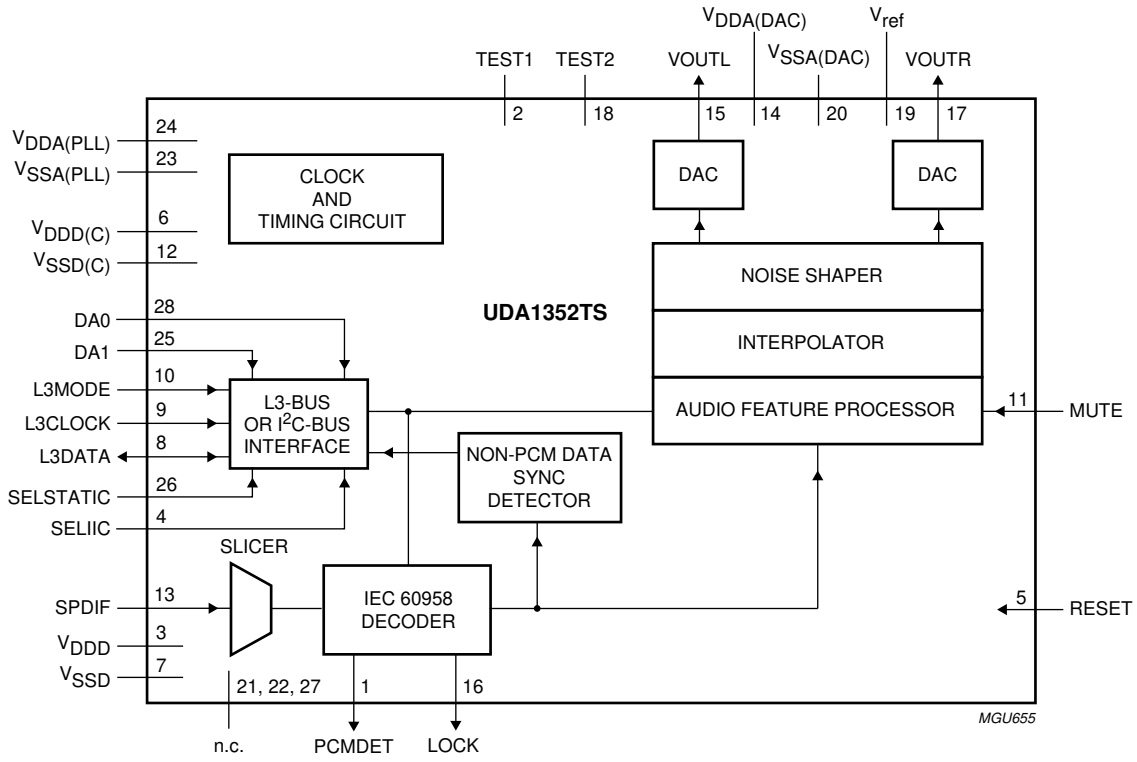


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
PCMDET	1	DO	PCM detection indicator output
TEST1	2	DO	test pin 1; must be left open-circuit in application
V_{DDD}	3	DS	digital supply voltage
SELIIC	4	DID	I^2C-bus or L3-bus mode selection input
RESET	5	DID	reset input
$V_{DDD(C)}$	6	DS	digital supply voltage for core
V_{SSD}	7	DGND	digital ground
L3DATA	8	IIC	L3-bus or I^2C-bus interface data input and output
L3CLOCK	9	DIS	L3-bus or I^2C-bus interface clock input
L3MODE	10	DIS	L3 interface mode input
MUTE	11	DID	mute control input
$V_{SSD(C)}$	12	DGND	digital ground for core
SPDIF	13	AIO	IEC 60958 channel input
$V_{DDA(DAC)}$	14	AS	analog supply voltage for DAC
VOUTL	15	AIO	DAC left channel analog output
LOCK	16	DO	SPDIF and PLL lock indicator output
VOUTR	17	AIO	DAC right channel analog output
TEST2	18	DID	test pin 2; must be connected to digital ground (V_{SSD}) in application
V_{ref}	19	AIO	DAC reference voltage
$V_{SSA(DAC)}$	20	AGND	analog ground for DAC
n.c.	21	–	not connected
n.c.	22	–	not connected
$V_{SSA(PLL)}$	23	AGND	analog ground for PLL
$V_{DDA(PLL)}$	24	AS	analog supply voltage for PLL
DA1	25	DISU	A1 device address selection input
SELSTATIC	26	DIU	static pin control selection input
n.c.	27	–	not connected (reserved)
DA0	28	DID	A0 device address selection input

Note

1. See Table 1.

Table 1 Pin types

TYPE	DESCRIPTION
DS	digital supply
DGND	digital ground
AS	analog supply
AGND	analog ground
DI	digital input
DIS	digital Schmitt-triggered input
DID	digital input with internal pull-down resistor
DISD	digital Schmitt-triggered input with internal pull-down resistor
DIU	digital input with internal pull-up resistor
DISU	digital Schmitt-triggered input with internal pull-up resistor
DO	digital output
DIO	digital input and output
DIOS	digital Schmitt-triggered input and output
IIC	input and open-drain output for I^2C-bus
AIO	analog input and output

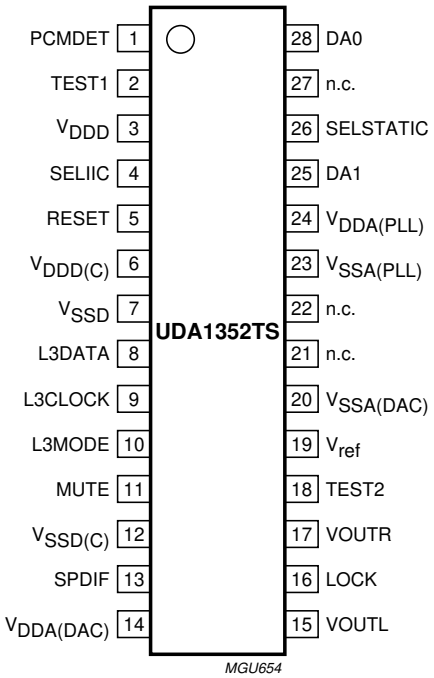


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 Clock regeneration and lock detection

The UDA1352TS contains an on-board PLL for regenerating a system clock from the IEC 60958 input bitstream.

Remark: If there is no input signal, the PLL generates a minimum frequency and the output spectrum shifts accordingly. Since the analog output does not have an analog mute, this means noise that is out of band under normal conditions can move into the audio band.

When the on-board clock locks to the incoming frequency, the lock indicator bit is set and can be read via the L3-bus or I^{2}C-bus interface. Internally, the PLL lock indication can be combined with the PCM status bit of the input data stream and the status whether any burst preamble is detected or not. By default, when both the IEC 60958 decoder and the on-board clock have locked to the incoming signal and the input data stream is PCM data, pin LOCK will be asserted. However, when the IC is locked but the PCM status bit reports non-PCM data, pin LOCK is returned to LOW level. This combination of the lock status and the PCM detection can be overruled by the L3-bus or I^{2}C-bus register setting.

The lock indication output can be used, for example, for muting purposes. The lock signal can be used to drive an external analog muting circuit to prevent out of band noise from becoming audible when the PLL runs at its minimum frequency (e.g. when there is no SPDIF input signal).

The UDA1352TS has a dedicated pin PCMDET to indicate whether valid PCM data stream is detected or (supposed to be) non-PCM data is detected.

8.2 Mute

The UDA1352TS is equipped with a cosine roll-off mute in the DSP data path of the DAC part. Muting the DAC (by pin MUTE or via bit MT in the L3-bus or I^{2}C-bus mode) will result in a soft mute as shown in Fig.3. The cosine roll-off soft mute takes 32 × 32 samples = 23 ms at 44.1 kHz sampling frequency.

When operating in the L3-bus or I^{2}C-bus mode, the device will mute on start-up. In the L3-bus or I^{2}C-bus mode, it is necessary to explicitly switch off the mute for audio output by means of bit MT in the device register.

In the L3-bus or I^{2}C-bus mode, pin MUTE will at all time mute the output signal. This is in contrast to the UDA1350 and the UDA1351 in which pin MUTE in the L3-bus mode does not have any function.

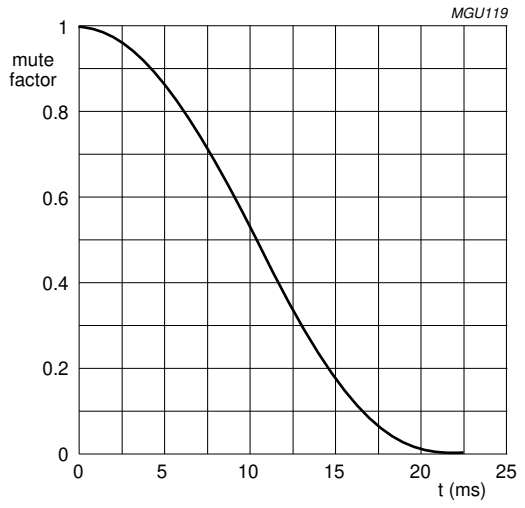


Fig.3 Mute as a function of raised cosine roll-off.

8.3 Auto mute

By default, the DAC outputs will be muted until the UDA1352TS is locked, regardless of the level on pin MUTE or the state of bit MT. In this way, only valid data will be passed to the outputs. This mute is done in the SPDIF interface and is a hard mute, not a cosine roll-off mute.

If needed, this muting can be bypassed by setting bit MUTEBP = 1 via the L3-bus or I^{2}C-bus interface. As a result, the UDA1352TS will no longer mute during out-of-lock situations.

8.4 Data path

The UDA1352TS data path consists of the IEC 60958 decoder, the audio feature processor, the digital interpolator and noise shaper and the DACs.

8.4.1 IEC 60958 INPUT

The IEC 60958 decoder features an on-chip amplifier with hysteresis, which amplifies the SPDIF input signal to CMOS level (see Fig.4).

All 24 bits of data for left and right are extracted from the input bitstream as well as 40 channel status bits for left and right. These bits can be read via the L3-bus or I^2C-bus interface.

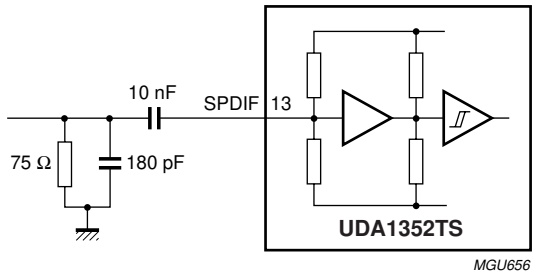


Fig.4 IEC 60958 input circuit and typical application.

The UDA1352TS supports the following sample frequencies and data bit rates:

- f_s = 32.0 kHz, resulting in a data rate of 2.048 Mbits/s
- f_s = 44.1 kHz, resulting in a data rate of 2.8224 Mbits/s
- f_s = 48.0 kHz, resulting in a data rate of 3.072 Mbits/s.

The UDA1352TS supports timing levels I, II and III, as specified by the IEC 60958 standard. This means that the accuracy of the above mentioned sampling frequencies depends on the timing level I, II or III as mentioned in Section 11.4.1.

8.4.2 AUDIO FEATURE PROCESSOR

The audio feature processor automatically provides de-emphasis for the IEC 60958 data stream in the static pin control mode and default mute at start-up in the L3-bus or I^2C-bus mode.

When used in the L3-bus or I^2C-bus mode, it provides the following additional features:

- Left and right independent volume control
- Bass boost control
- Treble control
- Mode selection of the sound processing bass boost and treble filters: flat, minimum and maximum
- Soft mute control with raised cosine roll-off.

8.4.3 INTERPOLATOR

The UDA1352TS includes an on-board interpolating filter which converts the incoming data stream from $1f_s$ to $64f_s$ by cascading a recursive filter and a FIR filter.

Table 2 Interpolator characteristics

PARAMETER	CONDITIONS	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	±0.03
Stop band	$>0.55f_s$	−50
Dynamic range	0 to $0.45f_s$	114
DC gain	−	−5.67

8.4.4 NOISE SHAPER

The fifth-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted to an analog signal using a filter stream DAC.

8.4.5 FILTER STREAM DAC

The Filter Stream DAC (FSDAC) is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage.

The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way, very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC is scaled proportionally with the power supply voltage.

8.5 Control

The UDA1352TS can be controlled by means of static pins (when pin SELSTATIC = HIGH), via the I^2C-bus (when pin SELSTATIC = LOW and pin SELIIC = HIGH) or via the L3-bus (when pins SELSTATIC and SELIIC are LOW). For optimum use of the features of the UDA1352TS, the L3-bus or I^2C-bus mode is recommended since only basic functions are available in the static pin control mode.

It should be noted that the static pin control mode and the L3-bus or I^2C-bus mode are mutually exclusive.

8.5.1 STATIC PIN CONTROL MODE

The default values for all non-pin controlled settings are identical to the default values at start-up in the L3-bus or I^2C-bus mode (see Table 3).

Table 3 Pin description of static pin control mode

PIN	NAME	VALUE	FUNCTION
Mode selection pin			
26	SELSTATIC	1	select static pin control mode; must be connected to V_{DDD}
Input pins			
5	RESET	0	normal operation
		1	reset
9	L3CLOCK	0	must be connected to V_{SSD}
10	L3MODE	0	must be connected to V_{SSD}
8	L3DATA	0	must be connected to V_{SSD}
11	MUTE	0	no mute
		1	mute active
Status pins			
1	PCMDET	0	non-PCM data or burst preamble detected
		1	PCM data detected
16	LOCK	0	clock regeneration and IEC 60958 decoder out-of-lock or non-PCM data detected
		1	clock regeneration and IEC 60958 decoder locked and PCM data detected
Test pins			
2	TEST1	–	must be left open-circuit
18	TEST2	0	must be connected to V_{SSD}

8.5.2 L3-BUS OR I²C-BUS MODE

The L3-bus or I²C-bus mode allows maximum flexibility in controlling the UDA1352TS (see Table 4).

It should be noted that in the L3-bus or I²C-bus mode, several base-line functions are still controlled by pins on the device and that, on start-up in the L3-bus or I²C-bus mode, the output is explicitly muted by bit MT via the L3-bus or I²C-bus interface.

Table 4 Pin description in the L3-bus or I²C-bus mode

PIN	NAME	VALUE	FUNCTION
Mode selection pins			
26	SELSTATIC	0	select L3-bus mode or I²C-bus mode; must be connected to V_{SSD}
4	SELIIC	0	select L3-bus mode; must be connected to V_{SSD}
		1	select I²C-bus mode; must be connected to V_{DDD}
Input pins			
5	RESET	0	normal operation
		1	reset
8	L3DATA	–	must be connected to the L3-bus
		–	must be connected to the SDA line of the I²C-bus
9	L3CLOCK	–	must be connected to the L3-bus
		–	must be connected to the SCL line of the I²C-bus
10	L3MODE	–	must be connected to the L3-bus
11	MUTE	0	no mute
		1	mute active
Status pins			
1	PCMDET	0	non-PCM data or burst preamble detected
		1	PCM data detected
16	LOCK	0	clock regeneration and IEC 60958 decoder out-of-lock or non-PCM data detected
		1	clock regeneration and IEC 60958 decoder locked and PCM data detected
Test pins			
2	TEST1	–	must be left open-circuit
18	TEST2	0	must be connected to V_{SSD}

9 L3-BUS DESCRIPTION

9.1 General

The UDA1352TS has an L3-bus microcontroller interface and all the digital sound processing features and various system settings can be controlled by a microcontroller.

The controllable settings are:

- Restoring L3-bus default values
- Power-on
- Selection of filter mode and settings of treble and bass boost
- Volume settings left and right
- Selection of soft mute via cosine roll-off and bypass of auto mute.

The readable settings are:

- Mute status of interpolator
- PLL locked
- SPDIF input signal locked
- Audio sample frequency
- Valid PCM data detected
- Pre-emphasis of the IEC 60958 input signal
- Accuracy of the clock.

The exchange of data and control information between the microcontroller and the UDA1352TS is LSB first and is accomplished through the serial hardware L3-bus interface comprising the following pins:

- L3DATA: data line
- L3MODE: mode line
- L3CLOCK: clock line.

The L3-bus format has two modes of operation:

- Address mode
- Data transfer mode.

The address mode is used to select a device for a subsequent data transfer. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 bits (see Fig.5). The data transfer mode is characterized by L3MODE being HIGH and is used to transfer one or more bytes representing a register address, instruction or data.

Basically, two types of data transfers can be defined:

- Write action: data transfer to the device
- Read action: data transfer from the device.

Remark: when the device is powered-up, at least one L3CLOCK pulse must be given to the L3-bus interface to wake-up the interface before starting sending to the device (see Fig.5). This is only needed once after the device is powered-up.

9.2 Device addressing

The device address consists of 1 byte with:

- Data Operating Mode (DOM) bits 0 and 1 representing the type of data transfer (see Table 5)
- Address bits 2 to 7 representing a 6-bit device address. The bits 2 and 3 of the address can be selected via the external pins DA0 and DA1, which allows up to 4 UDA1352TS devices to be independently controlled in a single application.

The primary address of the UDA1352TS is ‘001000’ (LSB to MSB) and the default address is ‘011000’.

Table 5 Selection of data transfer

DOM		TRANSFER
BIT 0	BIT 1	
0	0	not used
1	0	not used
0	1	write data or prepare read
1	1	read data

9.3 Register addressing

After sending the device address (including DOM bits), indicating whether the information is to be read or written, one data byte is sent using bit 0 to indicate whether the information will be read or written and bits 1 to 7 for the destination register address.

Basically, there are three methods for register addressing:

1. Addressing for write data: bit 0 is logic 0 indicating a write action to the destination register, followed by bits 1 to 7 indicating the register address (see Fig.5)
2. Addressing for prepare read: bit 0 is logic 1, indicating that data will be read from the register (see Fig.6)
3. Addressing for data read action. Here, the device returns a register address prior to sending data from that register. When bit 0 is logic 0, the register address is valid; when bit 0 is logic 1, the register address is invalid.

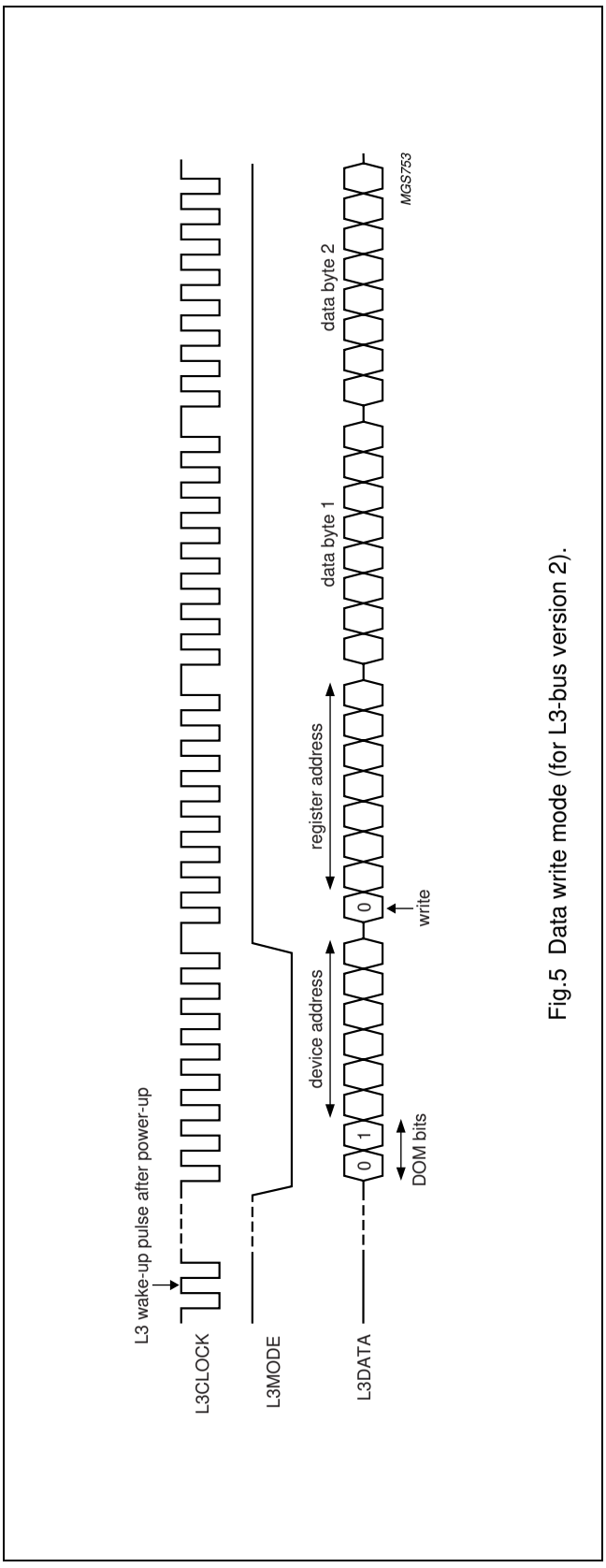


Fig.5 Data write mode (for L3-bus version 2).

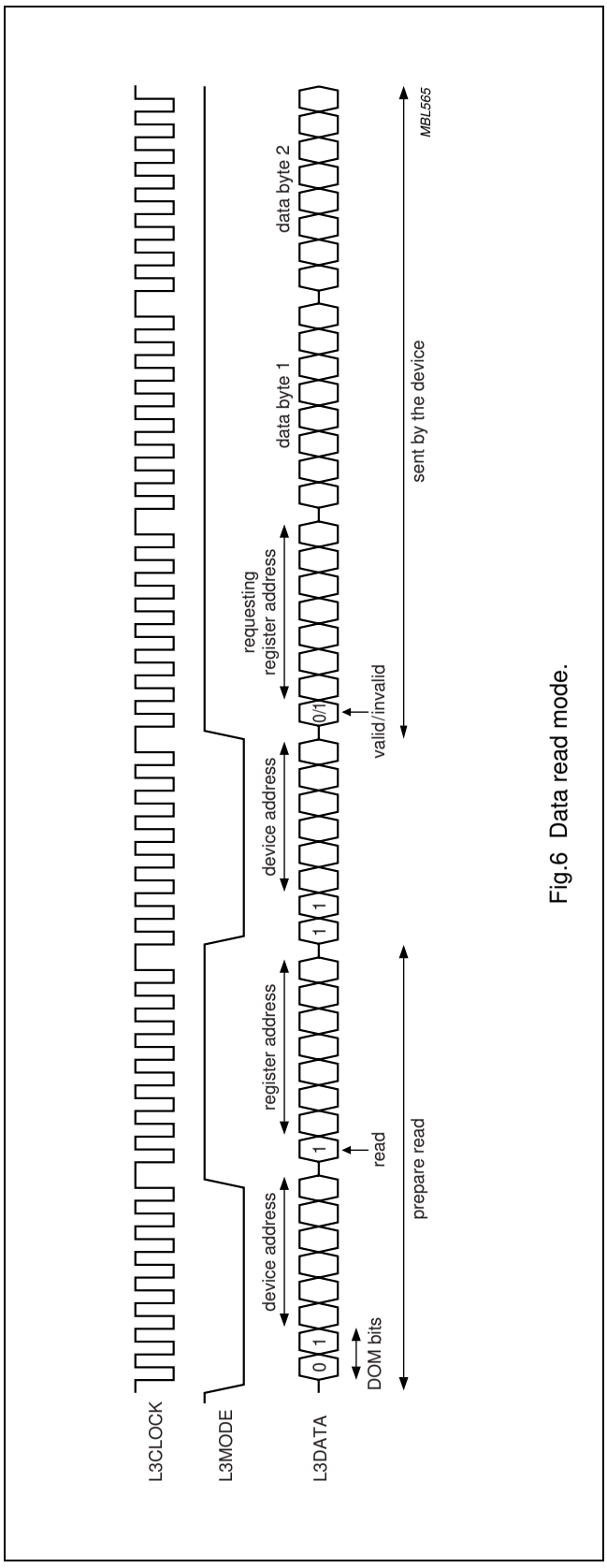


Fig.6 Data read mode.

9.4 Data write mode

The data write mode is explained in the signal diagram of Fig.5. For writing data to a device, 4 bytes must be sent (see Table 6):

1. One byte starting with '01' for signalling the write action to the device, followed by the device address ('011000' for the UDA1352TS default)
2. One byte starting with a '0' for signalling the write action, followed by 7 bits indicating the destination register address in binary format with A6 being the MSB and A0 being the LSB
3. One data byte (from the two data bytes) with D15 being the MSB
4. One data byte (from the two data bytes) with D0 being the LSB.

It should be noted that each time a new destination register address needs to be written, the device address must be sent again.

9.5 Data read mode

To read data from the device, a prepare read must first be done and then data read. The data read mode is explained in the signal diagram of Fig.6.

For reading data from a device, the following 6 bytes are involved (see Table 7):

1. One byte with the device address, including '01' for signalling the write action to the device
2. One byte is sent with the register address from which data needs to be read; this byte starts with a '1', which indicates that there will be a read action from the register, followed by seven bits for the source register address in binary format, with A6 being the MSB and A0 being the LSB
3. One byte with the device address preceded by '11' is sent to the device; the '11' indicates that the device must write data to the microcontroller
4. One byte, sent by the device to the bus, with the (requested) register address and a flag bit indicating whether the requested register was valid (bit is logic 0) or invalid (bit is logic 1)
5. One byte (from the two bytes), sent by the device to the bus, with the data information in binary format, with D15 being the MSB
6. One byte (from the two bytes), sent by the device to the bus, with the data information in binary format, with D0 being the LSB.

Table 6 L3-bus write data

BYTE	L3-BUS MODE	ACTION	FIRST IN TIME							LAST IN TIME
			BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1	address	device address	0	1	DA0	DA1	1	0	0	0
2	data transfer	register address	0	A6	A5	A4	A3	A2	A1	A0
3	data transfer	data byte 1	D15	D14	D13	D12	D11	D10	D9	D8
4	data transfer	data byte 2	D7	D6	D5	D4	D3	D2	D1	D0

Table 7 L3-bus read data

BYTE	L3-BUS MODE	ACTION	FIRST IN TIME							LAST IN TIME
			BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1	address	device address	0	1	DA0	DA1	1	0	0	0
2	data transfer	register address	1	A6	A5	A4	A3	A2	A1	A0
3	address	device address	1	1	DA0	DA1	1	0	0	0
4	data transfer	register address	0 or 1	A6	A5	A4	A3	A2	A1	A0
5	data transfer	data byte 1	D15	D14	D13	D12	D11	D10	D9	D8
6	data transfer	data byte 2	D7	D6	D5	D4	D3	D2	D1	D0

9.6 Initialization string

For proper and reliable operation, the UDA1352TS must be initialized in the L3-bus mode. This is required to have the PLL start-up after powering up of the device under all conditions. The initialization string is given in Table 8.

Table 8 L3-bus initialization string and set defaults after power-up

BYTE	L3-BUS MODE	ACTION		FIRST IN TIME							LAST IN TIME
				BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1	address	init string	device address	0	1	DA0	DA1	1	0	0	0
2	data transfer		register address	0	1	0	0	0	0	0	0
3	data transfer		data byte 1	0	0	0	0	0	0	0	0
4	data transfer		data byte 2	0	0	0	0	0	0	0	1
5	address	set defaults	device address	0	1	DA0	DA1	1	0	0	0
6	data transfer		register address	0	1	1	1	1	1	1	1
7	data transfer		data byte 1	0	0	0	0	0	0	0	0
8	data transfer		data byte 2	0	0	0	0	0	0	0	0

10 I²C-BUS DESCRIPTION

10.1 Characteristics of the I²C-bus

The bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to the V_{DD} via a pull-up resistor when connected to the output stages of a microcontroller. For a 400 kHz IC the recommendation for this type of bus from NXP Semiconductors must be followed (e.g. up to loads of 200 pF on the bus a pull-up resistor can be used, between 200 to 400 pF a current source or switched resistor must be used). Data transfer can only be initiated when the bus is not busy.

10.2 Bit transfer

One data bit is transferred during each clock pulse (see Fig.7). The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals. The maximum clock frequency is 400 kHz.

To be able to run on this high frequency all the inputs and outputs connected to this bus must be designed for this high-speed I²C-bus according to specification *"The I²C-bus and how to use it"*, (order code 9398 393 40011).

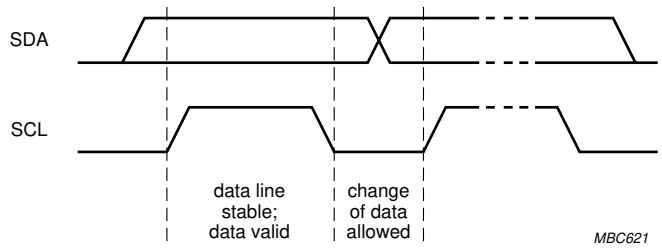


Fig.7 Bit transfer on the I²C-bus.

10.3 Byte transfer

Each byte (8 bits) is transferred with the MSB first (see Table 9).

Table 9 Byte transfer

MSB			BIT NUMBER				LSB
7	6	5	4	3	2	1	0

10.4 Data transfer

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves.

10.5 Start and stop conditions

Both data and clock line will remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as a start condition (S); see Fig.8. A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a stop condition (P).

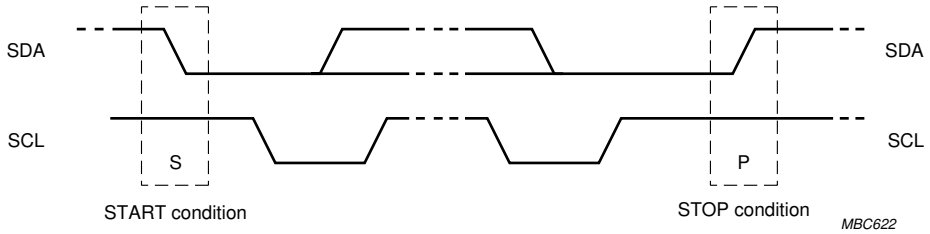


Fig.8 START and STOP conditions on the I²C-bus.

10.6 Acknowledgment

The number of data bits transferred between the start and stop conditions from the transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit (see Fig.9). At the acknowledge bit the data line is released by the master and the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

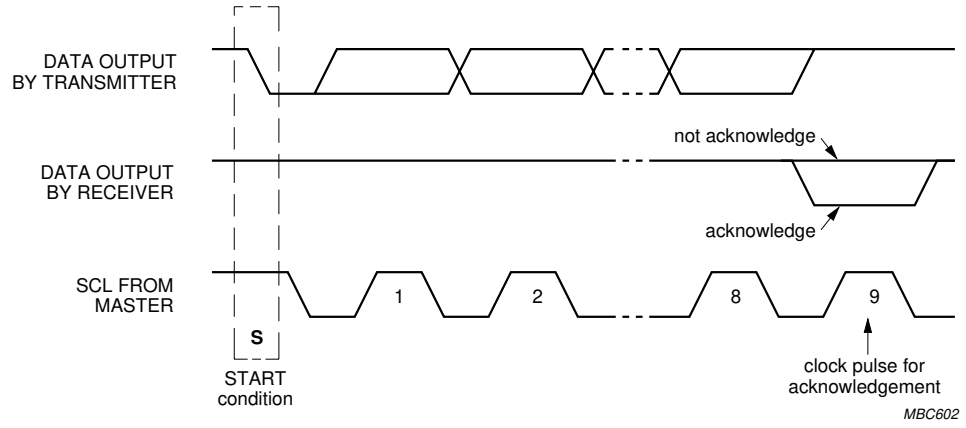


Fig.9 Acknowledge on the I²C-bus.

10.7 Device address

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with byte 1 transmitted after the start procedure.

The device address can be one out of four, being set by pin DA0 and pin DA1.

The UDA1352TS acts as a slave receiver or a slave transmitter. Therefore, the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The UDA1352TS device address is shown in Table 10.

Table 10 I²C-bus device address

DEVICE ADDRESS							R/$\overline{W}$
A6	A5	A4	A3	A2	A1	A0	–
1	0	0	1	1	DA1	DA0	0/1

10.8 Register address

The register addresses in the I²C-bus mode are the same as in the L3-bus mode.

10.9 Write and read data

The I²C-bus configuration for a write and read cycle are shown respectively in Tables 11 and 12. The write cycle is used to write groups of two bytes to the internal registers for the digital sound feature control and system setting. It is also possible to read these locations for the device status information.

10.10 Write cycle

The I²C-bus configuration for a write cycle is shown in Table 11. The write cycle is used to write the data to the internal registers. The device and register addresses are one byte each, the setting data is always a pair of two bytes.

The format of the write cycle is as follows:

1. The microcontroller starts with a start condition (S).
2. The first byte (8 bits) contains the device address '1001 110' and a logic 0 (write) for the R/$\overline{W}$ bit.
3. This is followed by an acknowledge (A) from the UDA1352TS.
4. After this the microcontroller writes the 8-bit register address (ADDR) where the writing of the register content of the UDA1352TS must start.
5. The UDA1352TS acknowledges this register address (A).
6. The microcontroller sends 2 bytes data with the Most Significant (MS) byte first and then the Least Significant (LS) byte. After each byte an acknowledge is followed from the UDA1352TS.
7. If repeated groups of 2 bytes are transmitted, then the register address is auto incremented. After each byte an acknowledge is followed from the UDA1352TS.
8. Finally, the UDA1352TS frees the I²C-bus and the microcontroller can generate a stop condition (P).

Table 11 Master transmitter writes to the UDA1352TS registers in the I²C-bus mode.

	DEVICE ADDRESS	**R/$\overline{W}$**		**REGISTER ADDRESS**		**DATA 1**				**DATA 2**(1)				**DATA n**(1)				
S	1001 110	0	A	ADDR	A	MS1	A	LS1	A	MS2	A	LS2	A	MSn	A	LSn	A	P
	acknowledge from UDA1352TS																	

Note

1. Auto increment of register address.

10.11 Read cycle

The read cycle is used to read the data values from the internal registers. The I²C-bus configuration for a read cycle is shown in Table 12.

The format of the read cycle is as follows:

1. The microcontroller starts with a start condition (S).
2. The first byte (8 bits) contains the device address ‘1001 110’ and a logic 0 (write) for the R/$\overline{W}$ bit.
3. This is followed by an acknowledge (A) from the UDA1352TS.
4. After this the microcontroller writes the register address (ADDR) where the reading of the register content of the UDA1352TS must start.
5. The UDA1352TS acknowledges this register address.
6. Then the microcontroller generates a repeated start (Sr).
7. Then the microcontroller generates the device address ‘1001 110’ again, but this time followed by a logic 1 (read) of the R/$\overline{W}$ bit. An acknowledge is followed from the UDA1352TS.
8. The UDA1352TS sends 2 bytes data with the Most Significant (MS) byte first and then the Least Significant (LS) byte. After each byte an acknowledge is followed from the microcontroller.
9. If repeated groups of 2 bytes are transmitted, then the register address is auto incremented. After each byte an acknowledge is followed from the microcontroller.
10. The microcontroller stops this cycle by generating a negative acknowledge (NA).
11. Finally, the UDA1352TS frees the I²C-bus and the microcontroller can generate a stop condition (P).

Table 12 Master transmitter reads from the UDA1352TS registers in the I²C-bus mode.

	DEVICE ADDRESS	**R/$\overline{W}$**		**REGISTER ADDRESS**			**DEVICE ADDRESS**	**R/$\overline{W}$**		**DATA 1**				**DATA 2**(1)				**DATA n**(1)				
S	1001 110	0	A	ADDR	A	Sr	1001 110	1	A	MS1	A	LS1	A	MS2	A	LS2	A	MSn	A	LSn	NA	P
	acknowledge from UDA1352TS									acknowledge from master												

Note

1. Auto increment of register address.

11 SPDIF SIGNAL FORMAT

11.1 SPDIF channel encoding

The digital signal is coded using Bi-phase Mark Code (BMC), which is a kind of phase-modulation. In this scheme, a logic 1 in the data corresponds to two zero-crossings in the coded signal, and a logic 0 to one zero-crossing. An example of the encoding is given in Fig.10.

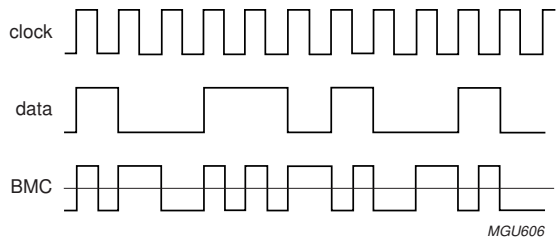


Fig.10 Bi-phase mark encoding.

11.2 SPDIF hierarchical layers for audio data

From an abstract point of view an SPDIF signal can be represented as in Fig.11. A 2-channel PCM signal can be transmitted as various sequential blocks. Each block in turn consists of 192 frames. Each frame contains two sub-frames, one for each channel.

Each sub-frame is preceded by a preamble. There are three types of preambles being B, M and W. Preambles can be spotted easily in an SPDIF stream because these sequences can never occur in the channel parts of a valid SPDIF stream. Table 13 indicates the values of the preambles.

A sub-frame in turn contains a single audio sample which may be up to 24 bits wide, a validity bit which indicates whether the sample is valid, a single bit of user data, and a single bit of channel status. Finally, there is a parity bit for this particular sub-frame (see Fig.12).

The data bits from 4 to 31 in each sub-frame will be modulated using a BMC scheme. The sync preamble actually contains a violation of the BMC scheme and consequently can be detected easily.

Table 13 Preambles

PRECEDING STATE	CHANNEL CODING	
	0	1
B	1110 1000	0001 0111
M	1110 0010	0001 1101
W	1110 0100	0001 1011

11.3 SPDIF hierarchical layers for digital data

The difference with the audio format is that the data contained in the SPDIF signal is not audio but is digital data.

When transmitting digital data via SPDIF using the IEC 60958 protocol, the allocation of the bits inside the data word is done as shown in Table 14.

Table 14 Bit allocation for digital data

FIELD	IEC 60958 TIME SLOT BITS	DESCRIPTION
0 to 3	preamble	according to IEC 60958
4 to 7	auxiliary bits	not used; all logic 0
8 to 11	unused data bits	not used; all logic 0
12	16 bits data	sections of the digital bitstream
13	user data	according to IEC 60958
14 to 27	16 bits data	sections of the digital bitstream
28	validity bit	according to IEC 60958
29	user data	according to IEC 60958
30	channel status bit	according to IEC 60958
31	parity bit	according to IEC 60958

As shown in Table 14 and Fig.13, the non-PCM encoded data bitstreams are transferred within the basic 16 bits data area of the IEC 60958 sub-frames [time-slots 12 (LSB) to 27 (MSB)].

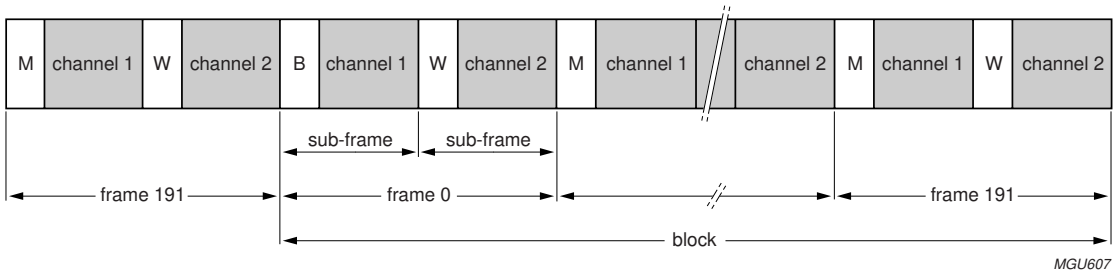


Fig.11 SPDIF block format.

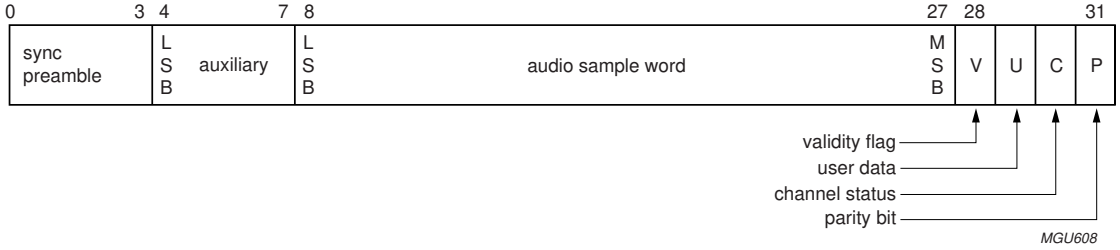


Fig.12 Sub-frame format in audio mode.

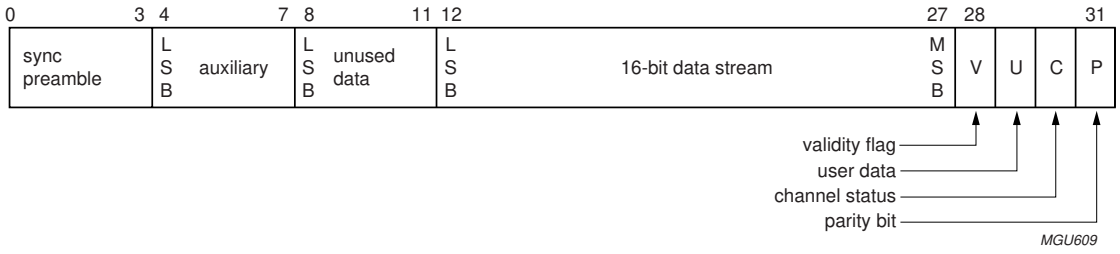


Fig.13 Sub-frame format in non-PCM mode.

11.3.1 Format of the bitstream

The non-PCM data is transmitted in data bursts, consisting of four 16-bit words (called Pa, Pb, Pc and Pd) followed by the so called burst-payload. The definition of the burst preambles is given in Table 15.

Table 15 Burst preamble words

PREAMBLE WORD	LENGTH OF THE FIELD	CONTENTS	VALUE
Pa	16 bits	sync word 1	F872 (hex)
Pb	16 bits	sync word 2	4E1F (hex)
Pc	16 bits	burst information	see Table 16
Pd	16 bits	length code	number of bits

11.3.2 Burst information

The burst information given in preamble Pc, meaning the information contained in the data stream, is defined according to IEC 60958 as given in Table 16.

Table 16 Fields of burst information in preamble Pc

BITS OF Pc	VALUE	CONTENTS	REFERENCE POINT R	REPETITION TIME OF DATA BURST IN IEC 60958 FRAMES
0 to 4	0	NULL data	–	none
	1	AC-3 data	R_AC-3	1536
	2	reserved	–	–
	3	pause	bit 0 of Pa	refer to IEC 60958
	4	MPEG-1 layer 1 data	bit 0 of Pa	384
	5	MPEG-1 layer 1, 2 or 3 data or MPEG-2 without extension	bit 0 of Pa	1152
	6	MPEG-2 with extension	bit 0 of Pa	1152
	7	reserved	–	–
	8	MPEG-2, layer 1 low sampling rate	bit 0 of Pa	768
	9	MPEG-2, layer 2 or 3 low sampling rate	bit 0 of Pa	2304
	10	reserved	–	–
	11 to 13	reserved (DTS)	–	refer to IEC 61937
	14 to 31	reserved	–	–
5 to 6	0	reserved	–	–
7	0	error flag indicating a valid burst-payload	–	–
	1	error flag indicating an invalid burst-payload	–	–
8 to 12	–	data type dependant information	–	–
13 to 15	0	bitstream number	–	–

11.3.3 MINIMUM BURST SPACING

In order to be able to detect the start of a data burst, it is prescribed to have a data-burst which does not exceed 4096 frames. After 4096 frames there must be a synchronization sequence containing 2 frames of complete zero data (being 4 times 16 bits) followed by the preamble burst Pa and Pb. In this way a comparison with a sync code of 96 bits can detect the start of a new burst-payload including the Pc and Pd preambles containing additional stream information.

11.4 Timing characteristics

11.4.1 FREQUENCY REQUIREMENTS

The SPDIF specification IEC 60958 supports three levels of clock accuracy, being:

- Level I, high accuracy: tolerance of transmitting sampling frequency shall be within 50×10^{-6}
- Level II, normal accuracy: all receivers should receive a signal of 1000×10^{-6} of nominal sampling frequency
- Level III, variable pitch shifted clock mode: a deviation of 12.5% of the nominal sampling frequency is possible.

11.4.2 RISE AND FALL TIMES

Rise and fall times (see Fig.14) are defined as:

$$\text{Rise time} = \frac{t_r}{(t_L + t_H)} \times 100\%$$

$$\text{Fall time} = \frac{t_f}{(t_L + t_H)} \times 100\%$$

Rise and fall times should be in the range:

- 0% to 20% when the data bit is a logic 1
- 0% to 10% when the data bits are two succeeding logic zeros.

11.4.3 DUTY CYCLE

The duty cycle (see Fig.14) is defined as:

$$\text{Duty cycle} = \frac{t_H}{(t_L + t_H)} \times 100\%$$

The duty cycle should be in the range:

- 40% to 60% when the data bit is a logic 1
- 45% to 55% when the data bits are two succeeding logic zeros.

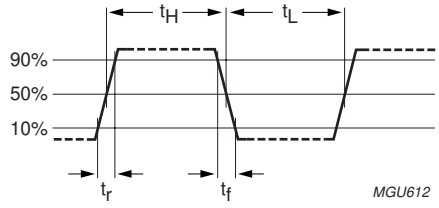


Fig.14 Rise and fall times.

12 REGISTER MAPPING

Table 17 Register map of control settings (write)

REGISTER ADDRESS	FUNCTION
System settings	
01H	SPDIF mute setting
03H	power-down settings
Interpolator	
10H	volume control left and right
12H	sound feature mode, treble and bass boost
13H	mute
14H	polarity
SPDIF input settings	
30H	SPDIF input settings
Software reset	
7FH	restore L3-bus default values

Table 18 Register map of status bits (read-out)

REGISTER ADDRESS	FUNCTION
Interpolator	
18H	interpolator status
SPDIF input	
59H	SPDIF status
5AH	channel status bits left [15:0]
5BH	channel status bits left [31:16]
5CH	channel status bits left [39:32]
5DH	channel status bits right [15:0]
5EH	channel status bits right [31:16]
5FH	channel status bits right [39:32]
FPLL	
68H	FPLL status

12.1 SPDIF mute setting (write)

Table 19 Register address 01H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	–	–	MUTEBP
Default	–	–	–	–	–	–	–	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	–	–	–
Default	–	–	–	–	–	0	0	0

Table 20 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 9	–	reserved
8	MUTEBP	**Mute bypass setting.** A 1-bit value to disable the mute bypass setting. When this mute bypass setting is enabled, then even in out-of-lock situations or non-PCM data detected, the output data will not be suppressed. If this bit is logic 0, then the output will be muted in out-of-lock situations. If this bit is logic 1, then the output will not be muted in out-of-lock situations. Default value 0.
7 to 3	–	reserved
2 to 0	–	When writing new settings via the L3-bus or I^2C-bus interface, these bits should always remain at logic 0 (default value) to guarantee correct operation.