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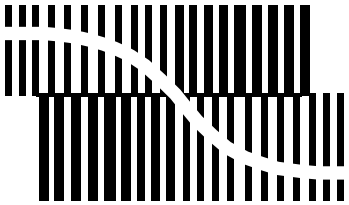
DATA SHEET



UDA1355H

Stereo audio codec with SPDIF interface

Preliminary specification

2003 Apr 10

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1 FEATURES

1.1 General

- 2.7 to 3.6 V power supply
- Integrated digital interpolator filter and Digital-to-Analog Converter (DAC)
- 24-bit data path in interpolator
- No analog post filtering required for DAC
- Integrated Analog-to-Digital Converter (ADC), Programmable Gain Amplifier (PGA) and digital decimator filter
- 24-bit data path in decimator
- Master or slave mode for digital audio data I/O interface
- I^2S-bus, MSB-justified, LSB-justified 16, 18, 20, and 24 bits formats supported on digital I/O interface.

1.2 Control

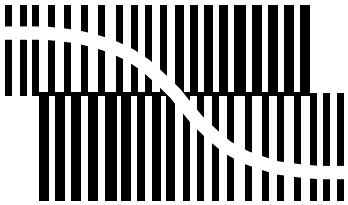
- Controlled by means of static pins or microcontroller (L3-bus or I^2C-bus) interface.

1.3 IEC 60958 input

- On-chip amplifier for converting IEC 60958 input to CMOS levels
- Supports level I, II and III timing
- Selectable IEC 60958 input channel, one of four
- Supports input frequencies from 28 to 96 kHz
- Lock indication signal available on pin LOCK
- 40 status bits can be read for left and right channel via L3-bus or I^2C-bus
- Channel status bits available via L3-bus or I^2C-bus: lock, pre-emphasis, audio sample frequency, two channel Pulse Code Modulation (PCM) indication and clock accuracy
- Pre-emphasis information of incoming IEC 60958 bitstream available in register
- Detection of digital data preamble, such as AC3, available on pin in microcontroller mode.

1.4 IEC 60958 output

- CMOS output level converted to IEC 60958 output signal
- Full-swing digital signal, with level II timing using crystal oscillator clock
- 32, 44.1 and 48 kHz output frequencies supported in static mode



- 32, 44.1 and 48 kHz output frequencies (including double and half of these frequencies) supported in microcontroller mode
- Via microcontroller, 40 status bits can be set for left and right channel.

1.5 Digital I/O interface

- Supports sampling frequencies from 16 to 100 kHz
- Supported static mode:
  - I^2S-bus format
  - LSB-justified 16 and 24 bits format
  - MSB-justified format.
- Supported microcontroller mode:
  - I^2S-bus format
  - LSB-justified 16, 18, 20 or 24 bits format
  - MSB-justified format.
- BCK and WS signals can be slave or master, depending on application mode.

1.6 ADC digital sound processing

- Supports sampling frequencies from 16 to 100 kHz
- Analog front-end includes a 0 to +24 dB PGA in steps of 3 dB, selectable via microcontroller interface
- Digital independent left and right volume control of +24 to −63.5 dB in steps of 0.5 dB via microcontroller interface
- Bitstream ADC operating at $64f_s$
- Comb filter decreases sample rate from $64f_s$ to $8f_s$
- Decimator filter ($8f_s$ to f_s) made of a cascade of three FIR half-band filters.

1.7 DAC digital sound processing

- Digital de-emphasis for 32, 44.1, 48 and 96 kHz audio sampling frequencies
- Automatic de-emphasis when using IEC 60958 to DAC
- Soft mute made of a cosine roll-off circuit selectable via pin MUTE or L3-bus interface

- Programmable digital silence detector
- Interpolating filter (f_s to $64f_s$ or f_s to $128f_s$) comprising a recursive and a FIR filter in cascade
- Selectable fifth-order noise shaper operating at $64f_s$ or third-order noise shaper operating at $128f_s$ (specially for low sampling frequencies, e.g. 16 kHz) generating bitstream for DAC
- Filter Stream DAC (FSDAC)
- In microcontroller mode:
  - Left and right volume control (for balance control) 0 to −78 dB and $-\infty$
  - Left and right bass boost and treble control
  - Optional resonant bass boost control
  - Mixing possibility of two data streams.

2 GENERAL DESCRIPTION

The UDA1355H is a single-chip IEC 60958 decoder and encoder with integrated stereo digital-to-analog converters and analog-to-digital converters employing bitstream conversion techniques.

The UDA1355H has a selectable one-of-four SPDIF input (accepting level I, II and III timing) and one SPDIF output which can generate level II output signals with CMOS levels. In microcontroller mode the UDA1355H offers a large variety of possibilities for defining signal flows through the IC, offering a flexible analog, digital and SPDIF converter chip with possibilities for off-chip sound processing via the digital input and output interface.

A lock indicator is available on pin LOCK when the IEC 60958 decoder and the clock regeneration mechanism is in lock. By default the DAC output and the digital data interface output are muted when the decoder is not in lock.

The UDA1355H contains two clock systems which can run at independent frequencies, allowing to lock-on to an incoming SPDIF or digital audio signal, and in the mean time generating a stable signal by means of the crystal oscillator for driving, for example, the ADC or SPDIF output signal.

Using the crystal oscillator (which requires a 12.288 MHz crystal) and the on-chip low jitter PLL, all standard audio sampling frequencies (f_s = 32, 44.1 and 48 kHz including half and double these frequencies) can be generated.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1355H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm	SOT307-2

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA1}	DAC supply voltage		2.7	3.0	3.6	V
V_{DDA2}	ADC supply voltage		2.7	3.0	3.6	V
V_{DDX}	crystal oscillator and PLL supply voltage		2.7	3.0	3.6	V
V_{DDI}	digital core supply voltage		2.7	3.0	3.6	V
V_{DDE}	digital pad supply voltage		2.7	3.0	3.6	V
I_{DDA1}	DAC supply current	f_s = 48 kHz; power-on	–	4.7	–	mA
		f_s = 96 kHz; power-on	–	4.7	–	mA
		f_s = 48 kHz; power-down	–	1.7	–	μA
		f_s = 96 kHz; power-down	–	1.7	–	μA
I_{DDA2}	ADC supply current	f_s = 48 kHz; power-on	–	10.2	–	mA
		f_s = 96 kHz; power-on	–	10.4	–	mA
		f_s = 48 kHz; power-down	–	0.2	–	μA
		f_s = 96 kHz; power-down	–	0.2	–	μA
I_{DDX}	crystal oscillator and PLL supply current	f_s = 48 kHz; power-on	–	0.9	–	mA
		f_s = 96 kHz; power-on	–	1.2	–	mA
I_{DDI}	digital core supply current	f_s = 48 kHz; all on	–	18.2	–	mA
		f_s = 96 kHz; all on	–	34.7	–	mA
I_{DDE}	digital pad supply current	f_s = 48 kHz; all on	–	0.5	–	mA
		f_s = 96 kHz; all on	–	0.7	–	mA
T_{amb}	ambient temperature		−40	–	+85	°C
Digital-to-analog converter; f_i = 1 kHz; V_{DDA1} = 3.0 V						
$V_{o(rms)}$	output voltage (RMS value)		–	900	–	mV
ΔV_o	output voltage unbalance		–	0.1	–	dB
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	IEC 60958 input; f_s = 48 kHz				
		at 0 dB	–	−88	–	dB
		at −20 dB	–	−75	–	dB
		at −60 dB; A-weighted	–	−37	–	dB
		IEC 60958 input; f_s = 96 kHz				
		at 0 dB	–	−83	–	dB
		at −60 dB; A-weighted	–	−37	–	dB
S/N	signal-to-noise ratio	IEC 60958 input; code = 0; A-weighted				
		f_s = 48 kHz	–	98	–	dB
		f_s = 96 kHz	–	96	–	dB
α_{cs}	channel separation		–	100	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter; f_i = 1 kHz; V_{DDA2} = 3.0 V						
V_i(rms)	input voltage (RMS value)	V_o = −1.16 dBFS digital output	–	1.0	–	V
ΔV_i	input voltage unbalance		–	0.1	–	dB
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 48 kHz				
		at 0 dB	–	−85	–	dB
		at −60 dB; A-weighted	–	−35	–	dB
		f_s = 96 kHz				
		at 0 dB	–	−85	–	dB
		at −60 dB; A-weighted	–	−35	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted				
		f_s = 48 kHz	–	97	–	dB
		f_s = 96 kHz	–	95	–	dB
α_{cs}	channel separation		–	100	–	dB
External crystal						
f_{xtal}	crystal frequency		–	12.288	–	MHz
$C_{L(xtal)}$	crystal load capacitor		–	10	–	pF
Device reset						
t_{rst}	reset time		–	250	–	μs
Power consumption						
P_{tot}	total power consumption	IEC 60958 input; f_s = 48 kHz				
		DAC in playback mode	–	74	–	mW
		DAC in Power-down mode	–	63	–	mW

5 BLOCK DIAGRAM

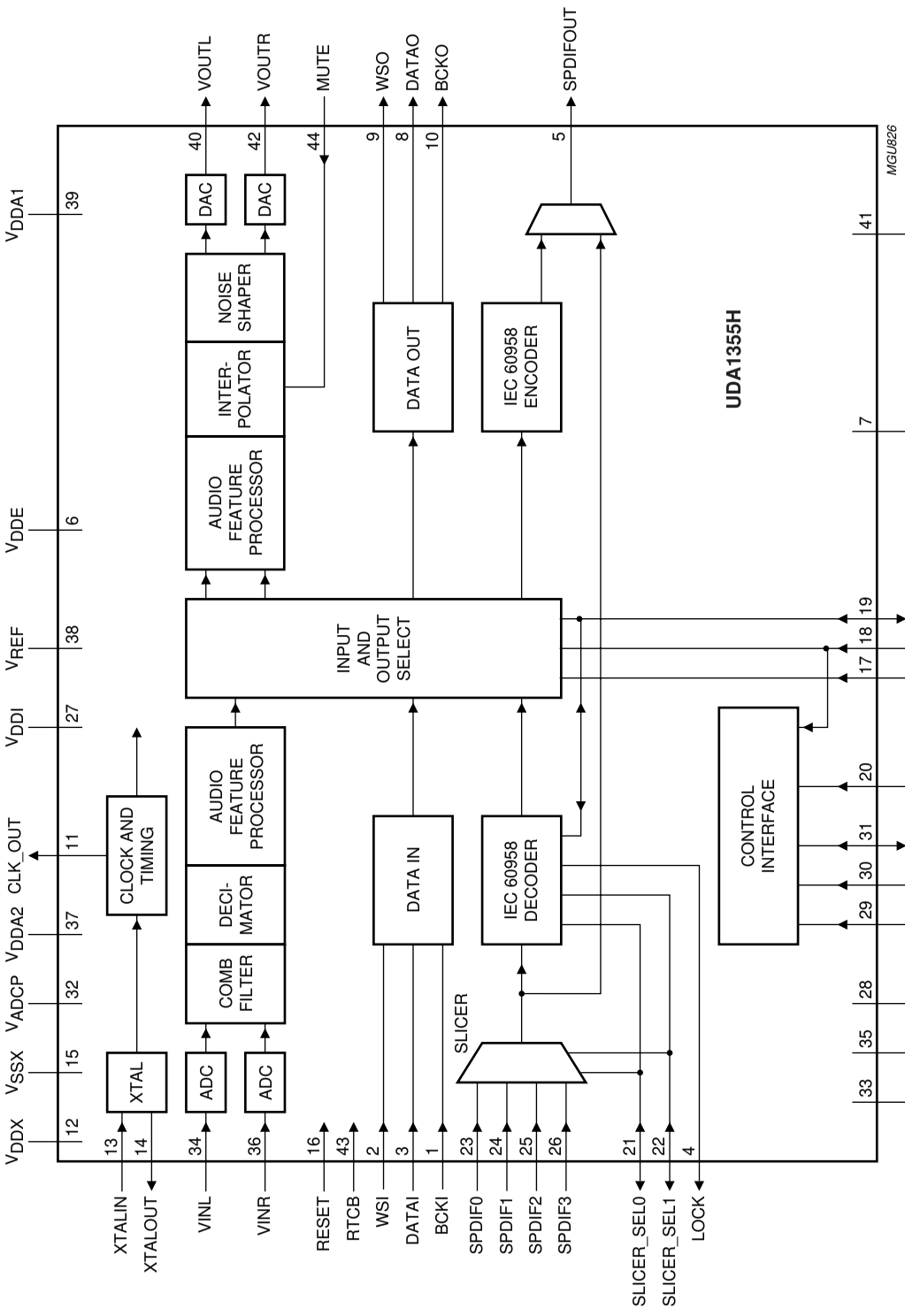


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	PAD[1]	DESCRIPTION
BCKI	1	bpt4mtht5v	bit clock input (master or slave)
WSI	2	bpt4mtht5v	word select input (master or slave)
DATAI	3	iptht5v	digital data input
LOCK	4	op4mc	PLL lock indicator output
SPDIFOUT	5	op4mc	SPDIF output
V_{DDE}	6	vdde	digital pad supply voltage
V_{SSE}	7	vsse	digital pad ground
DATAO	8	ops5c	digital data output
WSO	9	bpt4mtht5v	word select output (master or slave)
BCKO	10	bpt4mtht5v	bit clock output (master or slave)
CLK_OUT	11	op4mc	clock output; $256f_s$ or $384f_s$
V_{DDX}	12	vddco	crystal oscillator and PLL supply voltage
XTALIN	13	apio	crystal oscillator input
XTALOUT	14	apio	crystal oscillator output
V_{SSX}	15	vssco	crystal oscillator and PLL ground
RESET	16	ipthdt5v	reset input
MODE0	17	apio	mode selection input 0 for static mode or microcontroller mode (grounded for I^2C-bus)
MODE1	18	bpts5tht5v	mode selection input 1 for static mode or AO address input and output for microcontroller mode
MODE2	19	bpts5tht5v	mode selection input 2 for static mode or U_RDY output for microcontroller mode
SEL_STATIC	20	apio	selection input for static mode, I^2C-bus mode or L3-bus mode
SLICER_SEL0	21	bpts5tht5v	SPDIF slicer selection input 0 for static mode and USER bit output for microcontroller mode
SLICER_SEL1	22	bpts5tht5v	SPDIF slicer selection input 1 for static mode and AC3 preamble detect output for microcontroller mode
SPDIF0	23	apio	SPDIF input 0
SPDIF1	24	apio	SPDIF input 1
SPDIF2	25	apio	SPDIF input 2
SPDIF3	26	apio	SPDIF input 3
V_{DDI}	27	vddi	digital core supply voltage
V_{SSIS}	28	vssis	digital core ground
MP0	29	apio	multi-purpose pin 0: frequency select for static mode, not used for microcontroller mode
MP1	30	iptht5v	multi-purpose pin 1: SFOR1 for static mode, SCL for I^2C-bus mode and L3CLOCK for L3-bus mode
MP2	31	iic400kt5v	multi-purpose pin 2: SFOR0 for static mode, SDA for I^2C-bus mode and L3DATA for L3-bus mode
V_{ADCP}	32	vddco	positive ADC reference voltage
V_{ADCN}	33	vssco	negative ADC reference voltage

SYMBOL	PIN	PAD[1]	DESCRIPTION
VINL	34	apio	ADC left channel input
V_{SSA2}	35	vssco	ADC ground
VINR	36	apio	ADC right channel input
V_{DDA2}	37	vddco	ADC supply voltage
V_{REF}	38	apio	reference voltage for ADC and DAC
V_{DDA1}	39	vddco	DAC supply voltage
VOUTL	40	apio	DAC left channel output
V_{SSA1}	41	vssco	DAC ground
VOUTR	42	apio	DAC right channel output
RTCB	43	ipthdt5v	test control input
MUTE	44	iipthdt5v	DAC mute input

Note

1. See Table 1.

Table 1 Pad description

PAD	DESCRIPTION
ipthtt5v	input pad; push-pull; TTL with hysteresis; 5 V tolerant
ipthdt5v	input pad; push-pull; TTL with hysteresis; pull-down; 5 V tolerant
op4mc	output pad; push-pull; 4 mA output drive; CMOS
ops5c	output pad; push-pull; 5 ns slew rate control; CMOS
bpt4mtht5v	bidirectional pad; push-pull input; 3-state output; 4 mA output drive; TTL with hysteresis; 5 V tolerant
bpts5tht5v	bidirectional pad; push-pull input; 3-state output; 5 ns slew rate control; TTL with hysteresis; 5 V tolerant
iic400kt5v	I^2C-bus pad; 400 kHz I^2C-bus specification with open drain; 5 V tolerant
apio	analog pad; analog input or output
vddco	analog supply pad
vssco	analog ground pad
vdde	digital supply pad
vsse	digital ground pad
vddi	digital core supply pad
vssis	digital core ground pad

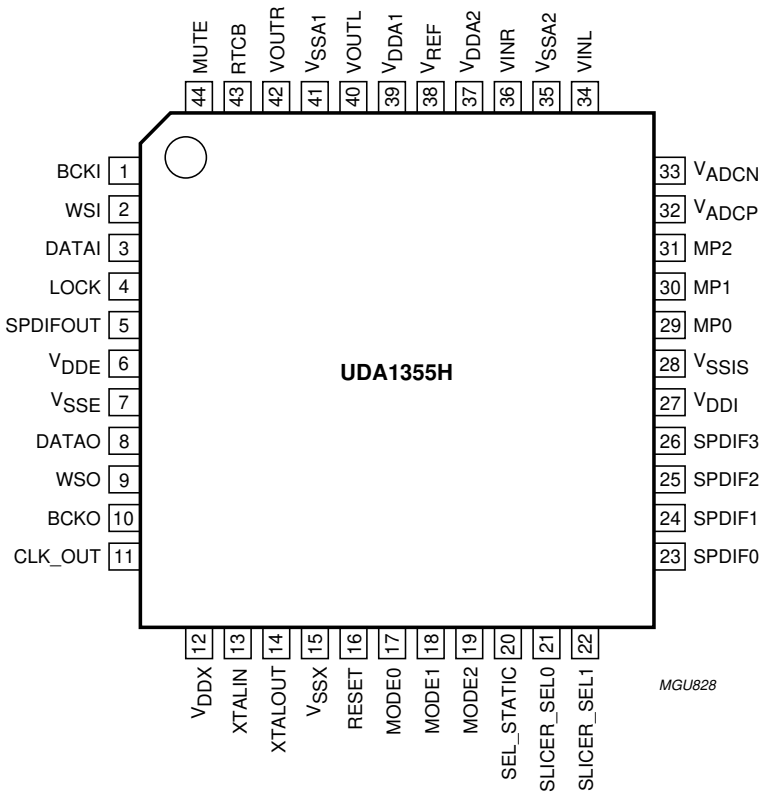


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 IC control

The UDA1355H can be controlled either via static pins or via the microcontroller serial hardware interface being the I²C-bus with a clock up to 400 kHz or the L3-bus with a clock up to 2 MHz. It is recommended to use the microcontroller interface since this gives full access to all the IC features.

The two microcontroller interfaces only differ in interface format. The register addresses and features that can be controlled are identical for L3-bus mode and I²C-bus mode.

The UDA1355H can operate in three control modes:

- Static mode with limited features
- L3-bus mode with full featuring
- I²C-bus mode with full featuring.

The modes are selected via the 3-level pin SEL_STATIC according to Table 2.

Table 2 Control mode selection via pin SEL_STATIC

LEVEL	MODE
HIGH	static mode
MID	I²C-bus mode
LOW	L3-bus mode

7.2 Microcontroller interface

The UDA1355H has a microcontroller interface and all the sound processing features and system settings can be controlled by the microcontroller.

The controllable settings are:

- Restoring L3-bus defaults
- Power-on settings for all blocks
- Digital interface input and output formats
- Volume settings for the decimator
- PGA gain settings

- Set two times 40 bits of channel status bits of the SPDIF output
- Select one of four SPDIF input sources
- Enable digital mixer inside interpolator
- Control mute and mixer volumes of digital mixer
- Selection of filter mode and settings of treble and bass boost for the interpolator (DAC) section
- Volume settings of interpolator
- Selection of soft mute via cosine roll-off (only effective in L3-bus control mode) and bypass of auto mute
- Selection of de-emphasis
- Enable and control of digital mixer inside interpolator.

The readable settings are:

- Mute status of interpolator
- PLL lock and adaptive lock
- Two times 40 bits of channels status bits of the SPDIF input signal.

7.3 Clock systems

The UDA1355H has two clock systems.

The first system uses an external crystal of 12.288 MHz to generate the audio related system clocks. Only a crystal with a frequency of 12.288 MHz is allowed.

The second system is a PLL which locks on the SPDIF or incoming digital audio signal (e.g. I^2S-bus) and recovers the system clock.

7.3.1 Crystal oscillator clock system

The crystal oscillator and the on-chip PLL and divider circuit can be used to generate internal and external clock signals related to standard audio sampling frequencies (such as 32, 44.1 and 48 kHz including half and double of these frequencies).

The audio frequencies supported in either microcontroller mode or static mode are given in Table 3.

Table 3 Output frequencies

BASIC AUDIO FREQUENCY	OUTPUT FREQUENCY	
	MICRO-CONTROLLER MODE	STATIC MODE
32 kHz	256 × 16 kHz	
	384 × 16 kHz	
	256 × 32 kHz	256 × 32 kHz
	384 × 32 kHz	
	256 × 64 kHz	
	384 × 64 kHz	
44.1 kHz	256 × 22.05 kHz	
	384 × 22.05 kHz	
	256 × 44.1 kHz	256 × 44.1 kHz
	384 × 44.1 kHz	
	256 × 88.2 kHz	
	384 × 88.2 kHz	
48 kHz	256 × 24 kHz	
	384 × 24 kHz	
	256 × 48 kHz	256 × 48 kHz
	384 × 48 kHz	
	256 × 96 kHz	
	384 × 96 kHz	

Remarks:

- If an application mode is selected which does not need a crystal oscillator, the crystal oscillator cannot be omitted. The reason is that the interpolator switches to the crystal clock when an SPDIF input signal is removed. This switch prevents the noise shaper noise from moving inside the audio band as the PLL gradually decreases in frequency.
- If no accurate output frequency is needed, the crystal can be replaced with a resonator.
- Instead of the crystal, a 12.288 MHz system clock can be applied to pin XTALIN.

The block diagram of the crystal oscillator and the PLL circuit is given in Fig.3.

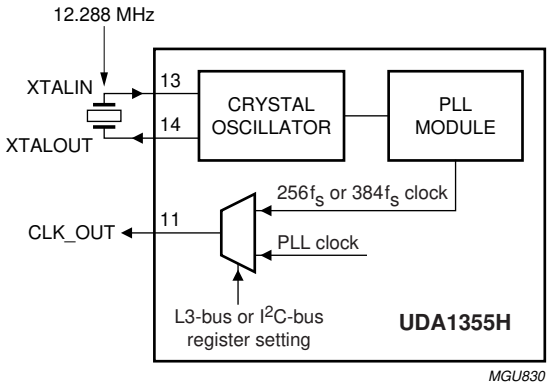


Fig.3 Crystal oscillator clock system.

7.3.2 PLL CLOCK SYSTEM

The PLL locks on the incoming digital data of the SPDIF or WS input signal. The PLL recovers the clock from the SPDIF or WSI signal and removes jitter to produce a stable system clock (see Fig.4).

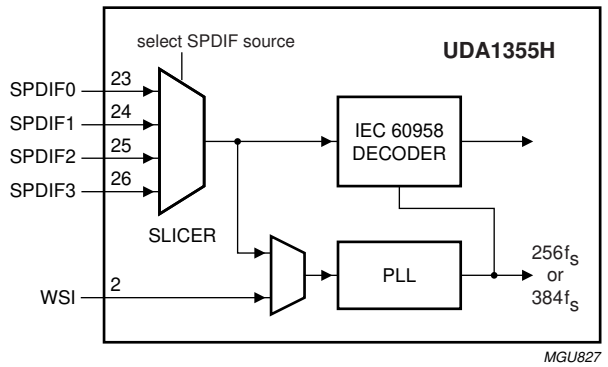


Fig.4 PLL clock system.

7.3.3 WORD SELECTION DETECTION CIRCUIT

This circuit is clocked by the 12.288 MHz crystal oscillator clock and generates a Word Selection (WS) detection signal. If the WS detector does not detect any WS edge, defined as 7 times LOW and 7 times HIGH, then the WS detection signal is LOW. This information can be used to set the clock for the noise shaper in the interpolator. This will prevent noise shaper noise in the audio band.

7.3.4 CLOCK OUTPUT

The UDA1355H has a clock output pin (pin CLK_OUT), which can be used to drive other audio devices in the system. In microcontroller mode the output clock is $256f_s$ or $384f_s$. In static mode the output clock is 256 times 32, 44.1 and 48 kHz.

The source of the output clock is either the crystal oscillator or the PLL, depending on the selected application and control mode.

7.4 IEC 60958 decoder

The UDA1355H IEC 60958 decoder can select one of four SPDIF input channels. An on-chip amplifier with hysteresis amplifies the SPDIF input signal to CMOS level, making it possible to accept both analog and digital SPDIF signals (see Fig.5).

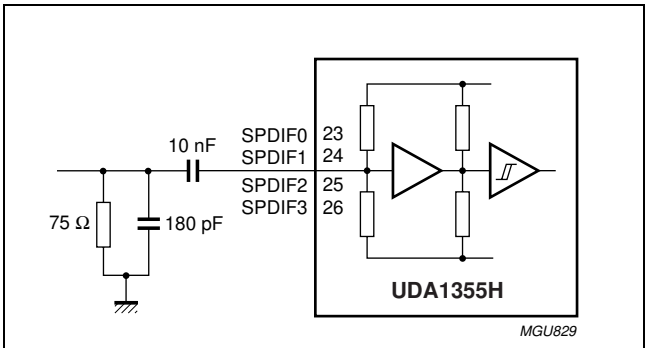


Fig.5 IEC 60958 input circuit.

7.4.1 AUDIO DATA

From the incoming SPDIF bitstream 24 bits of data for the left and right channel are extracted.

There is a hard mute (not a cosine roll-off mute) if the IEC 60958 decoder is out of lock or detects bi-mark phase encoding violations. The lock indicator and the key channel status bits are accessible in L3-bus mode.

The UDA1355H supports the following sample frequencies and data rates, including half and double of these frequencies:

- f_s = 32 kHz; resulting in a data rate of 2.048 Mbit/s
- f_s = 44.1 kHz; resulting in a data rate of 2.8224 Mbit/s
- f_s = 48 kHz; resulting in a data rate of 3.072 Mbit/s.

7.4.2 CHANNEL STATUS AND USER BITS

As well as the data bits there are several IEC 60958 key channel status bits:

- Pre-emphasis and audio sampling frequency bits
- Two channel PCM indicator bits
- Clock accuracy bits.

In total 40 status bits per channel are recovered from the incoming IEC 60958 bitstream. These are readable via the microcontroller interface.

User bits, which can contain a large variety of data, such as CD text, are output to pin SLICER_SEL0 (see Table 4). In microcontroller mode this signal contains the raw user bits extracted from the SPDIF bitstream. Signal U_RDY gives a pulse on pin MODE2 each time there is a new user bit available. Both signals can be used by an external microcontroller to grab and decode the user bits.

Table 4 Signal names in microcontroller mode

PIN NAME	SIGNAL NAME
SLICER_SEL0	USER
MODE2	U_RDY
SLICER_SEL1	AC3

7.4.3 DIGITAL DATA

Audio and digital data can be transmitted in the SPDIF bitstream. The PCM channel status bit should be set to logic 1 if the SPDIF bitstream is carrying digital data instead of audio data, but in practice it proves that not all equipment handles these channel status bits properly.

In the UDA1355H, digital data is detected via bit PCM, or via the sync bytes as specified by IEC. These sync bytes are two sync words, F872H and 4E1FH (two subframes) preceded by four or more subframes filled with zeros. Signal AC3 is kept HIGH for 4096 frames when the UDA1355H detects this burst preamble. Signal AC3 is present on pin SLICER_SEL1 in microcontroller mode (see Table 4).

7.5 IEC 60958 encoder

When using the crystal oscillator clock, the IEC 60958 encoder output is a full-swing digital signal with level II timing.

When the recovered clock from the PLL is used the IEC 60958 encoder will function correctly but will not meet level II timing requirements.

7.5.1 STATIC MODE

All user and channel status bits are set to logic 0. This is default value specified by IEC.

In static mode 0 and 2, the selected SPDIF input channel can be looped through to pin SPDIFOUT (see Fig.6).

7.5.2 MICROCONTROLLER MODE

Two times 40 channel status bits can be set. Default value for each status bit is logic 0. When setting the channel status bits, it is possible to set only the left channel status bits and have the bits copied to the right channel.

The procedure of writing the channel status bits is as follows:

1. Set bit SPDO_VALID = 0 to prevent immediately sending the status bits during writing.
2. Set bit l_r_copy = 1 if the right channel needs the same status bits as the left channel or set bit l_r_copy = 0 if the right channel needs different status bits to the left channel.
3. Write the left and right channel status bits.
4. Set bit SPDO_VALID = 1 after writing all channel status bits to the register. Starting from the next SPDIF block the IEC 60958 encoder will use the new status bits.

In microcontroller modes 2 and 13, the selected SPDIF input channel can be looped through to pin SPDIFOUT (see Fig.6).

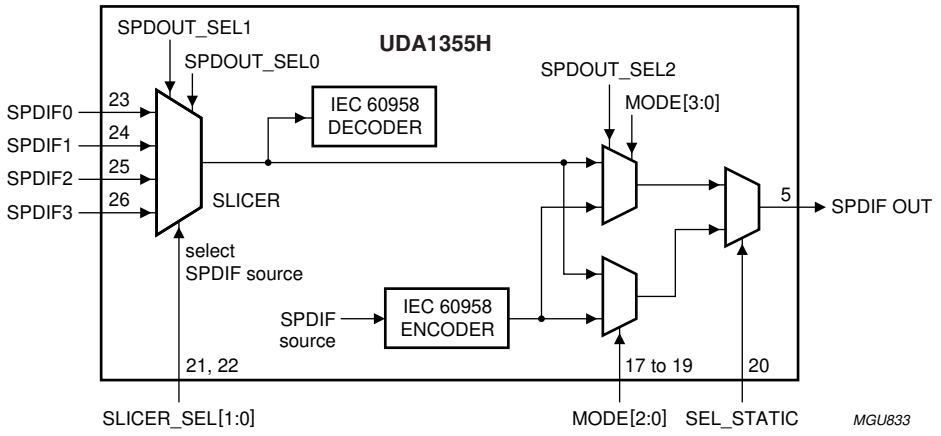


Fig.6 Selection options for SPDIF output.

7.6 Analog input

7.6.1 ADC

The analog input is equipped with a Programmable Gain Amplifier (PGA) which can be controlled via the microcontroller interface. The control range is from 0 to 24 dB gain in 3 dB steps independent for the left and right channels.

In applications in with a 2 V (RMS) input signal, a 12 kΩ resistor must be used in series with the input of the ADC. The 12 kΩ resistor forms a voltage divider together with the internal ADC resistor and ensures that the voltage, applied to the input of the IC, never exceeds 1 V (RMS). In the application for a 2 V (RMS) input signal, the PGA must be set to 0 dB. When a 1 V (RMS) input signal is applied to the ADC in the same application, the PGA gain must be set to 6 dB.

An overview of the maximum input voltages allowed with and without an external resistor and the PGA gain setting is given in Table 5.

Table 5 Maximum input voltage; V_{DD} = 3 V

EXTERNAL RESISTOR (12 kΩ)	PGA GAIN SETTING	MAXIMUM INPUT VOLTAGE
Present	0 dB	2 V (RMS)
	6 dB	1 V (RMS)
Absent	0 dB	1 V (RMS)
	6 dB	0.5 V (RMS)

7.6.2 DECIMATION

The decimation from $64f_s$ is performed in two stages: comb filter and decimation filter. The first stage realizes a fourth-order $\frac{\sin x}{x}$ characteristic with a decimation factor of eight. The second stage consists of three half-band filters each decimating by a factor of two. Table 6 shows the characteristics.

Table 6 Decimation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	±0.02
Stop band	$>0.55f_s$	−60
Dynamic range	0 to $0.45f_s$	140
Overall gain from ADC input to digital output	DC; V_I = 0 dB; note 1	−1.16

Note

1. The output is not 0 dB when $V_{I(rms)}$ = 1 V at V_{DD} = 3 V. This is because the analog components can spread over the process. When there is no external resistor, the −1.16 dB scaling prevents clipping caused by process mismatch.

In the ADC path there are left and right independent digital volume controls with a range from +24 to −63.5 dB and −∞ dB. This volume control is also used as a digital linear mute that can be used to prevent plops when powering-up or powering down the ADC front path.

7.6.3 DC FILTERING

In the decimator there are two digital DC blocking circuits.

The first blocking circuit is in front of the volume control to remove DC bias from the ADC output. The DC bias is added in the ADC to prevent audio band Idle tones occurring in the noise shaper. With the DC components removed, a signal gain of 24 dB can be achieved.

The second blocking circuit removes the DC components introduced by the decimator stage.

7.6.4 OVERLOAD DETECTION

Bit OVERFLOW = 1 when the output data in the left or right channel is larger than −1.16 dB of the maximum possible digital swing. This condition is set for at least $512f_s$ cycles (that is 11.6 ms at f_s = 44.1 kHz). This time-out is reset for each infringement.

7.7 Analog output

7.7.1 AUDIO FEATURE PROCESSOR

The audio feature processor provides automatic de-emphasis for the IEC 60958 bitstream.
In microcontroller mode all features are available and there is a default mute on start up.

7.7.2 INTERPOLATING FILTER

The digital filter interpolates from $1f_s$ to $64f_s$, or from $1f_s$ to $128f_s$, by cascading a half-band filter and a FIR filter.

The stereo interpolator has the following basic features:

- 24-bit data path
- Mixing of two channels:
  - To prevent clipping inside the core, there is an automatic signal level correction of −6 dB scaling before mixing and +6 dB gain after digital volume control
  - Position of mixing can be set before or after bass boost and treble
  - Master volume control and mute with independent left and right channel settings for balance control
  - Independently left and right channel de-emphasis, volume control and mute (no left or right)
  - Output of the mixer is to the I²S-bus or IEC 60958 decoder.
- Full FIR filter implementation for all the upsampling filters
- Integrated digital silence detection for left and right channels with selectable silence detection time
- Support for $1f_s$ and $2f_s$ input data rate and 192 kHz audio via I²S-bus.

The stereo interpolator has the following sound features:

- Linear volume control using 14-bit coefficients with 0.25 dB steps: range 0 to −78 dB and $-\infty$ dB; hold for master volume and mixing volume control
- A cosine roll-off soft mute with 32 coefficients; each coefficient is used for four samples, in total 128 samples are needed to fully mute or de-mute (approximately 3 ms at f_s = 44.1 kHz)
- Independent selectable de-emphasis for 32, 44.1, 48 and 96 kHz for both channels
- Treble is the selectable positive gain for high frequencies. The edge frequency of the treble is fixed and depends on the sampling frequency. Treble can be set independently for left and right channel with two settings:
  - f_c = 1.5 kHz; f_s = 44.1 kHz; 0 to 6 dB gain range with 2 dB steps
  - f_c = 3 kHz; f_s = 44.1 kHz; 0 to 6 dB gain range with 2 dB steps.
- Normal bass boost is the selectable positive gain for low frequencies. The edge frequency of the bass boost is fixed and depends on the sampling frequency. Normal bass boost can be set independently for the left and right channel with two sets:
  - f_c = 250 Hz; f_s = 44.1 kHz; 0 to 18 dB gain range with 2 dB steps
  - f_c = 300 Hz; f_s = 44.1 kHz; 0 to 24 dB gain range with 2 dB steps.
- Resonant bass boost optional function is selected if bit BASS_SEL = 1. When selected, the characteristics are determined by six 14-bit coefficients. Resonant bass boost controls the left and right channel with the same characteristics. When resonant bass boost is selected, the treble control also changes to a single control for both channels following the gain setting of the left channel.

  A software program is available for users to generate the required six 14-bit coefficients by entering the desired centre frequency (f_c), positive or negative peak gain, sampling frequency (f_s) and shape factor (see Figs 7 and 8).

Table 7 Interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	±0.035
Stop band	$>0.55f_s$	−60
Dynamic range	0 to $0.4535f_s$	140

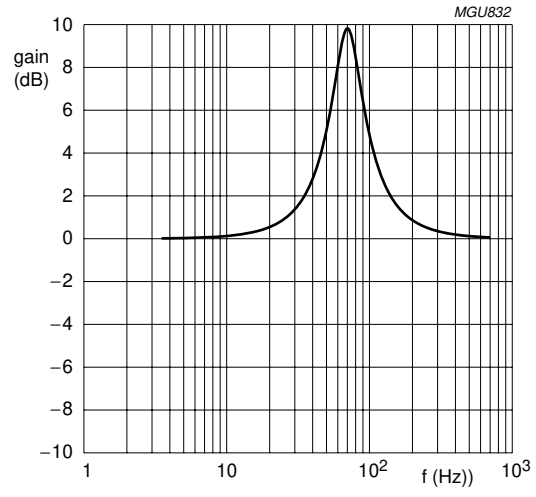
7.7.3 DIGITAL MIXER

The UDA1355H has a digital mixer inside the interpolator. The digital mixer can be used as a cross over or a selector. A functional block diagram of the mixer mode is shown in Fig.9. This mixer can be used in microcontroller mode only.

The UDA1355H can be set to the mixer mode by setting bit MIX = 1. In the mixer mode, there are three volume and mute controls available: for source 1, for source 2 and for the master (sum) signal. All three volume ranges can be controlled in 0.25 dB steps.

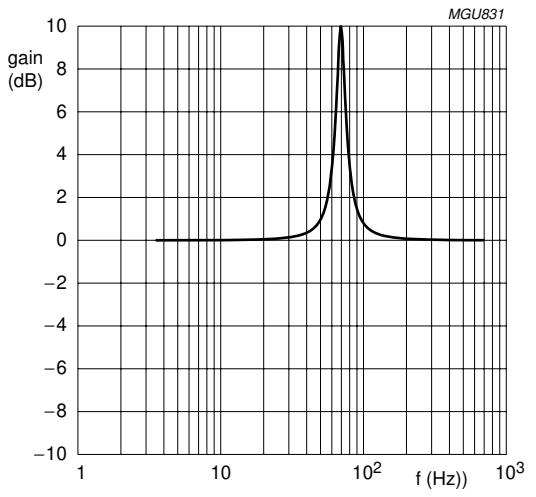
To prevent clipping inside the mixer, the signals are scaled with −6 dB before mixing, therefore the sum of the two signals is always equal to or lower than 0 dB. After the mixing there is a 6 dB gain in the master volume control. This means that at the analog output the signal can clip, but the clipping can be undone by decreasing the master volume control.

The output of the mixer is available via the I^2S-bus output or via the SPDIF output. The output signal of the mixer is scaled to a maximum of 0 dB, so the digital output can never clip.



f_c = 70 Hz Peak gain = 10 dB
f_s = 44.1 kHz Shape factor = 1.4142

Fig.7 Resonant bass boost example 1.



f_c = 70 Hz Peak gain = 10 dB
f_s = 44.1 kHz Shape factor = 1.4142

Fig.8 Resonant bass boost example 2.

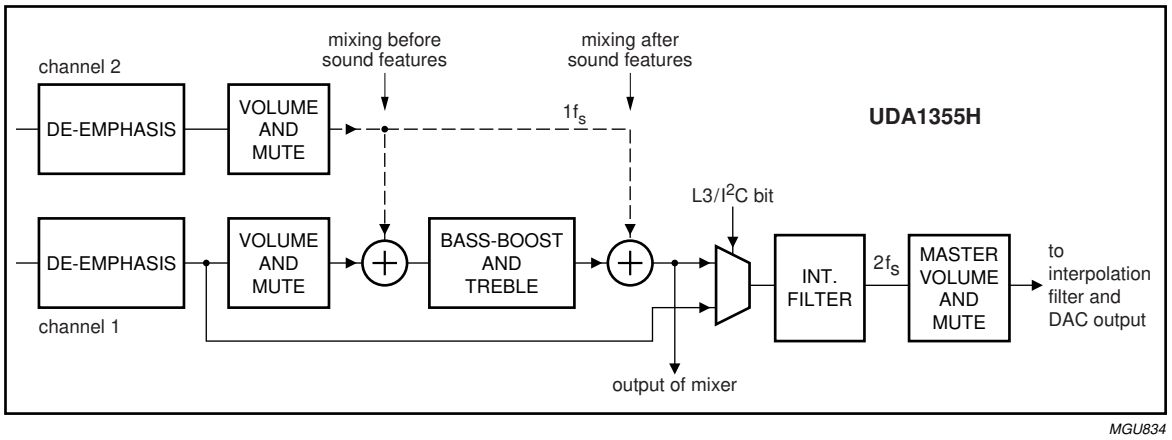


Fig.9 Digital mixer (DAC) inside the interpolator DSP.

7.7.4 Digital silence detector

The UDA1355H is equipped with a digital silence detector. This detects whether a certain amount of consecutive samples are 0. The number of samples can be set with bits SD_VALUE[1:0] to 3200, 4800, 9600 or 19600 samples.

The digital silence detection status can be read via the microcontroller interface.

7.7.5 Noise shaper (DAC)

The noise shaper shifts in-band quantization noise to frequencies above the audio band. The noise shaper output is converted into an analog signal using a Filter Stream Digital-to-Analog Converter (FSDAC). This noise shaping technique enables high signal-to-noise ratios to be achieved.

The UDA1355H is equipped with two noise shapers:

- A third-order noise shaper operating at 128fs. Which is used at low sampling frequencies (8 to 16 kHz) to prevent noise shaper noise shifting into the audio band for the fifth-order noise shaper
- A fifth-order noise shaper operating at $64f_s$. Which is used at high sampling frequencies (from 32 kHz upwards).

When the noise shaper changes, the clock to the FSDAC changes and the filter characteristic of the FSDAC also changes. The effect on the roll of is compensated by selecting the filter matching speed and order of the noise shaper.

7.7.6 Filter stream DAC

The FSDAC is a semi digital reconstruction filter that converts the 1-bit data bitstream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the operational amplifier output. In this way, very high signal-to-noise performance and low clock jitter sensitivity are achieved. A post filter is not needed due to the inherent filter function of the FSDAC. On-chip amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output. The output voltage of the FSDAC scales proportionally with the supply voltage.

7.7.7 DAC mute

The DAC and interpolator can be muted by setting pin MUTE to a HIGH level. The output signal is muted to zero via a cosine roll-off curve and the DAC is powered down. When pin MUTE is at LOW level the signal rise follows the same cosine curve.

To prevent plops in case of changing inputs, clock to the DAC or application modes, a special mute circuit for the DAC is implemented (see Table 8).

In all application modes in which the DAC is active the DAC can be muted by pin MUTE. The microcontroller mute bits and pin MUTE act as an OR function.

Table 8 Muting to prevent plopping

OCCASION	BIT			DE-MUTE CONDITION
	MT1	MT2	MTM	
Input selection				
Select channel 1 source	x	–	–	no mute after selection
Select channel 2 source	–	x	–	no mute after selection
Select chip mode				
PLL is source for the DAC	–	–	x	wait until PLL is locked again
Crystal is source for the DAC	–	–	x	no mute after selection
Select between microcontroller mode and static mode				
PLL is source for the DAC	–	–	x	wait until PLL is locked again
Crystal is source for the DAC	–	–	x	no mute after selection
Audio features				
Select noise shaper order	–	–	x	no mute after selection
Select FSDAC output polarity	–	–	x	no mute after selection
Select SPDIF input	–	–	x	PLL is locked again
Select mixer	–	–	–	no mute needed
Select mixer position	–	–	–	no mute needed
Select crystal clock source	–	–	x	no mute after selection

7.8 Digital audio input and output

The selection of the digital audio input and output formats and master or slave modes differ for static and microcontroller mode.

In master mode, when $256f_s$ output clock is selected and the digital interface is master, the BCK output clock will be $64f_s$. In case $384f_s$ output clock is selected, the BCK output clock will be $48f_s$.

In the static mode the digital audio input formats are:

- I^2S-bus
- LSB-justified; 16 bits
- LSB-justified; 24 bits
- MSB-justified.

The digital audio output formats are:

- I^2S-bus
- MSB-justified.

In the microcontroller mode, the following formats are independently selectable:

- I^2S-bus
- LSB-justified; 16 bits
- LSB-justified; 18 bits
- LSB-justified; 20 bits
- LSB-justified; 24 bits
- MSB-justified.

7.9 Power-on reset

The UDA1355H has a dedicated reset pin with an internal pull-down resistor. In this way a Power-on reset circuit can be made with a capacitor and a resistor at pin RESET. The external resistor is needed since the pad is 5 V tolerant. This means that there is a transmission gate in series with the input and the resistor inside the pad cannot be seen from the outside world (see Fig.10).

The reset timing is determined by the external pull-down resistor and the external capacitor which is connected to pin RESET. At Power-on reset, all the digital sound processing features and the system controlling features are set to the default setting of the microcontroller mode. Since the bit controlling the clock of the synchronous registers is set to enable, the synchronous registers are also reset.

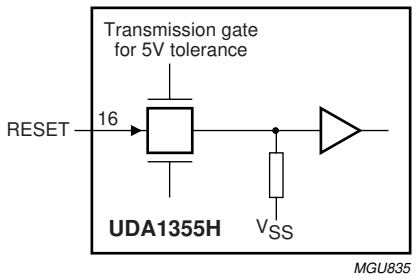


Fig.10 5 V tolerant pull-down input pad.

The clock should be running during the reset time. When no clock can be guaranteed in microcontroller mode, a soft reset should be given when the system is running by writing to register 7FH.

8 APPLICATION MODES

In this chapter the application modes for static mode and microcontroller mode are described.

The UDA1355H can be controlled by static pins, the L3-bus or I²C-bus interface. Due to the limitations imposed by the pin count, only basic functions are available in static mode. For optimum use of the UDA1355H features, the microcontroller mode is strongly recommended.

There are 11 application modes available in the static mode and 14 application modes in microcontroller mode. The application modes are explained in the two sections: Section 8.2 explains the application modes 0 to 10. Section 8.4 explains the more advanced features of modes 0 to 10 and modes 12 to 14 available in the microcontroller mode.

8.1 Static mode pin assignment

The default values for all non-pin controlled settings are identical to the start-up defaults from the microcontroller mode. Whether BCK and WS are master or slave depends on the selected application mode.

Table 9 defines the pin functions in static mode.

Table 9 Static mode pin assignment

PIN	STATIC MODE SYMBOL	LEVEL	DESCRIPTION
4	LOCK	LOW	IEC 60958 decoder out of lock (when SPDIF input) or clock regeneration out of lock (I²S-bus input)
		HIGH	IEC 60958 decoder in lock (when SPDIF input) or clock regeneration in lock (I²S-bus input)
16	RESET	LOW	normal operation
		HIGH	reset
17, 18, 19	MODE0, MODE1, MODE2	–	select application mode; see Table 10
20	SEL_STATIC	HIGH	static pin control
		LOW	microcontroller mode
22, 21	SLICER_SEL1, SLICER_SEL0	LOW, LOW	IEC 60958 input from pin SPDIF0
		LOW, HIGH	IEC 60958 input from pin SPDIF1
		HIGH, LOW	IEC 60958 input from pin SPDIF2
		HIGH, HIGH	IEC 60958 input from pin SPDIF3
29	FREQ_SEL	LOW	select 44.1 kHz sampling frequency for the crystal oscillator, note 1
		MID	select 32 kHz sampling frequency for the crystal oscillator, note 1
		HIGH	select 48 kHz sampling frequency for the crystal oscillator, note 1

PIN	STATIC MODE SYMBOL	LEVEL	DESCRIPTION
30, 31	SFOR1, SFOR0	LOW, LOW	set I^2S-bus format for digital data input and output interface
		LOW, HIGH	set LSB-justified 16 bits format for digital data input interface and MSB-justified format for digital data output interface
		HIGH, LOW	set LSB-justified 24 bits format for digital data input interface and MSB-justified format for digital data output interface
		HIGH, HIGH	set MSB-justified format for digital data input and output interface
44	MUTE	LOW	normal operation
		HIGH	mute active

Note

1. FPLL 256fs is output from pin CLKOUT in PLL locked static mode.

8.2 Static mode basic applications

The static application modes are selected with the pins MODE2, MODE1 and MODE0, with pin MODE0 being a 3-level pin. In Table 10, the encoding of the pins MODE[2:0] is given.

Table 10 Static mode basic applications

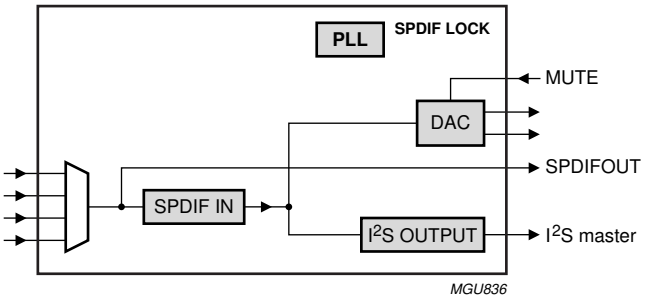
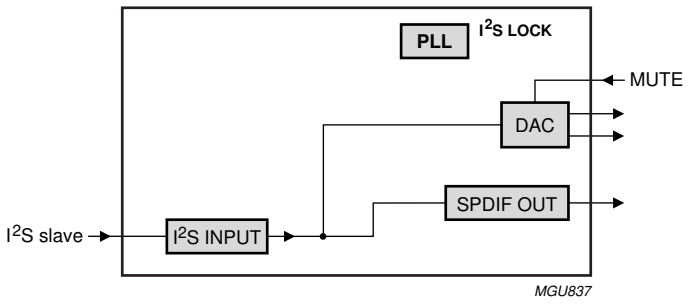
MODE	MODE SELECTION PINS(1)			CLOCK(2)						PLL LOCKS ON INPUT
	MODE2	MODE1	MODE0	SPDIF INPUT	SPDIF OUTPUT	ADC	DAC	I^2S-BUS INPUT SLAVE	I^2S-BUS OUTPUT MASTER	
0	L	L	L	PLL	PLL	–	PLL	–	PLL	SPDIF
1	L	L	M	–	PLL	–	PLL	PLL	–	I^2S-bus
2	L	L	H	PLL	PLL	–	PLL	PLL	PLL	SPDIF
3	L	H	L	–	xtal	xtal	–	–	xtal	–
4	L	H	M	–	xtal	xtal	xtal	xtal	xtal	–
5	L	H	H	–	xtal	xtal	xtal	xtal	xtal	–
6	H	L	L	–	PLL	xtal	PLL	PLL	xtal	I^2S-bus
7	H	L	M	PLL	xtal	xtal	PLL	–	xtal	SPDIF
8	H	L	H	–	xtal	xtal	PLL	PLL	xtal	I^2S-bus
9	H	H	L	PLL	xtal	–	xtal	xtal	PLL	SPDIF
10	H	H	M	PLL	xtal	–	PLL	xtal	PLL	SPDIF
11	H	H	H	not used						

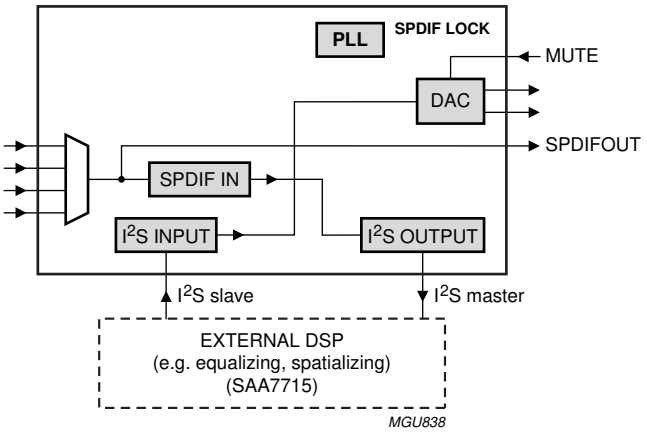
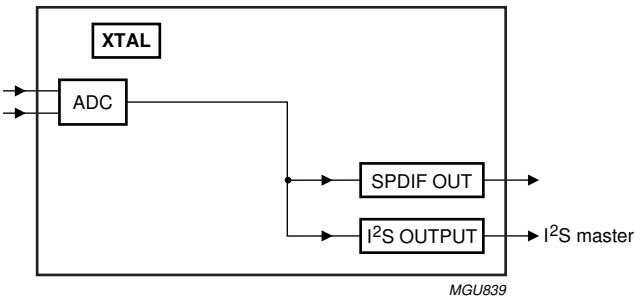
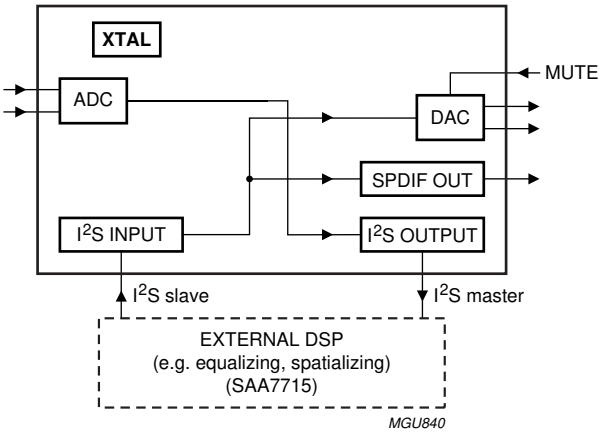
Notes

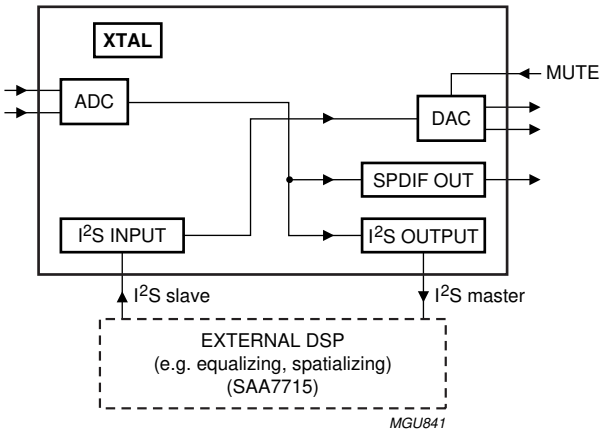
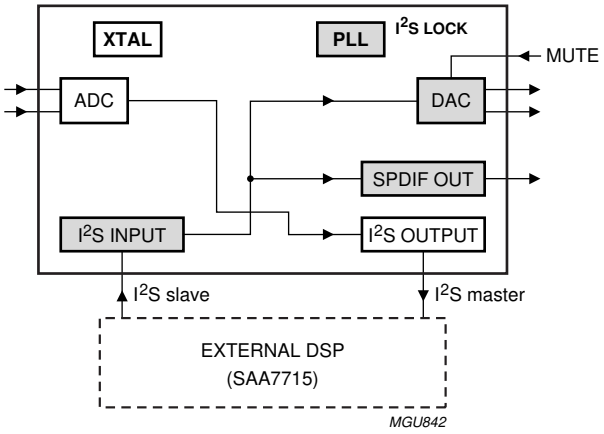
1. In column mode selection pins means:
   L: pin at 0 V; M: pin at half V_{DDD}; H: pin at V_{DDD}.
2. In column clock means:
   xtal: the clock is based on the crystal oscillator; PLL: the clock is based on the PLL.

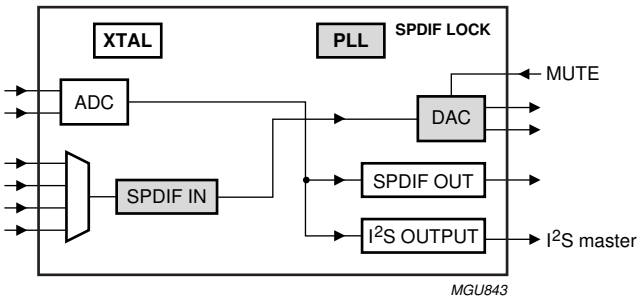
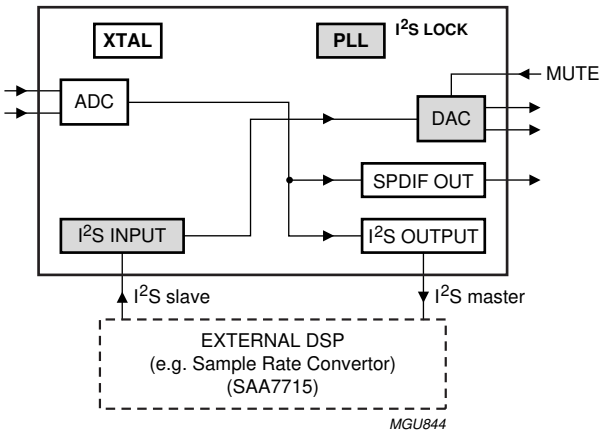
The first 11 application modes are given in this section. Schematic diagrams of these application modes are given in Table 11. In this table the basic features are mentioned and also the extra features in case of microcontroller mode are given. It should be noted that the blocks running at the crystal clock (XTAL) are marked unshaded while the blocks running at the PLL clock are shaded.

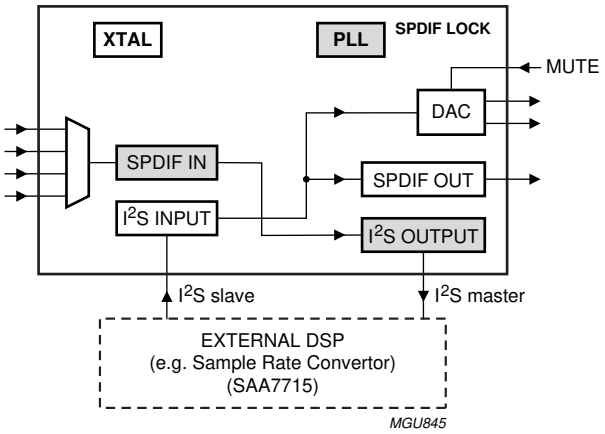
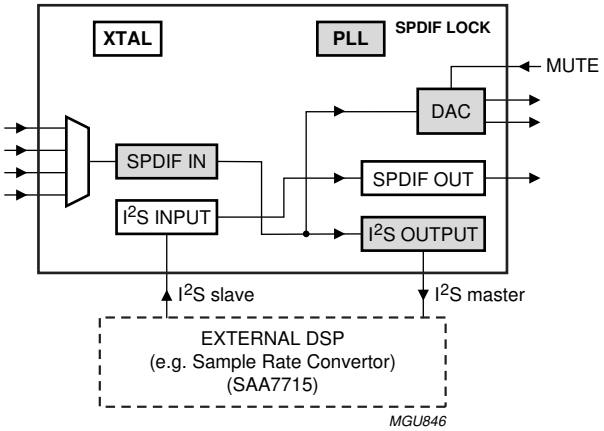
Table 11 Overview of static mode basic applications

MODE	FEATURES	SCHEMATIC
0	Data path: • Input SPDIF to outputs DAC, I^2S or SPDIFOUT via loop through. Features: • System locks onto the SPDIF input signal • BCK and WS are master • Microcontroller mode: – DAC sound features can be used – SPDIF input channel status bits (two times 40 bits) can be read.	
1	Data path: • Input I^2S to outputs DAC or SPDIF (level II not guaranteed: depends on I^2S-bus clock). Features: • System locks onto the WSI signal • BCKI and WSI are slave • Microcontroller mode: – DAC sound features can be used – SPDIF output channel status bits (two times 40 bits) setting.	

MODE	FEATURES	SCHEMATIC
2	Data path: • Input SPDIF to outputs I²S or SPDIFOUT via loop through • Input I²S to output DAC. Features: • Possibility to process input SPDIF via I²S-bus using an external DSP and then to output DAC • System locks onto the SPDIF input signal • I²S input and output with BCK and WS are master • Microcontroller mode: see Section 8.4.	
3	Data path: • Input ADC to outputs I²S or SPDIF. Features: • Crystal oscillator generates the clocks • Microcontroller mode: – PGA gain setting – Volume control in decimator setting – SPDIF output channel status bits (two times 40 bits) setting.	
4	Data path: • Input ADC to output I²S • Input I²S to outputs DAC or SPDIF. Features: • Possibility to process input ADC via I²S-bus using a external DSP and then to outputs DAC or SPDIF • Crystal oscillator generates the clocks • I²S input and output with BCK and WS are master • Microcontroller mode: see Section 8.4.	

MODE	FEATURES	SCHEMATIC
5	Data path: • Input ADC to outputs I²S or SPDIF • Input I²S to output DAC. Features: • Possibility to process input ADC via I²S-bus using an external DSP and then to output DAC • Crystal oscillator generates the clocks • I²S input and output with BCK and WS are master • Microcontroller mode: see Section 8.4.	
6	Data path: • Input ADC to output I²S • Input I²S to outputs DAC or SPDIF (level II not guaranteed: depends on I²S-bus clock). Features: • Possibility to process input ADC via I²S-bus using an external DSP and then to outputs DAC or SPDIF • Crystal oscillator generates the clocks for input ADC and output I²S • WSI is slave • WSO is master • Microcontroller mode: see Section 8.4.	

MODE	FEATURES	SCHEMATIC
7	Data path: • Input SPDIF to output DAC • Input ADC to outputs SPDIF or I²S. Features: • Crystal oscillator generates the clocks for outputs SPDIF and I²S • PLL locks onto the SPDIF input signal • WS of I²S output is master • Microcontroller mode: – Decimator features can be used – DAC sound features can be used – SPDIF input channel status bits (two times 40 bits) can be read – SPDIF output channel status bits (two times 40 bits) setting.	
8	Data path: • Input ADC to outputs SPDIF or I²S • Input I²S to output DAC. Features: • Possibility to process input ADC, via I²S-bus using an external DSP and then to output DAC • Crystal oscillator generates the clocks for outputs SPDIF and I²S • WSI is slave • WSO master • Microcontroller mode: – Decimator features can be used – DAC sound features can be used – SPDIF output channel status bits (two times 40 bits) setting.	

MODE	FEATURES	SCHEMATIC
9	Data path: • Input SPDIF to output I^2S • Input I^2S to outputs DAC or SPDIF. Features: • Possibility to process input SPDIF, via I^2S-bus using an external DSP and then to outputs DAC or SPDIF • BCK and WS being master for both I^2S input and output (different clocks) • Input I^2S to outputs DAC and SPDIF; BCK and WS being master; clocks based on crystal oscillator • Microcontroller mode: – DAC sound features can be used – SPDIF output channel status bits (two times 40) setting.	
10	Data path: • Input SPDIF to output DAC or I^2S • Input I^2S-bus to output SPDIF. Features: • Possibility to process input SPDIF, via I^2S-bus using an external DSP and then to output SPDIF • Input SPDIF to outputs I^2S and DAC; locking onto the SPDIF input signal; BCK and WS being master • Input I^2S to output SPDIF; BCK and WS being master; clocks are generated by the crystal oscillator • Microcontroller mode: – DAC sound features can be used – SPDIF input channel status bits (two times 40) can be read – SPDIF output channel status bits (two times 40) setting.	
11	Not used	
12	See microcontroller mode	
13	See microcontroller mode	
14	See microcontroller mode	
15	Not used	