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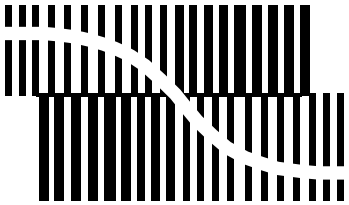
# DATA SHEET


# UDA1380
## Stereo audio coder-decoder for MD, CD and MP3

Product specification
Supersedes data of 2003 Apr 04

2004 Apr 22

# Stereo audio coder-decoder for MD, CD and MP3

# UDA1380

**CONTENTS**

## 1 FEATURES

### 1.1 General

- 2.4 to 3.6 V power supply
- 5 V tolerant digital inputs (at 2.7 to 3.6 V power supply)
- 24-bit data path for Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC)
- Selectable control via L3-bus microcontroller interface or I²C-bus interface; choice of 2 device addresses in L3-bus and I²C-bus mode

  **Remark**: This device does not have a static mode.
- Supports sample frequencies from 8 to 55 kHz for the ADC part, and 8 to 100 kHz for the DAC part. The ADC does not support DVD audio (96 kHz audio), only Mini-Disc (MD), Compact-Disc (CD) and Moving Picture Experts Group Layer-3 Audio (MP3). For playback 8 to 100 kHz is specified. DVD playback is supported
- Power management unit:
  - Separate power control for ADC, Automatic Volume Control (AVC), DAC, Phase Locked Loop (PLL) and headphone driver
  - Analog blocks like ADC and Programmable Gain Amplifier (PGA) have a block to power-down the bias circuits
  - When ADC and/or DAC are powered-down, the clocks to these blocks are also stopped to save power.

  **Remark:** By default, when the IC is powered-up, the complete chip will be in the Power-down mode.
- ADC part and DAC part can run at different frequencies, either system clock or Word Select PLL (WSPLL)
- ADC and PGA plus integrated high-pass filter to cancel DC offset
- The decimation filter is equipped with a digital Automatic Gain Control (AGC)
- Mono microphone input with Low Noise Amplifier (LNA) of 29 dB fixed gain and Variable Gain Amplifier (VGA) from 0 to 30 dB in steps of 2 dB
- Integrated digital filter plus DAC
- Separate single-ended line output and one stereo headphone output, capable of driving a 16 Ω load. The headphone driver has a built-in short-circuit protection with status bits which can be read out from the L3-bus or I²C-bus interface
- Digital silence detection in the interpolator (playback) with read-out status via L3-bus or I²C-bus interface
- Easy application.

BITSTREAM CONVERSION

### 1.2 Multiple format data input interface

- Slave BCK and WS signals
- I²S-bus format
- MSB-justified format compatible
- LSB-justified format compatible.

### 1.3 Multiple format data output interface

- Select option for digital output interface: either the decimator output (ADC signal) or the output signal of the digital mixer which is in the interpolator DSP
- Selectable master or slave BCK and WS signals for digital ADC output

  **Remark**: SYSCLK must be applied in WSPLL mode and master mode
- I²S-bus format
- MSB-justified format compatible
- LSB-justified format compatible.

### 1.4 ADC front-end features

- ADC plus decimator can run at either WSPLL, regenerating the clock from WSI signal, or on SYSCLK
- Stereo line input with PGA: gain range from 0 to 24 dB in steps of 3 dB
- LNA with 29 dB fixed gain for mono microphone input, including VGA with gain from 0 to 30 dB in steps of 2 dB
- Digital left and right independent volume control and mute from +24 to −63.5 dB in steps of 0.5 dB.

### 1.5 DAC features

- DAC plus interpolator can run at either WSPLL (regenerating the clock from WSI) or at SYSCLK
- Separate digital logarithmic volume control for left and right channels via L3-bus or I²C-bus from 0 to −78 dB in steps of 0.25 dB
- Digital tone control, bass boost and treble via L3-bus or I²C-bus interface
- Digital de-emphasis for sample frequencies of: 32, 44.1, 48 and 96 kHz via L3-bus or I²C-bus interface
- Cosine roll-off soft mute function
- Output signal polarity control via L3-bus or I²C-bus interface
- Digital mixer for mixing ADC output signal and digital serial input signal, if they run at the same sampling frequency.

## 2 APPLICATIONS

This audio coder-decoder is suitable for home and portable applications like MD, CD and MP3 players.

## 3 GENERAL DESCRIPTION

The UDA1380 is a stereo audio coder-decoder, available in TSSOP32 (UDA1380TT) and HVQFN32 (UDA1380HN) packages. All functions and features are identical for both package versions. The term ‘UDA1380’ in this document refers to both UDA1380TT and UDA1380HN, unless particularly specified.

The front-end of the UDA1380 is equipped with a stereo line input, which has a PGA control, and a mono microphone input with an LNA and a VGA. The digital decimation filter is equipped with an AGC which can be used in case of voice-recording.

The DAC part is equipped with a stereo line output and a headphone driver output. The headphone driver is capable of driving a 16 Ω load. The headphone driver is also capable of driving a headphone without the need for external DC decoupling capacitors, since the headphone can be connected to a pin $V_{REF(HP)}$ on the chip.

In addition, there is a built-in short-circuit protection for the headphone driver output which, in case of short-circuit, limits the current through the operational amplifiers and signals the event via its L3-bus or I²C-bus register.

The UDA1380 also supports an application mode in which the coder-decoder itself is not running, but an analog signal, for instance coming from an FM tuner, can be controlled in gain and applied to the output via the headphone driver and line outputs.

The UDA1380 supports the I²S-bus data format with word lengths of up to 24 bits, the MSB-justified data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 18, 20 or 24 bits (LSB-justified 24 bits is only supported for the output interface).

The UDA1380 has sound processing features in playback mode, de-emphasis, volume, mute, bass boost and treble which can be controlled by the L3-bus or I²C-bus interface.

## 4 QUICK REFERENCE DATA

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = V_{DDA(HP)} = 3.0$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages measured with respect to ground; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DDA(AD)}$ | ADC analog supply voltage | | 2.4 | 3.0 | 3.6 | V |
| $V_{DDA(DA)}$ | DAC analog supply voltage | | 2.4 | 3.0 | 3.6 | V |
| $V_{DDA(HP)}$ | headphone analog supply voltage | note 1 | 2.4 | 3.0 | 3.6 | V |
| $V_{DDD}$ | digital supply voltage | | 2.4 | 3.0 | 3.6 | V |
| $I_{DDA(AD)}$ | ADC analog supply current | one ADC and microphone amplifier enabled; $f_s = 48$ kHz | – | 4.5 | – | mA |
| | | two ADCs and PGA enabled; $f_s = 48$ kHz | – | 7.0 | – | mA |
| | | all ADCs and PGAs power-down, but AVC activated; $f_s = 48$ kHz | – | 3.3 | – | mA |
| | | all ADCs, PGAs and LNA power-down; $f_s = 48$ kHz | – | 1.0 | – | μA |
| $I_{DDA(DA)}$ | DAC analog supply current | operating mode; $f_s = 48$ kHz | – | 3.4 | – | mA |
| | | Power-down mode; $f_s = 48$ kHz | – | 0.1 | – | μA |
| $I_{DDA(HP)}$ | headphone analog supply current | no signal applied (quiescent current) | – | 0.9 | – | mA |
| | | Power-down mode | – | 0.1 | – | μA |
| $I_{DDD}$ | digital supply current | operating mode; $f_s = 48$ kHz | – | 10.0 | – | mA |
| | | playback mode; $f_s = 48$ kHz | – | 5.0 | – | mA |
| | | record mode; $f_s = 48$ kHz | – | 6.0 | – | mA |
| | | Power-down mode; $f_s = 48$ kHz | – | 1.0 | – | μA |
| $I_{DD(tot)}$ | total supply current | playback mode (without headphone); $f_s = 48$ kHz | – | 8 | – | mA |
| | | playback mode (with headphone); no signal; $f_s = 48$ kHz | – | 9 | – | mA |
| | | record mode (audio); $f_s = 48$ kHz | – | 13 | – | mA |
| | | record mode (speech); $f_s = 48$ kHz | – | 10 | – | mA |
| | | record mode (audio and speech); $f_s = 48$ kHz | – | 13 | – | mA |
| | | fully operating; $f_s = 48$ kHz | – | 23 | – | mA |
| | | signal mix-in operating, using FSDAC, AVC (with headphone); no signal; $f_s = 48$ kHz | – | 12 | – | mA |
| | | Power-down mode; $f_s = 48$ kHz | – | 2 | – | μA |
| $T_{amb}$ | ambient temperature | | −40 | – | +85 | °C |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Analog-to-digital converter (supply voltage 3.0 V)** | | | | | | |
| $D_o$ | digital output level | at 0 dB setting; $V_{i(rms)}$ = 1.0 V | −1.5 | −1 | −0.5 | dBFS |
| (THD+N)/$S_{48}$ | total harmonic distortion-plus-noise to signal ratio at $f_s$ = 48 kHz | at −1 dBFS | − | −85 | −80 | dB |
| | | at −60 dBFS; A-weighted | − | −37 | −32 | dB |
| $S/N_{48}$ | signal-to-noise ratio at $f_s$ = 48 kHz | $V_i$ = 0 V; A-weighted | 92 | 97 | − | dB |
| $\alpha_{cs}$ | channel separation | | − | 100 | − | dB |
| **LNA input plus analog-to-digital converter (supply voltage 3.0 V)** | | | | | | |
| $V_{i(rms)}$ | input voltage (RMS value) | at 0 dBFS digital output; 2.2 kΩ source impedance | − | − | 35 | mV |
| (THD+N)/$S_{48}$ | total harmonic distortion-plus-noise to signal ratio at $f_s$ = 48 kHz | at 0 dB | − | −74 | − | dB |
| | | at −60 dB; A-weighted | − | −25 | − | dB |
| $S/N_{48}$ | signal-to-noise ratio at $f_s$ = 48 kHz | $V_i$ = 0 V; A-weighted | − | 85 | − | dB |
| $\alpha_{cs}$ | channel separation | | − | 70 | − | dB |
| **Digital-to-analog converter (supply voltage 3.0 V)** | | | | | | |
| $V_{o(rms)}$ | output voltage (RMS value) | at 0 dBFS digital input; note 2 | − | 0.9 | − | V |
| (THD+N)/$S_{48}$ | total harmonic distortion-plus-noise to signal ratio at $f_s$ = 48 kHz | at 0 dB | − | −85 | −80 | dB |
| | | at −60 dB; A-weighted | − | −40 | −35 | dB |
| (THD+N)/$S_{96}$ | total harmonic distortion-plus-noise to signal ratio at $f_s$ = 96 kHz | at 0 dB | − | −80 | −75 | dB |
| | | at −60 dB; A-weighted | − | −37 | −32 | dB |
| $S/N_{48}$ | signal-to-noise ratio at $f_s$ = 48 kHz | code = 0; A-weighted | 95 | 100 | − | dB |
| $S/N_{96}$ | signal-to-noise ratio at $f_s$ = 96 kHz | code = 0; A-weighted | 92 | 97 | − | dB |
| $\alpha_{cs}$ | channel separation | | − | 90 | − | dB |
| **AVC (line input via ADC input; output on line output and headphone driver; supply voltage 3.0 V)** | | | | | | |
| $V_{i(rms)}$ | input voltage (RMS value) | | − | 150 | − | mV |
| (THD+N)/$S_{48}$ | total harmonic distortion-plus-noise to signal ratio at $f_s$ = 48 kHz | at 0 dB | − | −80 | − | dB |
| | | at −60 dB; A-weighted | − | −28 | − | dB |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $S/N_{48}$ | signal-to-noise ratio at $f_s$ = 48 kHz | $V_i$ = 0 V; A-weighted | – | 87 | – | dB |
| **Headphone driver (supply voltage 3.0 V)** | | | | | | |
| $P_{o(rms)}$ | output power (RMS value) | at 0 dBFS digital input; $R_L$ = 16 Ω | 30 | 35 | 40 | mW |
| $(THD+N)/S_{48}$ | total harmonic distortion-plus-noise to signal ratio at $f_s$ = 48 kHz | at 0 dB; $R_L$ = 16 Ω; note 1 | – | −60 | −52 | dB |
| | | at 0 dB; $R_L$ = 5 kΩ | – | −82 | −77 | dB |
| | | at −60 dB; A-weighted | – | −33 | −27 | dB |
| $S/N_{48}$ | signal-to-noise ratio at $f_s$ = 48 kHz | code = 0; A-weighted | 87 | 93 | – | dB |
| $\alpha_{cs}$ | channel separation | $R_L$ = 16 Ω using pin $V_{REF(HP)}$; no DC decoupling capacitors; note 3 | 55 | 60 | – | dB |
| | | $R_L$ = 16 Ω single-ended application with DC decoupling capacitors (100 μF typical) | 63 | 68 | – | dB |
| | | $R_L$ = 32 Ω single-ended application with DC decoupling capacitors (100 μF typical) | 69 | 74 | – | dB |
| **Power consumption (supply voltage 3.0 V; $f_s$ = 48 kHz)** | | | | | | |
| $P_{tot}$ | total power dissipation | playback mode (without headphone) | – | 24 | – | mW |
| | | playback mode (with headphone) | – | 27 | – | mW |
| | | record mode (audio) | – | 39 | – | mW |
| | | record mode (speech) | – | 30 | – | mW |
| | | record mode (audio and speech) | – | 40 | – | mW |
| | | full operation | – | 69 | – | mW |
| | | Power-down mode | – | 6 | – | μW |

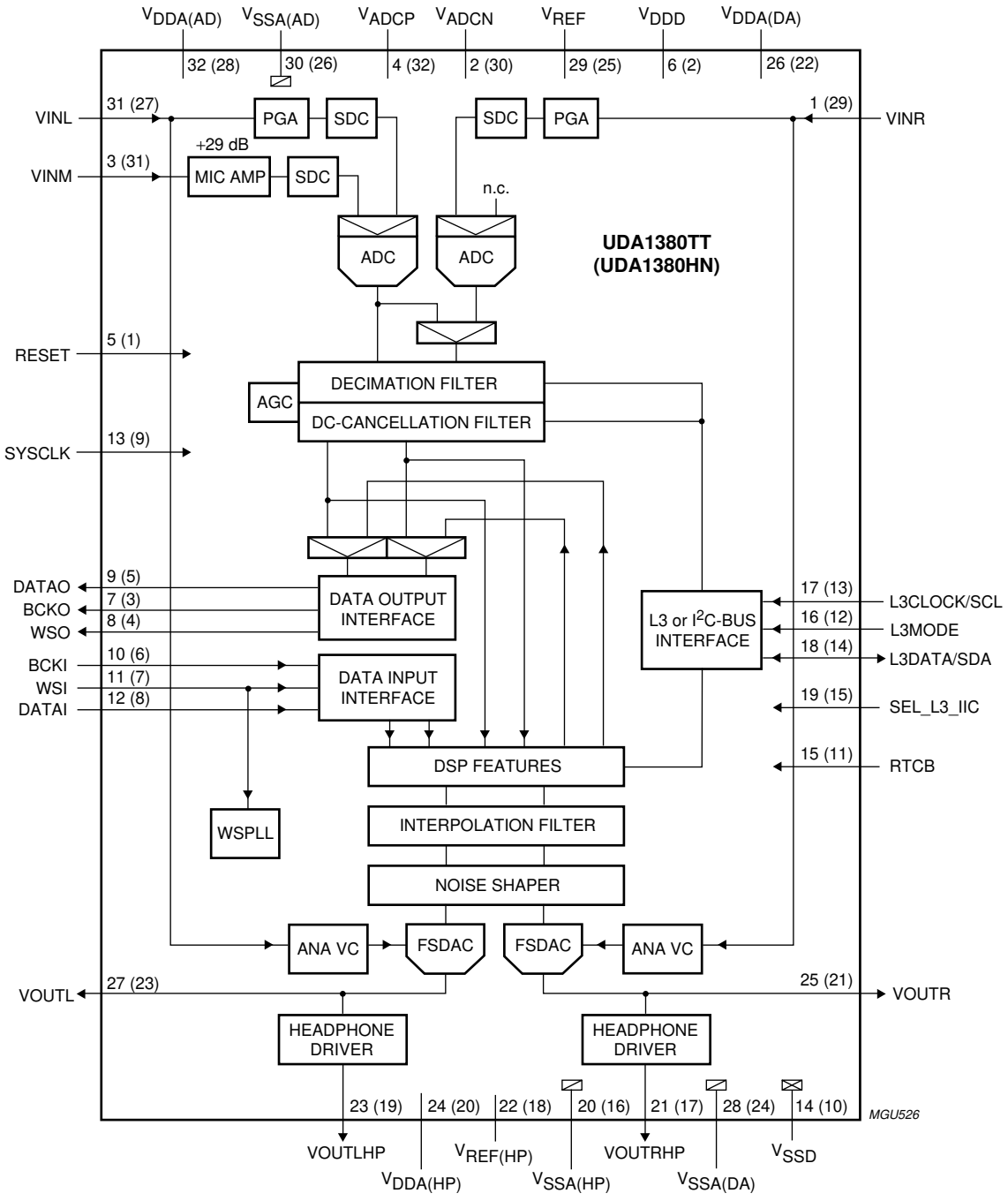
**Notes**

1. When the supply voltages are below 2.7 V and the headphone load impedance is 16 Ω, it is recommended to limit the DAC and the headphone output to less than -2dB; otherwise clipping may occur.
2. The output voltage of the DAC is proportional to the DAC power supply voltage.
3. Channel separation performance is measured at the IC pin.

## 5 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| UDA1380TT | TSSOP32 | plastic thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm | SOT487-1 |
| UDA1380HN | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm | SOT617-1 |

## 6 BLOCK DIAGRAM




Pin numbers for UDA1380HN in parentheses.

Fig.1 Block diagram.

## 7 PINNING

| SYMBOL | PIN | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| | UDA1380TT | UDA1380HN | | |
| VINR | 1 | 29 | analog pad | ADC input right, also connected to the mixer input of the FSDAC |
| $V_{ADCN}$ | 2 | 30 | analog pad | ADC reference voltage |
| VINM | 3 | 31 | analog pad | microphone input |
| $V_{ADCP}$ | 4 | 32 | analog pad | ADC reference voltage |
| RESET | 5 | 1 | 5 V tolerant digital input pad; push-pull; TTL with hysteresis; pull-down | pin RESET with pull-down, for making Power-On Reset (POR) |
| $V_{DDD}$ | 6 | 2 | digital supply pad | digital supply voltage |
| BCKO | 7 | 3 | 5 V tolerant digital bidirectional pad; push-pull input; 3-state output; 5 ns slew-rate control; TTL with hysteresis | bit clock output |
| WSO | 8 | 4 | | word select output |
| DATAO | 9 | 5 | output pad; push-pull; 5 ns slew-rate control; CMOS | data output |
| BCKI | 10 | 6 | 5 V tolerant digital input pad; push-pull; TTL with hysteresis | bit clock input |
| WSI | 11 | 7 | | word select input |
| DATAI | 12 | 8 | | data input |
| SYSCLK | 13 | 9 | | system clock $256f_s$, $384f_s$, $512f_s$ or $768f_s$ input |
| $V_{SSD}$ | 14 | 10 | digital ground pad | digital ground |
| RTCB | 15 | 11 | 5 V tolerant digital input pad; push-pull; TTL with hysteresis; pull-down | test control input, to be connected to digital ground in the application |
| L3MODE | 16 | 12 | 5 V tolerant digital bidirectional pad; push-pull input; 3-state output; 5 ns slew-rate control; TTL with hysteresis | L3-bus mode input or pin A1 for $I^2C$-bus slave address setting |
| L3CLOCK/SCL | 17 | 13 | 5 V tolerant digital input pad; push-pull; TTL with hysteresis | L3-bus or $I^2C$-bus clock input |
| L3DATA/SDA | 18 | 14 | $I^2C$-bus pad; 400 kHz $I^2C$-bus specification | L3-bus or $I^2C$-bus data input and output |
| SEL_L3_IIC | 19 | 15 | 5 V tolerant digital input pad; push-pull; TTL with hysteresis | input channel select |
| $V_{SSA(HP)}$ | 20 | 16 | analog ground pad | headphone ground |
| VOUTRHP | 21 | 17 | analog pad | headphone output right |
| $V_{REF(HP)}$ | 22 | 18 | analog pad | headphone reference voltage |
| VOUTLHP | 23 | 19 | analog pad | headphone output left |
| $V_{DDA(HP)}$ | 24 | 20 | analog supply pad | headphone supply voltage |
| VOUTR | 25 | 21 | analog pad | DAC output right |
| $V_{DDA(DA)}$ | 26 | 22 | analog supply pad | DAC analog supply voltage |
| VOUTL | 27 | 23 | analog pad | DAC output left |

| SYMBOL | PIN | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| | UDA1380TT | UDA1380HN | | |
| $V_{SSA(DA)}$ | 28 | 24 | analog ground pad | DAC analog ground |
| $V_{REF}$ | 29 | 25 | analog pad | ADC and DAC reference voltage |
| $V_{SSA(AD)}$ | 30 | 26 | analog ground pad | ADC analog ground |
| VINL | 31 | 27 | analog pad | ADC input left, also connected to the mixer input of the FSDAC |
| $V_{DDA(AD)}$ | 32 | 28 | analog supply pad | ADC analog supply voltage |

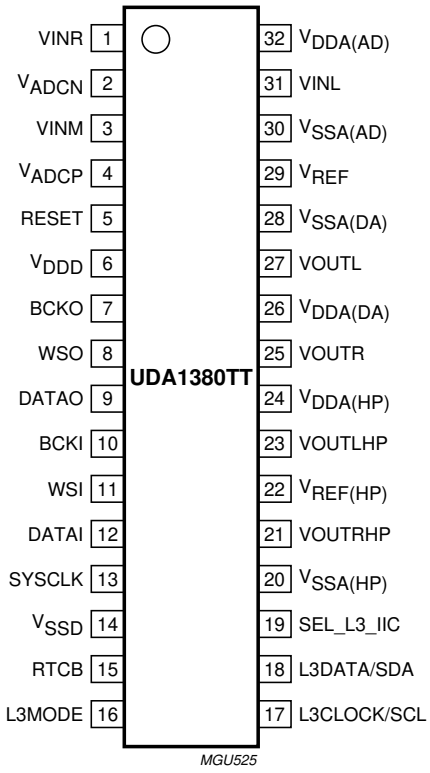



Fig.2 Pin configuration UDA1380TT.

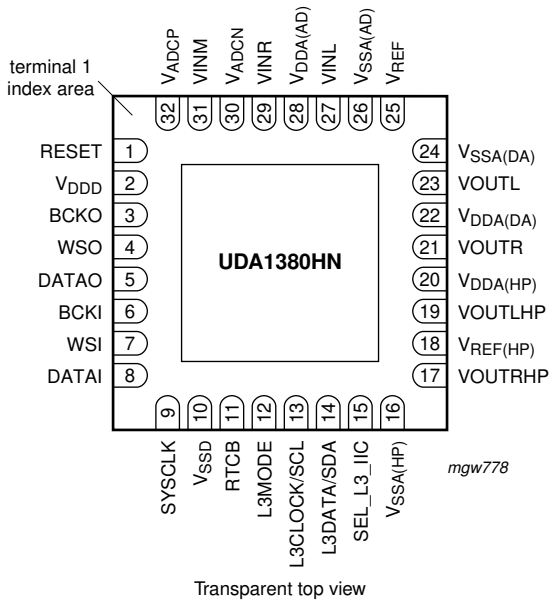



Fig.3 Pin configuration UDA1380HN.

## 8 FUNCTIONAL DESCRIPTION

### 8.1 Clock modes

There are two clock systems:

- A SYSCLK signal, coming from the system
- A WSPLL which generates the internal clocks from the incoming WSI signal.

The system frequency applied to pin SYSCLK is selectable. The options are $256f_s$, $384f_s$, $512f_s$ and $768f_s$. The system clock must be locked in frequency to the digital interface signals.

**Remark**: Since there is neither a fixed reference clock available in the IC itself, nor a fixed clock available in the system the IC is in, there is no auto sample rate conversion detection circuitry.

The system can run in several modes, using the two clock systems:

- Both the DAC and the ADC part can run at the applied SYSCLK input. In this case the WSPLL is powered-down
- The ADC can run at the SYSCLK input, and at the same time the DAC part can run (at a different frequency) at the clock re-generated from the WSI signal
- The ADC and the DAC can both run at the clock regenerated from the WSI signal.

#### 8.1.1 WSPLL REQUIREMENTS

The WSPLL is meant to lock onto the WSI input signal, and regenerates $256f_s$ and $128f_s$ signals for the FSDAC and the interpolator core (and for the decimator if needed). Since the operating range of the WSPLL is from 75 to 150 MHz, the complete range of 8 to 100 kHz sampling frequency must be divided into smaller parts, as given in Table 1, using Fig.4 as a reference. This means that the user must set the input range of the WSI input signal.

In case the SYSCLK is used for clocking the complete system (decimator including interpolator) the WSPLL must be powered-down with bit ADC_CLK via the L3-bus or I²C-bus.

The SEL_LOOP_DIV[1:0] can be controlled by the PLL1 and PLL0 bits in the L3-bus or I²C-bus register.

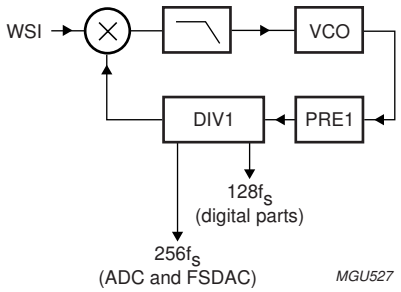



Fig.4 WSPLL set-up.

**Table 1** WSPLL divider settings

| WORD SELECT FREQUENCY (kHz) | SEL_LOOP_DIV[1:0] | PRE1 | DIV1 | VCO FREQUENCY (MHz) |
|---|---|---|---|---|
| 6.25 to 12.5 | 00 | 8 | 1536 | 76 to 153 |
| 12.5 to 25 | 01 | 4 | 1536 | |
| 25 to 50 | 10 | 2 | 1536 | |
| 50 to 100 | 11 | 2 | 768 | |

### 8.1.2 CLOCK DISTRIBUTION

Figure 5 shows the main clock distribution for the SYSCLK domain and the WSPLL clock domain.

For power saving reasons each clock signal inside the system must be controlled and enabled via a separate bit in the L3-bus and I²C-bus registers (ADC_CLK).

The DAC part of the UDA1380 can operate from 8 to 100 kHz sampling frequency ($f_s$). This applies to the DAC part only; the ADC part can run from 8 to 55 kHz.

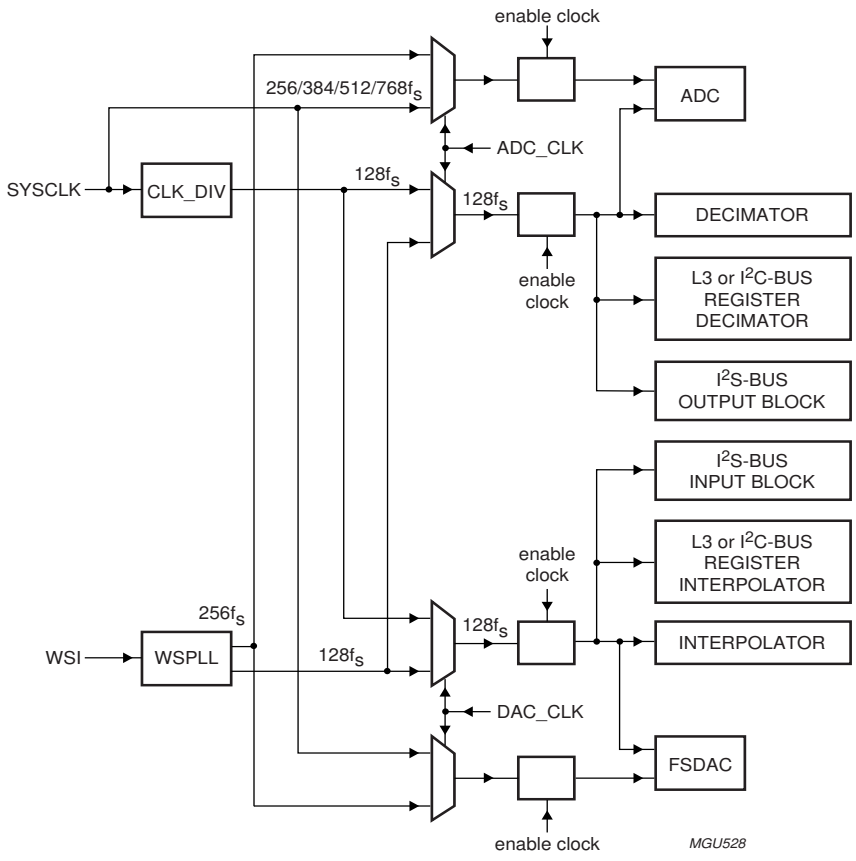



Fig.5 Clock routing for the main blocks inside the coder-decoder.

### 8.2 ADC analog front-end

The analog front-end of the UDA1380 consists of one stereo ADC with a selector in front of it (see Fig.6). Using this selector one can either select the microphone input with the microphone amplifier (LNA) with a fixed 29 dB gain and VGA (no PGA, since a real microphone amplifier is much better with respect to noise), or the line input which has a PGA for having 0 or 6 dB gain (for supporting 1 and 2 V (RMS) input). The PGA also provides gain control from 0 to 24 dB in steps of 3 dB.

**Remark**:

- The input impedance of the PGA (line input) is 12 kΩ, for the LNA this is 5 kΩ

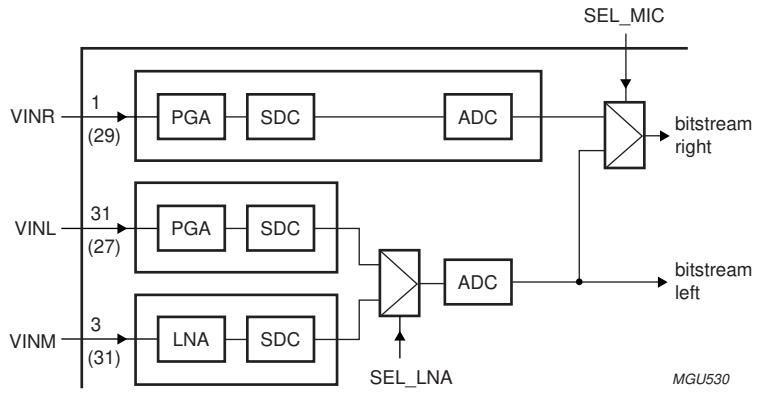
#### 8.2.1 Applications and Power-down modes

The following Power-down modes and functional modes are supported:

- Power-down mode in which the power consumption is very low (only leakage currents)

  In this mode there is no reference voltage at the line input
- Line input mode, in which the PGA can be used
- Microphone mode, in which the rest of the non-used PGAs and ADCs are powered-down
- Mixed PGA and LNA mode: one line input and one microphone input.

More information on the analog frond-end is given in Section 8.11.1.




Pin numbers for UDA1380HN in parentheses.

Fig.6 Analog front-end.

#### 8.2.2 LNA with VGA

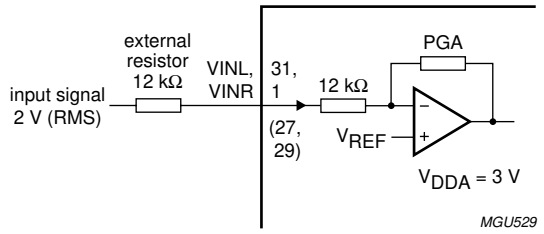
The LNA is equipped with a VGA. The function of the VGA is to have additional variable analog gain from 0 to 30 dB in steps of 2 dB. This provides more flexibility in the choice of the microphone.

#### 8.2.3 Applications with 2 V (RMS) input

For the line input it is preferable to have 0 dB and 6 dB gain settings in order to be able to apply both 1 and 2 V (RMS) input signals, using a series resistance. For this purpose a PGA is used which has 0 to 24 dB gain, in steps of 3 dB.

In applications in which a 2 V (RMS) input signal is used, a 12 kΩ resistor must be used in series with the input of the ADC (see Fig.7). This forms a voltage divider together with the internal ADC resistor and ensures that the voltage, applied to the input of the IC, never exceeds 1 V (RMS). Using this application for a 2 V (RMS) input signal, the switch must be set to 0 dB. When a 1 V (RMS) input signal is applied to the ADC in the same application, the gain switch must be set to 6 dB.

An overview of the maximum input voltages allowed against the presence of an external resistor and the setting of the gain switch is given in Table 2; the power supply voltage is assumed to be 3 V.




Pin numbers for UDA1380HN in parentheses.

Fig.7 ADC front-end with PGA (line input).

**Table 2** Application modes using input gain stage

| RESISTOR (12 kΩ) | INPUT GAIN SWITCH | MAXIMUM INPUT VOLTAGE |
|---|---|---|
| Present | 0 dB | 2 V (RMS) |
| | 6 dB | 1 V (RMS) |
| Absent | 0 dB | 1 V (RMS) |
| | 6 dB | 0.5 V (RMS) |

### 8.3 Decimation filter (ADC)

The decimation from $128f_s$ is performed in two stages. The first stage realizes a $\frac{\sin x}{x}$ characteristic with a decimation factor of 16. The second stage consists of 3 half-band filters, each decimating by a factor 2. The filter characteristics are shown in Table 3.

**Table 3** Decimation filter characteristics

| ITEM | CONDITION | VALUE (dB) |
|---|---|---|
| Pass-band ripple | 0 to $0.45f_s$ | 0.01 |
| Stop band | $>0.55f_s$ | −70 |
| Dynamic range | 0 to $0.45f_s$ | >135 |
| Digital output level | at 0 dB input analog | −1.5 |

#### 8.3.1 Overload detection

The UDA1380 is equipped with an overload detector which can be read out from the L3-bus or I²C-bus interface.

In practice the output is used to indicate whenever the output data, in either the output of the left or right channel, exceeds −1 dB (the actual figure is −1.16 dB) of the maximum possible digital swing. When this condition is detected output bit OVERFLOW in the L3-bus register is forced to logic 1 for at least $512f_s$ cycles (11.6 ms at $f_s$ = 44.1 kHz). This time-out is reset for each infringement.

#### 8.3.2 Volume control

The decimator is equipped with a digital volume control. This volume control is separate for left and right, and can be set with bits ML_DEC [7:0] and bits MR_DEC [7:0] via the L3-bus or I²C-bus interface. The range is from +24 dB to −63.5 dB and mutes in steps of 0.5 dB.

#### 8.3.3 Mute

The decimator is equipped with a dB-linear mute which mutes the signal in 256 steps of 0.5 dB.

#### 8.3.4 AGC function

The decimation filter is equipped with an AGC block. This function is intended, when enabled, to keep the output signal at a constant level. The AGC can be used for microphone applications in which the distance to the microphone is not always the same.

The AGC can be enabled via an L3-bus or I²C-bus bit by setting the bit to logic 1. In that case it bypasses the digital volume control.

Via the L3-bus or I²C-bus interface also some other settings of the AGC, like the attack and decay settings and the target level settings, can be made.

**Remark**: The DC filter before the decimation filter must be enabled by setting the L3-bus or I²C-bus bit SKIP_DCFIL to logic 0 when AGC is in operation; otherwise the output will be disturbed by the DC offset added in the ADC.

### 8.4 Interpolation filter (DAC)

The interpolation digital filter interpolates from 1 to 64$f_s$ or to 128$f_s$, by cascading FIR filters, see Table 4. The interpolator is equipped with several sound features like volume control, mute, de-emphasis and tone control.

**Table 4** Interpolation filter characteristics

| ITEM | CONDITION | VALUE (dB) |
|---|---|---|
| Pass-band ripple | 0 to 0.45$f_s$ | ±0.025 |
| Stop band | >0.55$f_s$ | −60 |
| Dynamic range | 0 to 0.45$f_s$ | >135 |

#### 8.4.1 DIGITAL MUTE

Muting the DAC will result in a cosine roll-off soft mute, using 4 × 32 = 128 samples in normal mode (or 3 ms at 44.1 kHz sampling frequency). The cosine roll-off curve is illustrated in Fig.8. These cosine roll-off functions are implemented for both the digital mixer and the master mute inside the DAC data path, see Section 8.8.

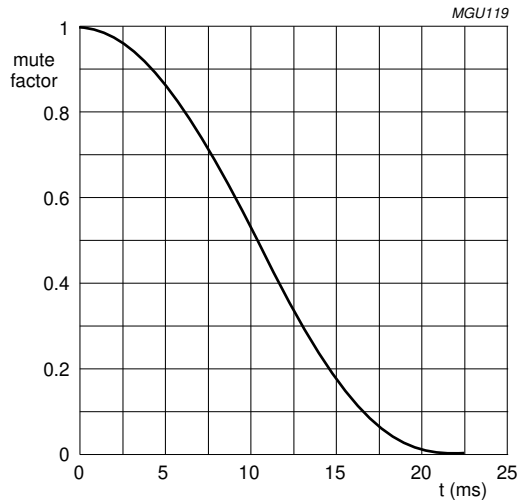



Fig.8 Mute as a function of raised cosine roll-off, displayed assuming 44.1 kHz.

#### 8.4.2 SOUND FEATURES

In addition, there are basic sound features:

- dB-linear volume control using 14-bit coefficients in steps of 0.25 dB: range 0 to −78 dB maximum suppression and −∞ dB: applies to both master volume and mixing volume control
- De-emphasis for 32, 44.1, 48 and 96 kHz for both channel 1 and 2 (selectable independently)
- Treble, which is selectable gain for high frequencies (positive gain only), the edge frequency of the treble is fixed (depends on the sampling frequency). Can be set for left and right independently:
  - Two settings: $f_c$ = 1.5 kHz and $f_c$ = 3 kHz, assuming sampling frequency is 44.1 kHz
  - Both settings have 0 to 6 dB gain range in steps of 2 dB
- Bass boost, which is selectable gain for low frequencies (positive gain only). The edge frequency of the bass boost is fixed and depends on the sampling frequency. Can be set for left and right independently:
  - Two settings: $f_c$ = 250 Hz and $f_c$ = 300 Hz, assuming sampling frequency is 44.1 kHz
  - First setting: 0 to 18 dB gain range in steps of 2 dB
  - Second setting: 0 to 24 dB gain range in steps of 2 dB.

### 8.5 Noise shaper

The noise shaper consists of two mono 3rd-order noise shapers and one time-multiplexed stereo 5th-order noise shaper.

The order of the noise shaper can be chosen between 3rd-order (which runs at 128$f_s$) and 5th-order (which runs at 64$f_s$) via bit SEL_NS in the L3-bus or $I^2C$-bus register. The preferable choice for the noise shaper order is:

- 3rd-order noise shaper is preferred at low sampling frequencies, for instance between 8 and 32 kHz. This is for preventing out-of-band noise from the noise shaper to move into the audio band
- 5th-order noise shaper is normally used at higher sampling frequencies, normally from 32 to 100 kHz.

The noise shaper shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using an FSDAC.

### 8.6 FSDAC

#### 8.6.1 General information

The Filter-Stream Digital-to-Analog Converter (FSDAC) is a semi-digital reconstruction filter that converts the 1-bit data stream (running at either $64f_s$ for the 5th-order noise shaper or $128f_s$ for the 3rd-order noise shaper) of the noise shaper into an analog output voltage. The filter coefficients are implemented as current sources, and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity are achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal, capable of driving a line output. The output voltage of the FSDAC scales proportionally with the power supply voltage.

**Remark:** When the FSDAC is powered-down, the output of the FSDAC becomes high impedance.

#### 8.6.2 Analog mixer input

The FSDAC has a mixer input, which makes it possible to mix an analog signal to the output signal of the FSDAC itself. In schematic form this is given in Fig.9.

This mixer input can be used for instance for mixing-in a GSM signal or an FM signal directly to the line output. In the UDA1380, the mixer input is connected from the ADC line input via an AVC unit.

**Remark**: Before the AVC unit can be used stand-alone, meaning without the digital part running, first the DAC part must be initialised in order to have the DAC output generating zero current. Otherwise the signal will be clipped.

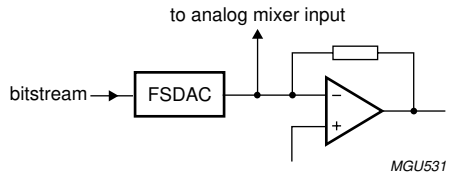



Fig.9 Mixing signals to the FSDAC output (analog domain).

### 8.7 Headphone driver

The UDA1380 is equipped with a headphone driver which can deliver 35 mW (at 3.0 V power supply) into a 16 Ω load.

The headphone driver does not need external DC decoupling capacitors because it can be DC coupled with respect to a special headphone output reference voltage. This saves two external capacitors (which is quite useful in a portable device).

The headphone driver is equipped with short-circuit protection on all three operational amplifiers (left, right and the virtual ground). Each of the operational amplifiers has a signalling bit which becomes logic 1 in case the limiter is activated, for instance in case of a short-circuit. This means the microcontroller in the system can poll the L3-bus or $I^2C$-bus register of the headphone driver and as soon as (and for as long as) the short-circuit detection bits are activated, the microcontroller can signal the user that something is wrong or power-down the headphone driver (for instance, for energy-saving purposes).

**Remark:** To improve headphone channel separation performance, the distance between $V_{REF(HP)}$ and the micro speaker port must be minimized.

### 8.8 Digital and analog mixers (DAC)

#### 8.8.1 Digital mixer

The ADC output signal and digital input signal can be mixed without external DSP as shown in Fig.10. This mixer can be controlled via the microcontroller interface, and must only be enabled when the ADC and the DAC are running at the same frequency. In addition, the mixer output signal can also be applied to the $I^2S$-bus output interface.

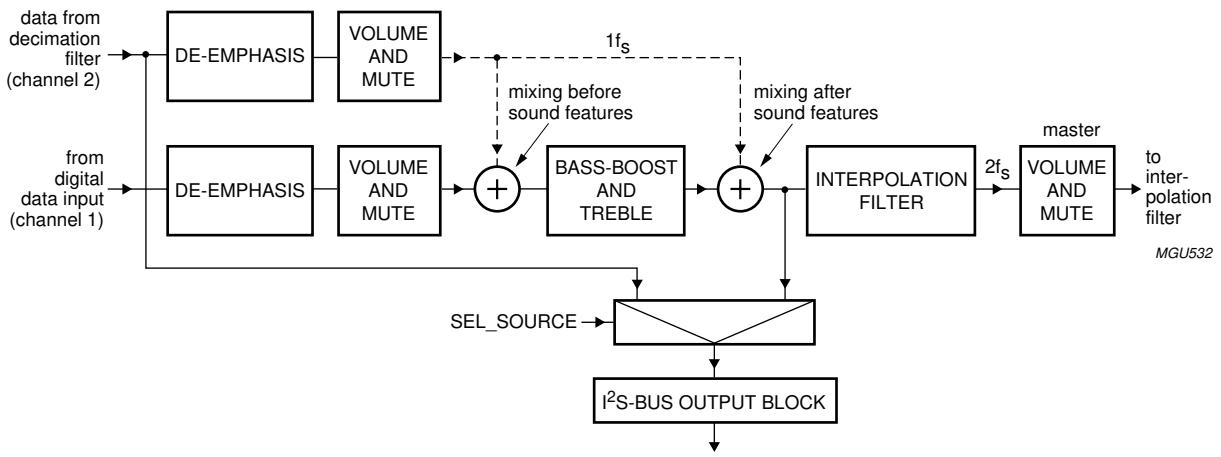



Fig.10 Digital mixer (DAC).

### 8.8.2 ANALOG MIXER

The analog mixer, which uses the mixer input of the FSDAC, can mix a signal into the FSDAC output signal via an AVC unit (see Fig.11). The mixer can be used to mix a signal into the FSDAC output signal and play it via the headphone driver without the complete coder-decoder running. The analog control range is 0 to −64.5 dB with a gain of 16.5 dB, and mutes in steps of 1.5 dB (so actually the range is from +16.5 dB to −48 dB plus mute).

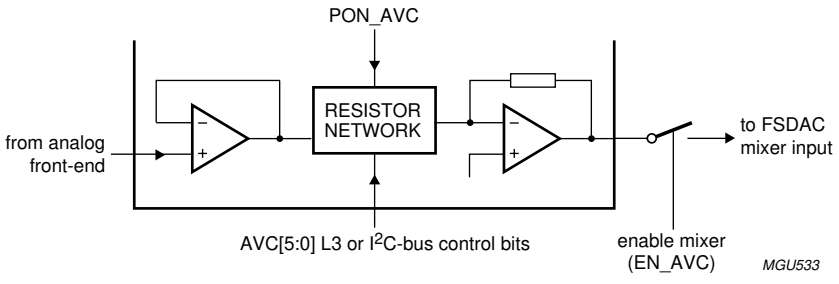



Fig.11 Analog mixer configuration.

### 8.9 Application modes

The operation mode can be set with pin SEL_L3_IIC, either to L3-bus mode (LOW) or to the I²C-bus mode (HIGH) as given in Table 5.

For all features in microcontroller mode see Chapter 9.

**Table 5** Pin function in the selected mode

| PIN | L3-BUS MODE SEL_L3_IIC = L | I²C-BUS MODE SEL_L3_IIC = H |
|---|---|---|
| L3CLOCK/SCL | L3CLOCK | SCL |
| L3MODE | L3MODE | A1 |
| L3DATA/SDA | L3DATA | SDA |

**Remark**: In the I²C-bus mode there is a bit A1 which sets the LSB bit of the address of the UDA1380. In L3-bus mode this bit is not available, meaning the device has only one L3-bus device address.

### 8.10 Power-on reset

The UDA1380 has a dedicated reset pin, which has a pull-down resistor. This way a Power-on reset circuit can be made with a capacitor and a resistor at the pin. The internal pull-down resistor cannot be used because of the 5 V tolerant nature of the pad. The pull-down resistor is shielded from the outside world by a transmission gate in order to support 5 V tolerance.

The reset timing is determined by the external capacitor and resistor which are connected to pin RESET, and the internal pull-down resistor. On Power-on reset, all the digital sound processing features and the system controlling features are set to the default setting of the L3-bus and I²C-bus control modes.

**Remark**: The reset time should be at least 1 μs, and during the reset time the system clock should be running. In case the WSPLL is selected as the clock source, a clock must be connected to the SYSCLK input in order to have a proper reset of the L3-bus or I²C-bus registers. This is because the clock source is set to SYSCLK by default.

### 8.11 Power-down requirements

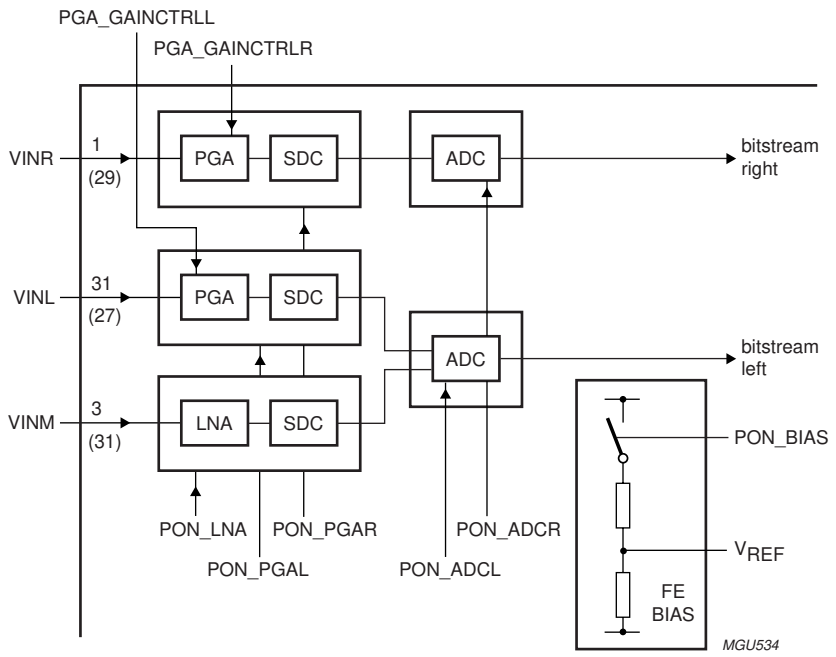
The following blocks have power-down control via the L3-bus or I²C-bus interface:

- Microphone amplifier (LNA) including its Single-Ended to Differential Converter (SDC) and VGA
- ADC plus SDC and the PGA, for left and right separate
- Bias generation circuit for the front-end and the FSDAC
- Headphone driver
- WSPLL
- FSDAC.

Clocks of the decimator, interpolator and the analog blocks have separate enable and disable controls.

### 8.11.1 ANALOG FRONT-END

Figure 12 shows the power control inside the analog front-end. The control of all power-on pins of the ADC front-end is done via separate L3-bus or I²C-bus bits.




Pin numbers for UDA1380HN in parentheses.

Fig.12 Analog front-end power-down.

### 8.11.2 FSDAC POWER CONTROL

The FSDAC block has power-on pins: one of which shuts down the DAC itself, but leaves the output still at $V_{REF}$ voltage (which is half the power supply). This function is set by the bit PON_DAC in the L3-bus or I²C-bus register.

A second L3-bus or I²C-bus bit shuts down the complete bias circuit of the FSDAC, via bit PON_BIAS in the L3-bus or I²C-bus register. This bit PON_BIAS acts the same as given in Fig.12 for the analog front-end.

## 8.12 Plop prevention

Plops are ticks and other strange sounds that can occur when a part of a device is powered-up or powered-down, or when switching between modes is done.

Some ways to prevent plops from occurring are:

- When the FSDAC or headphone driver must be powered-down, first a digital mute is applied. After that the FSDAC or headphone driver can be powered-down. In case the FSDAC or headphone driver must be powered-up, first the analog part is switched on, then the digital part is demuted
- When the ADC must be powered-down, a digital mute sequence must be applied. When the digital output signal is completely muted, the ADC can be powered-down. In case the ADC must be powered-up, first the analog part must be powered-up, then the digital part must be demuted
- When there is a change of, for example, clock divider settings or clock source (selecting between SYSCLK and WSPLL clock), then also digital mute for that block (either decimator or interpolator) should be used.

**Remark**: All items mentioned in Section 8.12 are not ‘hard-wired’ implemented, but are to be followed by the user as a guideline for plop prevention.

### 8.13 Digital audio data input and output

The supported audio formats for the control modes are:

- $I^2S$-bus
- MSB-justified
- LSB-justified, 16 bits
- LSB-justified, 18 bits
- LSB-justified, 20 bits
- LSB-justified, 24 bits (only for the output interface).

The bit clock BCK can be up to $128f_s$, or in other words the BCK frequency is 128 times the WS frequency or less: $f_{BCK} \leq 128f_{WS}$.

**Remark**: The WS edge must coincide with the negative edge of the BCK at all times, for proper operation of the digital I/O data interface. Figure 13 shows the interface signals.

#### 8.13.1 Digital audio input interface

The digital audio input interface is slave only, meaning the system must provide the WSI and BCKI signals (next to the DATAI signal).

Either the WSPLL locks onto the WSI signal and provides the internal clocks for the interpolator and the FSDAC, or a system clock must be applied which must be in frequency lock to the digital data input interface signals.

#### 8.13.2 Digital audio output interface

The digital audio output interface can be either master or slave. The data source for the data output can be selected from either the decimator (ADC front-end) or the digital mixer output.

**Remark:** The digital mixer output is only valid if both the decimator and the interpolator run at the same clock:

- In slave mode the signals on pins BCKO, WSO and SYSCLK must be applied from the application (signals must be in frequency lock) and the UDA1380 returns the DATAO signal from the decimator. The applied signal from pin BCKO can be for instance: $32f_s$, $48f_s$, $64f_s$, $96f_s$ or $128f_s$
- In master mode the SYSCLK signal must be applied from the system, then the UDA1380 returns with the BCKO, WSO and the DATAO signals. For the BCKO clock, there are 2 general rules:
  - When the SYSCLK is either $256f_s$ or $512f_s$, the BCKO frequency is $64f_s$
  - When the SYSCLK is either $384f_s$ or $768f_s$, the BCKO signal is $48f_s$.

The slave and master modes can be selected by the bit Serial Interface Mode (SIM) in the L3-bus or $I^2C$-bus interface.

## 9 L3-BUS INTERFACE DESCRIPTION

The UDA1380 has an L3-bus microcontroller interface mode. Controllable system and digital sound processing features are:

- Software reset
- System clock frequency (selection between $256f_s$, $384f_s$, $512f_s$ and $768f_s$ clock divider settings)
- Clock mode setting, for instance, which block runs at which clock, and clock enabling
- Power control for the WSPLL
- Data input and data output format control, for input and output independently including data source selection for the digital output interface
- ADC features:
  - Digital mute
  - AGC enable and settings
  - Polarity control
  - Input line amplifier control (0 to 24 dB in steps of 3 dB)
  - DC filtering control
  - Digital gain control (+24 to −63 dB gain in steps of 0.5 dB) for left and right
  - Power control
  - VGA of the microphone input
  - Selection of line or microphone input.
- DAC and headphone driver features:
  - Power control FSDAC and headphone driver
  - Polarity control
  - Mixing control (only available when both decimator and interpolator run at the same speed). This includes the mixer volumes, mute and mixer position switch
  - De-emphasis control
  - Master volume and balance control
  - Flat/minimum/maximum settings for bass boost and treble
  - Tone control: bass boost and treble
  - Master mute control
  - Headphone driver short-circuit protection status bits.

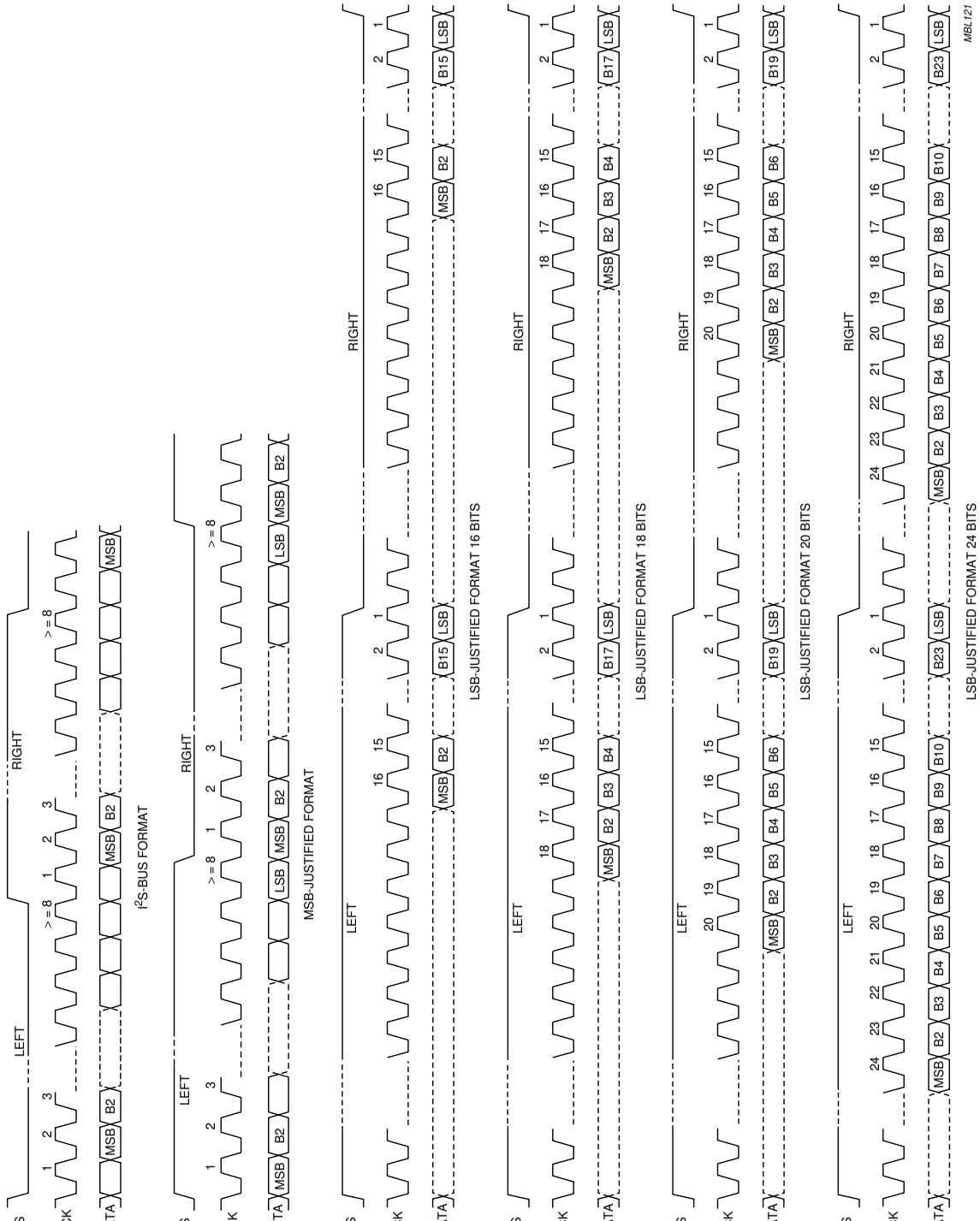



Fig.13 Serial interface input and output formats.

### 9.1 Introduction

The exchange of data and control information between the microcontroller and the UDA1380, is accomplished through a serial hardware interface comprising the following pins:

L3DATA/SDA: microcontroller interface data line

L3MODE: microcontroller interface mode line

L3CLOCK/SCL: microcontroller interface clock line.

Information transfer via the microcontroller bus is organized LSB first, and in accordance with the so called 'L3' format, in which two different modes of operation can be distinguished: address mode and data transfer mode.

Inside the microcontroller interface there is a hand-shake mechanism which takes care of proper data transfer from the microcontroller interface clock to the destination clock domains. This means that when data is sent to the microcontroller interface, the system clock must be running.

### 9.2 Device addressing

The device addressing mode is used to select a device for subsequent data transfer. The address mode is characterized by the signal on pin L3MODE being LOW and a burst of 8 pulses on pin L3CLOCK/SCL, accompanied by an 8 bit device address on pin L3DATA/SDA. The fundamental timing is shown in Figs 14 and 15.

**Table 6** Selection of data transfer

| DOM BIT 1 | DOM BIT 0 | TRANSFER |
|---|---|---|
| 0 | 0 | not used |
| 0 | 1 | not used |
| 1 | 0 | DATA and STATUS write or pre-read |
| 1 | 1 | DATA and STATUS read |

Table 6 shows that there are two types of data transfers: DATA and STATUS which can be read and written. Table 6 also shows that the DATA and STATUS read and write actions are combined.

The device address consists of one byte, which is split-up in two parts:

- Bits 7 to 2 represent a 6-bit device address. In the UDA1380 this is 000001
- Bits 1 to 0 called Data Operation Mode, or DOM bits, represent the type of data transfer according to Table 6.

### 9.3 Slave address

The UDA1380 acts as a slave receiver or a slave transmitter. Therefore the signals L3CLOCK and L3MODE are only input signals. The data signal L3DATA is a bidirectional line. The UDA1380 slave address is shown in Table 7.

**Table 7** L3 slave address

| (MSB) | | BIT | | | (LSB) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |

### 9.4 Register addressing

After sending the device address, including the flags (the DOM bits) whether information is read or written, one byte is sent with the destination register address using 7 bits, and one bit which signals whether information will be read or written. The fundamental timing for L3 is given in Fig.19.

Basically there are three forms for register addressing:

- Register addressing for L3 write: the first bit is a logic 0 indicating a write action to the destination register, followed by seven register address bits
- Prepare read addressing: the first bit of the byte is logic 1; signalling data will be read from the register indicated
- The read action itself: in this case the device returns a register address prior to sending data from that register. When the first bit of the byte is logic 0, the register address was valid, in case the first bit is a logic 1 the register address was invalid.

**Remarks**:

- Each time a new destination address needs to be written, the device address must be sent again
- When addressing the device for the first time after power-up of the device, at least one L3 clock-cycle must be given to enable the L3 interface.

### 9.5 Data write mode

For writing data to a device, four bytes must be sent. Figure 14 explains the data write mode in a signal diagram:

- One byte with the device address, being '00000110', which is including the LSB code 01 for signalling write to the device
- One byte starting with a logic 0 for signalling write, followed by 7 bits indicating the destination address
- Two data bytes.

The SYSCLK signal must be applied in data write mode.

**Table 8** L3 write data

| L3 MODE | DATA TYPE | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | **0**(1) | **1** | **2** | **3** | **4** | **5** | **6** | **7**(2) |
| Addressing mode | device address | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Data transfer 1 | register address | 0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Data transfer 2 | MS data byte | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| Data transfer 3 | LS data byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Notes**

1. First bit in time.
2. Last bit in time.

### 9.6 Data read mode

For reading from the device, first a prepare-read must be done. After this, the device address is sent again. The device then returns with the register address, indicating whether the address was valid or not, and the data of the register. The following five steps explain this procedure, and an example of transmission is given in Fig.15.

- One byte with the device address, being '00000110', which is including the LSB code 01 for signalling write to the device
- One byte is sent with the register address from which it needs to be read. This byte starts with a logic 1, which indicates that there will be a read action from the register
- One byte with the device address including '11' is sent to the device, being 00000111. The '11' indicates that the device must write data to the microcontroller, then the microcontroller frees the L3DATA-bus so the UDA1380 can send the register address byte and its two-byte contents
- The device now writes the requested register address on the bus, indicating whether the requested register was valid or not (logic 0 means valid, logic 1 means invalid)
- The device writes the data from the requested register on the bus, being two bytes.

The SYSCLK signal must be applied in data read mode.

**Table 9** L3 prepare read data

| L3 MODE | DATA TYPE | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | **0**[1] | **1** | **2** | **3** | **4** | **5** | **6** | **7**[2] |
| Addressing mode | device address | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Data transfer 1 | register address | 1 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

**Notes**

1. First bit in time.
2. Last bit in time.

**Table 10** L3 read data

| L3 MODE | DATA TYPE | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | **0**[1] | **1** | **2** | **3** | **4** | **5** | **6** | **7**[2] |
| Addressing mode | device address | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Data transfer 1; note 3 | register address | 0: valid<br>1: invalid | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Data transfer 2; note 3 | MS data byte | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| Data transfer 3; note 3 | LS data byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Notes**

1. First bit in time.
2. Last bit in time.
3. Data transfer from the UDA1380 to the microcontroller.

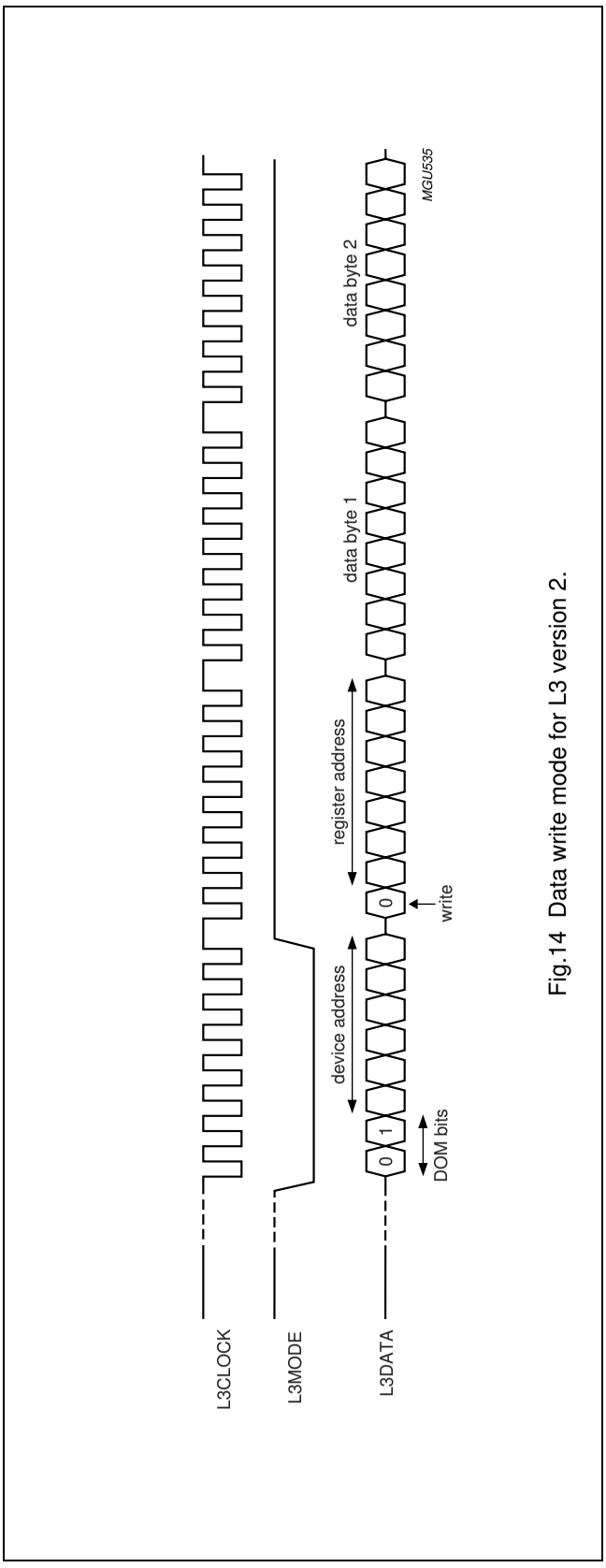



Fig.14 Data write mode for L3 version 2.

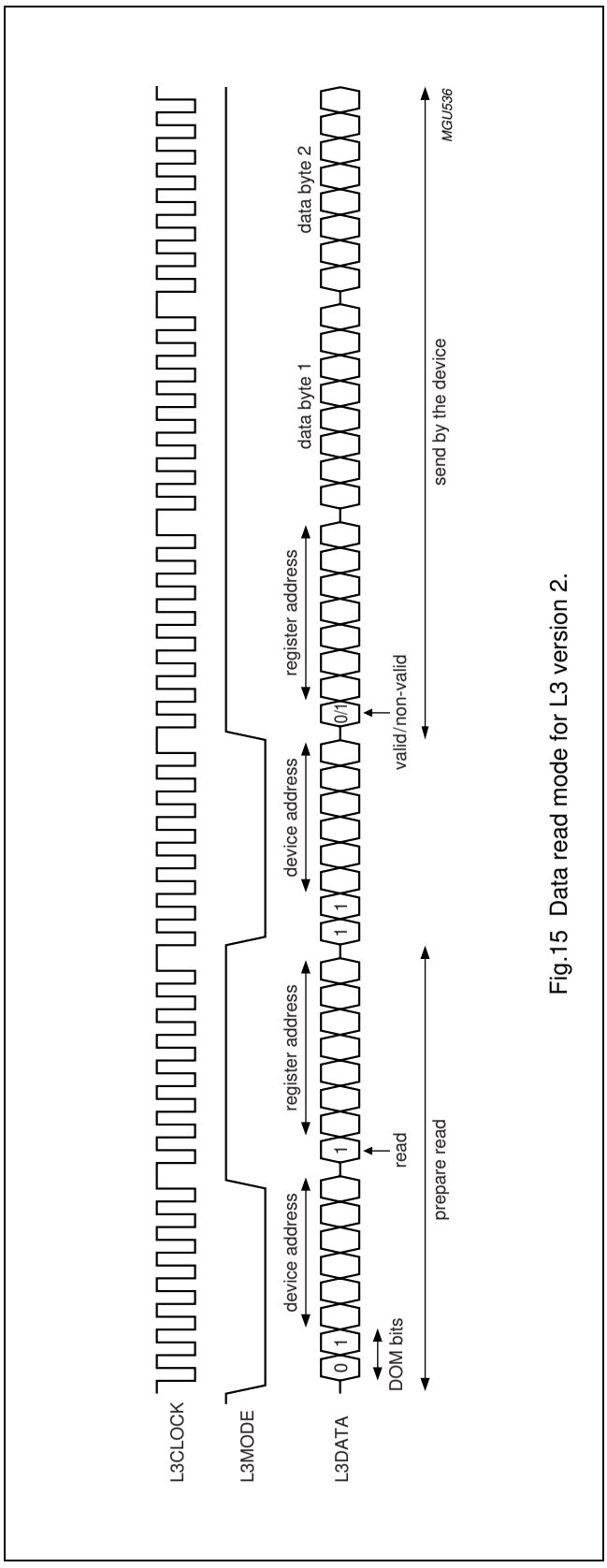



Fig.15 Data read mode for L3 version 2.