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UJA1023

LIN-I/O slave

Rev. 5 — 17 August 2010 Product data sheet

1. General description

The UJA1023 is a stand-alone Local Interconnect Network (LIN) I/O slave that replaces basic components commonly used in electronic control units for input and output handling. The UJA1023 contains a LIN 2.0 controller, an integrated LIN transceiver which is LIN 2.0 / SAE J2602 compliant and LIN 1.3 compatible, a 30 kΩ termination resistor necessary for LIN-slaves, and eight I/O ports which are configurable via the LIN bus.

An automatic bit rate synchronization circuit adapts to any (master) bit rate between 1 kbit/s and 20 kbit/s. For this, an oscillator is integrated.

The LIN protocol will be handled autonomously and both Node Address (NAD) and LIN frame Identifier (ID) programming will be done by a master request and an optional slave response message in combination with a daisy chain or plug coding function.

The eight bidirectional I/O pins are configurable via LIN bus messages and can have the following functions:

- Input:
  - Standard input pin
  - Local wake-up
  - Edge capturing on falling, rising or both edges
  - Analog input pin
  - Switch matrix (in combination with output pins)
- Output:
  - Standard output pin as high-side driver, low-side driver or push-pull driver
  - Cyclic sense mode for local wake-up
  - Pulse Width Modulation (PWM) mode; for example, for back light illumination
  - Switch matrix (in combination with input pins)

On entering a low-power mode it is possible to hold the last output state or to change over to a user programmable output state. In case of a failure (e.g. LIN bus short to ground) the output changes over to a user programmable limp home output state and the low-power Limp home mode will be entered.

Due to the advanced low-power behavior the power consumption of the UJA1023 in low-power mode is minimal.

2. Features and benefits

- Automatic bit rate synchronization to any (master) bit rate between 1 kbit/s and 20 kbit/s
- Integrated LIN 2.0 / SAE J2602 transceiver (including 30 kΩ termination resistor)
- Eight bidirectional I/O pins
- 4 × 2, 4 × 3, or 4 × 4 switch matrix to support reading and supplying a maximum number of 16 switches
- Outputs configurable as high-side and/or low-side driver and as cyclic or PWM driver
- 8-bit ADC
- Advanced low-power behavior
- On-chip oscillator
- Node Address (NAD) configuration via daisy chain or plug coding
- Inputs supporting local wake-up and edge capturing
- Configurable Sleep mode
- Limp home configuration in case of error conditions
- Extremely low electromagnetic emission
- High immunity against electromagnetic interference
- Bus line protected in accordance with ISO 7637
- Extended ambient temperature range (−40 °C to +125 °C)

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	supply voltage on pin BAT	all operating modes	[1]	5.5	-	27	V
I_{BAT}	supply current on pin BAT	LH sleep, Sleep and Limp home mode; V_{BAT} = 8.1 V to 27 V	[2]	-	45	65	μA
V_{LIN}	voltage on pin LIN	DC value		−27	-	+40	V
T_{vj}	virtual junction temperature		[3]	−40	-	+150	°C
V_{ESD}	electrostatic discharge voltage on pins LIN, BAT, C1, C2 and C3	human body model; C = 100 pF; R = 1.5 kΩ		−8	-	+8	kV

[1] Valid for the UJA1023T/2R04/C; for the UJA1023T/2R04, V_{BAT} = 6.5 V to 27 V.

[2] All outputs turned off, LIN recessive, V_{th1} selected.

[3] Junction temperature in accordance with IEC60747-1. An alternative definition of $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value to be used for calculating T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
UJA1023T/2R04/C[1]	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
UJA1023T/2R04[1]	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

[1] V_{BAT} = 5.5 V to 27 V for the UJA1023T/2R04/C; V_{BAT} = 6.5 V to 27 V for the UJA1023T/2R04 (see Table 32).

5. Block diagram

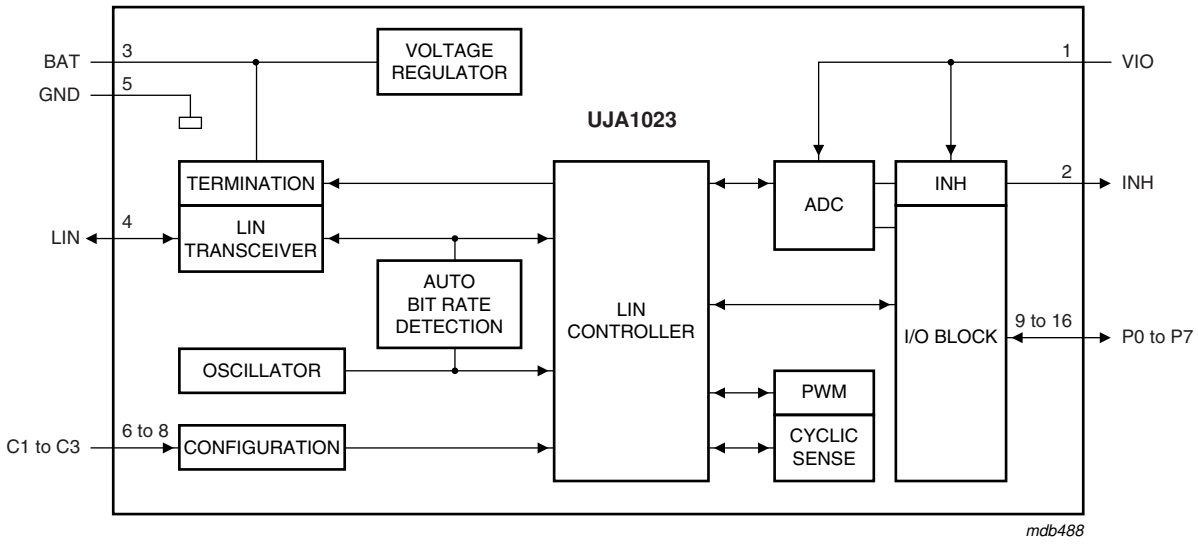


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

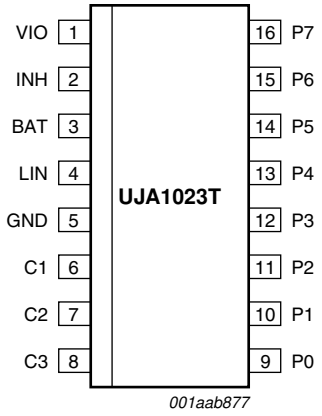


Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
VIO	1	I	reference input for level adaptation of the I/O pins P0 to P7
INH	2	O	inhibit output for controlling an external voltage regulator or internal ADC
BAT	3	I	battery supply
LIN	4	I/O	LIN bus line
GND	5	I	ground
C1	6	I	configuration input 1 for LIN slave NAD assignment
C2	7	I	configuration input 2 for LIN slave NAD assignment
C3	8	I/O	configuration input / output 3 for LIN slave NAD assignment
P0	9	I/O	bidirectional I/O pin 0
P1	10	I/O	bidirectional I/O pin 1
P2	11	I/O	bidirectional I/O pin 2
P3	12	I/O	bidirectional I/O pin 3
P4	13	I/O	bidirectional I/O pin 4
P5	14	I/O	bidirectional I/O pin 5
P6	15	I/O	bidirectional I/O pin 6
P7	16	I/O	bidirectional I/O pin 7

[1] I = input;
O = output;
I/O = input or output.

7. Functional description

The UJA1023 combines all blocks necessary to work as a stand-alone LIN slave. Various I/O functions typically used in a car are supported. For a more detailed description refer to Section 7.2 to Section 7.6. The block diagram is shown in Figure 1.

7.1 Short description of the UJA1023

7.1.1 LIN controller

The LIN 2.0 controller monitors and evaluates the LIN messages in order to process the LIN commands. It supervises and executes the NAD assignment, ID assignment and I/O-configuration and controls the operating modes of the UJA1023.

The NAD configuration is done by a combination of a LIN master request frame and a setting done by either a daisy chain or plug ID code.

7.1.2 LIN transceiver (including termination)

The LIN transceiver, which is LIN 2.0 / SAE J2602 compliant, is the interface between the internal LIN controller and the physical LIN bus. The transmit data stream of the LIN controller is converted into a bus signal with an optimized wave shape to minimize electromagnetic emission. The required LIN slave termination of 30 kΩ is already integrated. In case of LIN bus faults the UJA1023 switches to the low-power Limp home mode.

7.1.3 Automatic bit rate detection

The automatic bit rate detection adapts to the LIN master's bit rate. Any bit rate between 1 kbit/s and 20 kbit/s can be handled. This block checks whether the synchronization break and synchronization field are valid. If not, the message will be rejected.

7.1.4 Oscillator

The on-chip oscillator provides the internal clock signal for some digital functions and is the time reference for the automatic bit rate detection.

7.1.5 I/O block

The I/O block controls the configuration of the I/O pins. The LIN master configures the I/O pin functionality by means of a master request frame and an optional slave response frame.

Besides the standard level input and output behavior the following functions are also handled by the UJA1023: local wake-up, cyclic input, edge capture, PWM output, switch matrix I/O and AD conversion.

7.1.6 ADC

With three external components an 8-bit ADC function can be implemented. Each of the eight bidirectional I/O pins can be used as input for the ADC, one at a time.

7.1.7 PWM

Each pin can be configured with a Pulse Width Modulation (PWM) function. The resolution is 8-bit and the base frequency is approximately 2.7 kHz.

7.1.8 Cyclic sense

To reduce current consumption, the cyclic sense function can be used to read a switch. The switch will be supplied and read back periodically.

7.2 LIN controller

7.2.1 Configuration

In this data sheet basic knowledge of the *"LIN diagnostic and configuration specification, Rev. 2.0"* is expected.

7.2.1.1 Message sequence

The UJA1023 conforms to the *"LIN diagnostic and configuration specification, Rev. 2.0"* and is compatible with LIN 1.3.

The UJA1023 can be configured via the LIN command frames 'Master Request' (MasterReq) and 'Slave Response' (SlaveResp). Both frames consist of eight data bytes. The MasterReq is used to send configuration data from the master to the slaves, whereas the slave being addressed by the prior MasterReq will answer with the related data on demand.

Depending on the usage of the MasterReq the meaning of the data bytes can be different. Thus each LIN slave evaluates these data bytes.

Using MasterReq and SlaveResp for the UJA1023 configuration flow, as shown in Figure 3, is a so-called 'handshake' concept. The slave echoes its received MasterReq data in the SlaveResp, so the master can review slave configuration data. The use of the SlaveResp is optional.

The configuration flow is not disturbed if LIN commands other than shown in Figure 3 are sent to other LIN slave nodes. Thus the LIN master can transmit other LIN messages while it (re)configures the UJA1023.

Remarks:

- The I/O configuration will be enabled during the first usage of the UJA1023 message frames (see Section 7.2.5) of the PxResp or PxReq
- Notation Px is used in this document when referring to a function or property of any of the I/O pins P0 to P7
- For correct I/O configuration, the configuration requests must be sent in sequential order of first, second and third configuration data block

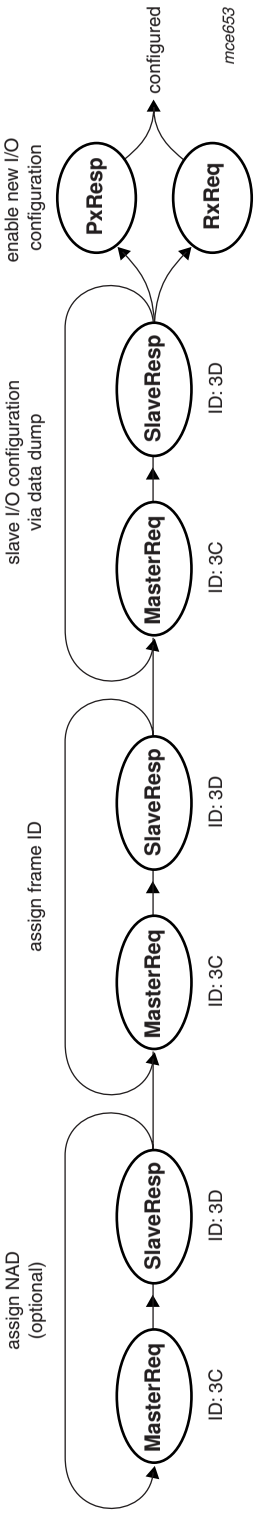


Fig 3. Typical configuration flow

7.2.1.2 LIN slave node address assignment

The default slave Node Address (NAD) after power-on depends on the input levels of the configuration pins C1, C2 and C3. These pins will be sampled directly after the power-on event. The relation between the configuration pins and the NAD is shown in Table 4.

Table 4. Default NAD after power-on

Configuration pins			Default NAD (hex)
C3	C2	C1	
0	0	0	60
0	0	1	61
0	1	0	62
0	1	1	63
1	0	0	64
1	0	1	65
1	1	0	66
1	1	1	67

In case a different NAD is necessary the assign NAD command has to be used. The assign NAD request is carried out if the Service Identifier (SID) in the third data byte of the MasterReq is the assign NAD request and the fourth to seventh data bytes are the LIN supplier codes of Philips (0x0011) and UJA1023 function ID (0x0000).

Table 5. Data bytes of assign NAD request[1]

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	d	d	d	d	d	d	d	d	08
D1	0	0	0	0	0	1	1	0	06
D2	1	0	1	1	0	0	0	0	B0
D3	0	0	0	1	0	0	0	1	11
D4	0	0	0	0	0	0	0	0	00
D5	0	0	0	0	0	0	0	0	00
D6	0	0	0	0	0	0	0	0	00
D7	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD

[1] d = different values possible; see Table 6.

Table 6. Bit description of assign NAD request

Byte	Bit	Symbol	Description
D0	7 to 0	C[3:1]	Initial NAD. This byte defines the initial NAD, refer to the related items topics
			0x08 to 0x0F (D0[0] = C1, D0[1] = C2 and D0[2] = C3) defines Plug ID; D0[3] = 1 for Plug ID configuration
			0x20 = daisy chain on; enable daisy chain pin drivers and receivers
			0x21 = assign NAD via daisy chain
			0x23 = daisy chain off; disable daisy chain pin drivers and receivers
D1	7 to 0	PCI	Protocol control information.
D2	7 to 0	SID	Service identifier. As SlaveResp the RSID code will be 0xF0.
D3 and D4	7 to 0	-	Supplier ID. Fixed code 0x0011 for Philips.
D5 and D6	7 to 0	-	Function ID. For the UJA1023 this code is fixed as 0x0000.
D7	7 to 0	NAD[7:0]	Slave Node Address (NAD). NAD values are in the range 1 to 127, while 0 and 128 to 255 are reserved for other purposes.

The format of the positive response is shown in Table 7.

Table 7. Positive response assign NAD request[1]

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	d	d	d	d	d	d	d	d	08
D1	0	0	0	0	0	0	0	1	01
D2	1	1	1	1	0	0	0	0	F0
D3	1	1	1	1	1	1	1	1	FF
D4	1	1	1	1	1	1	1	1	FF
D5	1	1	1	1	1	1	1	1	FF
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

[1] d = different values possible; see Table 6.

The NAD assignment can be done via Daisy Chain (DC), (see Section “Daisy chain NAD assignment”) as well as via Plug ID (see Section “Plug ID NAD assignment”). The type of NAD assignment can be distinguished on the value of the initial NAD, which is the first data byte D0 of the MasterReq assign NAD request. For reliability reasons the assignment mode decision is valid only if the combination of D0 to D6 (see Table 5) is true. After power-on the UJA1023 message identifiers PxReq and PxResp (see Section 7.2.5) are disabled. This is also true for NAD reassignment. In this case the message identifiers PxReq, PxResp and I/O configuration are disabled.

Daisy chain NAD assignment: Once the UJA1023 receives the assign NAD MasterReq frame and the type of configuration is daisy chain, the following actions can take place, depending on the initial NAD value:

- Initial NAD 0x20: Daisy chain on, the C1 to C3 pin drivers are enabled
- Initial NAD 0x21: The input level on the configuration pin C1 and the status flag of the internal DC-switch is read. The UJA1023 will be configured if C1 is LOW and the DC-switch is open (see slave 2 in Figure 4). The UJA1023 under daisy chain configuration uses the data byte D7 as new NAD for its further LIN configuration requests (e.g. Assign Frame ID). After the NAD assignment the DC-switch at pin C3 is closed, which puts through the daisy chain signal to the next slave. The switch will be opened again as soon as an Assign NAD request with initial NAD daisy chain off has been received
- Initial NAD 0x23: Daisy chain off, the C1 to C3 pin drivers are disabled

After the NAD assignment, for example, the ‘assign frame ID’ can be used to assign specific ID numbers.

The internal pull-up resistors at pin C1 to C3 are active during the assign NAD process only. Thus it causes no permanent current (see also Section 7.4) and reduces power consumption especially in the low-power modes.

Remark: There is no slave response to assign NAD requests using the initial NAD 0x20 and NAD 0x23.

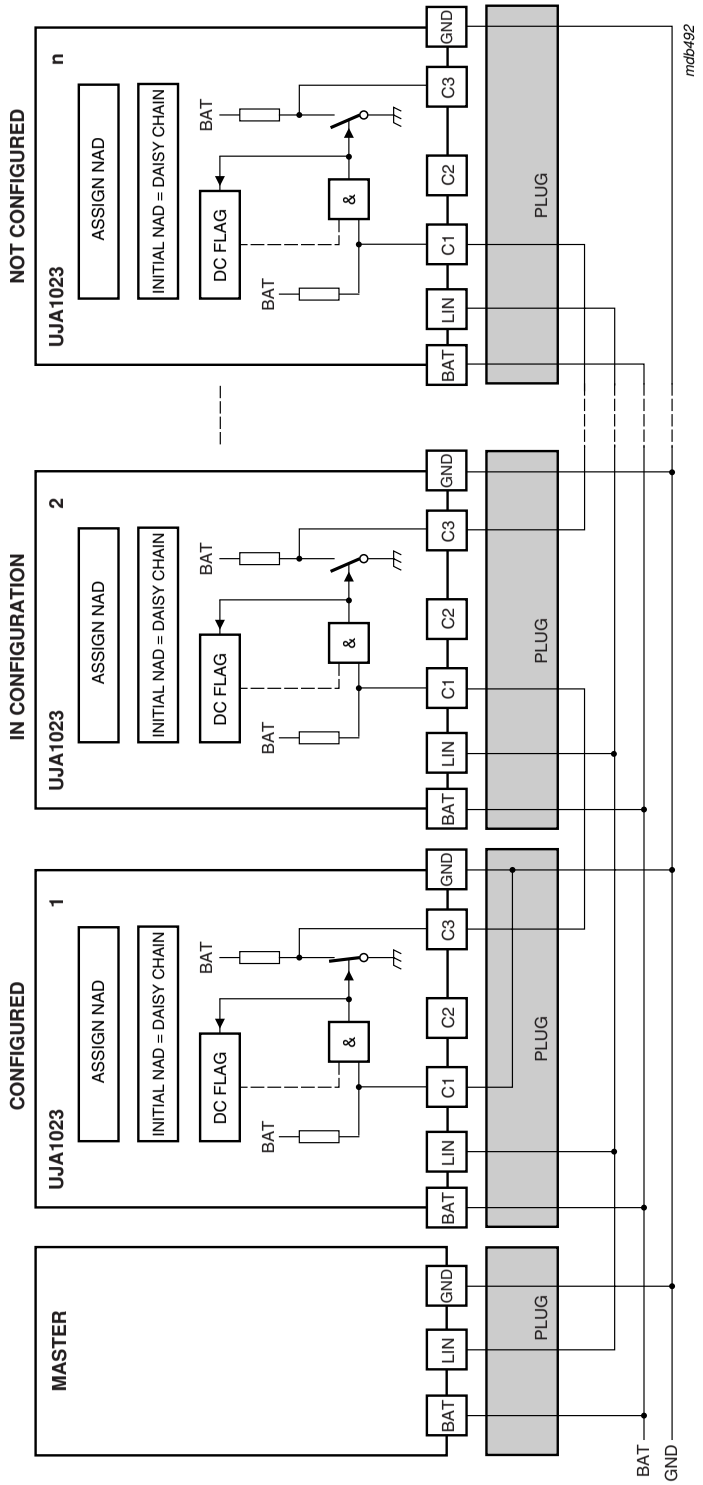


Fig 4. Daisy chain ID

Plug ID NAD assignment: Here the UJA1023 can be addressed via the pins C1, C2, and C3. Once the assign NAD MasterReq with the initial NAD 'Plug ID configuration' is received, the UJA1023 compares the values of the configuration pins C3, C2, and C1 with the values of the data bits D0[2:0]. If the values are equal and bits D0[7:4] are logic 0 and D0[3] is logic 1, the value of D7 is used as new NAD for the UJA1023.

Next, for example, the 'assign frame ID' can be used to assign specific ID numbers.

The internal pull-up resistors at pin C1 to C3 are active during the assign NAD process only. Thus it causes no permanent current (see also Section 7.4) and reduces power consumption especially in the low-power modes.

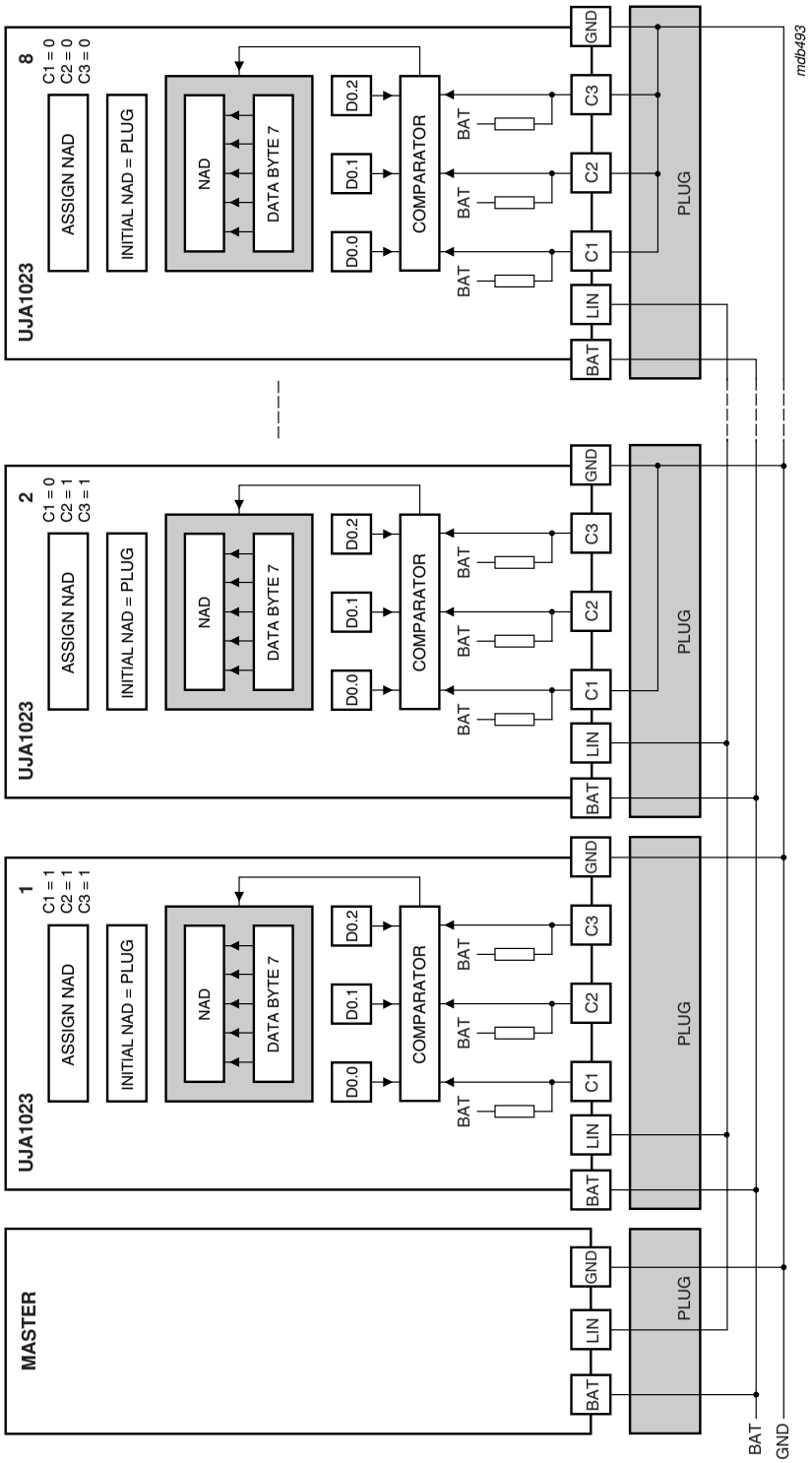


Fig 5. Plug ID

7.2.1.3 Assign frame ID

By means of the assign frame ID command the LIN message identifier PxReq and PxResp can be changed to the desired values.

Table 8. Assign frame ID request bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	1	0	06
D2	1	0	1	1	0	0	0	1	B1
D3	0	0	0	1	0	0	0	1	11
D4	0	0	0	0	0	0	0	0	00
D5	0	0	0	0	0	0	0	0	00
D6	0	0	0	0	0	0	0	0	00
D7	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	protected ID

Table 9. Assign frame ID request bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave Node Address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	SID[7:0]	Service identifier. As SlaveResp the RSID code will be 0xF1.
D3 and D4	7 to 0	-	Supplier ID. Fixed to 0x0011 for Philips.
D5 and D6	7 to 0	-	Message ID. Defines the assignment of the protected ID to PxResp and PxReq
			0x0000: PxReq = protected ID; PxResp = protected ID + 1
			0x0001: PxReq = unchanged; PxResp = protected ID
			0x0002: PxReq = protected ID; PxResp = unchanged
D7	7 to 0	ID[7:0]	Protected ID. Defines the protected ID.

The format of the positive response is shown in Table 10.

Table 10. Positive response assign frame ID

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	0	0	1	01
D2	1	1	1	1	0	0	0	1	F1
D3	1	1	1	1	1	1	1	1	FF
D4	1	1	1	1	1	1	1	1	FF
D5	1	1	1	1	1	1	1	1	FF
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

7.2.1.4 Read by identifier

It is possible to read the supplier identifier, function identifier and the variant of the UJA1023 by means of the read by identifier request. The format for this request is shown in Table 11. The positive response is shown in Table 13, the negative response is shown in Table 14.

Table 11. Read by identifier (LIN product identification)

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	1	0	06
D2	1	0	1	1	0	0	1	0	B2
D3	0	0	0	0	0	0	0	0	00
D4	0	0	0	1	0	0	0	1	11
D5	0	0	0	0	0	0	0	0	00
D6	0	0	0	0	0	0	0	0	00
D7	0	0	0	0	0	0	0	0	00

Table 12. Read by identifier bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave Node Address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	SID[7:0]	Service identifier. As SlaveResp the RSID code will be 0xF2 for a positive response and 0x7F for a negative response.
D3	7 to 1	-	Identifier. Only the LIN product identifier 0x00 is supported.
D4 and D5	7 to 0	-	Supplier ID. Fixed to 0x0011 for Philips.
D6 and D7	7 to 0	-	Function ID. For the UJA1023 this code is fixed to 0x0000.

Table 13. Read by identifier positive response[1]

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	1	0	06
D2	1	1	1	1	0	0	1	0	F2
D3	0	0	0	1	0	0	0	1	11
D4	0	0	0	0	0	0	0	0	00
D5	0	0	0	0	0	0	0	0	00
D6	0	0	0	0	0	0	0	0	00
D7	d	d	d	d	d	d	d	d	variant

[1] d = different values possible; see Table 12.

Table 14. Read by identifier negative response

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	0	1	1	03
D2	0	1	1	1	1	1	1	1	7F
D3	1	0	1	1	0	0	1	0	B2
D4	0	0	0	1	0	0	1	0	12
D5	1	1	1	1	1	1	1	1	FF
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

7.2.1.5 I/O configuration

The I/O configuration is done via the LIN configuration request ‘Data Dump’, where the first data byte of the MasterReq contains the slave node address NAD. The I/O-pin configuration process starts only, if the received slave node address matches the own UJA1023 node address and if data byte D2 (SID) is 0xB4.

As with the other configuration commands, the master transmits the I/O-pin configuration data via the MasterReq message. Due to the limited amount of data bytes within the LIN configuration command ‘Data Dump’, the configuration and diagnosis is split-up into four blocks. The configuration and diagnosis blocks are distinguished on bits 6 and 7 of data byte D3. The master can review the new configuration data via the SlaveResp message. Finally if the master considers the received configuration data of the LIN-I/O to be correct, it can enable the slave I/O-configuration by using the UJA1023 message frames (see Section 7.2.5) PxResp or PxReq.

It should be noted that for correct I/O configuration, the configuration requests must be sent in sequential order of: first, second and third configuration data block.

Table 15. First I/O configuration data block bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	1	0	06
D2	1	0	1	1	0	1	0	0	B4
D3	0	0	IM1	IM0	RxDL	ADCIN2	ADCIN1	ADCIN0	00
D4	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0	00
D5	LSE7	LSE6	LSE5	LSE4	LSE3	LSE2	LSE1	LSE0	00
D6	OM0_7	OM0_6	OM0_5	OM0_4	OM0_3	OM0_2	OM0_1	OM0_0	00
D7	OM1_7	OM1_6	OM1_5	OM1_4	OM1_3	OM1_2	OM1_1	OM1_0	00

Table 16. First I/O configuration data block bit description

Byte	Bit	Symbol	Description		
D0	7 to 0	NAD[7:0]	Slave node address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).		
D1	7 to 0	PCI[7:0]	Protocol control information.		
D2	7 to 0	SID[7:0]	Service identifier. As SlaveResp the RSID value will be 0xF4.		
D3	7 and 6	-	00 for first configuration data block.		
	5 and 4	IM[1:0]	Pin INH mode. Mode will be changed after PxReq or PxResp		
			00 = external regulator (control of external voltage regulator)		
			01 = ADC		
			10 = reserved, if selected both bits will be logic 1		
			11 = switch open		
	3	RxDL	Receive data length. Message PxReq contains two data bytes if RxDL = 0 and three data bytes if RxDL = 1.		
	2 to 0	ADCIN[2:0]	Analog source channel selection. The number of ADCIN[2:0] determines which of the P7 to P0 input is used. For example if ADCIN[2:0] = 101 then P5 will be the input. ADCIN[2:0] is used only if ADC mode is selected (IM[1:0] = 01) and RxDL = 0 (No analog input selection at PxReq).		
D4	7 to 0	HSE[7:0]	High-side enable for I/O pin Px.		
D5	7 to 0	LSE[7:0]	Low-side enable for I/O pin Px.		
D6 and D7	7 to 0	OM0_[7:0], OM1_[7:0]	Output mode for I/O pin Px.		
			OM1_x	OM0_x	
			0	0	level
			0	1	reserved
			1	0	cyclic sense
			1	1	PWM

The second configuration data block (shown in Table 17) is selected only if D3.7 = 0 and D3.6 = 1.

Table 17. Second I/O configuration data block bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	1	0	06
D2	1	0	1	1	0	1	0	0	B4
D3	0	1	LSLP	TxDL	SMC	SMW	SM1	SM0	40
D4	CM0_7	CM0_6	CM0_5	CM0_4	CM0_3	CM0_2	CM0_1	CM0_0	00
D5	CM1_7	CM1_6	CM1_5	CM1_4	CM1_3	CM1_2	CM1_1	CM1_0	00
D6	TH2/TH1	TH2/TH1	TH2/TH1	TH2/TH1	TH2/TH1	TH2/TH1	TH2/TH1	TH2/TH1	00
D7	LWM7	LWM6	LWM5	LWM4	LWM3	LWM2	LWM1	LWM0	00

Table 18. Second I/O configuration data block bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave node address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	SID[7:0]	Service identifier. As SlaveResp the RSID value will be 0xF4.
D3	7 and 6	-	01 for the second configuration data block.
	5	LSLP	Limp home sleep mode. If LSLP = 1, the Limp home sleep mode is enabled. In this case the Limp Home value (LH) is automatically used as output value if the Sleep mode is entered.
	4	TxDL	Transmit data length. Message PxResp contains two data bytes if TxDL = 0 and four data bytes if TxDL = 1.
	3	SMC	Switch matrix capture. If SMC = 1, the Switch matrix capture mode is enabled.
	2	SMW	Switch matrix wake-up. If SMW = 1, the switch matrix wakes up upon changed input level.
	1 and 0	SM[1:0]	Switch matrix enable
			00 = no switch matrix
			01 = 4 × 2: P3 to P0 input and P5 and P4 strong pull down
			10 = 4 × 3: P3 to P0 input and P6 to P4 strong pull down
			11 = 4 × 4: P3 to P0 input and P7 to P4 strong pull down
			Unassigned pins can be used as I/O. It should be noted, however, that for the unassigned pins, which are configured in Capture mode, the captured edge value will not be transferred.

Table 18. Second I/O configuration data block bit description *…continued*

Byte	Bit	Symbol	Description		
D4 and D5	7 to 0	CM0_[7:0], CM1_[7:0]	Capture mode for I/O pin Px.		
			CM1_x	CM0_x	
			0	0	no capture
			0	1	falling edge
			1	0	rising edge
			1	1	both edges
D6	7 to 0	TH2 and TH1	Threshold select. If logic 0 (= TH1), selects V_{th1} as input threshold. If logic 1 (= TH2) selects V_{th2} as input threshold, except in Cyclic sense mode, then V_{th3} is selected.		
D7	7 to 0	LWM_[7:0]	Local wake-up mask. If LWM_x = 1, the corresponding Px pin is configured as local wake-up pin. LWM_x is ignored if Px is configured as switch matrix.		

Table 19 shows the third configuration data block, that is used to define the slope of the transmitter, selection between classic or enhanced checksum model, limp home output value and PWM initial value. It is selected only if D3.7 = 1 and D3.6 = 0.

Table 19. Third I/O configuration data block bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	0	0	04
D2	1	0	1	1	0	1	0	0	B4
D3[1]	1	0	r	r	r	r	LSC	ECC	80
D4	LH7	LH6	LH5	LH4	LH3	LH2	LH1	LH0	00
D5	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0	00
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

[1] r = reserved, must be ‘0’.

Table 20. Third I/O configuration data block bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave node address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	SID[7:0]	Service identifier. As SlaveResp the RSID value will be 0xF4.

Table 20. Third I/O configuration data block bit description *...continued*

Byte	Bit	Symbol	Description
D3	7 and 6	-	10 for the third configuration data block.
	5 to 2	-	Reserved. Must be 0.
	1	LSC	LIN slope control
			0 = up to 20 kbit/s (default)
			1 = up to 10.4 kbit/s
	0	ECC	Enhanced checksum control
			0 = classic checksum (default)
			1 = enhanced checksum
D4	7	LH[7:0]	Limp home value. Output value in Limp home and Limp home sleep mode.
D5	7 to 0	PWM[7:0]	PWM initial value.
D6 and D7	7 to 0	-	Not used.

Table 21 shows the fourth data block, that is selected if D3.6 = 1 and D3.7 = 1. It is not used for I/O-pin configuration but to provide the master with diagnosis data of the UJA1023. It is a read-only data block. If the slave node address matches and the fourth data block is selected, the UJA1023 transmits its diagnosis data via the SlaveResp message.

Table 21. Fourth I/O diagnostic data block request frame bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	0	1	0	02
D2	1	0	1	1	0	1	0	0	B4
D3	1	1	0	0	0	0	0	0	C0
D4	1	1	1	1	1	1	1	1	FF
D5	1	1	1	1	1	1	1	1	FF
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

Table 22. Fourth I/O diagnostic data block request frame bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave node address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	SID[7:0]	Service identifier.
D3	7 and 6	-	11 for the fourth configuration data block.
	5 to 0	-	Not used.
D4 to D7	7 to 0	-	Not used.

Table 23. Fourth I/O diagnostic data block response frame bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	0	0	04
D2	1	1	1	1	0	1	0	0	F4
D3	1	1	0	0	0	0	0	0	C0
D4	P	RxB	CS	TxB	u[1]	NVM	LHE	ERR	00
D5	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

[1] Undefined.

Table 24. Fourth I/O diagnostic data block response frame bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave node address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	RSID[7:0]	Response service identifier.
D3	7 and 6	-	11 for the fourth configuration data block.
	5 to 0	-	Not used.
D4[1]	7	P	Parity error. Set if identifier parity bits are erroneous.
	6	RxB	Receive error. Set if start or stop bits are erroneous during reception.
	5	CS	Checksum error. Set if checksum is erroneous.
	4	TxB	Transmit error. Set if start, data or stop bits are erroneous during transmission.
	3	undefined	-
	2	NVM	No valid message. Set if there is bus activity, but no valid message frame for longer than $t_{to(idle)}$.
	1	LHE	Set if Limp home mode is entered.
	0	ERR	Response error. Sets internal signal Response_Error if there is an RxB, CS or TxB during a response frame.
D5	7 to 0	PL[7:0]	PxOut latch value.
D6 and D7	7 to 0	-	Not used.

[1] All diagnosis flags in byte D4 are reset after data access from master.

7.2.1.6 Configuration examples

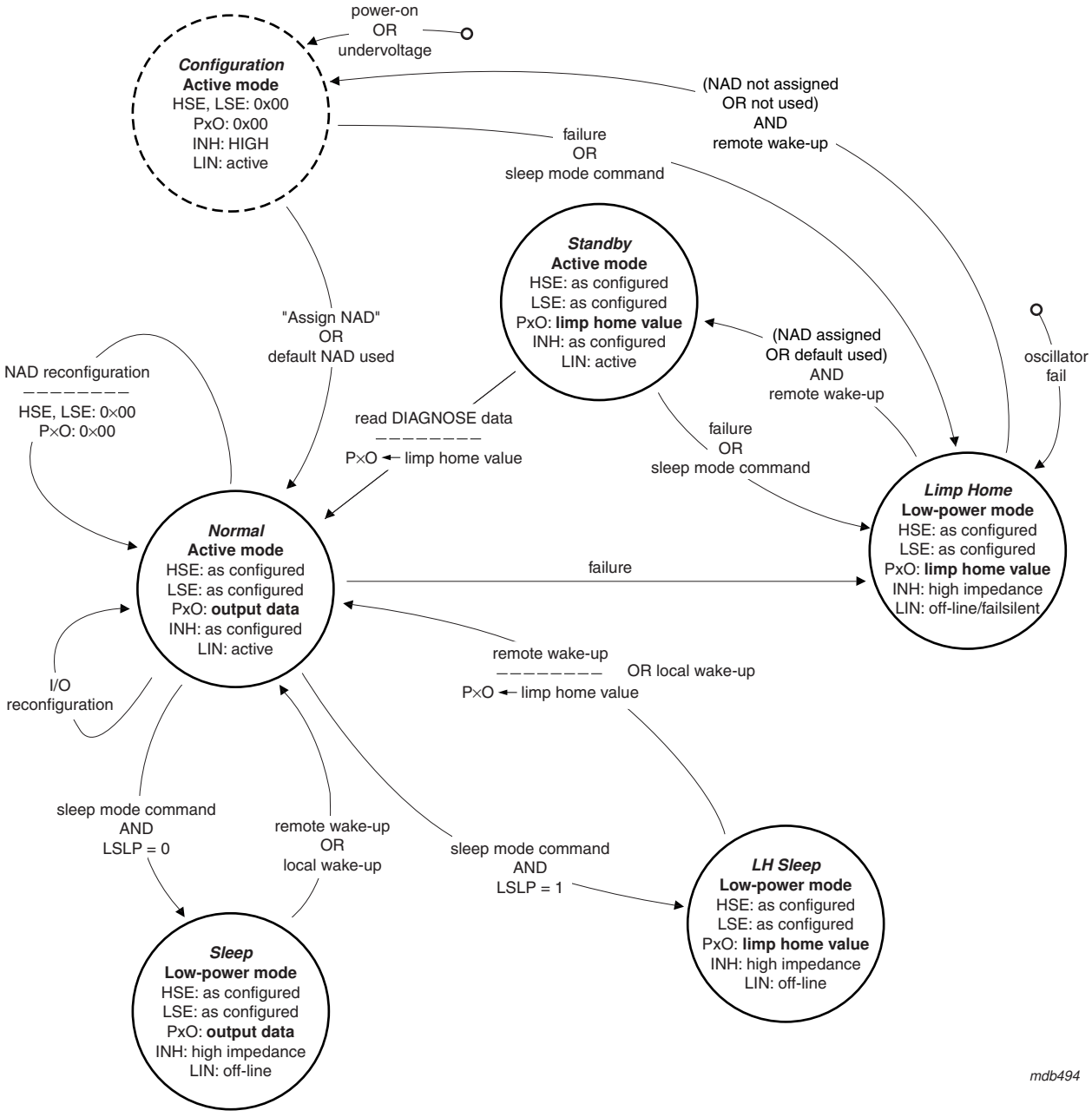
Example 1, UJA1023 configuration with eight low-side outputs.

```
//
//Example 8 LSE and walking '1' pattern
//C1, C2 and C3 are GND
//SB = SyncBreak; SF = SyncField
//
SB SF 3C 60 06 B1 11 00 00 00 04 D2   // Assign frameID, default NAD used and
                                      // ID(PxReq) = 04,ID(PxResp) = 05
SB SF 7D 60 01 F1 FF FF FF FF FF AC   // Positive response
SB SF 3C 60 06 B4 00 00 FF 00 00 E4   // Datadump1, 8 x LSE
SB SF 7D 60 06 F4 00 00 FF 00 00 A4   // Read back configuration sent
SB SF 3C 60 06 B4 40 00 00 00 00 A4   // Datadump2, no capture and
                                      // threshold select (optional)
SB SF 7D 60 06 F4 40 00 00 00 00 64   // Read back configuration sent
SB SF 3C 60 04 B4 80 55 10 FF FF 01   // Data dump3, LH value = 0x55, default
                                                        PWM = 0x10 (optional)
SB SF 7D 60 04 F4 80 55 10 FF FF C0   // Read back configuration sent
SB SF 3C 60 06 B2 00 11 00 00 00 D5   // Read by identifier request (optional)
SB SF 7D 60 06 F2 11 00 00 00 02 93   // Positive response
SB SF C4 01 80 7E                     // IO configuration enabled and low-side
                                      // switch P0 on
SB SF C4 02 80 7D                     // Low-sideswitch P1 on
SB SF C4 04 80 7B                     // Low-sideswitch P2 on
SB SF C4 08 80 77                     // Low-sideswitch P3 on
SB SF C4 10 80 6F                     // Low-sideswitch P4 on
SB SF C4 20 80 5F                     // Low-sideswitch P5 on
SB SF C4 40 80 3F                     // Low-sideswitch P6 on
SB SF C4 80 80 FE                     // Low-sideswitch P7 on
```

Example 2, UJA1023 configuration with eight inputs and edge capture.

```
//
//Example 8 inputs with capture
//C1, C2 and C3 are GND
//SB = SyncBreak; SF = SyncField
//
SB SF 3C 60 06 B1 11 00 00 00 04 D2   // Assign frameID, default NAD used and
                                      // ID(PxReq) = 04,ID(PxResp) = 05
SB SF 7D 60 01 F1 FF FF FF FF FF AC   // Positive response
SB SF 3C 60 06 B4 00 00 00 00 00 E4   // Datadump1, all outputs disabled (optional)
SB SF 7D 60 06 F4 00 00 00 00 00 A4   // Read back configuration sent
SB SF 3C 60 06 B4 40 FF FF 00 FF A4   // Datadump2, all both edge capture and
                                      // inputs as wake-up
SB SF 7D 60 06 F4 40 FF FF 00 FF 64   // Read back configuration sent
SB SF 3C 60 04 B4 80 55 10 FF FF 01   // Data dump3, LH value = 0x55, default
                                                          PWM = 0x10 (optional)
SB SF 7D 60 04 F4 80 55 10 FF FF C0   // Read back configuration sent
SB SF 3C 60 06 B2 00 11 00 00 00 D5   // Read by identifier request (optional)
SB SF 7D 60 06 F2 11 00 00 00 02 93   // Positive response
SB SF 85 00 00 FF                     // IO configuration enabled and read inputs
SB SF 80                              // Dummy message
SB SF 80                              // Dummy message and input 0 changes
SB SF 85 01 01 FD                     // Input 0 set and edge detected
SB SF 80                              //
SB SF 85 01 00 FE                     // Input 0 still set
```

7.2.2 Operating modes



HSE = High-Side Enable

LSE = Low-Side Enable

PxO = PxOut

LSLP = Limp-home sleep

LWM = Local Wake-up Mask

Failure: bus idle time-out or bus dominant time-out

Local: [(LWM = 1) AND ($t > t_{wake(local)}$; after edge capture) causes transmission of LIN wake-up request] AND [reception of LIN header]

Remote: [($t > t_{wake(bus)}$; after falling edge) AND recessive again] AND [reception of LIN header].

Fig 6. Overview of operating modes

7.2.2.1 Configuration mode

The Configuration mode can be seen as initial state after power-on or undervoltage detection. The UJA1023 configuration values are in the default settings. The I/O pins P0 to P7 (Px) are set to high-impedance behavior and the INH is in its External regulator mode, which outputs a HIGH-level in order to switch on an external voltage regulator.

In Configuration mode the UJA1023 is not configured and it has no valid identifier and, depending on the configuration pins, a default NAD. Thus, with the exception of the MasterReq command, all LIN slave commands are disabled. Once the UJA1023 NAD is assigned, via the assign NAD request, or the default NAD is used for the first time, the Normal mode is entered. If a LIN bus failure is present (bus idle time-out or bus dominant time-out) or the sleep command has been received, the UJA1023 enters its low-power (Limp home) mode.

7.2.2.2 Normal mode

In Normal mode the UJA1023 receives and/or transmits input/output data as well as configuration data.

A UJA1023 in Configuration mode enters the Normal mode only after its NAD assignment or the first usage of the default NAD. After a NAD reconfiguration, all ports that are configured in Output mode will be set to high-impedance.

Coming from Sleep mode or Limp home sleep mode the Normal mode can be entered via local or remote wake-up. The output register of each I/O pin P0 to P7 (PxOut) keeps its values of the Sleep mode or Limp home sleep mode. If the INH is in External regulator mode, it outputs a HIGH-level to switch on an external voltage regulator.

For a mode transition from Standby mode to Normal mode the diagnostic data must be read via a SlaveResp. With this request the master acknowledges the previous failure. The PxOut registers keep their limp home values.

7.2.2.3 Sleep mode

The UJA1023 enters its Sleep mode when the ‘Sleep mode command’ has been received and the limp home sleep bit LSLP is reset (LSLP = 0). In Sleep mode the UJA1023 keeps the current status on its Px. The INH will switch to high-impedance state.

After a local wake-up event the UJA1023 sends a ‘wake-up signal’ to wake up the master. In Sleep mode the PWM and ADC are reset. The first LIN message will be lost due to waking up the UJA1023.

7.2.2.4 Limp home sleep mode

Some applications may need dedicated HIGH and/or LOW output levels during Sleep mode in order to achieve the lowest power dissipation of the application. Therefore the UJA1023 provides the Limp home sleep mode (LH sleep mode). By enabling the LSLP bit, the LH sleep mode output behavior can be configured. The LH sleep mode is enabled if the configuration bit LSLP (D3.5) is set (LSLP = 1, see Table 18).

After a local wake-up event the UJA1023 sends a ‘wake-up signal’ to wake up the master. In the LH sleep mode the output registers (PxOut) of the UJA1023 are loaded with the limp home value. After a wake-up event (local or remote wake-up) the PxOut keep their limp home value.