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UJA1066

High-speed CAN fail-safe system basis chip

Rev. 03 — 17 March 2010

Product data sheet

1. General description

The UJA1066 fail-safe System Basis Chip (SBC) replaces basic discrete components which are common in every Electronic Control Unit (ECU) with a Controller Area Network (CAN) interface. The fail-safe SBC supports all networking applications that control various power and sensor peripherals by using high-speed CAN as the main network interface. The fail-safe SBC contains the following integrated devices:

- High-speed CAN transceiver, interoperable and downward compatible with CAN transceiver TJA1041 and TJA1041A, and compatible with the ISO 11898-2 standard and the ISO 11898-5 standard (in preparation)
- Advanced independent watchdog
- Dedicated voltage regulators for microcontroller and CAN transceiver
- Serial peripheral interface (full duplex)
- Local wake-up input port
- Inhibit/limp-home output port

In addition to the advantages of integrating these common ECU functions in a single package, the fail-safe SBC offers an intelligent combination of system-specific functions such as:

- Advanced low-power concept
- Safe and controlled system start-up behavior
- Advanced fail-safe system behavior that prevents any conceivable deadlock
- Detailed status reporting on system and subsystem levels

The UJA1066 is designed to be used in combination with a microcontroller that incorporates a CAN controller. The fail-safe SBC ensures that the microcontroller is always started up in a defined manner. In failure situations, the fail-safe SBC will maintain microcontroller functionality for as long as possible to provide a full monitoring and software-driven fallback operation.

The UJA1066 is designed for 14 V single power supply architectures and for 14 V and 42 V dual power supply architectures.



2. Features and benefits

2.1 General

- Contains a full set of CAN ECU functions:
 - ◆ CAN transceiver
 - ◆ Voltage regulator for the microcontroller (3.3 V or 5.0 V)
 - ◆ Separate voltage regulator for the CAN transceiver (5 V)
 - ◆ Enhanced window watchdog with on-chip oscillator
 - ◆ Serial Peripheral Interface (SPI) for the microcontroller
 - ◆ ECU power management system
 - ◆ Fully integrated autonomous fail-safe system
- Designed for automotive applications:
 - ◆ Supports 14 V and 42 V architectures
 - ◆ Excellent ElectroMagnetic Compatibility (EMC) performance
 - ◆ ±8 kV ElectroStatic Discharge (ESD) protection Human Body Model (HBM) for off-board pins
 - ◆ ±4 kV ElectroStatic Discharge (ESD) protection IEC 61000-4-2 for off-board pins
 - ◆ ±60 V short-circuit proof CAN-bus pins
 - ◆ Battery and CAN-bus pins are protected against transients in accordance with ISO 7637-3
 - ◆ Very low sleep current
- Supports remote flash programming via the CAN-bus
- Small 8 mm × 11 mm HTSSOP32 package with low thermal resistance

2.2 CAN transceiver

- ISO 11898-2 and ISO 11898-5 compliant high-speed CAN transceiver
- Enhanced error signalling and reporting
- Dedicated low dropout voltage regulator for the CAN-bus:
 - ◆ Independent of the microcontroller supply
 - ◆ Guarded by CAN-bus failure management
 - ◆ Significantly improves EMC performance
- Partial networking option with global wake-up feature; allows selective CAN-bus communication without waking up sleeping nodes
- Bus connections are truly floating when power is off
- SPLIT output pin for stabilizing the recessive bus level

2.3 Power management

- Smart operating modes and power management modes
- Cyclic wake-up capability in Standby and Sleep modes
- Local wake-up input with cyclic supply feature
- Remote wake-up capability via the CAN-bus
- External voltage regulators can easily be incorporated into the power supply system (flexible and fail-safe)
- 42 V battery-related high-side switch for driving external loads such as relays and wake-up switches
- Intelligent maskable interrupt output

2.4 Fail-safe features

- Safe and predictable behavior under all conditions
- Programmable fail-safe coded window and time-out watchdog with on-chip oscillator, guaranteeing autonomous fail-safe system supervision
- Fail-safe coded 16-bit SPI interface for the microcontroller
- Global enable pin for the control of safety-critical hardware
- Detection and detailed reporting of failures:
 - ◆ On-chip oscillator failure and watchdog alerts
 - ◆ Battery and voltage regulator undervoltages
 - ◆ CAN-bus failures (short circuits and open-circuit bus wires)
 - ◆ TXD and RXD clamping situations and short circuits
 - ◆ Clamped or open reset line
 - ◆ SPI message errors
 - ◆ Overtemperature warning
 - ◆ ECU ground shift (two selectable thresholds)
- Rigorous error handling based on diagnostics
- Supply failure early warning allows critical data to be stored
- 23 bits of access-protected RAM available (e.g. for logging cyclic problems)
- Reporting in a single SPI message; no assembly of multiple SPI frames needed
- Limp-home output signal for activating application hardware in case system enters Fail-safe mode (e.g. for switching on warning lights)
- Fail-safe coded activation of Software development mode and Flash mode
- Unique SPI readable device type identification
- Software-initiated system reset

3. Ordering information

Table 1. Ordering information

Type number ^[1]	Package		Version
	Name	Description	
UJA1066TW	HTSSOP32	plastic thermal enhanced thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad	SOT549-1

[1] UJA1066TW/5V0 is for the 5 V version; UJA1066TW/3V3 is for the 3.3 V version.

4. Block diagram

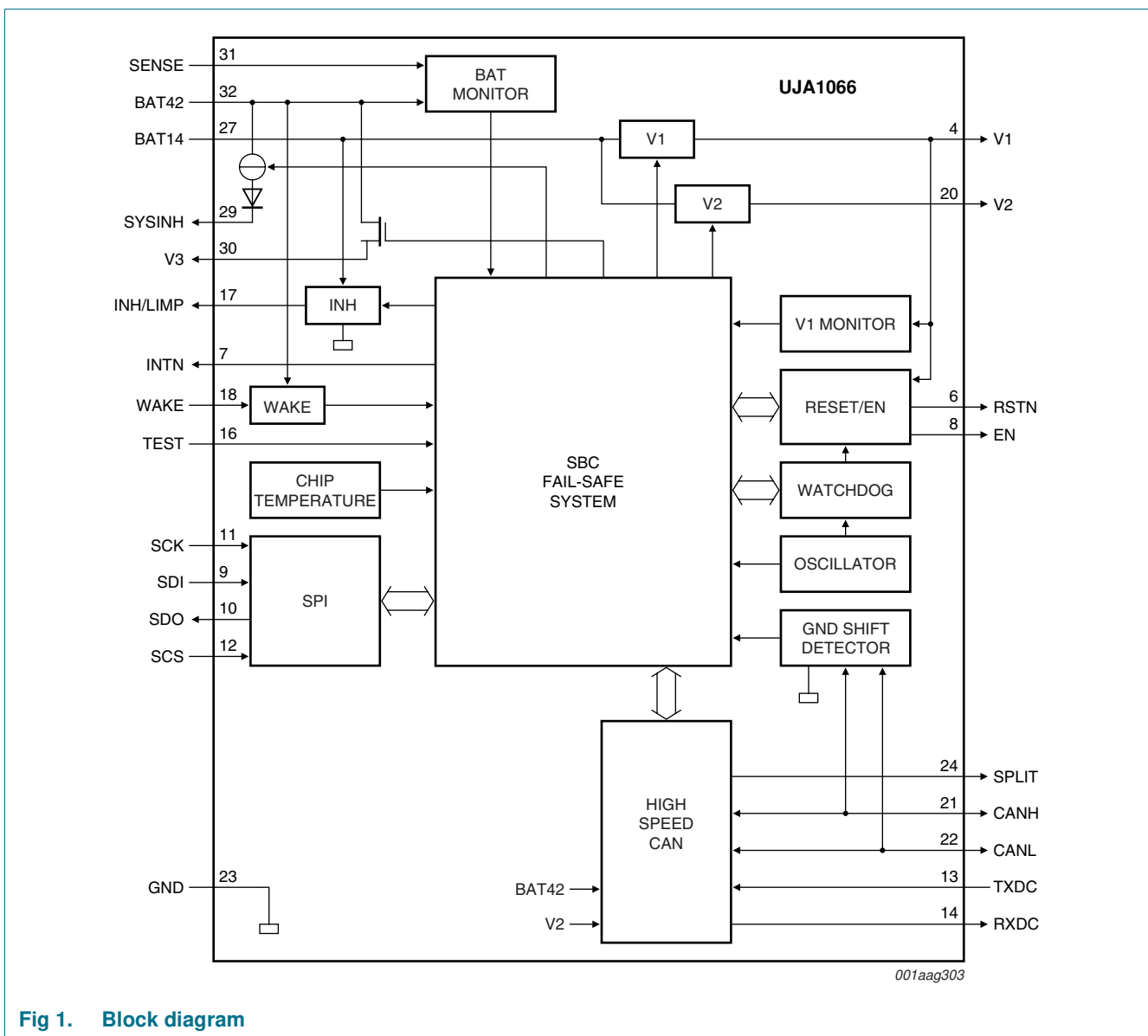


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

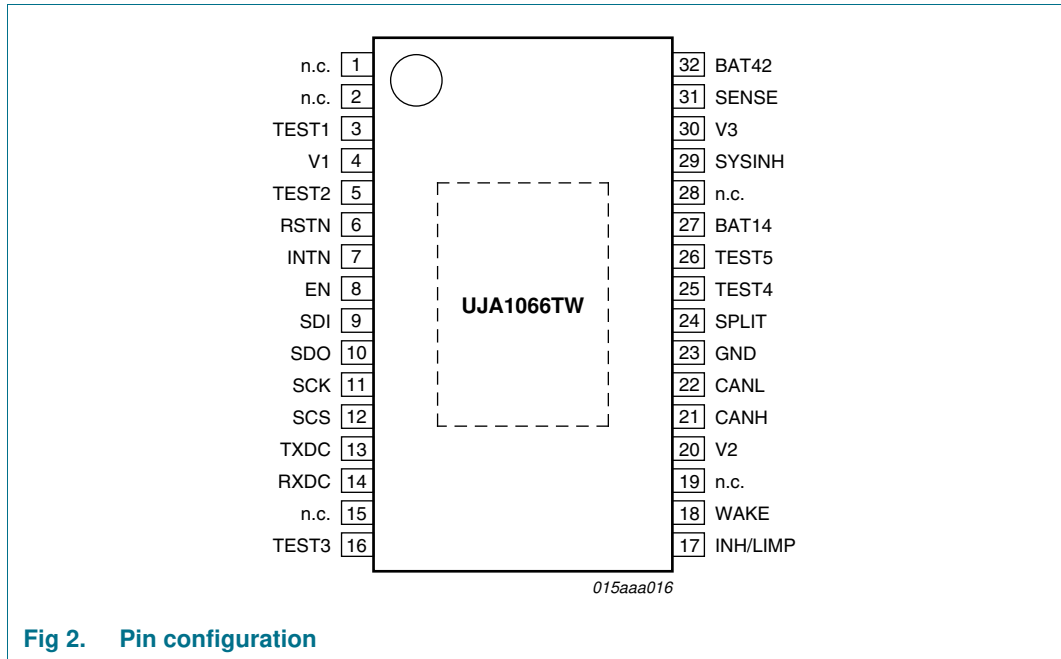


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	1	not connected
n.c.	2	not connected
i.c.	3	internally connected; must be left open in the application
V1	4	voltage regulator output for the microcontroller (3.3 V or 5 V depending on the SBC version)
i.c.	5	internally connected; must be left open in the application
RSTN	6	reset output to microcontroller (active LOW; will detect clamping situations)
INTN	7	interrupt output to microcontroller (active LOW; open-drain; wire-AND this pin to other ECU interrupt outputs)
EN	8	enable output (active HIGH; push-pull; LOW with every reset/watchdog overflow)
SDI	9	SPI data input
SDO	10	SPI data output (floating when pin SCS is HIGH)
SCK	11	SPI clock input
SCS	12	SPI chip select input (active LOW)
TXDC	13	CAN transmit data input (LOW when dominant; HIGH when recessive)
RXDC	14	CAN receive data output (LOW when dominant; HIGH when recessive)
n.c.	15	not connected
TEST	16	test pin (should be connected to ground in the application)

Table 2. Pin description ...continued

Symbol	Pin	Description
INH/LIMP	17	inhibit/limp-home output (BAT14 related, push-pull, default floating)
WAKE	18	local wake-up input (BAT42 related, continuous or cyclic sampling)
n.c.	19	not connected
V2	20	5 V voltage regulator output for CAN; connect a buffer capacitor to this pin
CANH	21	CANH bus line (HIGH in dominant state)
CANL	22	CANL bus line (LOW in dominant state)
GND	23	ground
SPLIT	24	CAN-bus common mode stabilization output
i.c.	25	internally connected; must be connected to pin BAT42 in the application
i.c.	26	internally connected; must be left open in the application
BAT14	27	14 V battery supply input
n.c.	28	not connected
SYSINH	29	system inhibit output; BAT42 related (e.g. for controlling external DC-to-DC converter)
V3	30	unregulated 42 V output (BAT42 related; continuous output or Cyclic mode synchronized with local wake-up input)
SENSE	31	fast battery interrupt / chatter detector input
BAT42	32	42 V battery supply input (connect this pin to BAT14 in 14 V applications)

The exposed die pad at the bottom of the package allows better dissipation of heat from the SBC via the printed-circuit board. The exposed die pad is not connected to any active part of the IC and can be left floating, or can be connected to GND for the best EMC performance.

6. Functional description

6.1 Introduction

The UJA1066 combines all the peripheral functions found around a microcontroller in a typical automotive networking application in a single, dedicated chip. These functions are:

- Power supply for the microcontroller
- Power supply for the CAN transceiver
- Switched BAT42 output
- System reset
- Watchdog with Window and Time-out modes
- On-chip oscillator
- High-speed CAN transceiver for serial communication; suitable for 14 V and 42 V applications
- SPI control interface
- Local wake-up input
- Inhibit or limp-home output
- System inhibit output port
- Compatible with 42 V power supply systems
- Fail-safe behavior

6.2 Fail-safe system controller

The fail-safe system controller is at the core of the UJA1066 and is supervised by a watchdog timer that is clocked directly by the dedicated on-chip oscillator. The system controller manages the register configuration and controls the internal functions of the SBC. Detailed device status information is collected and presented to the microcontroller. The system controller also provides the reset and interrupt signals.

The fail-safe system controller is a state machine. The SBC operating modes, and how transitions between modes are triggered, are illustrated in [Figure 3](#). These modes are discussed in more detail in the following sections.

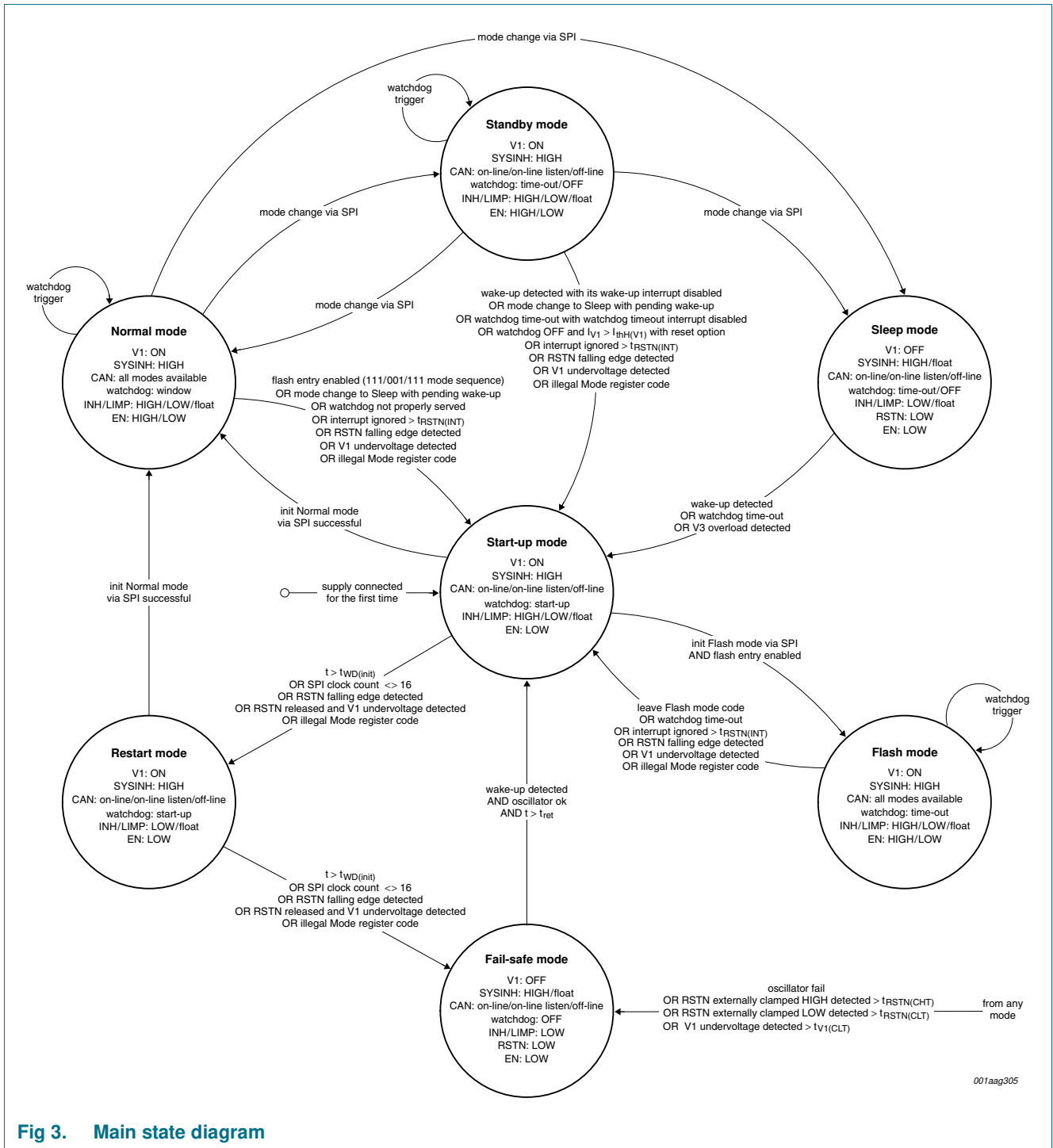


Fig 3. Main state diagram

6.2.1 Start-up mode

Start-up mode is the 'home page' of the SBC. This mode is entered when battery and ground are connected for the first time. Start-up mode is also entered after any event that results in a system reset. The reset source information is provided by the SBC to support software initialization cycles that depend on the reset event.

It is also possible to enter Start-up mode via a wake-up from Standby mode, Sleep mode or Fail-safe mode. Such a wake-up event can be triggered in the CAN-bus or by the local WAKE pin.

A lengthened reset time, t_{RSTNL} , is observed on entering Start-up mode. This reset time is either user-defined (via the RLC bit in the System Configuration register; see [Table 11](#) and [Table 27](#)) or defaults to the value given in [Section 6.12.12](#). Pin RSTN is held LOW by the SBC during the reset lengthening time.

When the reset time has elapsed (pin RSTN is released and goes HIGH) the watchdog timer will wait to be initialized. If the watchdog initialization is successful, the selected operating mode (Normal mode or Flash mode) will be entered. Otherwise the SBC will enter Restart mode.

6.2.2 Restart mode

The purpose of Restart mode is to give the application a second chance to start up, should the first attempt from Start-up mode fail. Entering Restart mode will always set the reset lengthening time t_{RSTNL} to the higher value (see [Table 27](#)) to guarantee the maximum reset length, regardless of previous events.

If start-up from Restart mode is successful (the earlier problems do not recur and watchdog initialization is successful), the SBC will enter Normal mode (see [Figure 3](#)). If problems persist or if V1 fails to start up, the SBC will enter Fail-safe mode.

6.2.3 Fail-safe mode

Severe fault situations will cause the SBC to enter Fail-safe mode. Fail-safe mode is also entered if start-up from Restart mode fails. Fail-safe mode offers the lowest possible system power consumption from the SBC and from the external components controlled by the SBC.

A wake-up (via the CAN-bus or the WAKE pin) is needed to leave Fail-safe mode. This is only possible if the on-chip oscillator is running correctly. The SBC restarts from Fail-safe mode with a defined delay, t_{ret} , to guarantee a discharged V1 before entering Start-up mode. Regulator V1 will restart and t_{RSTNL} will be set to the higher value (see [Section 6.5.1](#)).

6.2.4 Normal mode

Normal mode gives access to all SBC system resources, including CAN, INH/LIMP and EN. The SBC watchdog runs in (programmable) Window mode to guarantee the strictest software supervision. A system reset is performed whenever the watchdog is not being properly served.

Interrupts from the SBC to the host microcontroller are also monitored. A system reset is performed if the host microcontroller does not respond within $t_{RSTN(INT)}$.

Entering Normal mode does not activate the CAN transceiver automatically. The CAN Mode Control (CMC) bit must be set to activate the CAN medium if required, allowing local cyclic wake-up scenarios to be implemented without affecting the CAN-bus.

6.2.5 Standby mode

In Standby mode, the system is in a reduced current consumption state. Entering Standby mode overrides the CMC bit, allowing the CAN transceiver to enter the low-power mode autonomously. The watchdog will, however, continue to monitor the microcontroller (Time-out mode) since it is powered via pin V1.

If the host microcontroller supports a low-power Standby or Stop mode with reduced current consumption, the watchdog can be switched off entirely when the SBS is in Standby mode. The SBC will monitor the microcontroller supply current to ensure that no unobserved phases occur while the watchdog is disabled and the microcontroller is running. The watchdog will remain active until the supply current drops below $I_{thL(V1)}$, when it will be disabled.

Should the current increase to $I_{thH(V1)}$ (e.g. as result of a microcontroller wake-up from application specific hardware) the watchdog will start operating again with the previously used time-out period. If the watchdog is not triggered correctly, a system reset will occur and the SBC will enter Start-up mode.

If Standby mode is entered from Normal mode with the selected watchdog OFF option, the watchdog will use the maximum time-out as defined for Standby mode until the supply current drops below the current detection threshold; the watchdog is now OFF. If the current increases again, the watchdog will be activated immediately, again using the maximum watchdog time-out period. If the watchdog OFF option is selected during Standby mode, the watchdog period last used will define the time for the supply current to fall below the current detection threshold. This allows the user to align the current supervisor function with the requirements of the application.

Generally, the microcontroller can be activated from Standby mode via a system reset or via an interrupt without reset. This allows for the implementation of differentiated start-up behavior from Standby mode, depending on the needs of the application:

- If the watchdog is still running during Standby mode, it can be used for cyclic wake-up behavior of the system. A dedicated Watchdog Time-out Interrupt Enable (WTIE) bit allows the microcontroller to decide whether to receive an interrupt or a hardware reset upon overflow. The interrupt option will be cleared in hardware automatically with each watchdog overflow to ensure that a failing main routine is detected while the interrupt service is still operating. So the application software must set the interrupt behavior before each standby cycle begins.
- Any wake-up via the CAN-bus together with a local wake-up event will force a system reset event or generate an interrupt to the microcontroller. So it is possible to exit Standby mode without performing a system reset if necessary.

When an interrupt event occurs, the application software has to read the Interrupt register within $t_{RSTN(INT)}$. Otherwise a fail-safe system reset is forced and Start-up mode will be entered. If the application has read out the Interrupt register within the specified time, it can decide whether to switch to Normal mode via an SPI access or to remain in Standby mode.

The following operations are possible from Standby mode:

- Cyclic wake-up by the watchdog via an interrupt signal to the microcontroller (the microcontroller is triggered periodically and checked for the correct response)
- Cyclic wake-up by the watchdog via a reset signal (a reset is performed periodically; the SBC provides information about the reset source to allow different start sequences after reset)
- Wake-up by activity on the CAN-bus via an interrupt signal to the microcontroller
- Wake-up by bus activity on the CAN-bus via a reset signal
- Wake-up by increasing the microcontroller supply current without a reset signal (where a stable supply is needed for the microcontroller RAM contents to remain valid and wake-up from an external application not connected to the SBC)
- Wake-up by increasing the microcontroller supply current with a reset signal
- Wake-up due to a falling edge at pin WAKE forcing an interrupt to the microcontroller
- Wake-up due to a falling edge at pin WAKE forcing a reset signal

6.2.6 Sleep mode

In Sleep mode the microcontroller power supply (V1) and the INH/LIMP-controlled external supplies are switched off entirely, resulting in minimum system power consumption. In this mode, the watchdog runs in Time-out mode or is completely off.

Entering Sleep mode results in an immediate LOW level on pin RSTN, stopping all microcontroller operations. The INH/LIMP output is floating in parallel and pin V1 is disabled. Only pin SYSINH can remain active to support the V2 voltage supply (if bit V2C is set; see [Table 12](#)). V3 can also be ON, OFF or in Cyclic mode to supply external wake-up switches.

If the watchdog is not disabled by software, it will continue to run and will force a system reset once the programmed watchdog period has expired. The SBC then enters Start-up mode and pin V1 becomes active again. This behavior can be used to implement cyclic wake-up from Sleep mode.

Depending on the application, the following operations can be selected from Sleep mode:

- Cyclic wake-up by the watchdog (only in Time-out mode); a reset is performed periodically, the SBC provides information about the reset source to allow the microcontroller to choose between different start up sequences after reset
- Wake-up by activity on the CAN-bus or falling edge on pin WAKE
- An overload on V3, only if V3 is in a cyclic or a continuously ON mode

6.2.7 Flash mode

Flash mode can only be entered from Normal mode by entering a specific Flash mode entry sequence. This fail-safe control sequence comprises three consecutive write accesses to the Mode register, within the legal windows of the watchdog, using the operating mode codes 111, 001 and 111 respectively. Once this sequence has been received, the SBC will enter Start-up mode and perform a system reset using the related reset source information (bits RSS[3:0] = 0110).

Once in Start-up mode the application software has to write Operating Mode code 011 to the Mode register within $t_{WD(init)}$ to initiate a transition to Flash mode. This causes a successfully received hardware reset (handshake between the SBC and the microcontroller) to be fed back. The transition from Start-up mode to Flash mode can only occur once after the Flash entry sequence has been completed.

The application can choose not to enter Flash mode but instead return to Normal mode by using the Operating Mode code 101 for handshaking. This erases the Flash mode entry sequence.

The watchdog behavior in Flash mode is similar to its time-out behavior in Standby mode, but Operating Mode code 111 must be used for serving the watchdog. If this code is not used or if the watchdog overflows, the SBC will immediately force a reset and a transition to Start-up mode. Operating Mode code 110 (leave Flash mode) is used to correctly exit Flash mode. This results in a system reset with the corresponding reset source information. Other Mode register codes will cause a forced reset with reset source code 'illegal Mode register code'.

6.3 On-chip oscillator

The on-chip oscillator provides the clock signal for all digital functions and is the timing reference for the on-chip watchdog and the internal timers.

If the on-chip oscillator frequency is too low or the oscillator is not running at all, there is an immediate transition to Fail-safe mode. The SBC will stay in Fail-safe mode until the oscillator has recovered to its normal frequency and the system receives a wake-up event.

6.4 Watchdog

The watchdog provides the following timing functions:

- Start-up mode; needed to give the software the opportunity to initialize the system
- Window mode; detects 'too early' and 'too late' accesses in Normal mode
- Time-out mode; detects a 'too late' access, can also be used to restart or interrupt the microcontroller from time to time (cyclic wake-up function)
- OFF mode; fail-safe shutdown during operation prevents any blind spots occurring in the system supervision

The watchdog is clocked directly by the on-chip oscillator.

To guarantee fail-safe control of the watchdog via the SPI, all watchdog accesses are coded with redundant bits. Therefore, only certain codes are allowed for a proper watchdog service.

The following corrupted watchdog accesses result in an immediate system reset:

- Illegal watchdog period coding; only ten different codes are valid
- Illegal operating mode coding; only six different codes are valid

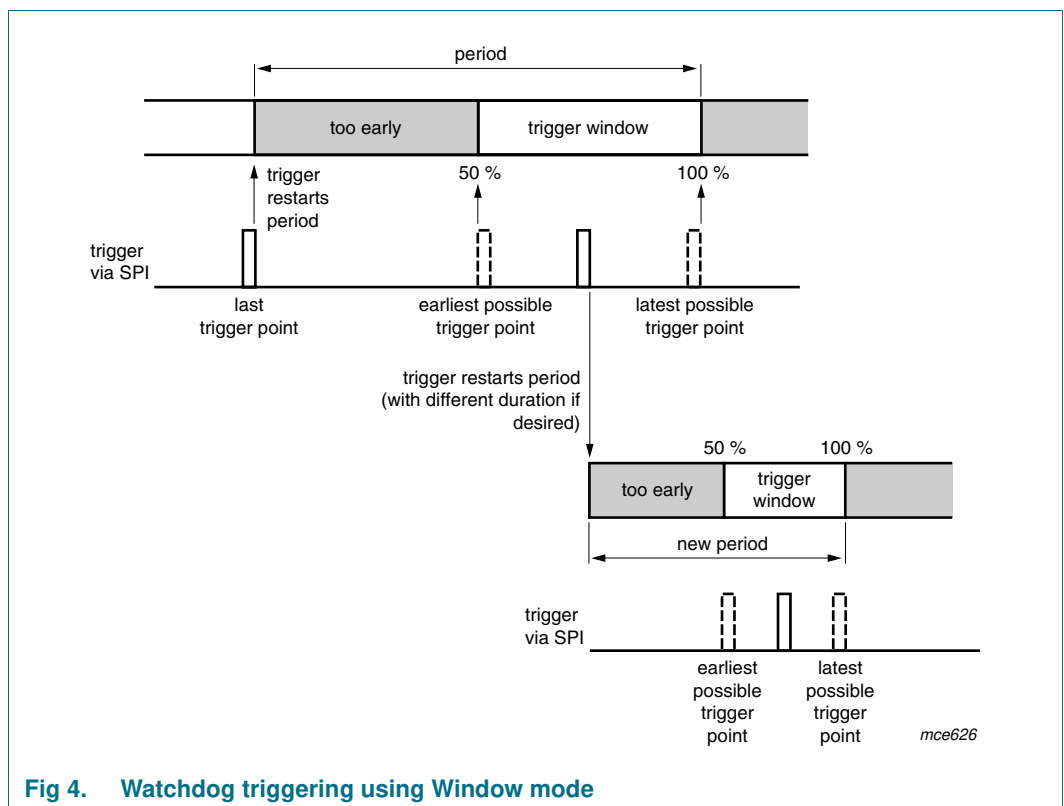
Any microcontroller-driven mode change is synchronized with a watchdog access by reading the mode information and the watchdog period information from the same register. This facilitates easy software flow control with defined watchdog behavior when switching between different software modules.

6.4.1 Watchdog start-up behavior

Following any reset event, the watchdog is used to monitor the ECU start-up procedure. It checks the behavior of the RSTN pin for clamping conditions or an interrupted reset wire. If the watchdog is not properly served within $t_{WD(init)}$, another reset is forced and the monitoring procedure is restarted. If the watchdog is again not properly served, the system enters Fail-safe mode (see also [Figure 3](#), Start-up mode and Restart mode).

6.4.2 Watchdog window behavior

When the SBC enters Normal mode, the Window mode of the watchdog is activated. This ensures that the microcontroller operates within the required speed window; an operation that is too fast or too slow will be detected. Watchdog triggering using Window mode is illustrated in [Figure 4](#).



The SBC provides 10 different period timings, scalable with a 4-factor watchdog prescaler. The period can be changed within any valid trigger window. Whenever the watchdog is triggered within the window time frame, the timer will be reset to start a new period.

The watchdog window is defined to be between 50 % and 100 % of the nominal programmed watchdog period. Any ‘too early’ or ‘too late’ watchdog access or incorrect Mode register code access will result in an immediate system reset, when the SBC will revert to Start-up mode.

6.4.3 Watchdog time-out behavior

When the SBC is in Standby, Sleep or Flash mode, the active watchdog operates in Time-out mode. The watchdog has to be triggered within the programmed time frame (see [Figure 5](#)). Time-out mode can be used to generate cyclic wake-up events for the host microcontroller from Standby and Sleep modes.

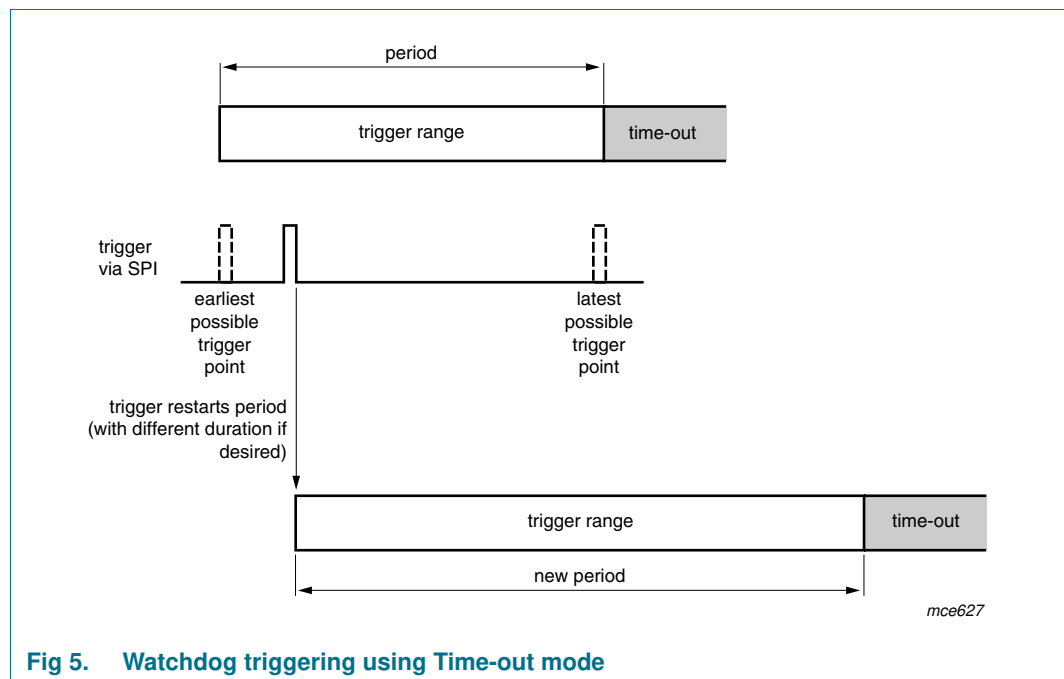


Fig 5. Watchdog triggering using Time-out mode

In Standby and Flash modes, the nominal periods can be changed with any SPI access to the Mode register.

Any illegal watchdog trigger code results in an immediate system reset, when the SBC will revert to Start-up mode.

6.4.4 Watchdog OFF behavior

In Standby and Sleep modes, the watchdog can be switched off entirely. For fail-safe reasons this is only possible if the microcontroller has halted program execution. To ensure that there is no continuing program execution, the V1 supply current is monitored by the SBC while the watchdog is switched off.

When selecting the watchdog OFF code, the watchdog remains active until the microcontroller supply current has dropped below the current monitoring threshold $I_{thL(V1)}$. Once the supply current has dropped below this threshold, the watchdog stops at the end of the watchdog period. The watchdog will remain active as long as the supply current remains above the monitoring threshold.

If the microcontroller supply current rises above $I_{thH(V1)}$ while the watchdog is OFF, the watchdog will be restarted using the watchdog period last used and, if enabled, a watchdog restart interrupt will be generated.

In the case of a direct mode change to Standby with watchdog OFF selected, the longest possible watchdog period is used. It should be noted that V1 current monitoring is not active in Sleep mode.

6.5 System reset

The reset function of the UJA1066 provides two signals to deal with reset events:

- RSTN; the global ECU system reset
- EN; a fail-safe global enable signal

6.5.1 RSTN pin

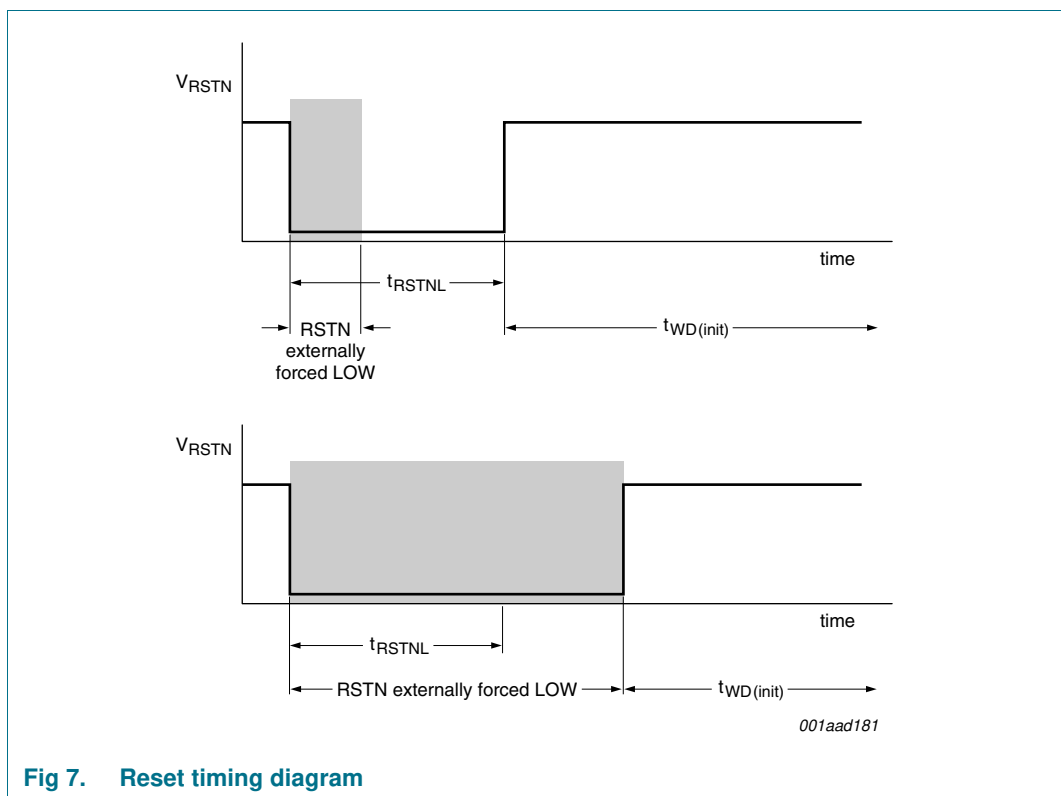
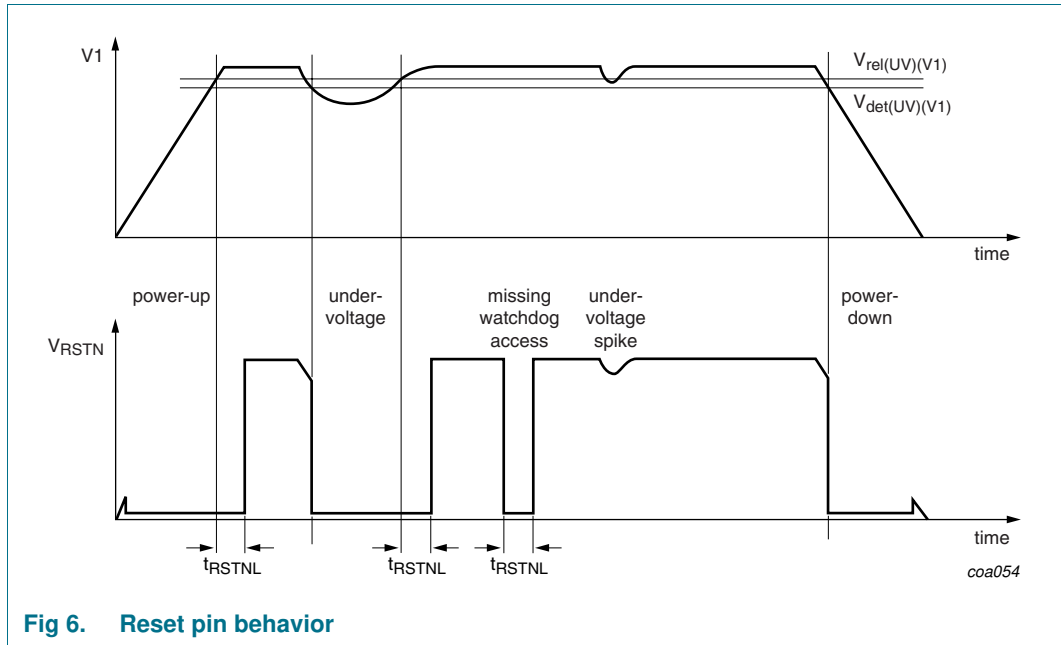
The system reset pin (RSTN) is a bidirectional input/output. RSTN is active LOW with a selectable pulse length triggered by the following events (see [Figure 3](#)):

- Power-on (first battery connection) or V_{BAT42} below power-on reset threshold voltage
- Low V1 supply
- V1 current above threshold in Standby mode while watchdog OFF behavior is selected
- V3 is down due to short-circuit condition in Sleep mode
- RSTN externally forced LOW, falling edge event
- Successful preparation for Flash mode completed
- Successful exit from Flash mode
- Wake-up from Standby mode via pins CAN or WAKE if programmed accordingly, or any wake-up event from Sleep mode
- Wake-up event from Fail-safe mode
- Watchdog trigger failure (too early, overflow, wrong code)
- Illegal mode code applied via SPI
- Interrupt not served within $t_{RSTN(INT)}$

The source of the reset event can be determined by reading the RSS[3:0] bits in the System Status registers.

The SBC will lengthen a reset event, to 1 ms or 20 ms, to ensure that external hardware is properly reset. When the battery is connected initially, a short power-on reset of 1 ms is generated once voltage V1 is present. Once started, the microcontroller can set the Reset Length Control (RLC) bit in the System Configuration register; this allows the reset pulse to be adjusted for future reset events. When this bit is set, reset events are lengthened to 20 ms. Fail-safe behavior ensures that this bit is set automatically (to 20 ms) in Restart and Fail-safe modes. This mechanism guarantees that an erroneously shortened reset pulse will still restart the microcontroller, at least within the second trial period by using the long reset pulse.

The behavior of pin RSTN is illustrated in [Figure 6](#). The duration of t_{RSTNL} depends on the setting of bit RLC (which defines the reset length). Once an external reset event has been detected, the system controller enters Start-up mode. The watchdog now starts to monitor pin RSTN as illustrated in [Figure 7](#). If the RSTN pin is not released in time, the SBC will enter Fail-safe mode (see [Figure 3](#)).



Pin RSTN is monitored for a continuously clamped LOW condition. If the SBC pulls RSTN HIGH, but it remains LOW for longer than $t_{RSTN(CL)}$, the SBC immediately enters Fail-safe mode since this indicates an application failure.

The SBC also detects if pin RSTN is clamped HIGH. If the SBC pulls RSTN LOW, but it remains HIGH for longer than $t_{RSTN(CH)}$, the SBC immediately falls back to Fail-safe mode since the microcontroller can no longer be reset. On entering Fail-safe mode, the V1 voltage regulator shuts down and the microcontroller stops running.

Additionally, chattering reset signals are handled by the SBC in such a way that the system safely falls back to Fail-safe mode with the lowest possible power consumption.

6.5.2 EN output

Pin EN can be used to control external hardware, such as power components, or as a general purpose output if the system is running properly. During all reset events, when pin RSTN is pulled LOW, the EN control bit is cleared and pin EN is forced LOW. It will remain LOW after pin RSTN is released. In Normal and Flash modes, the microcontroller can set the EN control bit via the SPI. This releases pin EN, which goes HIGH.

6.6 Power supplies

6.6.1 BAT14, BAT42 and SYSINH

The SBC contains two supply pins, BAT42 and BAT14. BAT42 supplies most of the SBC while BAT14 only supplies the linear voltage regulators and the INH/LIMP output pin. This supply architecture facilitates different supply strategies, including the use of external DC-to-DC converters controlled by pin SYSINH.

6.6.1.1 SYSINH output

The SYSINH output is a high-side switch from BAT42. It is activated whenever the SBC requires a supply voltage for pin BAT14 (e.g. when V1 or V2 is on; see [Figure 3](#) and [Figure 8](#)). Otherwise pin SYSINH is left floating. Pin SYSINH can be used, for example, to control an external step-down voltage regulator to BAT14, to reduce power consumption in low-power modes.

6.6.2 SENSE input

The SBC has a dedicated SENSE pin for dynamic monitoring of the battery contact in an ECU. Connecting this pin in front of the polarity protection diode in an ECU provides an early warning of a battery becoming disconnected.

6.6.3 Voltage regulators V1 and V2

The UJA1066 contains two independent voltage regulators supplied from pin BAT14. Regulator V1 is intended to supply the microcontroller. Regulator V2 is reserved for the high-speed CAN transceiver.

6.6.3.1 Voltage regulator V1

The voltage at V1 is continuously monitored to ensure a system reset signal is generated when an undervoltage event occurs. A hardware reset is forced if the output voltage at V1 falls below one of the three programmable thresholds.

A dedicated V1 supply comparator (V1 Monitor) monitors V1 for undervoltage events ($V_{O(V1)} < V_{UV(VF1)}$). This allows the application to receive a supply warning interrupt if one of the lower V1 undervoltage reset thresholds has been selected (see [Table 13](#)).

Regulator V1 is overload protected. The maximum output current available at pin V1 depends on the voltage applied at pin BAT14 (see [Section 9 “Static characteristics”](#)). Total power dissipation should be taken into account for thermal reasons.

6.6.3.2 Voltage regulator V2

Voltage regulator V2 provides a 5 V supply for the CAN transmitter. An external buffer capacitor should be connected to pin V2.

V2 is controlled autonomously by the CAN transceiver control system and is activated on any detected CAN-bus activity, or if the CAN transceiver is enabled by the application microcontroller. V2 is short-circuit protected and will be disabled in an overload situation. Dedicated bits in the System Diagnosis register and the Interrupt register provide V2 status feedback to the application.

In addition to being controlled autonomously by the CAN transceiver control system, V2 can be activated manually via bit V2C (in [Table 12](#)). This allows V2 to be used in applications when CAN is not actively used (e.g. while CAN is off-line). In general, V2 should not be used with other application hardware while CAN is in use.

If regulator V2 is unable to start up within the V2 clamped LOW time ($> t_{V2(CL T)}$), or if a short circuit is detected while V2 is active, V2 is disabled and bit V2D in the Diagnosis register is cleared (see [Table 8](#)). In addition, bit CTC in the Physical Layer register is set and the V2C bit is cleared (see in [Table 12](#)).

Any of the following events will reactivate regulator V2:

- Clearing bit CTC while CAN is in Active mode
- Wake up via CAN while CAN is not in Active mode
- Setting bit V2C
- Entering CAN Active mode

6.6.4 Switched battery output V3

V3 is a high-side switched BAT42-related output which is used to drive external loads such as wake-up switches or relays. The features of V3 are as follows:

- Three application controlled modes of operation; ON, OFF and Cyclic mode.
- Two different cyclic modes allow for the supply of external wake-up switches; these switches are powered intermittently, thus reducing system power consumption when a switch is continuously active; the wake-up input of the SBC is synchronized with the V3 cycle time.
- The switch is protected against current overloads. If V3 is overloaded, pin V3 is automatically disabled. The corresponding Diagnosis register bit (V3D) is reset and a VFI interrupt is generated (if enabled). During Sleep mode, a wake-up is forced and the corresponding reset source code (0100) can be read via the RSS bits of the System Status register. This signals that the wake-up source via V3 supplied wake-up switches has been lost.

6.7 CAN transceiver

The integrated high-speed CAN transceiver on the UJA1066 is an advanced ISO 11898-2 and ISO 11898-5 compliant transceiver. In addition to standard high-speed CAN transceiver features, the UJA1066 transceiver provides the following:

- Enhanced error handling and reporting of bus and RXD/TXD failures; these failures are separately identified in the System Diagnosis register
- Integrated autonomous control system for determining the mode of the CAN transceiver
- Ground shift detection with two selectable warning levels, to detect possible local ground problems before the CAN communication is affected
- On-line Listen mode with global wake-up message filter allows partial networking
- Bus connections are truly floating when power is off

6.7.1 Mode control

The CAN transceiver controller supports four operating modes: Active mode, On-line mode, On-line Listen mode and Off-line mode; see [Figure 8](#).

Two dedicated CAN status bits (CANMD) in the Diagnosis register are provided to indicate the operating mode.

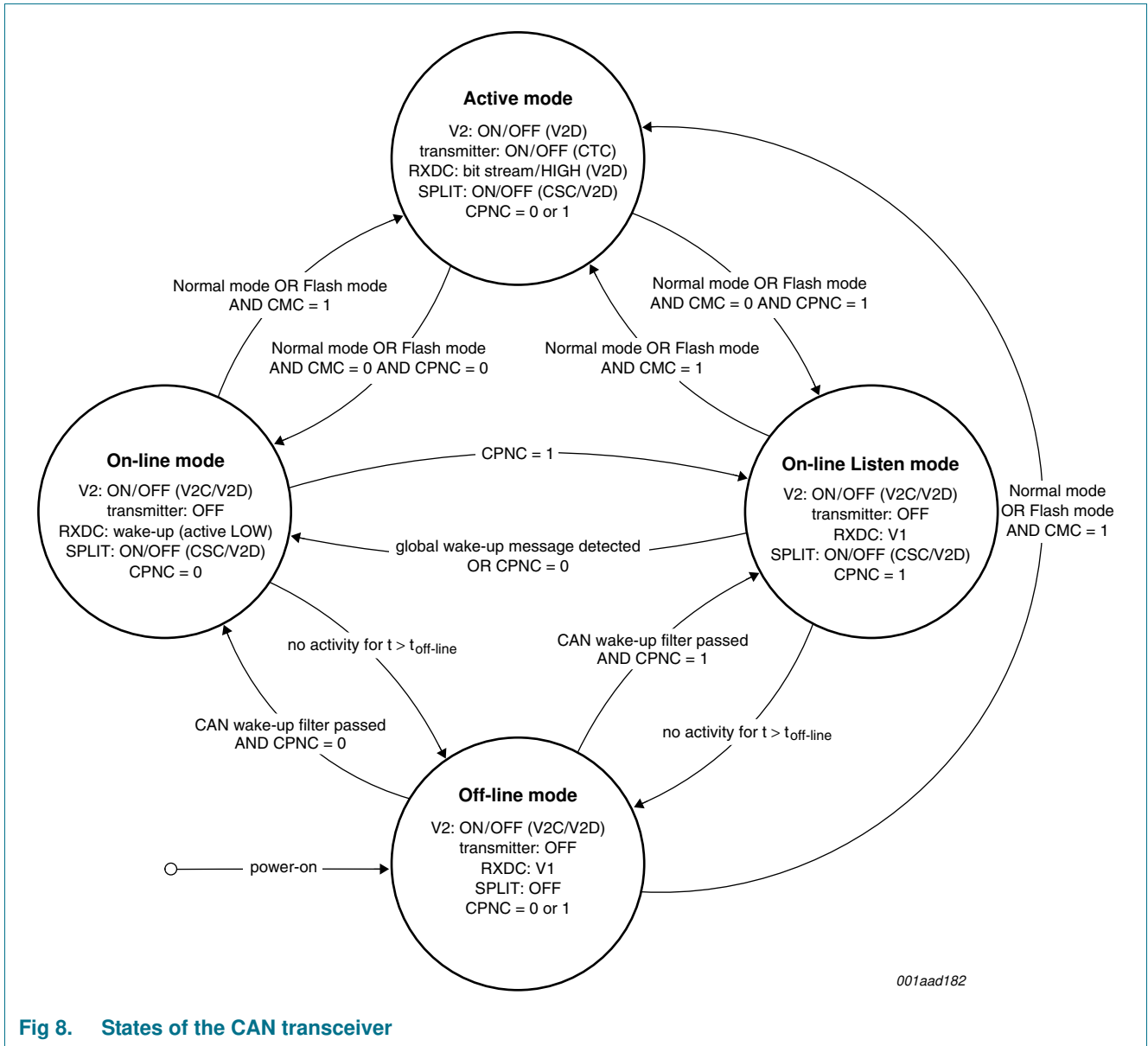


Fig 8. States of the CAN transceiver

6.7.1.1 Active mode

In Active mode, the CAN transceiver can transmit data to and receive data from the CAN-bus. The CMC bit in the Physical Layer register must be set and the SBC must be in Normal or Flash mode before the transceiver can enter Active mode. In Active mode, voltage regulator V2 is activated automatically.

The CTC bit can be used to set the CAN transceiver to a Listen-only mode. The transmitter output stage is disabled in this mode.

After an overload condition on voltage regulator V2, the CTC bit must be cleared to reactivate the CAN transmitter.

On leaving Active mode, the CAN transmitter is disabled and the CAN receiver monitors the CAN-bus for a valid wake-up. The CAN termination is then working autonomously.

6.7.1.2 On-line mode

In On-line mode the CAN-bus pins and pin SPLIT (if enabled) are biased to the normal levels. The CAN transmitter is deactivated and RXDC reflects the CAN wake-up status. A CAN wake-up event is signalled to the microcontroller by clearing RXDC.

If the bus stays continuously dominant or recessive for the Off-line time ($t_{\text{off-line}}$), the Off-line state will be entered.

6.7.1.3 On-line Listen mode

On-line Listen mode is similar to On-line mode, but all activity on the CAN-bus, with the exception of a special global wake-up request, is ignored. The global wake-up request is described in [Section 6.7.2](#). Pin RXDC is held HIGH.

6.7.1.4 Off-line mode

Off-line mode is the low-power mode of the CAN transceiver. The CAN transceiver is disabled to save supply current and is high-ohmic terminated to ground.

The CAN off-line time is programmable in two steps with the CAN Off-line Timer Control (COTC) bit. When entering On-line (Listen) mode from Off-line mode the CAN off-line time is temporarily extended to $t_{\text{off-line(Ext)}}$.

6.7.2 CAN wake-up

To wake-up the UJA1066 via CAN it is necessary to distinguish between a conventional wake-up and a global wake-up in case partial networking is enabled (bit CPNC = 1).

A dominant, recessive, dominant, recessive signal on the CAN-bus is needed to pass the wake-up filter for a conventional wake-up; see [Figure 9](#).

For a global wake-up from On-line Listen mode, two distinct CAN data patterns are required:

- In the initial message: C6 - EE - EE - EE - EE - EE - EE - EF (hexadecimal values)
- In the global wake-up message: C6 - EE - EE - EE - EE - EE - EE - 37 (hexadecimal values)

The second pattern must be received within t_{timeout} after receiving the first pattern. Any CAN-ID can be used with these data patterns.

If the CAN transceiver enters On-line Listen mode directly from Off-line mode, the global wake-up message is sufficient to wake-up the SBC. This pattern must be received within t_{timeout} after entering On-line Listen mode. Should t_{timeout} elapse before the global wake-up message is received, then both messages are required for a CAN wake-up.

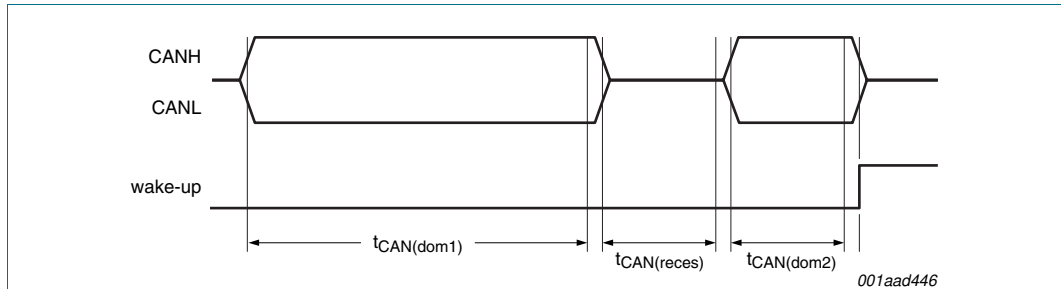


Fig 9. CAN wake-up timing diagram.

6.7.3 Termination control

In Active mode, On-line mode and On-line Listen mode, CANH and CANL are terminated to $0.5 \times V_{V2}$ via R_i . In Off-line mode CANH and CANL are terminated to GND via R_i . If V2 is disabled due to an overload condition both pins become floating.

6.7.4 Bus, RXD and TXD failure detection

The UJA1066 can distinguish between bus, RXD and TXD failures as indicated in Table 3.

All failures are signalled individually in the CANFD bits in the System Diagnosis register. Any change (detection and recovery) generates a CANFI interrupt to the microcontroller, if the interrupt is enabled.

Table 3. CAN-bus, RXD and TXD failure detection

Failure	Description
HxHIGH	CANH short-circuit to V_{CC} , V_{BAT14} or V_{BAT42}
HxGND	CANH short-circuit to GND
LxHIGH	CANL short-circuit to V_{CC} , V_{BAT14} or V_{BAT42}
LxGND	CANL short-circuit to GND
HxL	CANH short-circuit to CANL
Bus dom	bus is continuously clamped dominant
TXDC dom	pin TXDC is continuously clamped dominant
RXDC reces	pin RXDC is continuously clamped recessive
RXDC dom	pin RXDC is continuously clamped dominant

6.7.4.1 TXDC dominant clamping

If the TXDC pin is clamped dominant for longer than $t_{TXDC(dom)}$, the CAN transmitter will be disabled. After the TXDC pin becomes recessive, the transmitter is reactivated automatically when bus activity is detected or can be reactivated manually by setting and clearing the CTC bit.

6.7.4.2 RXDC recessive clamping

If the RXDC pin is clamped recessive while the CAN-bus is dominant, the CAN transmitter will be disabled. The transmitter will be reactivated automatically when RXDC becomes dominant or can be reactivated manually by setting and clearing the CTC bit.

6.7.4.3 GND shift detection

The SBC can detect ground shifts in reference to the CAN-bus. Two different ground shift detection levels can be selected with the GSTHC bit in the Configuration register. The failure can be read out in the System Diagnosis register. Any detected or recovered GND shift event is signalled via a GSI an interrupt, if enabled.

6.8 Inhibit and limp-home output

The INH/LIMP output pin is a 3-state output, which can be used either as an inhibit for an extra (external) voltage regulator or as a 'limp-home' output. The pin is controlled via bits ILEN and ILC in the System Configuration register; see [Figure 10](#).

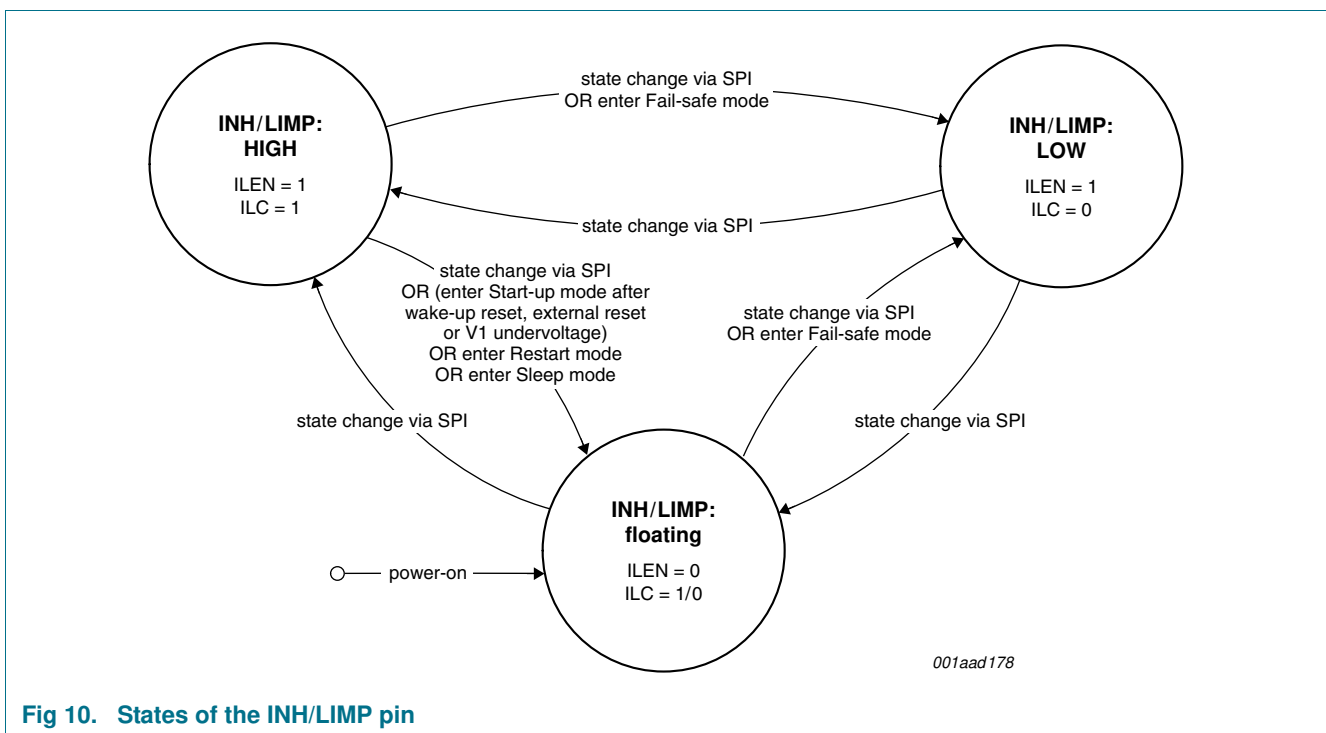


Fig 10. States of the INH/LIMP pin

When pin INH/LIMP is used as an inhibit output, a pull-down resistor to GND ensures a default LOW level. The pin can be set HIGH according to the state diagram.

When pin INH/LIMP is used as limp-home output, a pull-up resistor to V_{BAT42} ensures a default HIGH level. The pin is automatically set LOW when the SBC enters Fail-safe mode.

6.9 Wake-up input

The WAKE input comparator is triggered by negative edges on pin WAKE. Pin WAKE has an internal pull-up resistor to BAT42. It can be operated in two sampling modes, which are selected via the WAKE Sample Control bit (WSC in [Table 11](#)):

- Continuous sampling (with an internal clock) if the bit is set
- Sampling synchronized to the cyclic behavior of V3 if the bit is cleared; see [Figure 11](#). This is to minimize bias current in the external switches during low-power operation. Two repetition times are possible, 16 ms and 32 ms.

If V3 is continuously ON, the WAKE input will be sampled continuously, regardless of the level of bit WSC.

The dedicated bits Edge Wake-up Status (EWS) and WAKE Level Status (WLS) in the System Status register reflect the actual status of pin WAKE. The WAKE port can be disabled by clearing bit WEN in the System Configuration register.

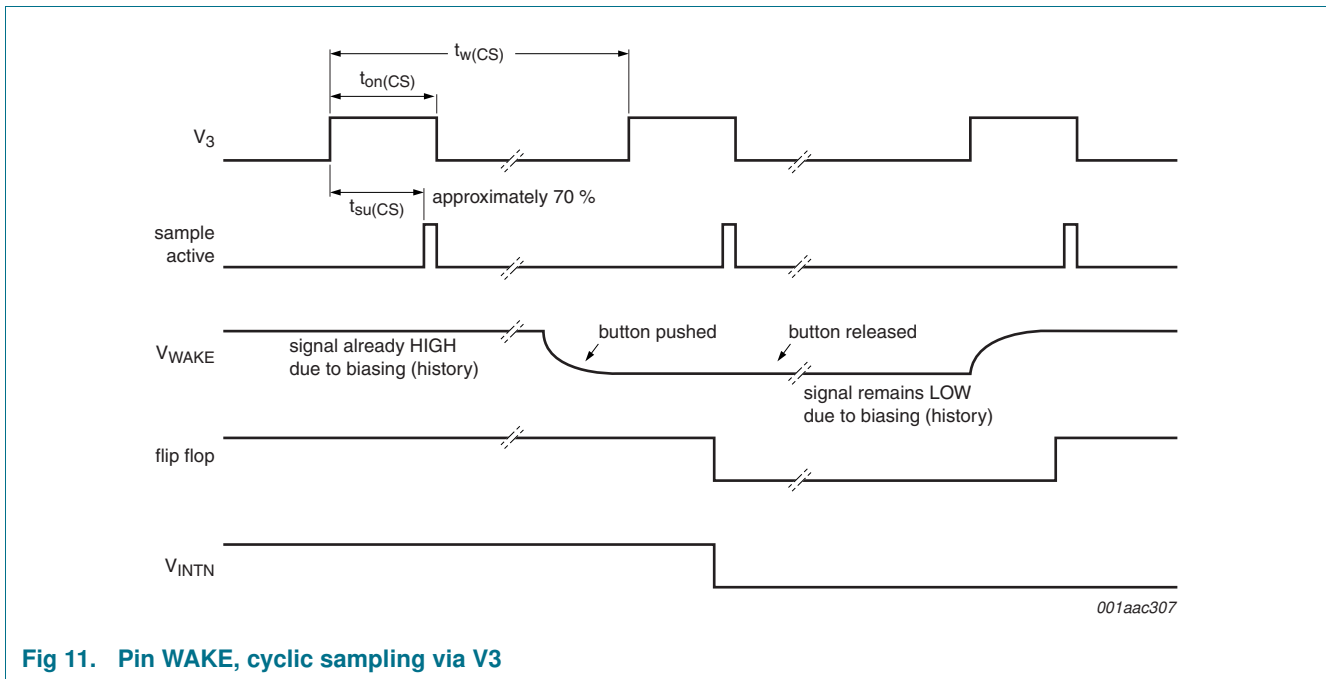


Fig 11. Pin WAKE, cyclic sampling via V3

6.10 Interrupt output

Pin INTN is an open-drain interrupt output. It is forced LOW when at least one bit in the Interrupt register is set. All bits are cleared when the Interrupt register is read. The Interrupt register is also cleared during a system reset (RSTN LOW).

As the microcontroller operates typically with an edge-sensitive interrupt port, pin INTN will be HIGH for at least t_{INTN} after each readout of the Interrupt register. If no further interrupts are generated within t_{INTNH} , INTN will remain HIGH; otherwise it will go LOW again.

To prevent the microcontroller being slowed down by repetitive interrupts, some interrupts are only allowed to occur once per watchdog period in Normal mode; see [Section 6.12.7](#).

If an interrupt is not read out within $t_{RSTN(INT)}$, a system reset is performed.

6.11 Temperature protection

The temperature of the SBC chip is monitored as long as the microcontroller voltage regulator V1 is active. To avoid an unexpected shutdown of the application by the SBC, temperature protection will not switch off any part of the SBC or activate a defined system stop of its own accord. If the temperature is too high, an OTI interrupt is generated (if enabled) and the corresponding status bit (TWS) is set. The microcontroller can then decide whether to switch off parts of the SBC to decrease the chip temperature.

6.12 SPI interface

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave and multi-master operation. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCS - SPI chip select; active LOW
- SCK - SPI clock; default level is LOW due to low-power concept
- SDI - SPI data input
- SDO - SPI data output; floating when pin SCS is HIGH

Bit sampling is performed on the falling clock edge and data is shifted on the rising clock edge; see [Figure 12](#).

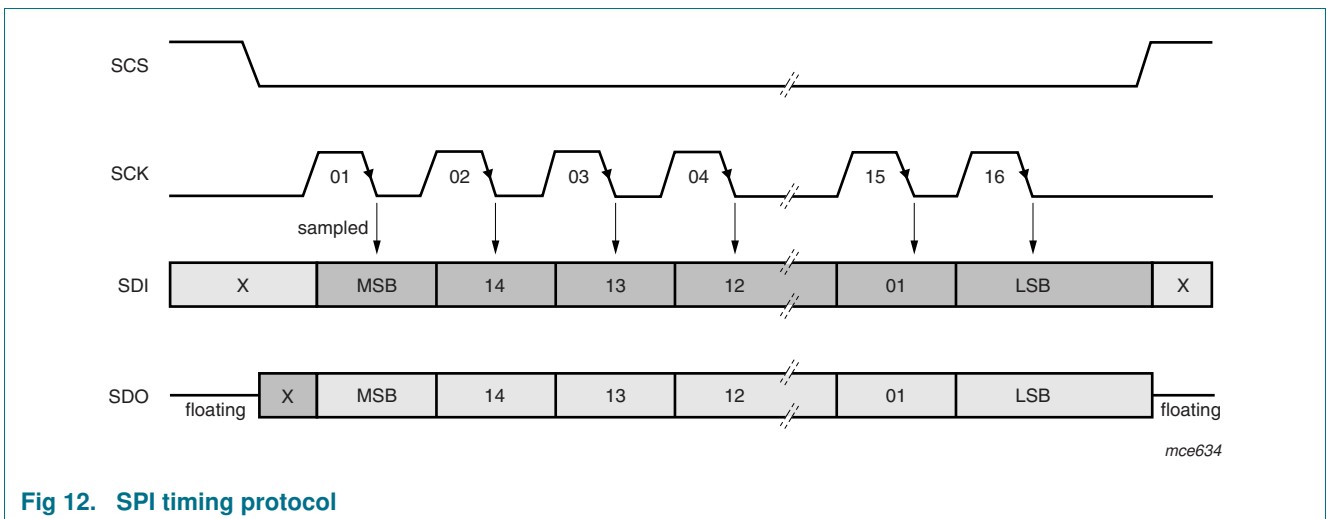


Fig 12. SPI timing protocol