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UJA1076

High-speed CAN core system basis chip

Rev. 02 — 27 May 2010 Product data sheet

1. General description

The UJA1076 core System Basis Chip (SBC) replaces the basic discrete components commonly found in Electronic Control Units (ECU) with a high-speed Controller Area Network (CAN).

The UJA1076 supports the networking applications used to control power and sensor peripherals by using a high-speed CAN as the main network interface.

The core SBC contains the following integrated devices:

- High-speed CAN transceiver, inter-operable and downward compatible with CAN transceiver TJA1042, and compatible with the ISO 11898-2 and ISO 11898-5 standards
- Advanced independent watchdog (UJA1076/xx/WD versions)
- 250 mA voltage regulator for supplying a microcontroller; extendable with external PNP transistor for increased current capability and dissipation distribution
- Separate voltage regulator for supplying the on-board CAN transceiver
- Serial Peripheral Interface (SPI) (full duplex)
- 2 local wake-up input ports
- Limp-home output port

In addition to the advantages gained from integrating these common ECU functions in a single package, the core SBC offers an intelligent combination of system-specific functions such as:

- Advanced low-power concept
- Safe and controlled system start-up behavior
- Detailed status reporting on system and sub-system levels

The UJA1076 is designed to be used in combination with a microcontroller that incorporates a CAN controller. The SBC ensures that the microcontroller always starts up in a controlled manner.

2. Features and benefits

2.1 General

- Contains a full set of CAN ECU functions:
  - CAN transceiver
  - Scalable 3.3 V or 5 V voltage regulator delivering up to 250 mA for a microcontroller and peripheral circuitry; an external PNP transistor can be connected for better heat distribution over the PCB
  - Separate voltage regulator for the CAN transceiver (5 V)
  - Watchdog with Window and Timeout modes and on-chip oscillator
  - Serial Peripheral Interface (SPI) for communicating with the microcontroller
  - ECU power management system
- Designed for automotive applications:
  - Excellent ElectroMagnetic Compatibility (EMC) performance
  - ±8 kV ElectroStatic Discharge (ESD) protection Human Body Model (HBM) on the CAN bus pins and the wake pins
  - ±6 kV ElectroStatic Discharge (ESD) protection IEC 61000-4-2 on the CAN bus pins and the wake pins
  - ±58 V short-circuit proof CAN bus pins
  - Battery and CAN bus pins are protected against transients in accordance with ISO 7637-3
- Supports remote flash programming via the CAN bus
- Small 6.1 mm × 11 mm HTSSOP32 package with low thermal resistance
- Pb-free; RoHS and dark green compliant

2.2 CAN transceiver

- ISO 11898-2 and ISO 11898-5 compliant high-speed CAN transceiver
- Dedicated low dropout voltage regulator for the CAN bus:
  - Independent of the microcontroller supply
  - Significantly improves EMC performance
- Bus connections are truly floating when power is off
- SPLIT output pin for stabilizing the recessive bus level

2.3 Power management

- Wake-up via CAN or local wake pins with wake-up source detection
- 2 wake pins:
  - WAKE1 and WAKE2 inputs can be switched off to reduce current flow
  - Output signal (WBIAS) to bias the wake pins, selectable sampling time of 16 ms or 64 ms
- Standby mode with very low standby current and full wake-up capability; V1 active to maintain supply to the microcontroller
- Sleep mode with very low sleep current and full wake-up capability

2.4 Control and Diagnostic features

- Safe and predictable behavior under all conditions
- Programmable watchdog with independent clock source:
  - Window, Timeout (with optional cyclic wake-up) and Off modes supported (with automatic re-enable in the event of an interrupt)
- 16-bit Serial Peripheral Interface (SPI) for configuration, control and diagnosis
- Global enable output for controlling safety-critical hardware
- Limp home output (LIMP) for activating application-specific 'limp home' hardware in the event of a serious system malfunction
- Overtemperature shutdown
- Interrupt output pin; interrupts can be individually configured to signal V1/V2 undervoltage, CAN/local wake-up and cyclic and power-on interrupt events
- Bidirectional reset pin with variable power-on reset length to support a variety of microcontrollers
- Software-initiated system reset

2.5 Voltage regulators

- Main voltage regulator V1:
  - Scalable voltage regulator for the microcontroller, its peripherals and additional external transceivers
  - ±2 % accuracy
  - 3.3 V and 5 V versions available
  - Delivers up to 250 mA and can be combined with an external PNP transistor for better heat distribution over the PCB
  - Selectable current threshold at which the external PNP transistor starts to deliver current
  - Undervoltage warning at 90 % of nominal output voltage and undervoltage reset at 90 % or 70 % of nominal output voltage
  - Can operate at V_{BAT} voltages down to 4.5 V (e.g. during cranking), in accordance with ISO7637 pulse 4/4b and ISO16750-2
  - Stable output under all conditions
- Voltage regulator V2 for CAN transceiver:
  - Dedicated voltage regulator for on-chip high-speed CAN transceiver
  - Undervoltage warning at 90 % of nominal output voltage
  - Can be switched off; CAN transceiver can be supplied by V1 or by an external voltage regulator
  - Can operate at V_{BAT} voltages down to 5.5 V (e.g. during cranking) in accordance with ISO7637, pulse 4
  - Stable output under all conditions

3. Ordering information

Table 1. Ordering information

Type number[1]	Package		
	Name	Description	Version
UJA1076TW/5V0/WD	HTSSOP32	plastic thermal enhanced thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad	SOT549-1
UJA1076TW/3V3/WD			
UJA1076TW/5V0			
UJA1076TW/3V3			

[1] UJA1076TW/5V0xx versions contain a 5 V regulator (V1); UJA1076TW/3V3xx versions contain a 3.3 V regulator (V1); WD versions contain a watchdog.

4. Block diagram

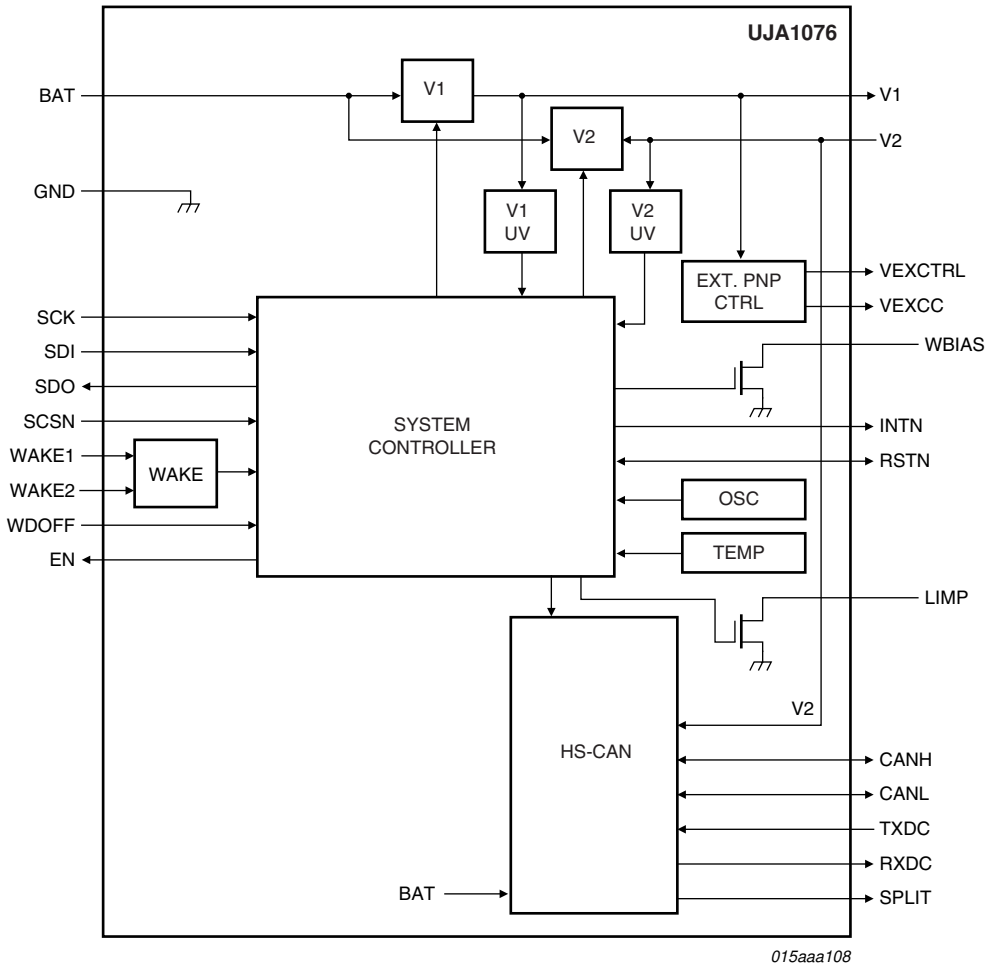

Fig 1. Block diagram

5. Pinning information

5.1 Pinning

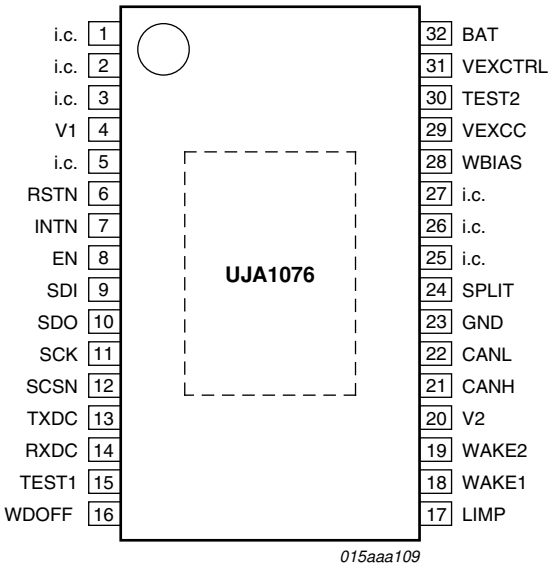

Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
i.c.	1	internally connected; should be left floating
i.c.	2	internally connected; should be left floating
i.c.	3	internally connected; should be left floating
V1	4	voltage regulator output for the microcontroller (5 V or 3.3 V depending on SBC version)
i.c.	5	internally connected; should be left floating
RSTN	6	reset input/output to and from the microcontroller
INTN	7	interrupt output to the microcontroller
EN	8	enable output
SDI	9	SPI data input
SDO	10	SPI data output
SCK	11	SPI clock input
SCSN	12	SPI chip select input
TXDC	13	CAN transmit data input
RXDC	14	CAN receive data output
TEST1	15	test pin; pin should be connected to ground
WDOFF	16	WDOFF pin for deactivating the watchdog
LIMP	17	limp home output

Table 2. Pin description *...continued*

Symbol	Pin	Description
WAKE1	18	local wake-up input 1
WAKE2	19	local wake-up input 2
V2	20	5 V voltage regulator output for CAN
CANH	21	CANH bus line
CANL	22	CANL bus line
GND	23	ground
SPLIT	24	CAN bus common mode stabilization output
i.c.	25	internally connected; should be left floating
i.c.	26	internally connected; should be left floating
i.c.	27	internally connected; should be left floating
WBIAS	28	control pin for external wake biasing transistor
VEXCC	29	current measurement for external PNP transistor; this pin is connected to the collector of the external PNP transistor
TEST2	30	test pin; pin should be connected to ground
VEXCTRL	31	control pin of the external PNP transistor; this pin is connected to the base of the external PNP transistor
BAT	32	battery supply for the SBC

The exposed die pad at the bottom of the package allows for better heat dissipation from the SBC via the printed circuit board. The exposed die pad is not connected to any active part of the IC and can be left floating, or can be connected to GND.

6. Functional description

The UJA1076 combines the functionality of a high-speed CAN transceiver, two voltage regulators and a watchdog (UJA1076/xx/WD versions) in a single, dedicated chip. It handles the power-up and power-down functionality of the ECU and ensures advanced system reliability. The SBC offers wake-up by bus activity, by cyclic wake-up and by the activation of external switches. Additionally, it provides a periodic control signal for pulsed testing of wake-up switches, allowing low-current operation even when the wake-up switches are closed in Standby mode.

All transceivers are optimized to be highly flexible with regard to bus topologies. In particular, the high-speed CAN transceiver is optimized to reduce ringing (bus reflections).

V1, the main voltage regulator, is designed to power the ECU's microcontroller, its peripherals and additional external transceivers. An external PNP transistor can be added to improve heat distribution. V2 supplies the integrated high-speed CAN transceiver. The watchdog is clocked directly by the on-chip oscillator and can be operated in Window, Timeout and Off modes.

6.1 System Controller

6.1.1 Introduction

The system controller manages register configuration and controls the internal functions of the SBC. Detailed device status information is collected and presented to the microcontroller. The system controller also provides the reset and interrupt signals.

The system controller is a state machine. The SBC operating modes, and how transitions between modes are triggered, are illustrated in Figure 3. These modes are discussed in more detail in the following sections.

6.1.2 Off mode

The SBC switches to Off mode from all other modes if the battery supply drops below the power-off detection threshold ($V_{th(det)poff}$). In Off mode, the voltage regulators are disabled and the bus systems are in a high-resistive state. The CAN bus pins are floating in this mode.

As soon as the battery supply rises above the power-on detection threshold ($V_{th(det)pon}$), the SBC goes to Standby mode, and a system reset is executed (reset pulse width of $t_{w(rst)}$, long or short; see Section 6.5.1 and Table 11).

6.1.3 Standby mode

The SBC will enter Standby mode:

- From Off mode if V_{BAT} rises above the power-on detection threshold ($V_{th(det)pon}$)
- From Sleep mode on the occurrence of a CAN or local wake-up event
- From Overtemp mode if the chip temperature drops below the overtemperature protection release threshold, $T_{th(rel)otp}$
- From Normal mode if bit MC is set to 00 or a system reset is performed (see Section 6.5)

In Standby mode, V1 is switched on. The CAN transceiver will either be in a low-power state (Lowpower mode; STBCC = 1; see Table 6) with bus wake-up detection enabled or completely switched off (Off mode; STBCC = 0) - see Section 6.7.1. The watchdog can be running in Timeout mode or Off mode, depending on the state of the WDOFF pin and the setting of the watchdog mode control bit (WMC) in the WD_and_Status register (Table 4).

The SBC will exit Standby mode if:

- Normal mode is selected by setting bits MC to 10 (V2 disabled) or 11 (V2 enabled)
- Sleep mode is selected by setting bits MC to 01
- The chip temperature rises above the OTP activation threshold, $T_{th(act)otp}$, causing the SBC to enter Overtemp mode

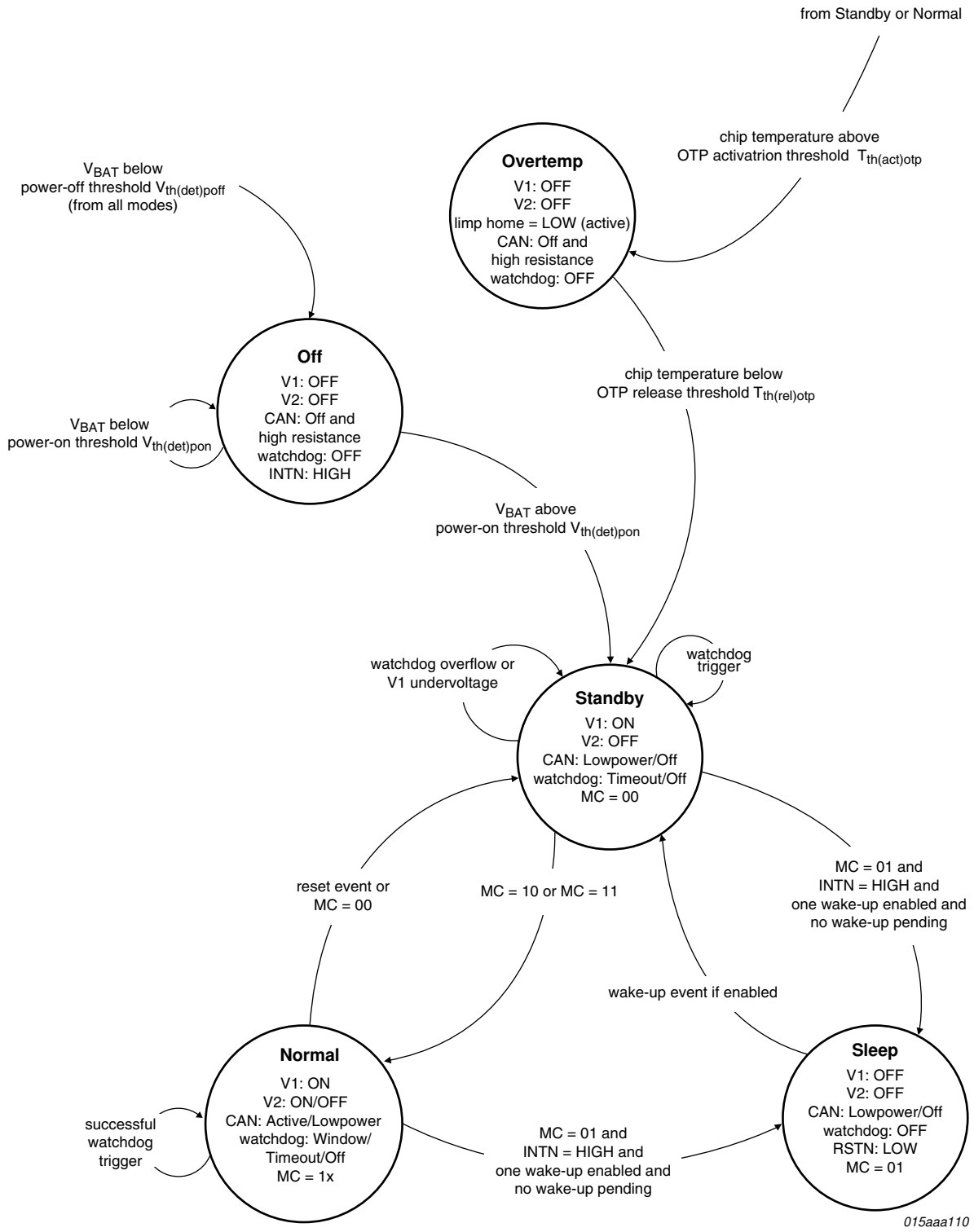

Fig 3. UJA1076 system controller

6.1.4 Normal mode

Normal mode is selected from Standby mode by setting bits MC in the Mode_Control register (Table 5) to 10 (V2 disabled) or 11 (V2 enabled).

In Normal mode, the CAN physical layer will be enabled (Active mode; STBCC = 0; see Table 6) or in a low-power state (Lowpower mode; STBCC = 1) with bus wake-up detection active.

The SBC will exit Normal mode if:

- Standby mode is selected by setting bits MC to 00
- Sleep mode is selected by setting bits MC to 01
- A system reset is generated (see Section 6.1.3; the SBC will enter Standby mode)
- The chip temperature rises above the OTP activation threshold, $T_{th(act)otp}$, causing the SBC to switch to Overtemp mode

6.1.5 Sleep mode

Sleep mode is selected from Standby mode or Normal mode by setting bits MC in the Mode_Control register (Table 5) to 01. The SBC will enter Sleep mode providing there are no pending interrupts (INTN = HIGH) or wake-up events and at least one wake-up source is enabled (CAN or WAKE). Any attempt to enter Sleep mode while one of these conditions has not been satisfied will result in a short reset (3.6 ms minimum pulse width; see Section 6.5.1 and Table 11).

In Sleep mode, V1 and V2 are off and the CAN transceiver will be switched off (Off mode; STBCC = 0; see Table 6) or in a low-power state (Lowpower mode; STBCC = 1) with bus wake-up detection active - see Section 6.7.1). The watchdog is off and the reset pin is LOW.

A CAN or local wake-up event will cause the SBC to switch from Sleep mode to Standby mode, generating a (short or long; see Section 6.5.1) system reset. The value of the mode control bits (MC) will be changed to 00 and V1 will be enabled.

6.1.6 Overtemp mode

The SBC will enter Overtemp mode from Normal mode or Standby mode when the chip temperature exceeds the overtemperature protection activation threshold, $T_{th(act)otp}$,

In Overtemp mode, the voltage regulators are switched off and the bus system is in a high-resistive state. When the SBC enters Overtemp mode, the RSTN pin is driven LOW and the limp home control bit, LHC, is set so that the LIMP pin is driven LOW.

The chip temperature must drop a hysteresis level below the overtemperature shutdown threshold before the SBC can exit Overtemp mode. After leaving Overtemp mode the SBC enters Standby mode and a system reset is generated (reset pulse width of $t_{w(rst)}$, long or short; see Section 6.5.1 and Table 11).

6.2 SPI

6.2.1 Introduction

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN: SPI chip select; active LOW
- SCK: SPI clock; default level is LOW due to low-power concept
- SDI: SPI data input
- SDO: SPI data output; floating when pin SCSN is HIGH

Bit sampling is performed on the falling clock edge and data is shifted on the rising clock edge (see Figure 4).

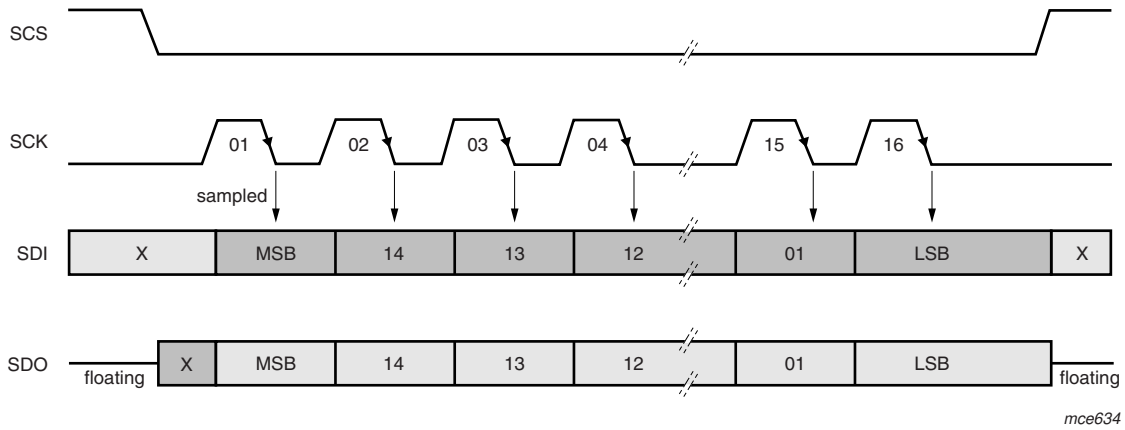

Fig 4. SPI timing protocol

6.2.2 Register map

The first three bits (A2, A1 and A0) of the message header define the register address. The fourth bit (RO) defines the selected register as read/write or read only.

Table 3. Register map

Address bits 15, 14 and 13	Write access bit 12 = 0	Read/Write access bits 11... 0
000	0 = read/write, 1 = read only	WD_and_Status register
001	0 = read/write, 1 = read only	Mode_Control register
010	0 = read/write, 1 = read only	Int_Control register
011	0 = read/write, 1 = read only	Int_Status register

6.2.3 WD_and_Status register

Table 4. WD_and_Status register

Bit	Symbol	Access	Power-on default	Description
15:13	A2, A1, A0	R	000	register address
12	RO	R/W	0	access status
				0: register set to read/write
				1: register set to read only
11	WMC	R/W	0	watchdog mode control
				0: Normal mode: watchdog in Window mode; Standby mode: watchdog in Timeout mode
				1: Normal mode: watchdog in Timeout mode; Standby mode: watchdog in Off mode
10:8	NWP[1]	R/W	100	nominal watchdog period
				000: 8 ms
				001: 16 ms
				010: 32 ms
				011: 64 ms
				100: 128 ms
				101: 256 ms
				110: 1024 ms
				111: 4096 ms
7	WOS/SWR	R/W	-	watchdog off status/software reset
				0: WDOFF pin LOW; watchdog mode determined by bit WMC
				1: watchdog disabled due to HIGH level on pin WDOFF; results in software reset
6	V1S	R	-	V1 status
				0: V1 output voltage above 90 % undervoltage recovery threshold (V_{uvr}; see Table 10)
				1: V1 output voltage below 90 % undervoltage detection threshold (V_{uvd}; see Table 10)
5	V2S	R	-	V2 status
				0: V2 output voltage above undervoltage release threshold (V_{uvr}; see Table 10)
				1: V2 output voltage below undervoltage detection threshold (V_{uvd}; see Table 10)
4	WLS1	R	-	wake-up 1 status
				0: WAKE1 input voltage below switching threshold ($V_{th(sw)}$)
				1: WAKE1 input voltage above switching threshold ($V_{th(sw)}$)
3	WLS2	R	-	wake-up 2 status
				0: WAKE2 input voltage below switching threshold ($V_{th(sw)}$)
				1: WAKE2 input voltage above switching threshold ($V_{th(sw)}$)
2:0	reserved	R	000	

[1] Bit NWP is set to it's default value (100) after a reset.

6.2.4 Mode_Control register

Table 5. Mode_Control register

Bit	Symbol	Access	Power-on default	Description
15:13	A2, A1, A0	R	001	register address
12	RO	R/W	0	access status
				0: register set to read/write
				1: register set to read only
11:10	MC	R/W	00	mode control
				00: Standby mode
				01: Sleep mode
				10: Normal mode; V2 off
				11: Normal mode; V2 on
9	LHWC[1]	R/W	1	limp home warning control
				0: no limp home warning
				1: limp home warning is set; next reset will activate LIMP output
8	LHC[2]	R/W	0	limp home control
				0: LIMP pin set floating
				1: LIMP pin driven LOW
7	ENC	R/W	0	enable control
				0: EN pin driven LOW
				1: EN pin driven HIGH in Normal mode
6	reserved	R	0	
5	WBC	R/W	0	wake bias control
				0: WBIAS floating if WSEn = 0; 16 ms sampling if WSEn = 1
				1: WBIAS on if WSEn = 0; 64 ms sampling if WSEn = 1
4	PDC	R/W	0	power distribution control
				0: V1 threshold current for activating the external PNP transistor; load current rising; $I_{th(act)PNP}$ = 85 mA; V1 threshold current for deactivating the external PNP transistor; load current falling; $I_{th(deact)PNP}$ = 50 mA; see Figure 7
				1: V1 threshold current for activating the external PNP transistor; load current rising; $I_{th(act)PNP}$ = 50 mA; V1 threshold current for deactivating the external PNP transistor; load current falling; $I_{th(deact)PNP}$ = 15 mA; see Figure 7
3:0	reserved	R	0000	

[1] Bit LHWC is set to 1 after a reset.

[2] Bit LHC is set to 1 after a reset, if LHWC was set to 1 prior to the reset.

6.2.5 Int_Control register

Table 6. Int_Control register

Bit	Symbol	Access	Power-on default	Description
15:13	A2, A1, A0	R	010	register address
12	RO	R/W	0	access status
				0: register set to read/write
				1: register set to read only
11	V1UIE	R/W	0	V1 undervoltage interrupt enable
				0: V1 undervoltage warning interrupts cannot be requested
				1: V1 undervoltage warning interrupts can be requested
10	V2UIE	R/W	0	V2 undervoltage interrupt enable
				0: V2 undervoltage warning interrupts cannot be requested
				1: V2 undervoltage warning interrupts can be requested
9:8	reserved	R	00	
7:6	WIC1	R/W	00	wake-up interrupt 1 control
				00: wake-up interrupt 1 disabled
				01: wake-up interrupt 1 on rising edge
				10: wake-up interrupt 1 on falling edge
				11: wake-up interrupt 1 on both edges
5:4	WIC2	R/W	00	wake-up interrupt 2 control
				00: wake-up interrupt 2 disabled
				01: wake-up interrupt 2 on rising edge
				10: wake-up interrupt 2 on falling edge
				11: wake-up interrupt 2 on both edges
3	STBCC	R/W	0	CAN standby control
				0: When the SBC is in Normal mode (MC = 1x): CAN is in Active mode. The wake-up flag (visible on RXDC) is cleared regardless of V2 output voltage. When the SBC is in Standby/Sleep mode (MC = 0x): CAN is in Off mode. Bus wake-up detection is disabled. CAN wake-up interrupts cannot be requested.
				1: CAN is in Lowpower mode with bus wake-up detection enabled, regardless of the SBC mode (MC = xx). CAN wake-up interrupts can be requested.
2	RTHC	R/W	0	reset threshold control
				0: The reset threshold is set to the 90 % V1 undervoltage detection voltage (V_{uvd}; see Table 10)
				1: The reset threshold is set to the 70 % V1 undervoltage detection voltage (V_{uvd}; see Table 10)
1	WSE1	R/W	0	WAKE1 sample enable
				0: sampling continuously
				1: sampling of WAKE1 is synchronized with WBIAS (sample rate controlled by WBC)

Table 6. Int_Control register

Bit	Symbol	Access	Power-on default	Description
0	WSE2	R/W	0	WAKE2 sample enable
				0: sampling continuously
				1: sampling of WAKE1 is synchronized with WBIAS (sample rate controlled by WBC)

6.2.6 Int_Status register

Table 7. Int_Status register[1]

Bit	Symbol	Access	Power-on default	Description
15:13	A2, A1, A0	R	011	register address
12	RO	R/W	0	access status
				0: register set to read/write
				1: register set to read only
11	V1UI	R/W	0	V1 undervoltage interrupts
				0: no V1 undervoltage warning interrupt pending
				1: V1 undervoltage warning interrupt pending
10	V2UI	R/W	0	V2 undervoltage interrupts
				0: no V2 undervoltage warning interrupt pending
				1: V2 undervoltage warning interrupt pending
9:8	reserved	R	00	
7	CI	R/W	0	cyclic interrupt
				0: no cyclic interrupt pending
				1: cyclic interrupt pending
6	WI1	R/W	0	wake-up interrupt 1
				0: no wake-up interrupt 1 pending
				1: wake-up interrupt 1 pending
5	POSI	R/W	1	power-on status interrupt
				0: no power-on interrupt pending
				1: power-on interrupt pending
4	WI2	R/W	0	wake-up interrupt 2
				0: no wake-up interrupt 2 pending
				1: wake-up interrupt 2 pending
3	CWI	R/W	0	CAN wake-up interrupt
				0: no CAN wake-up interrupt pending
				1: CAN wake-up interrupt pending
2:0	reserved	R	000	

[1] An interrupt can be cleared by writing 1 to the relevant bit in the Int_Status register.

6.3 On-chip oscillator

The on-chip oscillator provides the timing reference for the on-chip watchdog and the internal timers. The on-chip oscillator is supplied by an internal supply that is connected to V_{BAT} and is independent of V1/V2.

6.4 Watchdog (UJA1076/xx/WD versions)

Three watchdog modes are supported: Window, Timeout and Off. The watchdog period is programmed via the NWP control bits in the WD_and_Status register (see Table 4). The default watchdog period is 128 ms.

A watchdog trigger event is any write access to the WD_and_Status register. When the watchdog is triggered, the watchdog timer is reset.

In watchdog Window mode, a watchdog trigger event within a closed watchdog window (i.e. the first half of the window before $t_{trig(wd)1}$) will generate an SBC reset. If the watchdog is triggered before the watchdog timer overflows in Timeout or Window mode, or within the open watchdog window (after $t_{trig(wd)1}$ but before $t_{trig(wd)2}$), the timer restarts immediately.

The following watchdog events result in an immediate system reset:

- the watchdog overflows in Window mode
- the watchdog is triggered in the first half of the watchdog period in Window mode
- the watchdog overflows in Timeout mode while a cyclic interrupt (CI) is pending
- the state of the WDOFF pin changes in Normal mode or Standby mode
- the watchdog mode control bit (WMC) changes state in Normal mode

After a watchdog reset (short reset; see Section 6.5.1 and Table 11), the default watchdog period is selected (NWP = 100). The watchdog can be switched off completely by forcing pin WDOFF HIGH. The watchdog can also be switched off by setting bit WMC to 1 in Standby mode. If the watchdog was turned off by setting WMC, any pending interrupt will re-enable it.

Note that the state of bit WMC cannot be changed in Standby mode if an interrupt is pending. Any attempt to change WMC when an interrupt is pending will be ignored.

6.4.1 Watchdog Window behavior

The watchdog runs continuously in Window mode.

If the watchdog overflows, or is triggered in the first half of the watchdog period (less than $t_{trig(wd)1}$ after the start of the watchdog period), a system reset will be performed. Watchdog overflow occurs if the watchdog is not triggered within $t_{trig(wd)2}$ after the start of watchdog period.

If the watchdog is triggered in the second half of the watchdog period (at least $t_{trig(wd)1}$, but not more than $t_{trig(wd)2}$, after the start of the watchdog period), the watchdog will be reset.

The watchdog is in Window mode when pin WDOFF is LOW, the SBC is in Normal mode and the watchdog mode control bit (WMC) is set to 0.

6.4.2 Watchdog Timeout behavior

The watchdog runs continuously in Timeout mode. It can be reset at any time by a watchdog trigger. If the watchdog overflows, the cyclic interrupt (CI) bit is set. If a CI is already pending, a system reset is performed.

The watchdog is in Timeout mode when pin WDOFF is LOW and:

- the SBC is in Standby mode and bit WMC = 0 or
- the SBC is in Normal mode and bit WMC = 1

6.4.3 Watchdog Off behavior

The watchdog is disabled in this state.

The watchdog is in Off mode when:

- the SBC is in Off, Overtemp or Sleep modes
- the SBC is in Standby mode and bit WMC = 1
- the SBC is in any mode and the WDOFF pin is HIGH

6.5 System reset

The following events will cause the SBC to perform a system reset:

- V1 undervoltage (reset pulse length selected via external pull-up resistor on RSTN pin)
- An external reset (RSTN forced LOW)
- Watchdog overflow (Window mode)
- Watchdog overflow in Timeout mode with cyclic interrupt (CI) pending
- Watchdog triggered too early in Window mode
- WMC value changed in Normal mode
- WDOFF pin state changed
- SBC goes to Sleep mode (MC set to 01; see Table 5) while INTN is driven LOW
- SBC goes to Sleep mode (MC set to 01; see Table 5) while STBCC = WIC1 = WIC2 = 0
- SBC goes to Sleep mode (MC set to 01; see Table 5) while wake-up pending
- Software reset (SWR = 1)
- SBC leaves Overtemp mode (reset pulse length selected via external pull-up resistor on RSTN pin)

A watchdog overflow in Timeout mode requests a cyclic interrupt (CI), if a CI is not already pending.

The UJA1076 provides three signals for dealing with reset events:

- RSTN input/output for performing a global ECU system reset or forcing an external reset
- EN pin, a fail-safe global enable output
- LIMP pin, a fail-safe limp home output

6.5.1 RSTN pin

A system reset is triggered if the bidirectional RSTN pin is forced LOW for at least t_{fltr} by the microcontroller (external reset). A reset pulse is output on RSTN by the SBC when a system reset is triggered internally.

The reset pulse width ($t_{w(rst)}$) is selectable (short or long) if the system reset was generated by a V1 undervoltage event (see Section 6.6.2) or by the SBC leaving Off ($V_{BAT} > V_{th(det)pon}$) or Overtemp (temperature < $T_{th(rel)otp}$) modes. A short reset pulse is selected by connecting a 900 Ω ±10 % resistor between pins RSTN and V1. If a resistor is not connected, the reset pulse will be long (see Table 11).

In all other cases (e.g. watchdog-related reset events) the reset pulse length will be short.

6.5.2 EN output

The EN pin can be used to control external hardware, such as power components, or as a general-purpose output when the system is running properly.

In Normal and Standby modes, the microcontroller can set the EN control bit (bit ENC in the Mode_Control register; see Table 5) via the SPI interface. Pin EN will be HIGH when ENC = 1 and MC = 10 or 11. A reset event will cause pin EN to go LOW. EN pin behavior is illustrated in Figure 5.

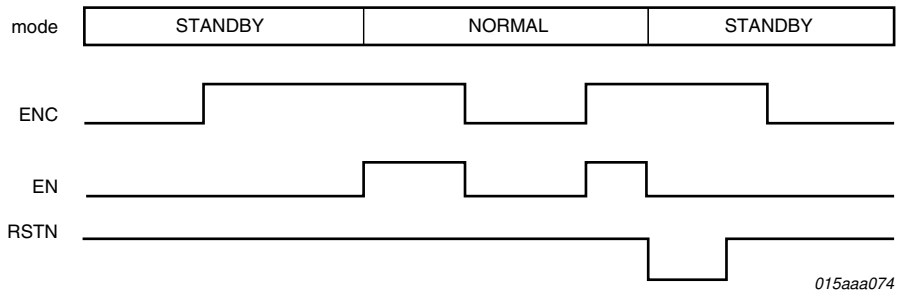

Fig 5. Behavior of EN pin

6.5.3 LIMP output

The LIMP pin can be used to enable the so called ‘limp home’ hardware in the event of an ECU failure. Detectable failure conditions include SBC overtemperature events, loss of watchdog service, RSTN or V1 clamped LOW and user-initiated or external reset events.

The LIMP pin is a battery-related, active-LOW, open-drain output.

A system reset will cause the limp home warning control bit (bit LHWC in the Mode_Control register; see Table 5) to be set. If LHWC is already set when the system reset is generated, bit LHC will be set which will force the LIMP pin LOW. The application should clear LHWC after each reset event to ensure the LIMP output is not activated during normal operation.

In Overtemp mode, bit LHC is always set and, consequently, the LIMP output is always active. If the application manages to recover from the event that activated the LIMP output, LHC can be cleared to deactivate the LIMP output.

6.6 Power supplies

6.6.1 Battery pin (BAT)

The SBC contains a single supply pin, BAT. An external diode is needed in series to protect the device against negative voltages. The operating range is from 4.5 V to 28 V. The SBC can handle maximum voltages up to 40 V.

If the voltage on pin BAT falls below the power-off detection threshold ($V_{th(det)poff}$), the SBC immediately enters Off mode, which means that the voltage regulators and the internal logic are shut down. The SBC leaves Off mode for Standby mode as soon as the voltage rises above the power-on detection threshold, $V_{th(det)pon}$. The POSI bit in the Int_Status register is set to 1 when the SBC leaves Off mode.

6.6.2 Voltage regulator V1

Voltage regulator V1 is intended to supply the microcontroller, its periphery and additional transceivers. V1 is supplied by pin BAT and delivers up to 250 mA at 3.3 V or 5 V (depending on the UJA1076 version).

To prevent the device overheating at high ambient temperatures or high average currents, an external PNP transistor can be connected as illustrated in Figure 6. In this configuration, the power dissipation is distributed between the SBC and the PNP transistor. Bit PDC in the Mode_Control register (Table 5) is used to regulate how the power dissipation is distributed – if PDC = 0, the PNP transistor will be activated when the load current reaches 85 mA (50 mA if PDC = 1) at T_{vj} = 150 °C. V1 will continue to deliver 85 mA while the transistor delivers the additional load current (see Figure 7 and Figure 8).

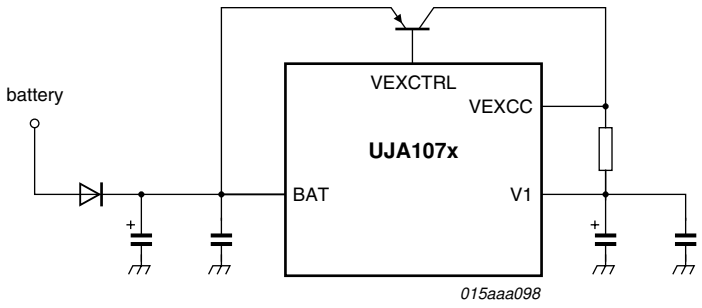

Fig 6. External PNP transistor control circuit

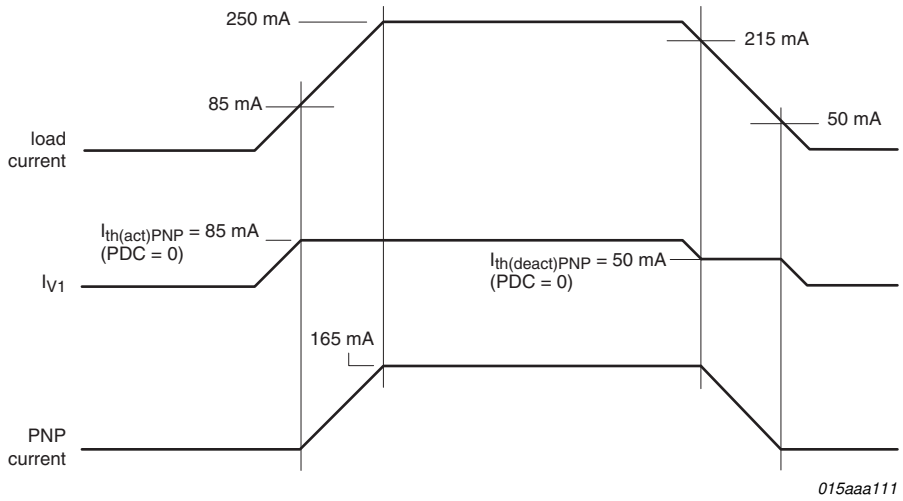

Fig 7. V1 and PNP currents at a slow ramping load current of 250 mA (PDC = 0)

Figure 7 illustrates how V1 and the PNP transistor combine to supply a slow ramping load current of 250 mA with PDC = 0. Any additional load current requirement will be supplied by the PNP transistor, up to its current limit. If the load current continues to rise, I_{V1} will increase above the selected PDC threshold (to a maximum of 250 mA).

For a fast ramping load current, V1 will deliver the required load current (to a maximum of 250 mA) until the PNP transistor has switched on. Once the transistor has been activated, V1 will deliver 85 mA (PDC = 0) with the transistor contributing the balance of the load current (see Figure 8).

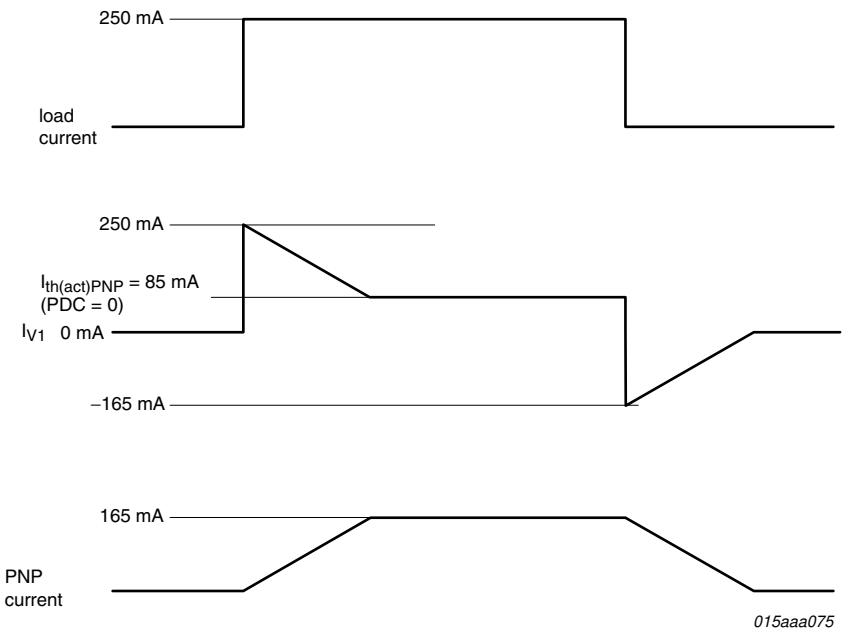

Fig 8. V1 and PNP currents at a fast ramping load current of 250 mA (PDC = 0)

For short-circuit protection, a resistor needs to be connected between pins V1 and VEXCC to allow the current to be monitored. This resistor limits the current delivered by the external transistor. If the voltage difference between pins VEXCC and V1 reaches $V_{th(act)Ilim}$, the PNP current limiting activation threshold voltage, the transistor current will not increase further.

The thermal performance of the transistor needs to be considered when calculating the value of this resistor. A 3.3 Ω resistor was used with the BCP52-16 (NXP Semiconductors) employed during testing. Note that the selection of the transistor is not critical. In general, any PNP transistor with a current amplification factor (β) of between 60 and 500 can be used.

If an external PNP transistor is not used, pin VEXCC must be connected to V1 while pin VEXCTRL can be left open.

One advantage of this scalable voltage regulator concept is that there are no PCB layout restrictions when using the external PNP. The distance between the UJA1076 and the external PNP doesn't affect the stability of the regulator loop because the loop is realized within the UJA1076. Therefore, it is recommended that the distance between the UJA1076 and PNP transistor be maximized for optimal thermal distribution.

The output voltage on V1 is monitored continuously and a system reset signal is generated if an undervoltage event occurs. A system reset is generated if the voltage on V1 falls below the undervoltage detection voltage (V_{uvd}; see Table 10). The reset threshold (90 % or 70 % of the nominal value) is set via the Reset Threshold Control bit (RTHC) in the Int_Control register (Table 6). In addition, an undervoltage warning (a V1UI interrupt) will be generated at 90 % of the nominal output voltage. The status of V1 can be read via bit V1S in the WD_and_Status register (Table 4).

6.6.3 Voltage regulator V2

Voltage regulator V2 is reserved for the high-speed CAN transceiver, providing a 5 V supply.

V2 can be activated and deactivated via the MC bits in the Mode_Control register (Table 5). An undervoltage warning (a V2UI interrupt) is generated when the output voltage drops below 90 % of its nominal value. The status of V2 can be read via bit V2S in the WD_and_Status register (Table 4) in Normal mode (V2S = 1 in all other modes).

V2 can be deactivated (MC = 10) to allow the internal CAN transceiver to be supplied from an external source or from V1. The alternative voltage source must be connected to pin V2. All internal functions (e.g. undervoltage protection) will work normally.

6.7 CAN transceiver

The analog section of the UJA1076 CAN transceiver corresponds to that integrated into the TJA1042/TJA1043. The transceiver is designed for high-speed (up to 1 Mbit/s) CAN applications in the automotive industry, providing differential transmit and receive capability to a CAN protocol controller.

6.7.1 CAN operating modes

6.7.1.1 Active mode

The CAN transceiver is in Active mode when:

- the SBC is in Normal mode (MC = 10 or 11)
- the transceiver is enabled (bit STBCC = 0; see Table 6)

and

- V2 is enabled and its output voltage is above its undervoltage threshold, V_{uvd} or
- V2 is disabled but an external voltage source, or V1, connected to pin V2 is above its undervoltage threshold (see Section 6.6.3)

In CAN Active mode, the transceiver can transmit and receive data via the CANH and CANL pins. The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXDC. The transmitter converts digital data generated by a CAN controller, and input on pin TXDC, to signals suitable for transmission over the bus lines.

6.7.1.2 Lowpower/Off modes

The CAN transceiver will be in Lowpower mode with bus wake-up detection enabled if bit STBCC = 1 (see Table 6). The CAN transceiver can be woken up remotely via pins CANH and CANL in Lowpower mode.

When the SBC is in Standby mode or Sleep mode (MC = 00 or 01), the CAN transceiver will be in Off mode if bit STBCC = 0. The CAN transceiver is powered down completely in Off mode to minimize quiescent current consumption.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI.

A recessive-dominant-recessive-dominant sequence must occur on the CAN bus within the wake-up timeout time ($t_{to(wake)}$) to pass the wake-up filter and trigger a wake-up event (see Figure 9; note that additional pulses may occur between the recessive/dominant phases). The minimum recessive/dominant bus times for CAN transceiver wake-up ($t_{wake(busrec)min}$ and $t_{wake(busdom)min}$) must be satisfied (see Table 11).

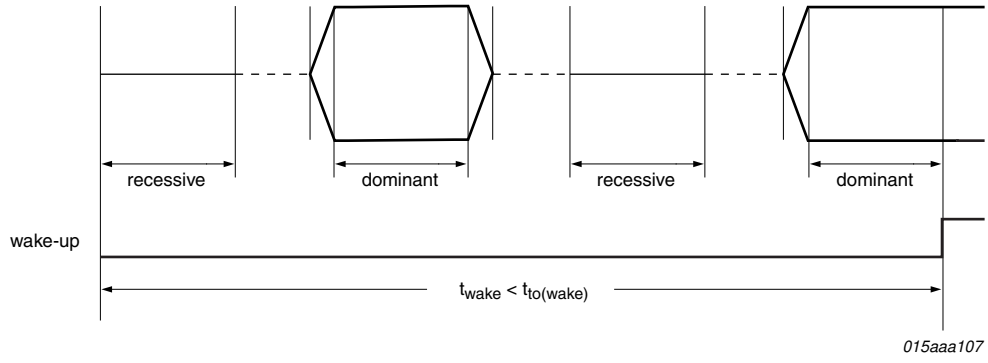

Fig 9. CAN wake-up timing diagram

6.7.2 Split circuit

Pin SPLIT provides a DC stabilized voltage of $0.5V_{V2}$. It is activated in CAN Active mode only. Pin SPLIT is floating in CAN Lowpower and Off modes. The V_{SPLIT} circuit can be used to stabilize the recessive common-mode voltage by connecting pin SPLIT to the center tap of the split termination (see Figure 10).

A transceiver in the network that is not supplied and that generates a significant leakage current from the bus lines to ground, can result in a recessive bus voltage of $< 0.5V_{V2}$. In this event, the split circuit will stabilize the recessive voltage at $0.5V_{V2}$. So a start of transmission will not generate a step in the common-mode signal which would lead to poor ElectroMagnetic Emission (EME) performance.

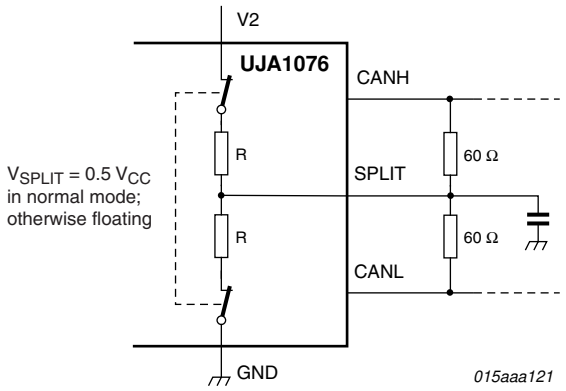

Fig 10. Stabilization circuitry and application using the SPLIT pin

6.7.3 Fail-safe features

6.7.3.1 TXDC dominant time-out function

A TXDC dominant time-out timer is started when pin TXDC is forced LOW. If the LOW state on pin TXDC persists for longer than the TXDC dominant time-out time ($t_{to(dom)TXDC}$), the transmitter will be disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXDC dominant time-out timer is reset when pin TXDC goes HIGH. The TXDC dominant time-out time also defines the minimum possible bit rate of 10 kbit/s.

6.7.3.2 Pull-up on TXDC pin

Pin TXDC has an internal pull-up towards V_{V1} to ensure a safe defined state in case the pin is left floating.

6.8 Local wake-up input

The SBC provides 2 local wake-up pins (WAKE1 and WAKE2). The edge sensitivity (falling, rising or both) of the wake-up pins can be configured independently via the WIC1 and WIC2 bits in the Int_Control register Table 6). These bits can also be used to disable wake-up via the wake-up pins. When wake-up is enabled, a valid wake-up event on either of these pins will cause a wake-up interrupt to be generated in Standby mode or Normal

mode. If the SBC is in Sleep mode when the wake-up event occurs, it will wake up and enter Standby mode. The status of the wake-up pins can be read via the wake-up level status bits (WLS1 and WLS2) in the WD_and_Status register (Table 4).

Note that bits WLS1 and WLS2 are only active when at least one of the wake up interrupts is enabled (WIC1 ≠ 00 or WIC2 ≠ 00).

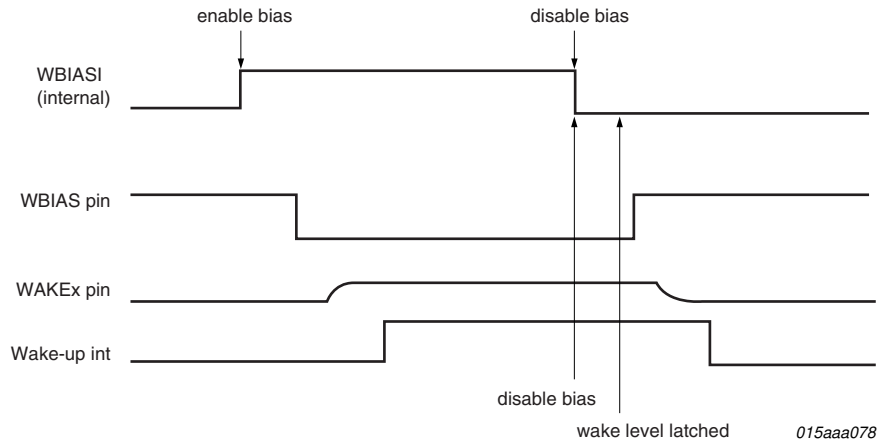

Fig 11. Wake-up pin sampling synchronized with WBIAS signal

The sampling of the wake-up pins can be synchronized with the WBIAS signal by setting bits WSE1 and WSE2 in the Int_Control register to 1 (if WSEx = 0, wake-up pins are sampled continuously). The sampling will be performed on the rising edge of WBIAS (see Figure 11). The sampling time, 16 ms or 64 ms, is selected via the Wake Bias Control bit (WBC) in the Mode_Control register.

Figure 12 shows typical circuit for implementing cyclic sampling of the wake-up inputs.

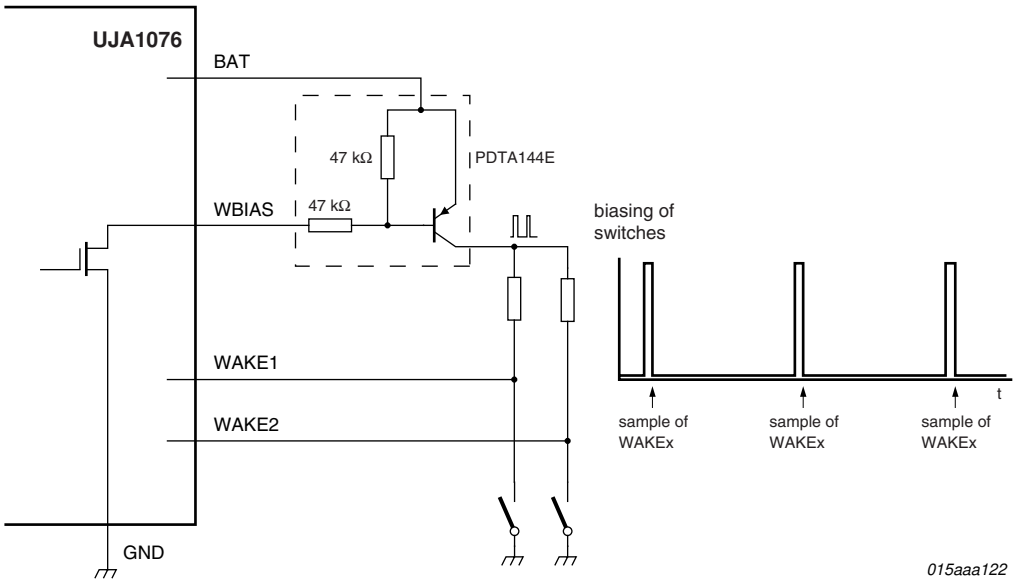

Fig 12. Typical application for cyclic sampling of wake-up signals

6.9 Interrupt output

Pin INTN is an active-LOW, open-drain interrupt output. It is driven LOW when at least one interrupt is pending. An interrupt can be cleared by writing 1 to the corresponding bit in the Int_Status register (Table 7). Clearing bit CWI in Standby mode only clears the interrupt status bit and not the pending wake-up. The pending wake-up is cleared on entering Normal mode and when the corresponding standby control bit (STBCC) is 0.

On devices that contain a watchdog, the Cyclic Interrupt (CI) is enabled when the watchdog switches to Timeout mode while the SBC is in Standby mode or Normal mode (provided WDOFF = LOW). A CI is generated if the watchdog overflows in Timeout mode.

The CI is provided to alert the microcontroller when the watchdog overflows in Timeout mode. The CI will wake up the microcontroller from a μC standby mode. After polling the Int_Status register, the microcontroller will be aware that the application is in cyclic wake up mode. It can then perform some checks on CAN before returning to the μC standby mode.

6.10 Temperature protection

The temperature of the SBC chip is monitored in Normal and Standby modes. If the temperature is too high, the SBC will go to Overtemp mode, where the RSTN pin is driven LOW and limp home is activated. In addition, the voltage regulators and the CAN transmitter are switched off (see also Section 6.1.6 “Overtemp mode”). When the temperature falls below the temperature shutdown threshold, the SBC will go to Standby mode. The temperature shutdown threshold is between 165 °C and 200 °C.

7. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_x	voltage on pin x	DC value				
		pins V1, V2 and INTN		−0.3	7	V
		pins TXDC, RXDC, EN, SDI, SDO, SCK, SCSN, RSTN and WDOFF		−0.3	V_{V1} + 0.3	V
		pin VEXCC		V_{V1} − 0.3	V_{V1} + 0.35	V
		pins WAKE1, WAKE2 and WBIAS; with respect to any other pin		−58	+58	V
		pin LIMP and BAT		−0.3	+40	V
		pin VEXCTRL		−0.3	V_{BAT} + 0.3	V
		pins CANH, CANL and SPLIT; with respect to any other pin		−58	+58	V
$I_{R(V1-BAT)}$	reverse current from pin V1 to pin BAT	$V_{V1} \leq 5$ V	[1]	-	250	mA
V_{trt}	transient voltage	on pins	[2]	−150	+100	V
		BAT: via reverse polarity diode/capacitor				
		CANL, CANH, SPLIT: coupling with two capacitors on the bus lines				
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2	[3]			
		pins BAT with capacitor, CANH and CANL; via a series resistor on pins SPLIT, WAKE1 and WAKE2	[4]	−6	+6	kV
		HBM	[5]			
		pins CANH, CANL, SPLIT, WAKE1 and WAKE2	[6]	−8	+8	kV
		pin BAT; referenced to ground		−4	+4	kV
		pin TEST2; referenced to pin BAT		−1.25	+2	kV
		pin TEST2; referenced to other reference pins		−2	+2	kV
		any other pin		−2	+2	kV
		MM	[7]			
		any pin		−300	+300	V
		CDM	[8]			
		corner pins		−750	+750	V
		any other pin		−500	+500	V
T_{vj}	virtual junction temperature		[9]	−40	+150	°C
T_{stg}	storage temperature			−55	+150	°C