Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

UJA1169L

Mini high-speed CAN companion system basis chip

Rev. 1 — 15 February 2016 **Product data sheet**

1. General description

The UJA1169L mini high-speed CAN companion System Basis Chip (SBC) belongs to the UJA1169 product series and can be used as a companion chip in applications where a second SBC is dedicated to the application microcontroller. It contains an ISO 11898-2:201x (upcoming merged ISO 11898-2/5/6) compliant HS-CAN transceiver and an integrated 5 V 250 mA scalable supply (V1) for additional transceivers and/or other loads. It also features a watchdog and a Serial Peripheral Interface (SPI). The UJA1169L companion SBC can be operated in very low-current Standby and Sleep modes with bus and local wake-up capability.

The UJA1169L is designed to be used in applications that require more than one transceiver or additional power supply resources. Using a standard device as the secondary SBC in an application can be problematic. The secondary SBC will have a different interface supply domain to the main SBC, creating a high risk of reverse supply currents. The UJA1169L resolves this issue by providing a dedicated VIO input pin that allows it to adapt to any other supply domain.

Incorporating the UJA1169L companion SBC in an application allows it to be easily scaled or extended by adding, for example, an additional 5 V power supply, CAN transceiver, off-board 5 V sensor supply or even a secondary independent watchdog function with independent LIMP output for special ASIL-related applications.

The UJA1169L comes in four variants. The UJA1169LTK and UJA1169LTK/F feature a second on-board 5 V regulator (V2) that supplies the internal CAN transceiver and can also be used to supply additional on-board hardware.

The UJA1169LTK/X and UJA1169LTK/X/F are equipped with a 5 V supply (VEXT) for off-board components. VEXT is short-circuit proof to the battery, ground and negative voltages. The integrated CAN transceiver is supplied internally via V1.

The UJA1169LTK/F and UJA1169LTK/X/F variants support ISO 11898-6:2013 and ISO 11898-2:201x compliant CAN partial networking with a selective wake-up function incorporating CAN FD-passive. CAN FD-passive is a feature that allows CAN FD bus traffic to be ignored in Sleep/Standby mode. CAN FD-passive partial networking is the perfect fit for networks that support both CAN FD and classic CAN communications. It allows normal CAN controllers that do not need to communicate CAN FD messages to remain in partial networking Sleep/Standby mode during CAN FD communication without generating bus errors.

The UJA1169L implements the standard CAN physical layer as defined in the current ISO11898 standard (-2:2003, -5:2007, -6:2013). Pending the release of the upcoming version of ISO11898-2:201x including CAN FD, additional timing parameters defining loop delay symmetry are included. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 2 Mbit/s.

A dedicated LIMP output pin is provided to flag system failures.

A number of configuration settings are stored in non-volatile memory. This arrangement makes it possible to configure the power-on and limp-home behavior of the UJA1169L to meet the requirements of different applications.

2. Features and benefits

2.1 General

- ISO 11898-2:201x (upcoming merged ISO 11898-2/5/6) compliant 1 Mbit/s high-speed CAN transceiver supporting CAN FD active communication up to 2 Mbit/s in the CAN FD data field (all four variants)
- Autonomous bus biasing according to ISO 11898-6:2013 and ISO 11898-2:201x
- Scalable 5 V 250 mA low-drop voltage regulator (V1) based on external PNP transistor concept for thermal scaling
- CAN-bus connections are truly floating when power to pin BAT is off
- No ‘false’ wake-ups due to CAN FD traffic (in variants supporting partial networking)

2.2 Designed for automotive applications

- ±8 kV ElectroStatic Discharge (ESD) protection, according to the Human Body Model (HBM) on the CAN-bus pins
- ±6 kV ESD protection according to IEC 61000-4-2 on pins BAT, WAKE, VEXT and the CAN-bus pins
- CAN-bus pins short-circuit proof to ±58 V
- Battery and CAN-bus pins protected against automotive transients according to ISO 7637-3
- Very low quiescent current in Standby and Sleep modes with full wake-up capability
- Leadless HVSON20 package (3.5 mm × 5.5 mm) with improved Automated Optical Inspection (AOI) capability and low thermal resistance
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.3 Low-drop voltage regulator (V1)

- 5 V nominal output; ±2 % accuracy
- 250 mA output current capability
- Thermal management via optional external PNP
- Current limiting above 250 mA
- V1 remains operational down to a battery voltage of 2 V
- V1 undervoltage detection with selectable detection thresholds of 60 %, 70 %, 80 % or 90 % of output voltage, configurable in non-volatile memory
- Excellent transient response with a small ceramic output capacitor
- Output is short-circuit proof to GND
- Turned off in Sleep mode

2.4 On-board CAN supply (V2; UJA1169LTK and UJA1169LTK/F only)

- 5 V nominal output; ±2 % accuracy
- 100 mA output current capability
- Current limiting above 100 mA
- Excellent transient response with a small ceramic output capacitor
- Output is short-circuit proof to GND
- User-defined on/off behavior via SPI

2.5 Off-board sensor supply (VEXT; UJA1169LTK/X and UJA1169LTK/X/F only)

- 5 V nominal output; ±2 % accuracy
- 100 mA output current capability
- Current limiting above 100 mA
- Excellent transient response with a small ceramic output load capacitor
- Output is short-circuit proof to BAT, GND and negative voltages down to −18 V
- User-defined on/off behavior via SPI

2.6 Power Management

- Standby mode featuring very low supply current; voltage V1 remains active
- Sleep mode featuring very low supply current with voltage V1 switched off
- Remote wake-up capability via standard CAN wake-up pattern or ISO 11898-6:2013 and ISO 11898-2:201x compliant selective wake-up frame detection including CAN FD passive support (/F versions only)
- Local wake-up via the WAKE pin
- Wake-up source recognition
- VIO input allows for direct interfacing with 3.3 V to 5 V microcontrollers

2.7 System control and diagnostic features

- Mode control via the Serial Peripheral Interface (SPI)
- Overtemperature warning and shutdown
- Watchdog with Window, Timeout and Autonomous modes and microcontroller-independent clock source
- Optional cyclic wake-up in watchdog Timeout mode
- Watchdog automatically re-enabled when wake-up event captured
- Watchdog period selectable between 8 ms and 4 s
- LIMP output pin with configurable activation threshold
- Watchdog failure and overtemperature events trigger the dedicated LIMP output signal
- 16-, 24- and 32-bit SPI for configuration, control and diagnosis
- Customer configuration of selected functions via non-volatile memory
- Dedicated modes for software development and end-of-line flashing

3. Product family overview

Table 1. Feature overview of UJA1169L SBC family

Device	Modes			Supplies				Host Interface		Additional Features					
	Normal and Standby modes	Sleep mode	Reset mode	V1: 5 V regulator	V1: 5 V regulator and CAN supply	V2: 5 V, CAN + on-board loads	VEXT: 5 V, external loads	SPI: for control and diagnostics	I/O level shifter	Watchdog	Local WAKE pin	LIMP pin	Non-volatile memory	CAN partial networking	CAN FD passive
UJA1169LTK	●	●	●	●		●		●	●	●	●	●	●		
UJA1169LTK/X	●	●	●		●		●	●	●	●	●	●	●		
UJA1169LTK/F	●	●	●	●		●		●	●	●	●	●	●	●	●
UJA1169LTK/X/F	●	●	●		●		●	●	●	●	●	●	●	●	●

4. Ordering information

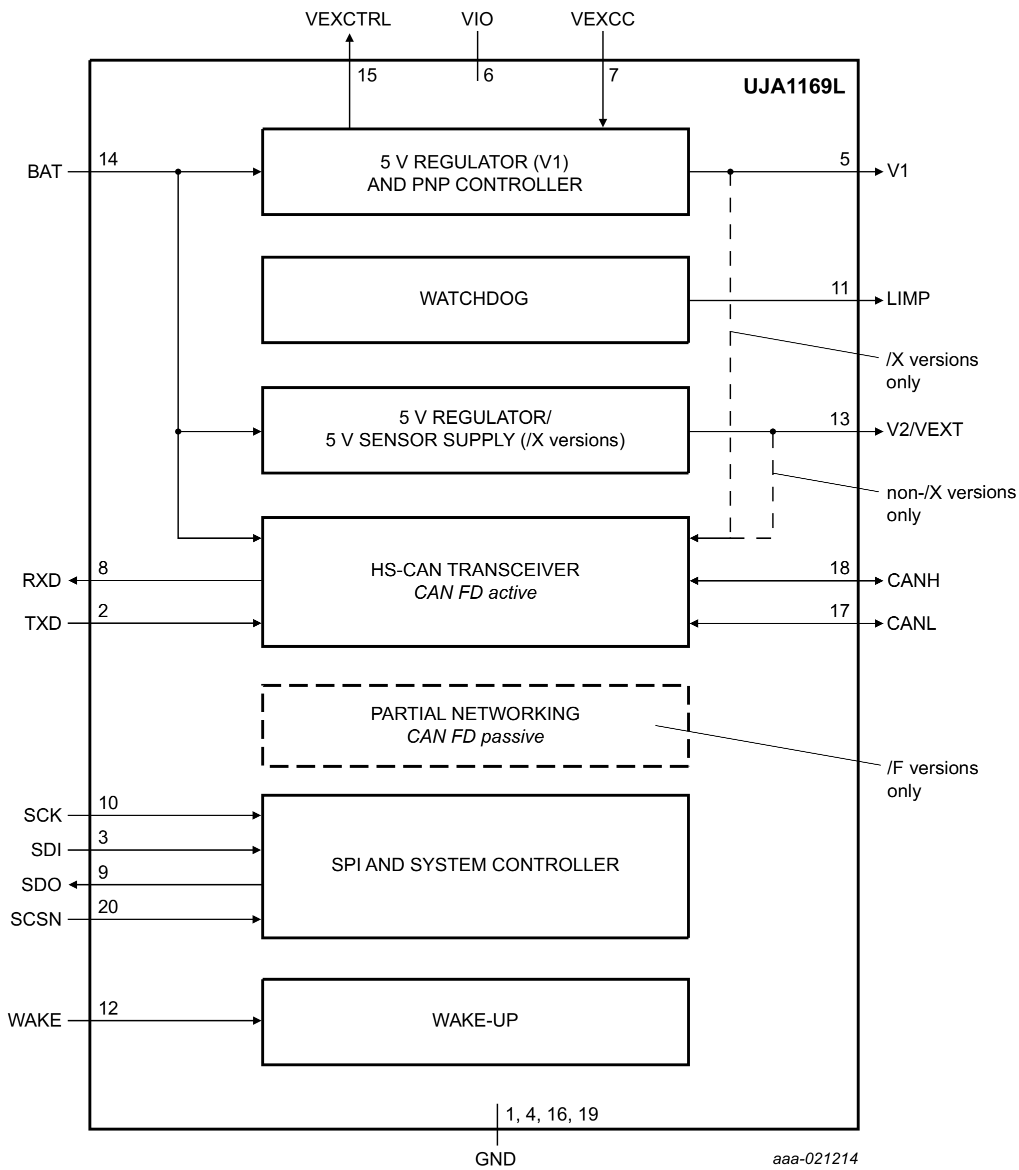
Table 2. Ordering information

Type number[1]	Package		
	Name	Description	Version
UJA1169LTK	HVSON20	plastic thermal enhanced extremely thin quad flat package; no leads; 20 terminals; body 3.5 × 5.5 × 0.85 mm	SOT1360-1
UJA1169LTK/X			
UJA1169LTK/F[2]			
UJA1169LTK/X/F[2]			

[1] UJA1169LTK and UJA1169LTK/F with dedicated CAN supply (V2); UJA1169LTK/X and UJA1169LTK/X/F with protected off-board sensor supply (VEXT).

[2] UJA1169LTK/F and UJA1169LTK/X/F with partial networking according to ISO 11898-6:2013 and ISO 11898-2:201x incorporating CAN FD passive support.

5. Block diagram

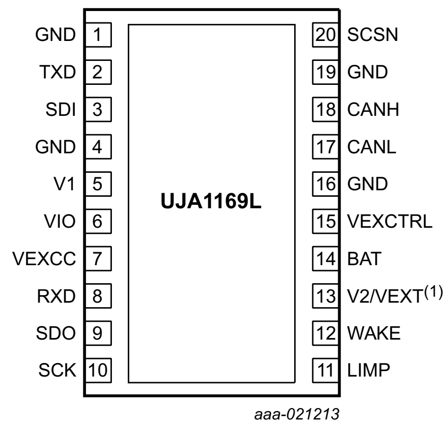


The internal CAN transceiver is supplied from V1 in the UJA1169LTK/X and UJA1169LTK/X/F and from V2 in the other variants.

Fig 1. Block diagram of UJA1169L

6. Pinning information

6.1 Pinning



(1) V2 in the UJA1169LTK and UJA1169LTK/F; VEXT in the UJA1169LTK/X and UJA1169LTK/X/F

Fig 2. Pin configuration diagram

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1[1]	ground
TXD	2	transmit data input
SDI	3	SPI data input
GND	4[1]	ground
V1	5	application supply voltage
VIO	6	supply voltage for I/O level shifter
VEXCC	7	current measurement for external PNP transistor; this pin is connected to the collector of the external PNP transistor
RXD	8	receive data output; reflects data on bus lines and wake-up conditions
SDO	9	SPI data output
SCK	10	SPI clock input
LIMP	11	limp home output, open-drain; active-LOW
WAKE	12	local wake-up input
V2	13	5 V CAN supply (UJA1169LTK and UJA1169LTK/F only)
VEXT	13	5 V sensor supply (UJA1169LTK/X and UJA1169LTK/X/F only)
BAT	14	battery supply voltage
VEXCTRL	15	control pin of the external PNP transistor; this pin is connected to the base of the external PNP transistor
GND	16[1]	ground
CANL	17	LOW-level CAN-bus line

Table 3. Pin description *...continued*

Symbol	Pin	Description
CANH	18	HIGH-level CAN-bus line
GND	19[1]	ground
SCSN	20	SPI chip select input; active-LOW

[1] The exposed die pad at the bottom of the package allows for better heat dissipation and grounding from the SBC via the printed circuit board. For enhanced thermal and electrical performance, connect the exposed die pad to GND.

7. Functional description

7.1 System controller

The system controller manages register configuration and controls the internal functions of the UJA1169L. Detailed device status information is collected and made available to the microcontroller.

7.1.1 Operating modes

The system controller contains a state machine that supports seven operating modes: Normal, Standby, Sleep, Reset, Forced Normal, Overtemp and Off. The state transitions are illustrated in Figure 3.

7.1.1.1 Normal mode

Normal mode is the active operating mode. In this mode, all the hardware on the device is available and can be activated (see Table 4). Voltage regulator V1 is enabled to supply the application.

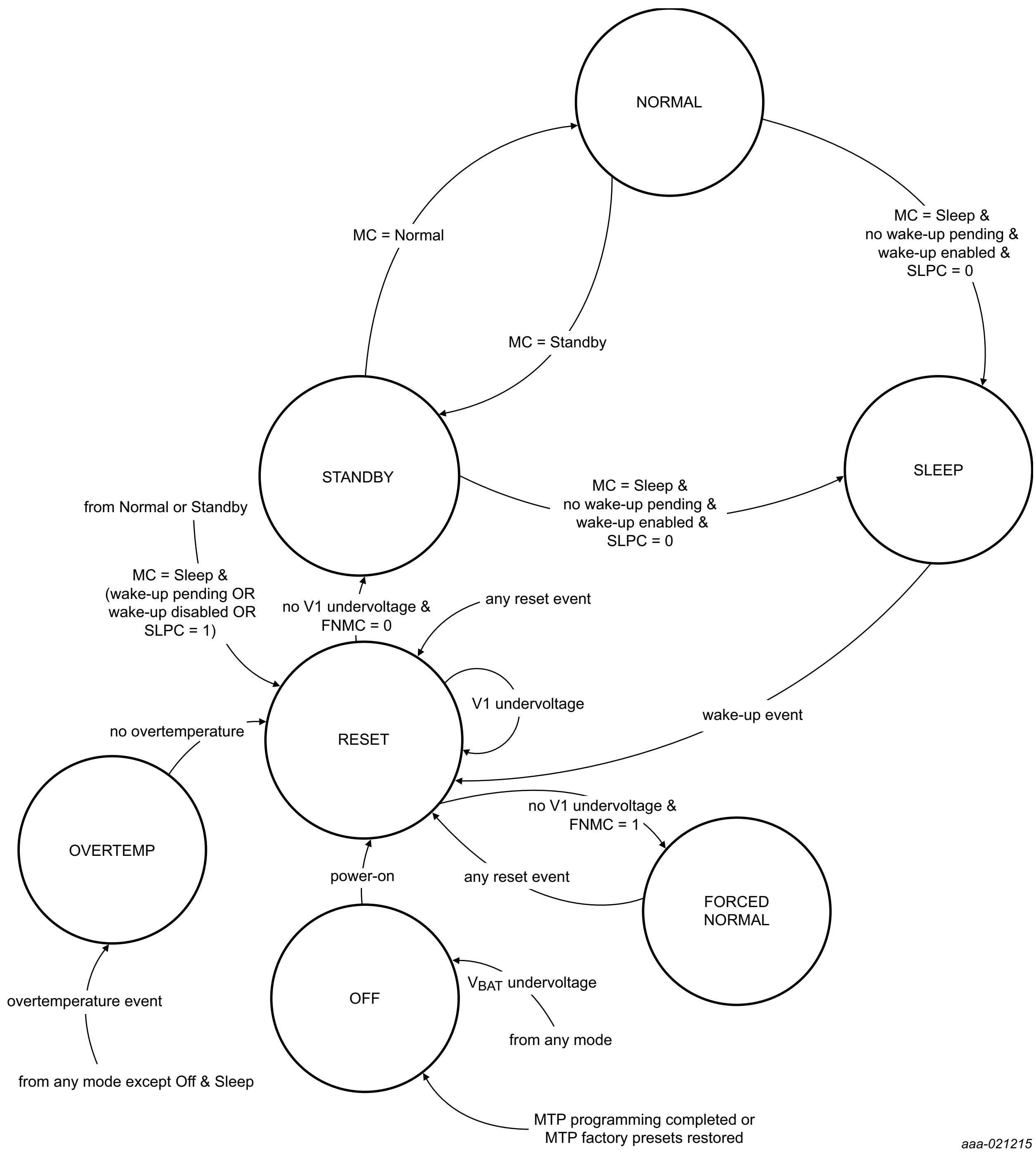
The CAN interface can be configured to be active and thus to support normal CAN communication. Depending on the SPI register settings, the watchdog may be running in Window or Timeout mode and the V2/VEXT output may be active.

7.1.1.2 Standby mode

Standby mode is the first-level power-saving mode of the UJA1169L, offering reduced current consumption. The transceiver is unable to transmit or receive data in Standby mode. V1 remains active and the SPI is enabled as long as V_{VIO}; the watchdog is active (in Timeout mode) if enabled. The behavior of V2/VEXT is determined by the SPI setting.

If remote CAN wake-up is enabled (CWE = 1; see Table 32), the receiver monitors bus activity for a wake-up request. The bus pins are biased to GND (via $R_{i(cm)}$) when the bus is inactive for $t > t_{to(silence)}$ and at approximately 2.5 V when there is activity on the bus (autonomous biasing). CAN wake-up can occur via a standard wake-up pattern or via a selective wake-up frame (selective wake-up is enabled when CPNC = PNCOK = 1, otherwise standard wake-up is enabled; see Table 15).

Pin RXD is forced LOW when any enabled wake-up event is detected. This event can be either a regular wake-up (via the CAN-bus or pin WAKE) or a diagnostic wake-up such as an overtemperature event (see Section 7.11).



State changes via SPI are only possible when a valid supply voltage is connected to VIO.

Fig 3. UJA1169L system controller state diagram

7.1.1.3 Sleep mode

Sleep mode is the second-level power-saving mode of the UJA1169L. The difference between Sleep and Standby modes is that V1 is off in Sleep mode and temperature protection is inactive.

Any enabled regular wake-up via CAN or WAKE or any diagnostic wake-up event will cause the UJA1169L to wake up from Sleep mode. The behavior of V2/VEXT is determined by the SPI settings. The SPI and the watchdog are disabled. Autonomous bus biasing is active.

Sleep mode can be permanently disabled in applications where, for safety reasons, the supply voltage must never be cut off. Sleep mode is permanently disabled by setting the Sleep control bit (SLPC) in the SBC configuration register (see Table 9) to 1. This register is located in the non-volatile memory area of the device (see Section 7.12). When SLPC = 1, a Sleep mode SPI command (MC = 001) triggers an SPI failure event instead of a transition to Sleep mode.

7.1.1.4 Reset mode

Reset mode is the reset execution state of the SBC.

The transceiver is unable to transmit or receive data in Reset mode. The behavior of V2/VEXT is determined by the settings of bits V2C/VEXTC and V2SUC/VEXTSUC (see Section 7.5.3). The SPI is inactive; the watchdog is disabled; V1 and overtemperature detection are active.

After the UJA1169L exits Reset mode, V_{VIO} must be valid for at least $t_{to(SPI)}$ before an SPI read/write access is attempted.

7.1.1.5 Off mode

The UJA1169L switches to Off mode when the battery is first connected or from any mode when $V_{BAT} < V_{th(det)poff}$. Only power-on detection is enabled; all other modules are inactive. The UJA1169L starts to boot up when the battery voltage rises above the power-on detection threshold $V_{th(det)pon}$ (triggering an initialization process) and switches to Reset mode after $t_{startup}$. In Off mode, the CAN pins disengage from the bus (high-ohmic with respect to GND).

7.1.1.6 Overtemp mode

Overtemp mode is provided to prevent the UJA1169L being damaged by excessive temperatures. The UJA1169L switches immediately to Overtemp mode from any mode (other than Off mode or Sleep mode) when the global chip temperature rises above the overtemperature protection activation threshold, $T_{th(act)otp}$.

To help prevent the loss of data due to overheating, the UJA1169L issues a warning when the IC temperature rises above the overtemperature warning threshold ($T_{th(warn)otp}$). When this threshold is reached, status bit OTWS (see Table 6) is set and an overtemperature warning event is captured (OTW = 1; see Table 26), if enabled (OTWE = 1; see Table 30).

In Overtemp mode, the CAN transmitter and receiver are disabled and the CAN pins are in a high-ohmic state. No wake-up event will be detected, but a pending wake-up will still be signaled by a LOW level on pin RXD, which will persist after the overtemperature event has been cleared. V1 is off. VEXT is off in the UJA1169LTK/X and UJA1169LTK/X/F. In the UJA1169LTK and UJA1169LTK/F, V2 is turned off when the SBC enters Overtemp mode.

7.1.1.7 Forced Normal mode

Forced Normal mode simplifies SBC testing and is useful for initial prototyping as well as first flashing of the microcontroller. The watchdog is disabled in Forced Normal mode. The low-drop voltage regulator (V1) is active, VEXT/V2 is enabled and the CAN transceiver is active.

Bit FNMC is factory preset to 1, so the UJA1169L initially boots up in Forced Normal mode (see Table 9). This feature allows a newly installed device to be run in Normal mode without a watchdog. So the microcontroller can, optionally, be flashed via the CAN-bus without having to consider the integrated watchdog.

The register containing bit FNMC (address 74h) is stored in non-volatile memory. So once bit FNMC is programmed to 0, the SBC will no longer boot up in Forced Normal mode, allowing the watchdog to be enabled.

Even in Forced Normal mode, a reset event (e.g. an undervoltage on V1) will trigger a transition to Reset mode with normal Reset mode behavior (except that the CAN transmitter remains active if there is no V_{CAN} undervoltage). When the UJA1169L exits Reset mode, however, it returns to Forced Normal mode instead of switching to Standby mode.

In Forced Normal mode, only the Main status register, the Watchdog status register, the Identification register and registers stored in non-volatile memory can be read. The non-volatile memory area is fully accessible for writing as long as the UJA1169L is in the factory preset state (for details see Section 7.12).

7.1.1.8 Hardware characterization for the UJA1169L operating modes

Table 4. Hardware characterization by functional block

Block	Operating mode						
	Off	Forced Normal	Standby	Normal	Sleep	Reset	Overtemp
V1	off[1]	on	on	on	off	on	off
VEXT/V2	off	on	[2]	[2]	[2]	[2]	VEXT/V2 off
SPI	disabled	active[3]	active	active	disabled	disabled	disabled
Watchdog	off	off	determined by bits WMC (see Table 8)[4]	determined by bits WMC	determined by bits WMC[4]	off	off
CAN	off	Active	Offline	Active/ Offline/ Listen-only (determined by bits CMC; see Table 15)	Offline	Offline	off
RXD	V_{VIO} level	CAN bit stream	V_{VIO} level/LOW if wake-up detected	CAN bit stream if CMC = 01/10/11; otherwise same as Standby/Sleep	V_{VIO} level/ LOW if wake-up detected	V_{VIO} level/ LOW if wake-up detected	V_{VIO} level/ LOW if wake up detected

[1] When the SBC switches from Reset, Standby or Normal mode to Off mode, V1 behaves as a current source during power down while V_{BAT} is falling from $V_{th(det)pof}$ down to 2 V (RAM retention feature; see Section 7.5.1).

[2] Determined by bits V2C/VEXTC and V2SUC/VEXTSUC (see Table 12)

[3] Limited register access: Main status register, Watchdog status register, Identification register and non-volatile memory only.

[4] Window mode is only active in Normal mode.

7.1.2 System control registers

7.1.2.1 Mode control register (0x01)

The operating mode is selected via bits MC in the Mode control register. The Mode control register is accessed via SPI address 0x01 (see Section 7.16).

Table 5. Mode control register (address 01h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	MC	R/W		mode control:
			001	Sleep mode
			100	Standby mode
			111	Normal mode

7.1.2.2 Main status register (0x03)

The Main status register can be accessed to monitor the status of the overtemperature warning flag and to determine whether the UJA1169L has entered Normal mode after initial power-up. It also indicates the source of the most recent reset event.

Table 6. Main status register (address 03h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	
6	OTWS	R		overtemperature warning status:
			0	IC temperature below overtemperature warning threshold
			1	IC temperature above overtemperature warning threshold
5	NMS	R		Normal mode status:
			0	UJA1169L has entered Normal mode (after power-up)
			1	UJA1169L has powered up but has not yet switched to Normal mode
4:0	RSS	R		reset source status:
			00000	left Off mode (power-on)
			00001	CAN wake-up in Sleep mode
			00100	wake-up via WAKE pin in Sleep mode
			01100	watchdog overflow in Sleep mode (Timeout mode)
			01101	diagnostic wake-up in Sleep mode
			01110	watchdog triggered too early (Window mode)
			01111	watchdog overflow (Window mode or Timeout mode with WDF = 1)
			10000	illegal watchdog mode control access
			10001	reserved
			10010	left Overtemp mode
			10011	V1 undervoltage
			10100	illegal Sleep mode command received
			10110	wake-up from Sleep mode due to a frame detect error

7.2 Watchdog

7.2.1 Watchdog overview

The UJA1169L contains a watchdog that supports three operating modes: Window, Timeout and Autonomous. In Window mode (available only in SBC Normal mode), a watchdog trigger event within a defined watchdog window triggers and resets the watchdog timer. In Timeout mode, the watchdog runs continuously and can be triggered and reset at any time within the watchdog period by a watchdog trigger. Watchdog time-out mode can also be used for cyclic wake-up of the microcontroller. In Autonomous mode, the watchdog can be off or autonomously in Timeout mode, depending on the selected SBC mode (see Section 7.2.5).

The watchdog mode is selected via bits WMC in the Watchdog control register (Table 8). The SBC must be in Standby mode when the watchdog mode is changed. If Window mode is selected (WMC = 100), the watchdog remains in (or switches to) Timeout mode until the SBC enters Normal mode. Any attempt to change the watchdog operating mode (via WMC) while the SBC is in Normal mode causes the UJA1169L to switch to Reset mode and the reset source status bits (RSS) to be set to 10000 ('illegal watchdog mode control access'; see Table 6).

Eight watchdog periods are supported, from 8 ms to 4096 ms. The watchdog period is programmed via bits NWP. The selected period is valid for both Window and Timeout modes. The default watchdog period is 128 ms.

A watchdog trigger event resets the watchdog timer. A watchdog trigger event is any valid write access to the Watchdog control register. If the watchdog mode or the watchdog period have changed as a result of the write access, the new values are immediately valid.

Unlike the UJA1169, the UJA1169L does not have a dedicated reset output pin. So watchdog-related events that trigger a system reset (watchdog overflow, watchdog triggered too early, illegal access; see Table 6) are not signaled to the outside application. Nevertheless, the UJA1169L performs an internal reset in the same way as the UJA1169 and switches to Reset mode for t_{rst}. A loss of watchdog service will activate the limp-home function (see Section 7.7).

If an application does not require the watchdog function, it can be permanently disabled via Software Development mode (see Section 7.2.2).

Table 7. Watchdog configuration

Operating/watchdog mode						
FNMC (Forced Normal mode control)		0	0	0	0	1
SDMC (Software Development mode control)		x	x	0	1	x
WMC (watchdog mode control)		100 (Window)	010 (Timeout)	001 (Autonomous)	001 (Autonomous)	n.a.
SBC Operating Mode	Normal mode	Window	Timeout	Timeout	off	off
	Standby mode (RXD HIGH)[1]	Timeout	Timeout	off	off	off
	Standby mode (RXD LOW)[1]	Timeout	Timeout	Timeout	off	off
	Sleep mode	Timeout	Timeout	off	off	off
	Other modes	off	off	off	off	off

[1] RXD LOW signals a pending wake-up.

7.2.1.1 Watchdog control register (0x00)

Table 8. Watchdog control register (address 00h)

Bit	Symbol	Access	Value	Description
7:5	WMC	R/W		watchdog mode control:
			001[1]	Autonomous mode
			010[2]	Timeout mode
			100[3]	Window mode
4	reserved	R	-	
3:0	NWP	R/W		nominal watchdog period:
			1000	8 ms
			0001	16 ms
			0010	32 ms
			1011	64 ms
			0100[2]	128 ms
			1101	256 ms
			1110	1024 ms
			0111	4096 ms

[1] Default value if SDMC = 1 (see Section 7.2.2)

[2] Default value.

[3] Selected in Standby mode but only activated when the SBC switches to Normal mode.

The watchdog is a valuable safety mechanism, so it is critical that it is configured correctly. Two features are provided to prevent watchdog parameters being changed by mistake:

- redundant coding of configuration bits WMC and NWP
- reconfiguration protection in Normal mode

Redundant codes associated with control bits WMC and NWP ensure that a single bit error cannot cause the watchdog to be configured incorrectly (at least 2 bits must be changed to reconfigure WMC or NWP). If an attempt is made to write an invalid code to WMC or NWP (e.g. 011 or 1001 respectively), the SPI operation is abandoned and an SPI failure event is captured, if enabled (see Section 7.11).

7.2.1.2 SBC configuration control register (0x74)

Two operating modes have a major impact on the operation of the watchdog: Forced Normal mode and Software Development mode (Software Development mode is provided for test and development purposes only and is not a dedicated SBC operating mode; the UJA1169L can be in any functional operating mode with Software Development mode enabled; see Section 7.2.2). These modes are enabled and disabled via bits FNMC and SDMC respectively in the SBC configuration control register (see Table 9). Note that this register is located in the non-volatile memory area. The watchdog is disabled in Forced Normal mode (FNM). In Software Development mode (SDM), the watchdog can be disabled or activated for test and software debugging purposes.

Table 9. SBC configuration control register (address 74h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5:4	V1RTSUC	R/W		V1 undervoltage threshold (defined by bit V1RTC) at start-up:
			00[1]	V1 undervoltage detection at 90 % of nominal value at start-up (V1RTC = 00)
			01	V1 undervoltage detection at 80 % of nominal value at start-up (V1RTC = 01)
			10	V1 undervoltage detection at 70 % of nominal value at start-up (V1RTC = 10)
			11	V1 undervoltage detection at 60 % of nominal value at start-up (V1RTC = 11)
3	FNMC	R/W	[2]	Forced Normal mode control:
			0	Forced Normal mode disabled
			1[1]	Forced Normal mode enabled
2	SDMC	R/W		Software Development mode control:
			0[1]	Software Development mode disabled
			1	Software Development mode enabled
1	reserved	R	-	
0	SLPC	R/W		Sleep control:
			0[1]	Sleep mode commands accepted
			1	Sleep mode commands ignored

[1] Factory preset value.

[2] FNMC settings overrule SDMC.

7.2.1.3 Watchdog status register (0x05)

Information on the status of the watchdog is available from the Watchdog status register (Table 10). This register also indicates whether Forced Normal and Software Development modes are active.

Table 10. Watchdog status register (address 05h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	
3	FNMS	R/W		Forced Normal mode status:
			0	SBC is not in Forced Normal mode
			1	SBC is in Forced Normal mode
2	SDMS	R/W		Software Development mode status:
			0	SBC is not in Software Development mode
			1	SBC is in Software Development mode
1:0	WDS	R		watchdog status:
			00	watchdog is off
			01	watchdog is in first half of the nominal period
			10	watchdog is in second half of the nominal period
			11	reserved

7.2.2 Software Development mode

Software Development mode is provided to simplify the software design process and to allow the UJA1169L to operate without watchdog supervision. When Software Development mode is enabled, the watchdog starts up in Autonomous mode (WMC = 001) and is inactive after a system reset, overriding the default value (see Table 8). The watchdog is always off in Autonomous mode if Software Development mode is enabled (SDMC = 1; see Table 7).

However, it is possible to activate and deactivate the watchdog for test purposes by selecting Window or Timeout mode via bits WMC while the SBC is in Standby mode.

7.2.3 Watchdog behavior in Window mode

In Window mode, the watchdog can only be triggered during the second half of the watchdog period. If the watchdog overflows, or is triggered in the first half of the watchdog period (before $t_{trig(wd)1}$), a system reset is performed. After the system reset, the reset source (either 'watchdog triggered too early' or 'watchdog overflow') can be read via the reset source status bits (RSS) in the Main Status register (Table 6). If the watchdog is triggered in the second half of the watchdog period (after $t_{trig(wd)1}$ but before $t_{trig(wd)2}$), the watchdog timer is restarted.

7.2.4 Watchdog behavior in Timeout mode

In Timeout mode, the watchdog timer can be reset at any time by a watchdog trigger. If the watchdog overflows, a watchdog failure event (WDF) is captured. If a WDF is already pending when the watchdog overflows, a system reset is performed. In Timeout mode, the watchdog can be used as a cyclic wake-up source for the microcontroller when the UJA1169L is in Standby or Sleep mode. In Sleep mode, a watchdog overflow generates a wake-up event while setting WDF.

When the SBC is in Sleep mode with watchdog Timeout mode selected, a wake-up event is generated after the nominal watchdog period (NWP), setting WDF. RXD is forced LOW and V1 is turned on. The application software can then clear the WDF bit and trigger the watchdog before it overflows again.

7.2.5 Watchdog behavior in Autonomous mode

In Autonomous mode, the watchdog will not be running when the SBC is in Standby (RXD HIGH) or Sleep mode. If a wake-up event is captured, pin RXD is forced LOW to signal the event and the watchdog is automatically restarted in Timeout mode. If the SBC was in Sleep mode when the wake-up event was captured, it switches to Standby mode.

7.2.6 Exceptional behavior of the watchdog after writing to the Watchdog register

A successful write operation to the Watchdog control register resets the watchdog timer. Bits WDS are set to 01 and the watchdog restarts at the beginning of the watchdog period (regardless of the selected watchdog mode). However, the watchdog may restart unexpectedly in the second half of the watchdog period or a WDF interrupt may be captured under the following conditions.

Case A: When the watchdog is running in Timeout mode (see Table 7) and a new watchdog period is selected (via bits NWP) that is shorter than the existing watchdog period, one of both of the following events may occur.

Status bits WDS can be set to 10. The timer then restarts at the beginning of the second half of the watchdog period, causing the watchdog to overflow earlier than expected. This can be avoided by writing the new NWP (or NWP + WMC) code twice whenever the watchdog period needs to be changed. The write commands should be sent consecutively. The gap between the commands must be less than half of the new watchdog period.

If the watchdog is in the second half of the watchdog period when the watchdog period is changed, the timer will be reset correctly. The watchdog then restarts at the beginning of the watchdog period and WDS is set 01. However, a WDF event may be captured unexpectedly. To counteract this effect, the WDF event should be cleared by default after the new watchdog period has been selected as described above (two consecutive write commands).

Case B: If the watchdog is triggered in Timeout mode (see Table 7) at exactly the same time that WDS is set to 10, it will start up again in the second half of the watchdog period. As in Case A, this causes the watchdog to overflow earlier than expected. This behavior appears identical to an ignored watchdog trigger event and can be avoided by issuing two consecutive watchdog commands. The second command should be issued before the end of the first half of the watchdog period. Use this trigger scheme if it is possible that the watchdog could be triggered exactly in the middle of the watchdog window.

7.3 System reset

When a system reset occurs, the SBC switches to Reset mode. It will remain in Reset mode for t_{rst} (set via bits RLC; see Table 11) before switching to Standby or Forced Normal mode (see Figure 3). The UJA1169L can distinguish up to 12 different reset sources, as detailed in Table 6.

The SBC distinguishes between a cold start and a warm start. A cold start is performed if the reset event was combined with a V1 undervoltage event (power-on reset, reset during Sleep mode, over-temperature reset, V1 undervoltage before entering or while in Reset mode). The setting of bits RLC determines the reset mode length for a cold start.

A warm start is performed if any other reset event occurs without a V1 undervoltage (watchdog failure, watchdog change attempt in Normal mode, illegal Sleep mode command). The SBC uses the shortest reset length (t_{rst} as defined when RLC = 11).

7.3.1 Start-up control register (0x73)

Table 11. Start-up control register (address 73h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5:4	RLC	R/W		reset mode length:
			00[1]	t_{rst} = 20 ms to 25 ms
			01	t_{rst} = 10 ms to 12.5 ms
			10	t_{rst} = 3.6 ms to 5 ms
			11	t_{rst} = 1 ms to 1.5 ms

Table 11. Start-up control register (address 73h) *…continued*

Bit	Symbol	Access	Value	Description
3	V2SUC[2] VEXTSUC[3]	R/W		V2/VEXT start-up control:
			0[1]	bits V2C/VEXTC set to 00 at power-up
			1	bits V2C/VEXTC set to 11 at power-up
2:0	reserved	R	-	

[1] Factory preset value.

[2] UJA1169LTK and UJA1169LTK/F only.

[3] UJA1169LTK/X and UJA1169LTK/X/F only.

7.4 Global temperature protection

The temperature of the UJA1169L is monitored continuously, except in Sleep and Off modes. The SBC switches to Overtemp mode if the temperature exceeds the overtemperature protection activation threshold, $T_{th(act)otp}$. In addition, V1, V2/VEXT and the CAN transceiver are switched off (if the optional external PNP transistor is connected, it will also be off; see Section 7.5.2). When the temperature drops below the overtemperature protection release threshold, $T_{th(rel)otp}$, the SBC switches to Standby mode via Reset mode.

In addition, the UJA1169L provides an overtemperature warning. When the IC temperature rises about the overtemperature warning threshold ($T_{th(warn)otp}$), status bit OTWS is set and an overtemperature warning event is captured (OTW = 1).

7.5 Power supplies

7.5.1 Battery supply voltage (V_{BAT})

The internal circuitry is supplied from the battery via pin BAT. The device must be protected against negative supply voltages, e.g. by using an external series diode. If V_{BAT} falls below the power-off detection threshold, $V_{th(det)poff}$, the SBC switches to Off mode. V1 remains active until V_{BAT} falls below 2 V, ensuring connected hardware remains active for as long as possible (RAM retention feature).

The SBC switches from Off mode to Reset mode $t_{startup}$ after the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$. Power-on event status bit PO is set to 1 to indicate the UJA1169L has powered up and left Off mode (see Table 26).

7.5.2 Voltage regulator V1

V1 provides a 5 V supply, delivering up to 250 mA load current. In the UJA1169LTK/X and UJA1169LTK/X/F variants, the CAN transceiver is supplied internally via V1, reducing the output current available for external components.

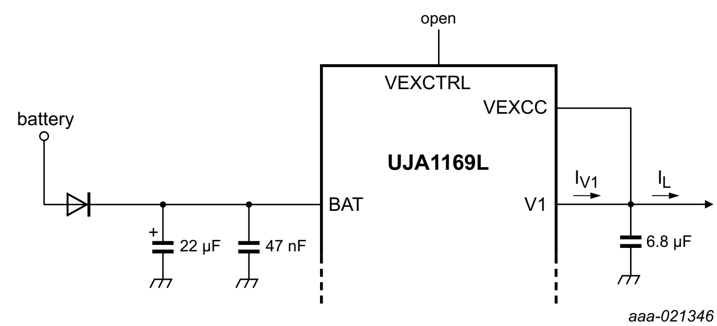


Fig 4. Typical application without external PNP (showing example component values)

To prevent the device overheating at high ambient temperatures or high average currents, an external PNP transistor can be connected as illustrated in Figure 5. In this configuration, the power dissipation is distributed between the SBC (I_{V1}) and the PNP transistor (I_{PNP}).

The PNP transistor is activated when the load current reaches the PNP activation threshold, $I_{th(act)PNP}$. Bit PDC in the Regulator control register (Table 12) is used to regulate how power dissipation is distributed.

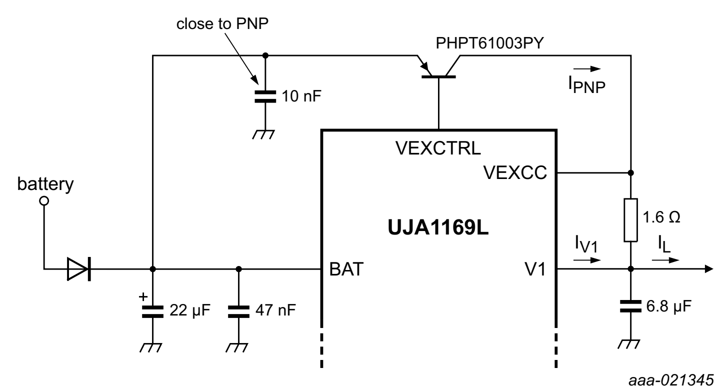


Fig 5. Typical application with external PNP (showing example component values)

For short-circuit protection, a resistor must be connected between pins V1 and VEXCC to allow the current to be monitored. This resistor limits the current delivered by the external transistor. If the voltage difference between pins VEXCC and V1 reaches $V_{th(act)Ilim}$, the PNP current limiting activation threshold voltage, the transistor current will not increase further. In general, any PNP transistor with a current amplification factor (β) of between 50 and 500 can be used.

The output voltage on V1 is monitored. A system reset is generated if the voltage on V1 drops below the selected undervoltage threshold (60 %, 70 %, 80 % or 90 % of the nominal V1 output voltage, selected via V1RTC in the Regulator control register; see Table 12).

The default value of the undervoltage threshold at power-up is determined by the value of bits V1RTSUC in the SBC configuration control register (Table 9). The SBC configuration control register is in non-volatile memory, allowing the user to define the default undervoltage threshold (V1RTC) at any battery start-up.

In addition, an undervoltage warning (a V1U event; see Section 7.11) is generated if the voltage on V1 falls below 90 % of the nominal value (and V1U event detection is enabled, V1UE = 1; see Table 31). This information can be used as a warning, when the 60 %, 70 % or 80 % threshold is selected, to indicate that the level on V1 is outside the nominal supply range. The actual status of V1, whether it is above or below the 90 % undervoltage threshold, can be polled via bit V1S in the Supply voltage status register (Table 13).

7.5.3 Voltage regulator V2

In the UJA1169LTK and UJA1169LTK/F, pin 13 is a voltage regulator output (V2) delivering up to 100 mA.

The CAN transceiver is supplied internally from V2, consuming a portion of the available current. V2 is not protected against shorts to the battery or to negative voltages and should not be used to supply off-board components.

V2 is software controlled and must be turned on (via bit V2C in the Regulator control register; see Table 12) to activate the supply voltage for the internal CAN transceiver. V2 is not required for wake-up detection via the CAN interface.

The default value of V2C at power-on is defined by bits V2SUC in non-volatile memory (see Section 7.12). The status of V2 can be polled from the Supply voltage status register (Table 13).

7.5.4 Voltage regulator VEXT

In the UJA1169LTK/X and UJA1169LTK/X/F, pin 13 is a voltage regulator output (VEXT) that can be used to supply off-board components, delivering up to 100 mA. VEXT is protected against short-circuits to the battery and negative voltages. Since the CAN controller is supplied internally via V1, the full 100 mA supply current is available for off-board loads connected to VEXT (provided the thermal limits of the PCB are not exceeded).

VEXT is software controlled and must be turned on (via bit VEXTC in the Regulator control register; see Table 12) to activate the supply voltage for off-board components.

The default value of VEXTC at power-on is defined by bits VEXTSUC in non-volatile memory (see Section 7.12). The status of VEXT can be read from the Supply voltage status register (Table 13).

7.5.5 Regulator control register (0x10)

Table 12. Regulator control register (address 10h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	
6	PDC	R/W		power distribution control:
			0	V1 threshold current for activating the external PNP transistor, load current rising; $I_{th(act)PNP}$ (higher value; see Table 52) V1 threshold current for deactivating the external PNP transistor, load current falling; $I_{th(deact)PNP}$ (higher value; see Table 52)
			1	V1 threshold current for activating the external PNP transistor; load current rising; $I_{th(act)PNP}$ (lower value; see Table 52) V1 threshold current for deactivating the external PNP transistor; load current falling; $I_{th(deact)PNP}$ (lower value; see Table 52)
5:4	reserved	R	-	reserved bits can be read and overwritten without affecting device functionality; default value at power-up is 00 (other reserved bits always return 0)
3:2	V2C[1] VEXTC[2]	R/W		V2/VEXT configuration:
			00	V2/VEXT off in all modes
			01	V2/VEXT on in Normal mode
			10	V2/VEXT on in Normal, Standby and Reset modes
			11	V2/VEXT on in Normal, Standby, Sleep and Reset modes
1:0	V1RTC[3]	R/W		set V1 undervoltage threshold:
			00	undervoltage threshold set to 90 % of V1 nominal output voltage
			01	undervoltage threshold set to 80 % of V1 nominal output voltage
			10	undervoltage threshold set to 70 % of V1 nominal output voltage
			11	undervoltage threshold set to 60 % of V1 nominal output voltage

[1] UJA1169LTK and UJA1169LTK/F: default value at power-up defined by V2SUC bit setting (see Table 11).

[2] UJA1169LTK/X and UJA1169LTK/X/F: default value at power-up defined by VEXTSUC bit setting (see Table 11).

[3] Default value at power-up defined by setting of bits V1RTSUC (see Table 9).

7.5.6 Supply voltage status register (0x1B)

Table 13. Supply voltage status register (address 1Bh)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:1	V2S[1] VEXTS[2]	R/W		V2/VEXT status:
			00[3]	V2/VEXT voltage ok
			01	V2/VEXT output voltage below undervoltage threshold
			10	V2/VEXT output voltage above overvoltage threshold
			11	V2/VEXT disabled
0	V1S	R/W		V1 status:
			0[3]	V1 output voltage above 90 % undervoltage threshold
			1	V1 output voltage below 90 % undervoltage threshold

[1] UJA1169LTK and UJA1169LTK/F only.

[2] UJA1169LTK/X and UJA1169LTK/X/F only.

[3] Default value at power-up.

7.6 VIO supply pin

Pin VIO should be connected to the microcontroller supply voltage. This will cause the signal levels of the TXD, RXD and the SPI interface pins to be adjusted to the I/O levels of the microcontroller, enabling direct interfacing without the need for glue logic.

7.7 LIMP output

The dedicated LIMP pin can be used to enable so called ‘limp home’ hardware in the event of a serious ECU failure. Detectable failure conditions include SBC overtemperature events, loss of watchdog service, short-circuit on pin V1 and user-initiated reset events (see Figure 6). The LIMP pin is a battery-robust, active-LOW, open-drain output. The LIMP pin can also be forced LOW by setting bit LHC in the Fail-safe control register (Table 14).

7.7.1 Reset counter

The UJA1169L uses a reset counter to detect serious failures. The reset counter is incremented (bits RCC = RCC + 1; see Table 14) every time the SBC enters Reset mode. When the system is running correctly, it is expected that the system software will reset this counter (RCC = 00) periodically to ensure that routinely expected reset events do not cause it to overflow.

If RCC is equal to 3 when the SBC enters Reset mode, the SBC assumes that a serious failure has occurred and sets the limp-home control bit, LHC. This action forces the external LIMP pin LOW with RCC overflowing to RCC = 0. Bit LHC can also be set via the SPI interface.

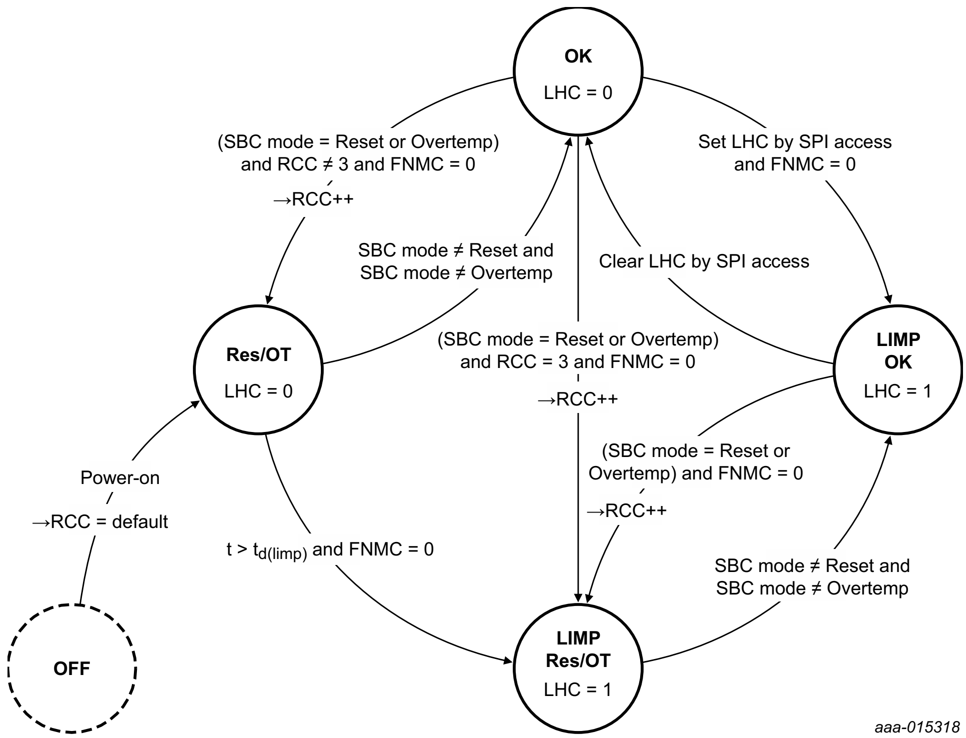
The LIMP pin is set floating again if LHC is reset to 0 through software control or at power-up when the SBC leaves Off mode.

The application software can preset the counter value to define how many reset events are tolerated before the limp-home function is activated. If RCC is initialized to 3, for example, the next reset event will immediately trigger the limp-home function. The default counter setting at power-up is RCC = 00.

Besides a reset counter (RCC) overflow, the following events cause bit LHC to be set and immediately trigger the limp-home function:

- overtemperature lasting longer than $t_{d(limp)}$
- SBC remaining in Reset mode for longer than $t_{d(limp)}$ (e.g. due to a permanent V1 undervoltage).

7.7.2 LIMP state diagram



SBC modes are derived from the SBC state diagram (see Figure 3). The reset counter overflows from 3 to 0; t is the time the SBC remains continuously in Reset or Overtemp mode; time t is reset at mode entry; time t is not reset on a transition between Reset and Overtemp modes

Fig 6. Limp function state diagram

Note that the SBC always switches to Reset mode after leaving Sleep mode, since the SBC powers up V1 in response to a wake-up event. So RCC is incremented after each Sleep mode cycle. The application software needs to monitor RCC and update the value as necessary to ensure that multiple Sleep mode cycles do not cause the reset counter to overflow.

The limp-home function and the reset counter are disabled in Forced Normal mode. The LIMP pin is floating, RCC remains unchanged and bit LHC = 0.

7.7.2.1 Fail-safe control register (0x02)

The Fail-safe control register contains the reset counter along with limp home control settings.

Table 14. Fail-safe control register (address 02h)

Bit	Symbol	Access	Value	Description
7:3	reserved			
2	LHC	R/W		LIMP home control:
			0	LIMP pin is floating
			1	LIMP pin is driven LOW
1:0	RCC	R/W		reset counter control:
			xx	incremented every time the SBC enters Reset mode while FNMC = 0; RCC overflows from 11 to 00; default at power-on is 00

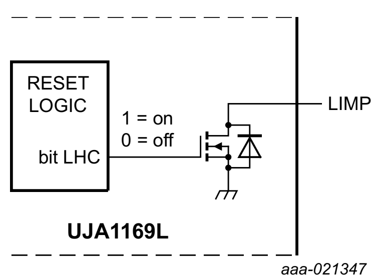


Fig 7. LIMP pin functional diagram

7.8 High-speed CAN transceiver

The integrated high-speed CAN transceiver is designed for active communication at bit rates up to 1 Mbit/s, providing differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2:201x (upcoming merged ISO 11898-2/5/6 standard) compliant. Depending on the derivative, the CAN transmitter is supplied internally from V1 (in /X variants) or V2 (in variants with a V2 regulator). Additional timing parameters defining loop delay symmetry are included to ensure reliable communication in fast phase at data rates up to 2 Mbit/s, as used in CAN FD networks.

The CAN transceiver supports autonomous CAN biasing as defined in ISO 11898-6:2013 and ISO 11898-2:201x. CANH and CANL are always biased to 2.5 V when the transceiver is in Active or Listen-only modes (CMC = 01/10/11; see Table 15).

Autonomous biasing is active in CAN Offline mode, to 2.5 V if there is activity on the bus (CAN Offline Bias mode) and to GND if there is no activity on the bus for $t > t_{to(silence)}$ (CAN Offline mode). The autonomous CAN bias voltage is derived directly from V_{BAT}.

7.8.1 CAN operating modes

The integrated CAN transceiver supports four operating modes: Active, Listen-only, Offline and Offline Bias (see Figure 8). The CAN transceiver operating mode depends on the UJA1169L operating mode and on the setting of bits CMC in the CAN control register (Table 15).

When the UJA1169L is in Normal mode, the CAN transceiver operating mode (Active, Listen-only or Offline) can be selected via bits CMC in the CAN control register (Table 15). When the UJA1169L is in Standby or Sleep modes, the transceiver is forced to Offline or Offline Bias mode (depending on bus activity).

7.8.1.1 CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines.

CAN Active mode is selected when CMC = 01 or 10.

When CMC = 01, V_{CAN} undervoltage detection is enabled and the transceiver goes to CAN Offline or CAN Offline Bias mode when the voltage at the CAN block drops below the 90 % threshold. V1 is monitored for the 90 % threshold in the /X versions; in the V2 versions, the 90 % threshold is related to the V2 supply voltage.

When CMC = 10, V_{CAN} undervoltage detection is disabled. The transmitter remains active even if the CAN supply falls below the 90 % threshold while V1 is still above the V1 reset threshold (selected via bits V1RTC).

If pin TXD is held LOW (e.g. by a short-circuit to GND) when CAN Active mode is selected via bits CMC, the transceiver does not enter CAN Active mode but switches to or remains in CAN Listen-only mode. In order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state, it remains in Listen-only mode until pin TXD goes HIGH.

In CAN Active mode, the CAN bias voltage is the CAN supply voltage divided by two (depending on the derivative, the bias voltage is either V1 divided by two or V2 divided by two).

The application can determine whether the CAN transceiver is ready to transmit/receive data (CAN supply above 90 % threshold) or is disabled by reading the CAN Transceiver Status (CTS) bit in the Transceiver Status Register (Table 16).

7.8.1.2 CAN Listen-only mode

CAN Listen-only mode allows the UJA1169L to monitor bus activity while the transceiver is inactive, without influencing bus levels. The CAN transmitter is disabled in Listen-only mode, reducing current consumption. The CAN receiver and CAN biasing remain active.

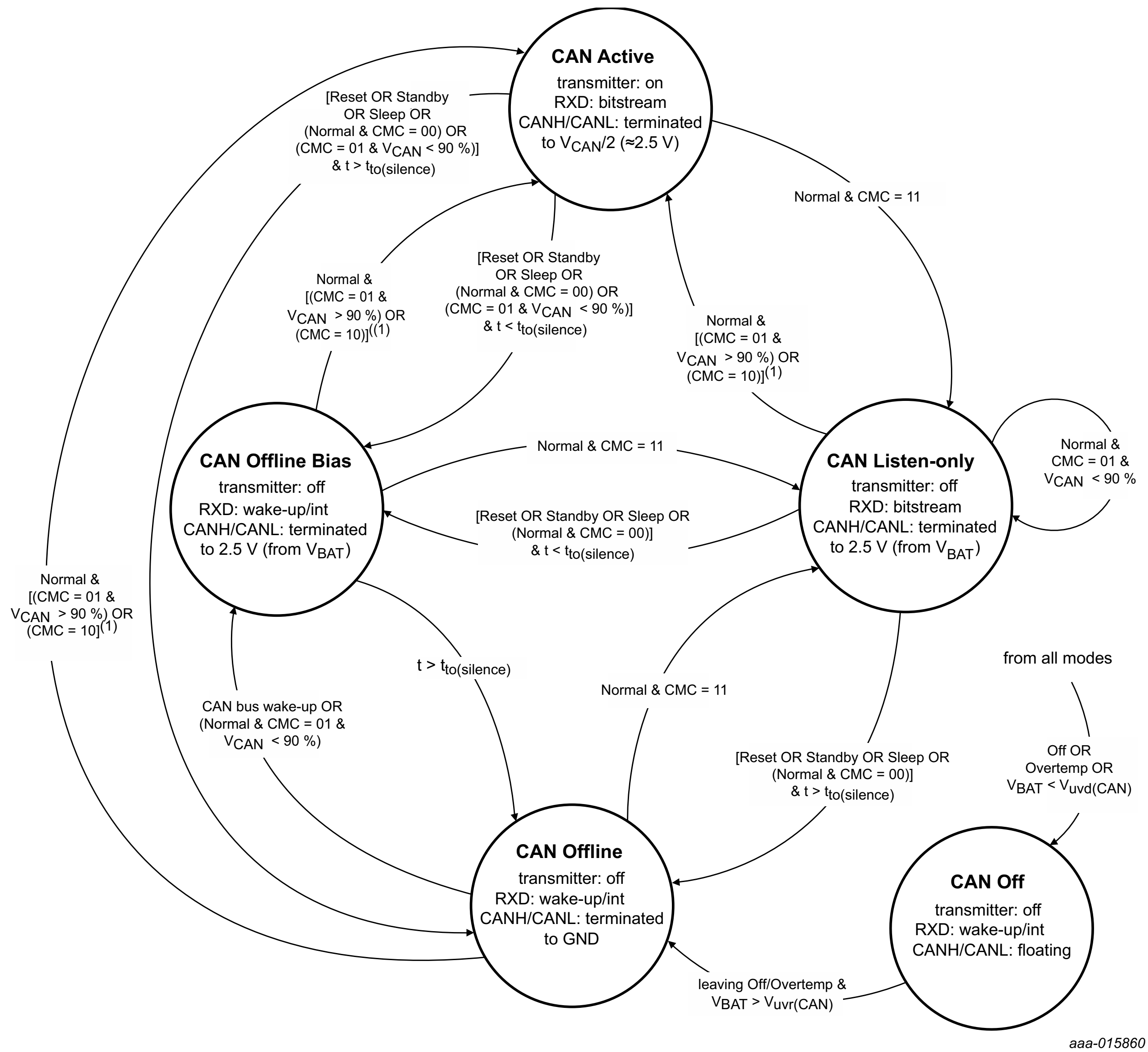
7.8.1.3 CAN Offline and Offline Bias modes

In CAN Offline mode, the transceiver monitors the CAN-bus for a wake-up event, provided CAN wake-up detection is enabled (CWE = 1; see Table 32). CANH and CANL are biased to GND.

CAN Offline Bias mode is the same as CAN Offline mode, with the exception that the CAN-bus is biased to 2.5 V. This mode is activated automatically when activity is detected on the CAN-bus while the transceiver is in CAN Offline mode. If the CAN-bus is silent (no CAN-bus edges) for longer than $t_{to(silence)}$, the transceiver returns to CAN Offline mode.

7.8.1.4 CAN Off mode

In CAN Off mode, bus pins CANH and CANL are set floating with respect to GND, which prevents reverse currents flowing from the bus to an unsupplied ECU. The differential input resistance between CANH and CANL remains constant.



(1) To prevent the bus lines being driven to a permanent dominant state, the transceiver will not switch to CAN Active mode or CAN Listen-only mode if pin TXD is held LOW (e.g. by a short-circuit to GND)

Fig 8. CAN transceiver state machine (with FNMC = 0)

7.8.2 CAN standard wake-up (partial networking not enabled)

If the CAN transceiver is in Offline mode and CAN wake-up is enabled (CWE = 1), but CAN selective wake-up is disabled (CPNC = 0 or PNCOK = 0), the UJA1169L monitors the bus for a wake-up pattern.