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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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INTEGRATED LOAD SWITCH μ PA1981

N-CHANNEL/P-CHANNEL MOS FET PAIR FOR LOAD SWITCH

DESCRIPTION

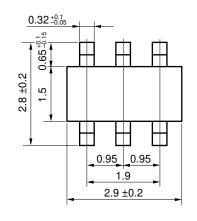
The μ PA1981 is a N-Channel/P-Channel MOS FET pair for compact power management in portable electronic equipment where 2.5 to 8 V input and 2.8 A output current capability are needed.

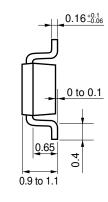
This load switch integrated a small N-Channel MOS FET (Q1), which drives a large P-Channel MOS FET (Q2) in one tiny package (SC-95).

FEATURES

- Vs2D21 = 0.2 V MAX. (Vs2S1 = 5.0 V, ID2 = -2.8 A, RD2S2(on)1 = 70 m Ω)
- $V_{S2D2}2 = 0.2 \text{ V MAX}$. ($V_{S2S1} = 2.5 \text{ V}$, $I_{D2} = -1.9 \text{ A}$, $R_{D2S2(on)}2 = 105 \text{ m}\Omega$)

PACKAGE DRAWING (Unit: mm)





ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1981TE	SC-95 (Mini Mold Thin Type)

Marking: TZ

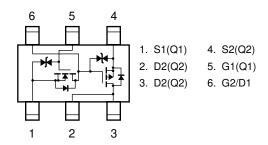
ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Source2 to Source1 Input Voltage Range	Vs2S1	2.5 to 8.0	V
Gate1 to Source1 On Voltage Range	V _{G1S1}	1.5 to 7.0	V
Drain2 Current (DC) Note1	ID2(DC)	-2.8	Α
Drain2 Current (pulse) Note2	D2(pulse)	-10.0	Α
Total Power Dissipation Note1	Рт	1.0	W
Channel Temperature	T_ch	150	°C
Storage Temperature	Tstg	-55 to +150	°C

Notes 1. Mounted on FR-4 Board of 2500 mm² x 1.6 mm, $t \le 5$ sec

2. PW \leq 10 μ s, Duty Cycle \leq 1%

PIN CONNECTION (Top View)



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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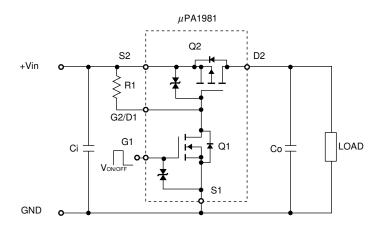
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ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT		
OFF CHARACTERISTICS								
Q2-S2 to D2 Leakage Current	ls2D2	V _{S2D2} = 8.0 V, V _{G1S1} = 0 V			1.0	μΑ		
Q1-D1 to S1 Leakage Current	I D1S1	V _{D1S1} = 8.0 V, V _{G1S1} = 0 V			1.0	μΑ		
ON CHARACTERISTICS								
Q2-S2 to D2 Voltage Note	Vs2D21	V _{S2S1} = 5.0 V, V _{G1S1} = 3.3 V, I _{D2} = -2.8 A		0.15	0.2	٧		
	Vs2D22	V _{S2S1} = 2.5 V, V _{G1S1} = 3.3 V, I _{D2} = -1.9 A		0.15	0.2	V		
Q2-Static On-Resistance Note	R _{D2S2(on)} 1	V _{G2S2} = -5.0 V, I _{D2} = -2.8A		52	70	mΩ		
	RD2S2(on)2	V _{G2S2} = -2.5 V, I _{D2} = -1.9 A		76	105	mΩ		
Q2-S2 to D2 Current Note	Is2D21	V _{S2D2} = 0.2 V, V _{S2S1} = 5.0 V, V _{G1S1} = 3.3 V	2.8			Α		
	Is2D2 2	V _{S2D2} = 0.2 V, V _{S2S1} = 2.5 V, V _{G1S1} = 3.3 V	1.9			Α		

Note Pulsed: PW \leq 350 μ s, Duty Cycle \leq 2%

CIRCUIT1 EXAMPLE OF APPLICATION CIRCUIT



RECOMMENDATION OF CIRCUIT1

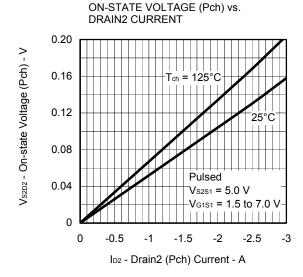
Co \leq 1 μ F for applications

R1 is required to turn Q2 off.

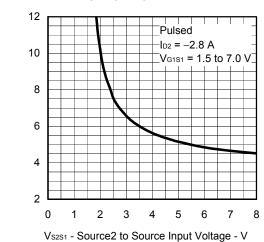
Select R1 in the range of 10 to 470 $k\Omega.$

RDZSZ(01) - Static On-Resistance - mΩ

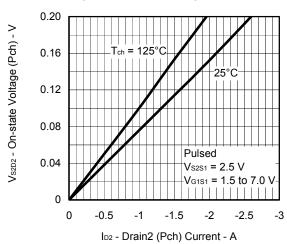
TYPICAL CHARACTERISTICS (TA = 25°C)



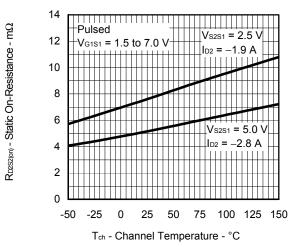
ON-STATE RESISTANCE (Pch) vs. INPUT VOLTAGE



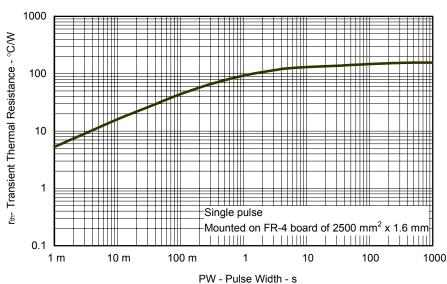
ON-STATE VOLTAGE (Pch) vs. CHANNEL TEMPERATURE



ON-STATE RESISTANCE (Pch) vs. CHANNEL TEMPERATURE



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



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