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USB Power Delivery Controller

Highlights

- Integrated USB Power Delivery (PD) PHY
- Support for Power Delivery Message Protocol
- Integrated Voltage and Current ADC Inputs
- Configuration Profile Selection
- On-chip Microcontroller
- SPI Interface
- Commercial and Industrial Grade Temperature Support
- Available in 32-SQFN Package

Target Applications

- Notebooks
- Ultrabooks
- Desktop PCs
- Docking Stations
- Monitors
- Printers

Key Benefits

- Integrated USB Power Delivery (PD) PHY
 - Integrated receive termination
 - Requires minimal external components
- Support for Power Delivery Message Protocol
 - Message Generation/Consumption
 - Retry Generation
 - Error Handling
 - State Behavior
- Cable Detect Logic
 - Cable attachment type
- CFG_SEL pins allow selection of multiple profiles
 - Provider
 - Provider/Consumer
 - Consumer
 - Consumer/Provider
- Integrated Voltage (VMON) and Current (IMON) ADC Inputs
- Dead Battery Support
- On-chip Microcontroller
 - Manages I/Os and other signals
 - Implements power delivery policy engine and device policy manager
- Configuration Programming via OTP, or Vendor Defined Messaging
- Supports Low Power Modes
- Serial Peripheral Interface (SPI) Bus
- Internal 3.3 V and 1.8 V Voltage Regulators
- Integrated Oscillator Reduces BOM Costs
- Package
 - 32-pin SQFN (5 x 5 mm)
- Environmental
 - Commercial temperature range (0°C to +70°C)
 - Industrial temperature range (-40°C to +85°C)

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UPD1002

1.0 INTRODUCTION

1.1 General Description

The UPD1002 is a USB Power Delivery (PD) controller designed to adhere to the *USB Power Delivery Specification*. USB Power Delivery allows a host (or device) to provide or consume up to 5 Amps and/or up to 20 Volts of power from a USB PD capable partner device on the other end of the USB cable. USB PD capable standard and custom cables/connectors are supported, which in most cases are backward compatible with standard USB connections.

The UPD1002 provides a complete USB Power Delivery solution for notebooks/ultrabooks, desktop PCs, monitors, and docking stations, (see [Table 1-1, “UPD1002 Package/Pin Configuration Summary,” on page 6](#) for available configurations and corresponding applications). The functionality of the UPD1002 is selected via two configuration selection pins, **CFG_SEL0** and **CFG_SEL1**, which can be used to select unique PD and system configurations. Designing the UPD1002 into a system can be as simple as selecting a configuration, with no external EEPROM required. Advanced programmability options exist with an external EEPROM installed.

The integrated USB Power Delivery MAC and PHY support provider and consumer operation via the PD communication protocol, as specified in Revision 1.0 (Version 1.2) of the *USB Power Delivery Specification*. Monitoring of VBUS and battery charging is accomplished via the integrated voltage and current ADC inputs. The PHY supports cable ID detection/identification and loopback modes. The PHY includes a 24MHz FSK modulator/demodulator and provides integrated terminations. The USB PD MAC supports both USB PD insertion detection (cold socket) and dead battery cases. The device provides an integrated voltage switch which is used to detect whether the VBUS or VTR (battery) power supply is active, enabling selection of the appropriate power supply at any given time.

The on-chip microcontroller manages the IOs and implements the power delivery local policy engine and device manager. The SPI ROM controller is used by the microcontroller for optional external code execution from ROM. A One Time Programmable (OTP) ROM is integrated in the UPD1002. Integrated 3.3 V and 1.8 V regulators allow device operation from a single power supply. The UPD1002 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the UPD1002 is shown in [Figure 1-1](#).

Power Delivery applications introduce two different types of USB ports. The Upstream Facing Port (UFP) and the Downstream Facing Port (DFP). The UFP and DFP have different usages and attributes due to the nature of their use cases, as detailed below. For a list of available UPD1002 configurations and corresponding target applications, refer to [Table 1-1, “UPD1002 Package/Pin Configuration Summary,” on page 6](#).

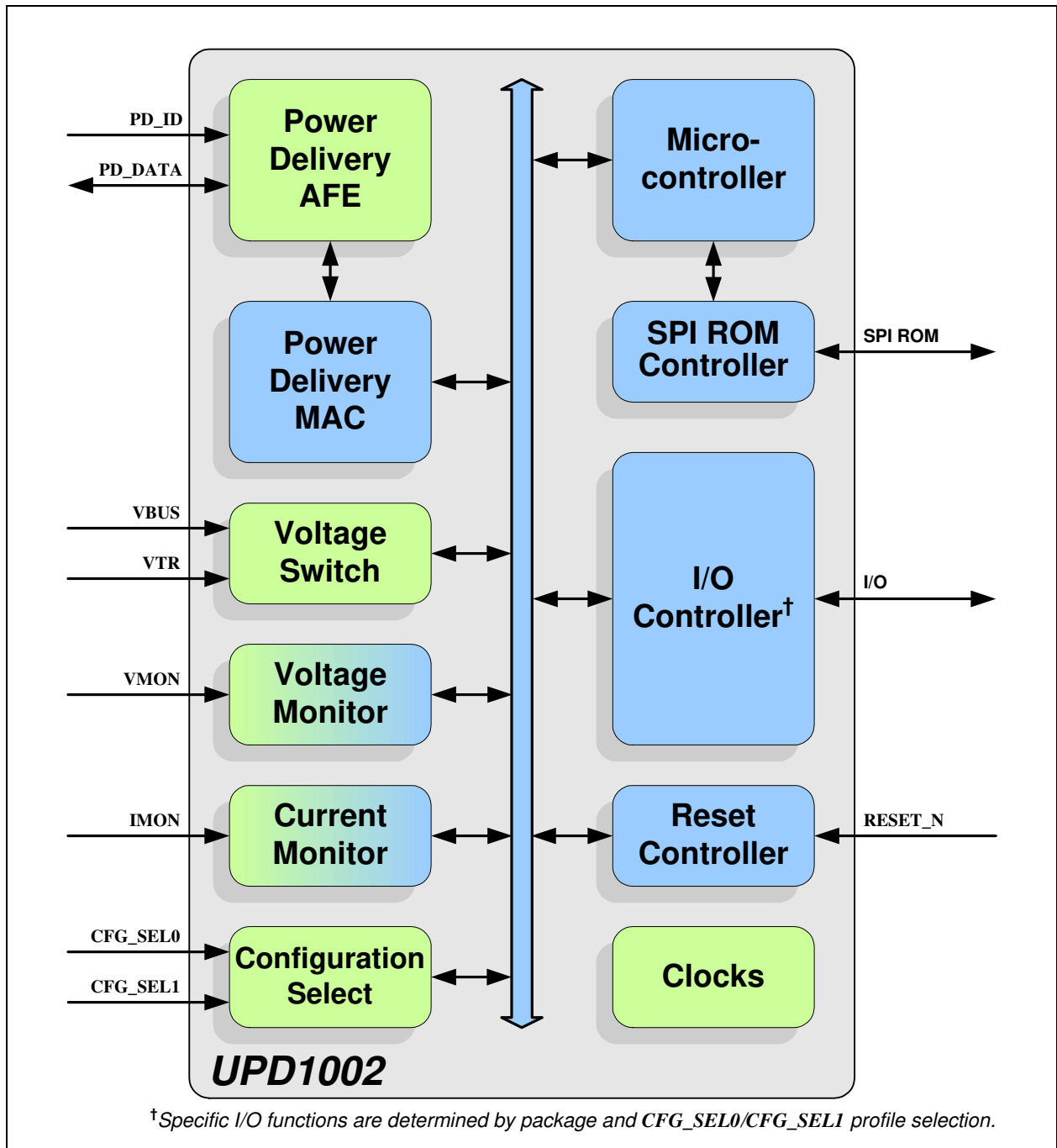
The Upstream Facing Port (UFP)

The primary use case of the UFP is to connect to a host computer. In this case, the UFP of the UPD1002 must have a Standard-B (STD-B) USB connector to connect to the host's Standard-A (STD-A) USB connector. If the host is a notebook/ultrabook, it may request to be charged from the UPD1002 UFP, requiring the system to be wall powered instead of bus-powered. In this case, the UFP must offer a Consumer/Provider role.

The Downstream Facing Port (DFP)

The primary use case of the DFP is to connect to other downstream USB devices such as speakers, keyboard, mice, scanners, external hard drives, external optical drives, printers, etcetera. These devices are mainly Consumers in nature in the first phase of adoption. DFPs are Providers by default and have Standard-A USB connectors. Battery Charging 1.2 support can be provided by a parallel USB hub or a Microchip UCS100x or other enhanced port power controller device.

FIGURE 1-1: INTERNAL BLOCK DIAGRAM



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The UPD1002 is offered in a 32-pin SQFN package. The package provides multiple pin configurations, based upon the **CFG_SEL0** and **CFG_SEL1** Configuration Select signals. [Table 1-1](#) summarizes the available pin combinations and their target applications. Refer to [Section 2.0, "Pin Descriptions and Configuration,"](#) on page 7 for detailed information on specific pin configurations.

TABLE 1-1: UPD1002 PACKAGE/PIN CONFIGURATION SUMMARY

| Package | Pin Config. Name | DFP/UFP | PD Role | USB Receptacle | Target Applications | Notes |
|---------|------------------|---------|-------------------|--------------------|--|--|
| 32-SQFN | 32-P_A | DFP | Provider | Standard-A (STD-A) | <ul style="list-style-type: none">• Monitors• Docking stations• Desktop PCs• Printers | See Section 2.1 |
| | 32-CP_B | UFP | Consumer/Provider | Standard-B (STD-B) | <ul style="list-style-type: none">• Monitors• Docking stations• Printers | See Section 2.1 |
| | 32-PC_A | DFP | Provider/Consumer | Standard-A (STD-A) | <ul style="list-style-type: none">• Notebooks | See Section 2.1 No VSEL _x _N |
| | 32-PC_uAB | DFP | Provider/Consumer | Micro-AB (uAB) | <ul style="list-style-type: none">• Notebooks• Ultrabooks | See Section 2.1 No VSEL _x _N |

2.0 PIN DESCRIPTIONS AND CONFIGURATION

The pinouts for the package, along with system-level application diagrams, are detailed in the following section:

- [32-Pin SQFN \(32-SQFN\)](#)

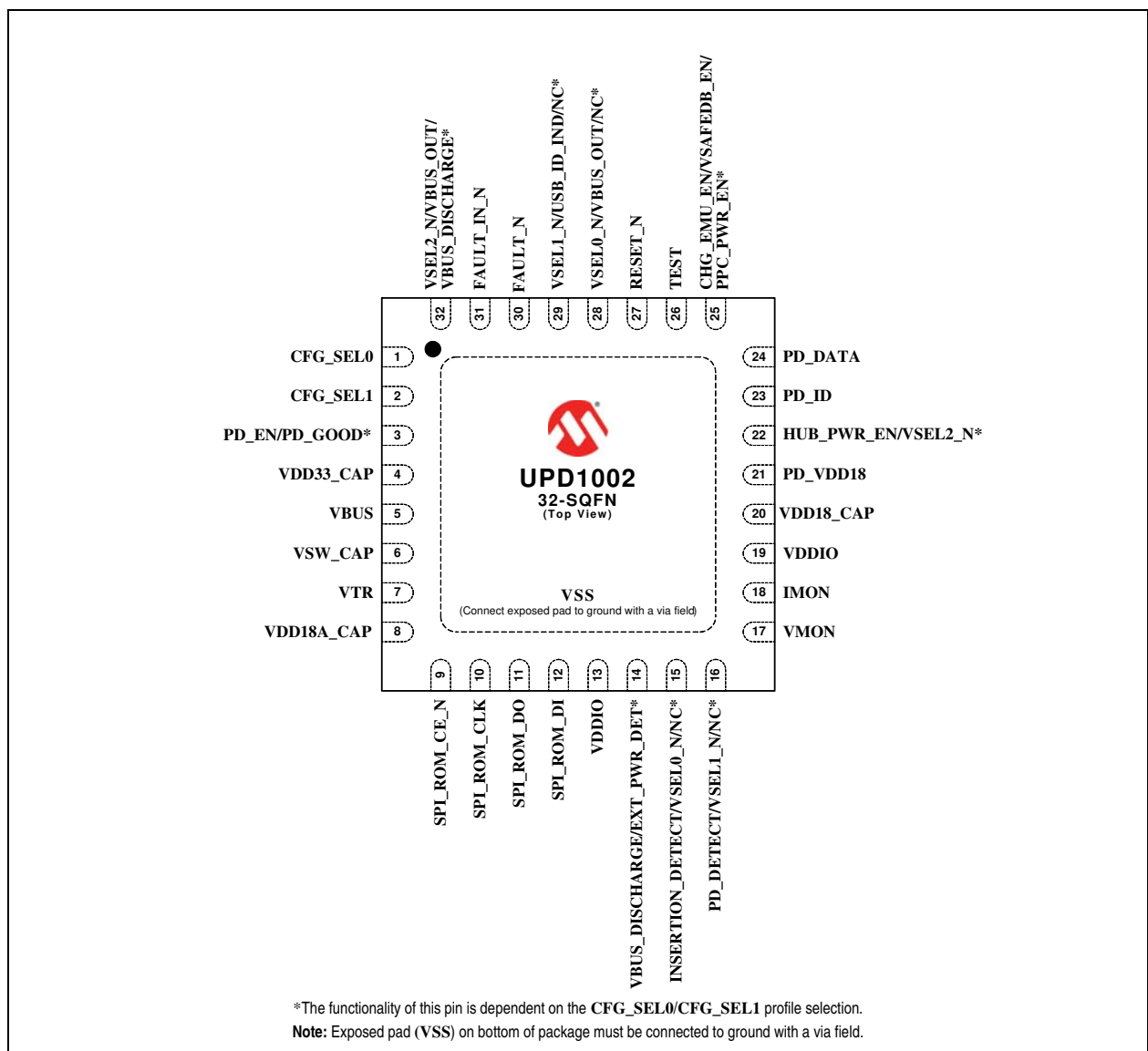
Note: For a summary of the available pin combinations and their corresponding target applications, refer to [Table 1-1](#).

Pin descriptions are detailed in [Section 2.2, "Pin Descriptions," on page 14](#). For details on the **CFG_SEL0** and **CFG_SEL1** Configuration Select signals, refer to [Section 3.3, "Configuration Selection \(CFG_SEL0/CFG_SEL1\)," on page 24](#).

2.1 32-Pin SQFN (32-SQFN)

2.1.1 32-SQFN PIN DIAGRAM

FIGURE 2-1: 32-SQFN PIN ASSIGNMENTS (TOP VIEW)



Note: When an “_N” is used at the end of the signal name, it indicates that the signal is active low. For example, **RESET_N** indicates that the reset signal is active low.

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Note: The buffer type for each signal is indicated in the BUFFER TYPE column of [Table 2-2, "Pin Descriptions"](#). A description of the buffer types is provided in [Section 2.3, "Buffer Types"](#).

2.1.2 32-SQFN PIN ASSIGNMENTS

The UPD1002 32-SQFN provides four distinct pin configurations (32-P_A, 32-CP_B, 32-PC_A, and 32-PC_uAB) based upon the CFG_SEL0 and CFG_SEL1 Configuration Select signals. These configurations are designed for specific applications, as outlined in [Table 1-1, "UPD1002 Package/Pin Configuration Summary,"](#) on page 6. The 32-SQFN package pin assignments for each configuration are detailed in [Table 2-1](#). For pin descriptions, refer to [Section 2.2, "Pin Descriptions"](#). For example connection diagrams, refer to [Section 2.4, "Power Connection Diagram,"](#) on page 22. For information on the Configuration Select signals, refer to [Section 3.3, "Configuration Selection \(CFG_SEL0/CFG_SEL1\)"](#).

TABLE 2-1: 32-SQFN PACKAGE PIN ASSIGNMENTS

| Pin Number | Configuration 32-P_A Pin Name | Configuration 32-CP_B Pin Name | Configuration 32-PC_A Pin Name | Configuration 32-PC_uAB Pin Name |
|------------|----------------------------------|-----------------------------------|-----------------------------------|-------------------------------------|
| 1 | CFG_SEL0 | | | |
| 2 | CFG_SEL1 | | | |
| 3 | PD_EN | PD_EN | PD_GOOD | PD_GOOD |
| 4 | VDD33_CAP | | | |
| 5 | VBUS | | | |
| 6 | VSW_CAP | | | |
| 7 | VTR | | | |
| 8 | VDD18A_CAP | | | |
| 9 | SPI_ROM_CE_N | | | |
| 10 | SPI_ROM_CLK | | | |
| 11 | SPI_ROM_DO | | | |
| 12 | SPI_ROM_DI | | | |
| 13 | VDDIO | | | |
| 14 | VBUS_DISCHARGE | VBUS_DISCHARGE | EXT_PWR_DET | EXT_PWR_DET |
| 15 | INSERTION_DETECT | VSEL0_N | INSERTION_DETECT | NC |
| 16 | PD_DETECT | VSEL1_N | PD_DETECT | NC |
| 17 | VMON | | | |
| 18 | IMON | | | |
| 19 | VDDIO | | | |
| 20 | VDD18_CAP | | | |
| 21 | PD_VDD18 | | | |
| 22 | HUB_PWR_EN | VSEL2_N | HUB_PWR_EN | HUB_PWR_EN |
| 23 | PD_ID | | | |
| 24 | PD_DATA | | | |
| 25 | CHG_EMU_EN | VSAFEDB_EN | PPC_PWR_EN | PPC_PWR_EN |
| 26 | TEST | | | |
| 27 | RESET_N | | | |

TABLE 2-1: 32-SQFN PACKAGE PIN ASSIGNMENTS (CONTINUED)

| Pin Number | Configuration 32-P_A Pin Name | Configuration 32-CP_B Pin Name | Configuration 32-PC_A Pin Name | Configuration 32-PC_uAB Pin Name |
|-------------------|--|---|---|---|
| 28 | VSEL0_N | NC | NC | VBUS_OUT |
| 29 | VSEL1_N | NC | NC | USB_ID_IND |
| 30 | FAULT_N | | | |
| 31 | FAULT_IN_N | | | |
| 32 | VSEL2_N | VBUS_OUT | VBUS_DISCHARGE | VBUS_DISCHARGE |
| Exposed Pad | VSS | | | |

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2.1.3 32-SQFN SYSTEM LEVEL DIAGRAMS

Figure 2-2, Figure 2-3, Figure 2-4, and Figure 2-5 provide typical system level diagrams of the UPD1002 for configurations 32-P_A, 32-CP_B, 32-PC_A, and 32-PC_uAB, respectively.

FIGURE 2-2: CONFIGURATION 32-P_A SYSTEM-LEVEL DIAGRAM

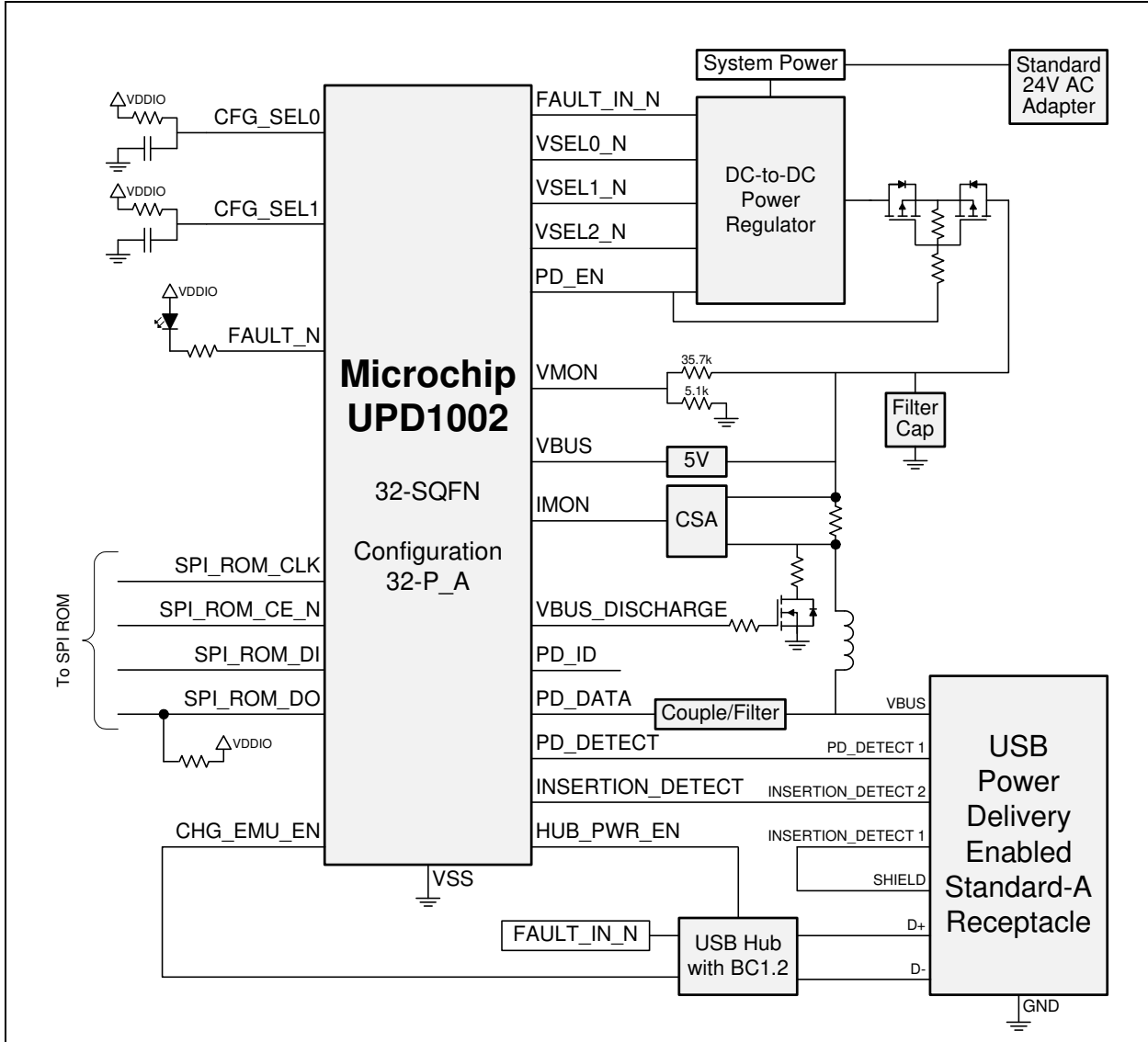
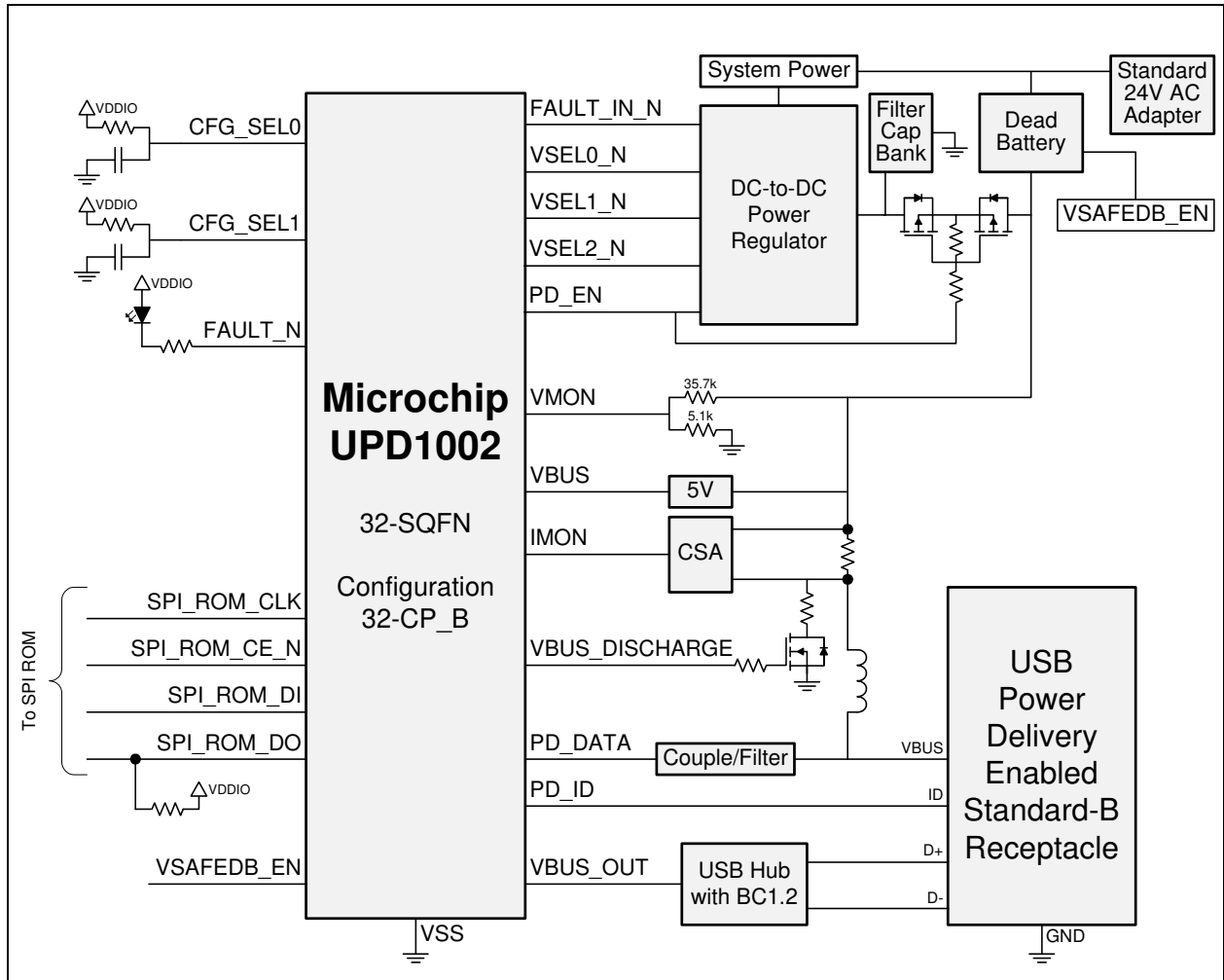


FIGURE 2-3: CONFIGURATION 32-CP_B SYSTEM-LEVEL DIAGRAM



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FIGURE 2-4: CONFIGURATION 32-PC_A SYSTEM-LEVEL DIAGRAM

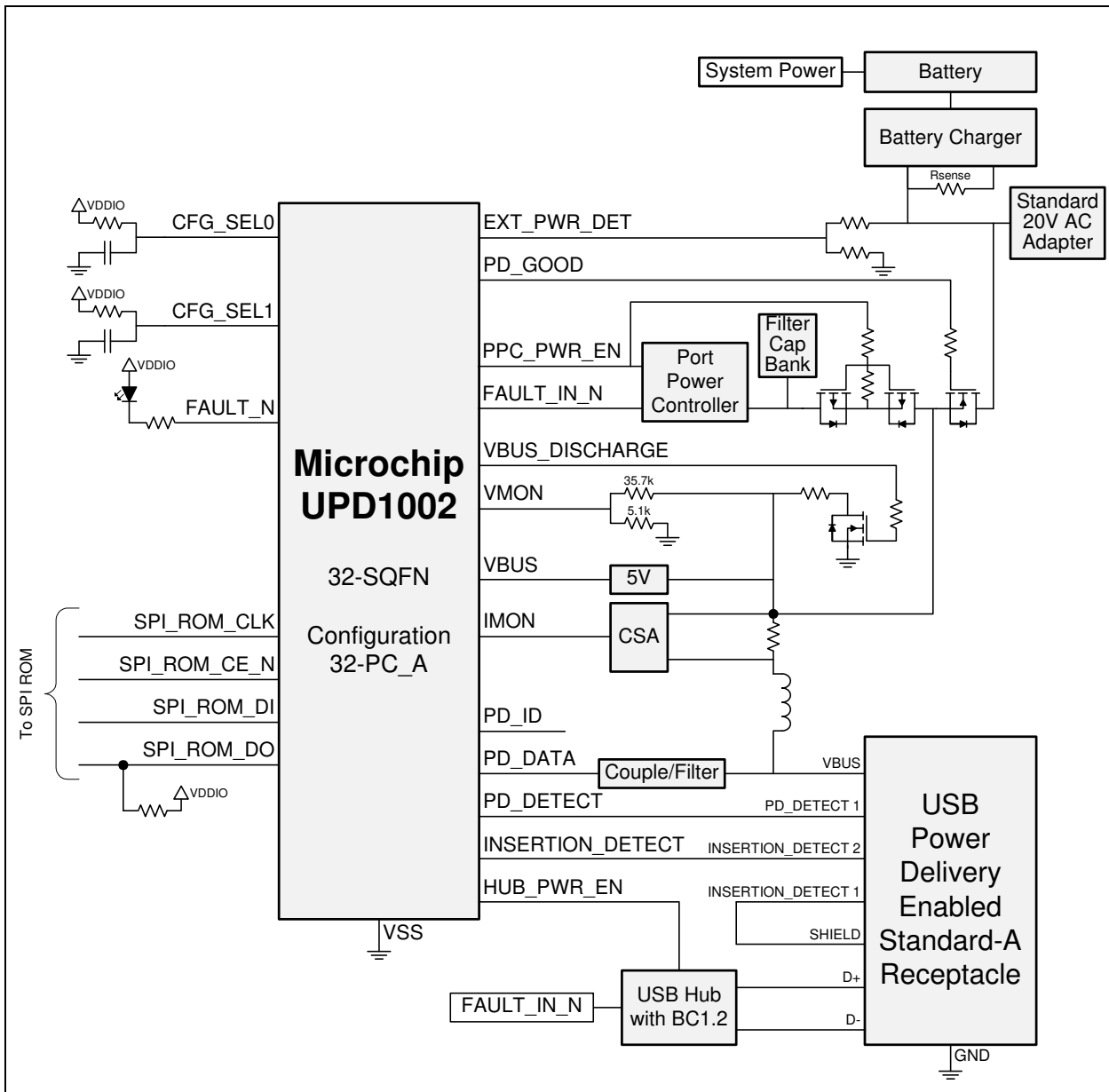
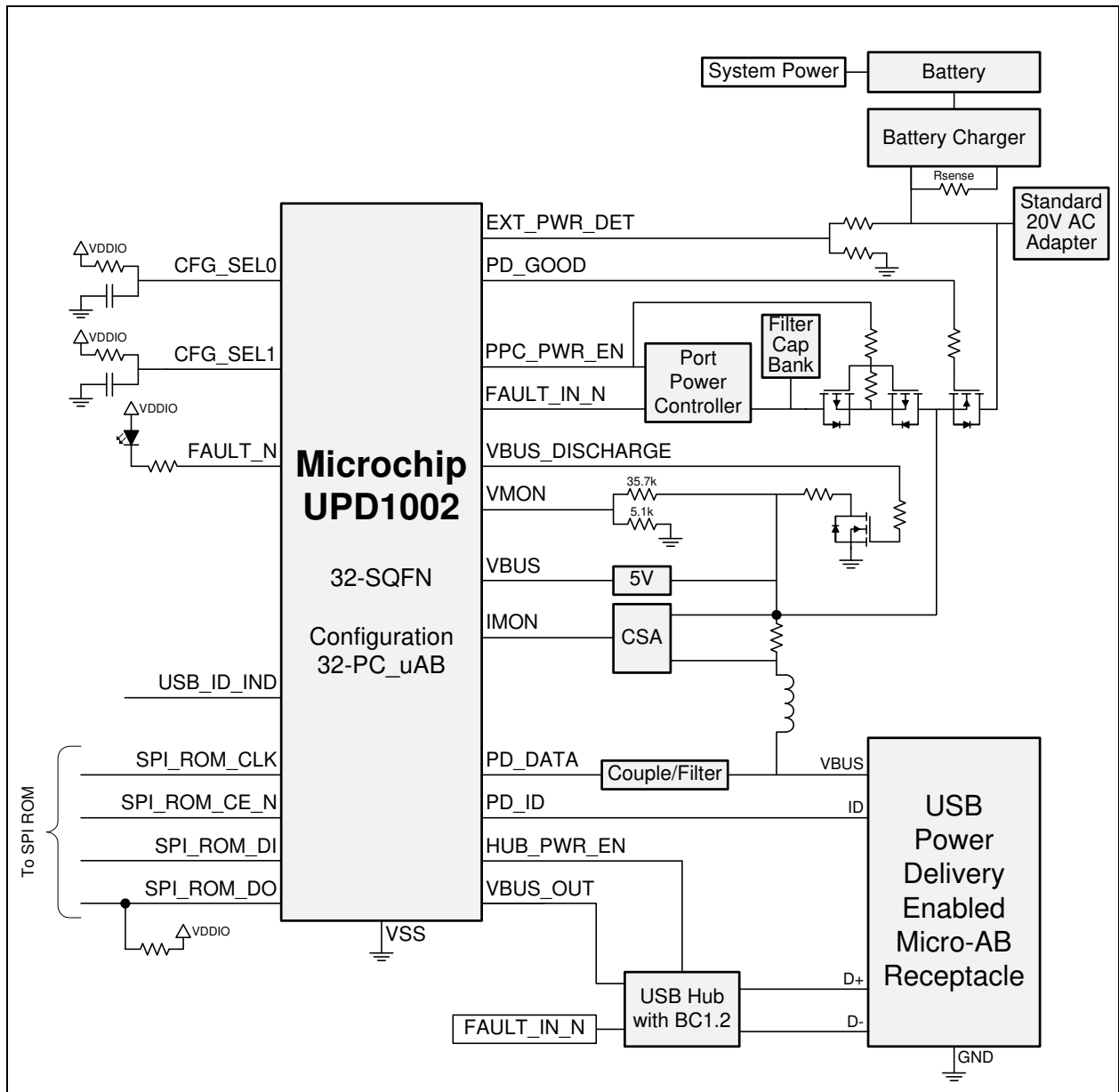


FIGURE 2-5: CONFIGURATION 32-PC_uAB SYSTEM-LEVEL DIAGRAM



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2.2 Pin Descriptions

TABLE 2-2: PIN DESCRIPTIONS

| Name | Symbol | Buffer Type | Description |
|-------------------------------------|------------------|-------------|---|
| Power Delivery | | | |
| Power Delivery Cable ID | PD_ID | AIO | USB connector signal used to indicate a high-current power delivery capable cable is inserted. This signal is to be connected to the PD_ID pin located on the USB PD Standard-B receptacle. |
| Power Delivery VBUS Data | PD_DATA | AIO | Modulated power delivery VBUS data. Requires in-line isolation filter. Reference schematic available on request. |
| Power Delivery Detect | PD_DETECT | IS (PU) | This signal is to be connected to the PD DETECT pins located on the USB PD Standard-A receptacle. This signal is pulled high via an internal pull-up resistor by default. Assertion (low value) of PD_DETECT qualifies a USB-PD plug detection event. |
| Power Delivery Enable (Active High) | PD_EN | O8 | This active high signal is used to drive the enable pin of the DC-to-DC solution direction directly. Alternatively, this signal may be used to drive an N-channel MOSFET into cutoff and isolate the input power of the DC-to-DC solution. Note: This function is only available in specific device configurations. |
| Power Delivery Good | PD_GOOD | O8 | This active high signal is asserted whenever a valid USB power delivery contract has been established and the device is operating as a sink in a configuration other than VSafe5V-0A. A valid contract is defined as a PD contract that matches one of the supported PD consumer/provider profiles, as determined by the CFG_SEL0/CFG_SEL1 configuration. When there is no valid contract established, this signal de-asserts. Note: This signal will not be asserted, or become de-asserted, if the VBUS voltage is not within the desired range, as determined by the VMON voltage monitoring (despite a contract being established). Note: This function is only available in specific device configurations. |
| Miscellaneous | | | |
| VBUS Voltage Monitor | VMON | AI | Stepped down voltage representation of the VBUS voltage. This signal must be connected to a voltage divider circuit as specified in Section 2.4, "Power Connection Diagram," on page 22 . Voltage must not exceed 5 V on this signal. Refer to Section 3.4, "Voltage/Current Monitors (VMON/IMON)," on page 29 for additional information. |

TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

| Name | Symbol | Buffer Type | Description |
|---|------------|-------------|---|
| Charger Current Monitor | IMON | AI | Voltage representation of the charger current. This signal should be fed by a current sense amplifier tuned to output 3.0 V when 6.0 A is flowing on VBUS. Voltage must not exceed 5 V on this signal. Refer to Section 3.4, "Voltage/Current Monitors (VMON/IMON)," on page 29 for additional information. |
| Power Supply Fault Indicator | FAULT_N | OD8 | This active low signal can be connected to an external LED or SoC and is used by the device to indicate power supply exceptions/failures as determined by the integrated voltage/current monitors. Refer to Section 3.4, "Voltage/Current Monitors (VMON/IMON)," on page 29 for additional information. |
| Fault Input | FAULT_IN_N | IS | <p>This active low signal is asserted by the power supplying device (DC to DC controller or port power controller) to notify the device when a system fault condition has occurred. Typically, this signal is used for overcurrent or overvoltage conditions, but it can be used for any system related failure. This signal should be debounced to 1 ms.</p> <p>Note: The board design must ensure this signal is in a valid state by the time PPC_PWR_EN or PD_GOOD asserts.</p> |
| Power Delivery Profile Configuration Selector 0 | CFG_SEL0 | AIO | This pin is used in conjunction with CFG_SEL1 to select the power delivery profile of the device via an externally connected RC circuit. Refer to Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)" for additional information. |
| Power Delivery Profile Configuration Selector 1 | CFG_SEL1 | AIO | This pin is used in conjunction with CFG_SEL0 to select the power delivery profile of the device via an externally connected RC circuit. Refer to Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)" for additional information. |

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TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

| Name | Symbol | Buffer Type | Description |
|-------------------------|---------|-------------|--|
| Source Voltage Select 0 | VSEL0_N | OD8 | <p>This active low signal is one in a series of output pins (VSEL0_N, VSEL1_N, and VSEL2_N) used to select the correct source voltage from the DC-to-DC solution. Each VSELx_N pin is dedicated to one voltage, assigned in order of increasing supported voltage.</p> <p>For example, if 5, 12 and 20 V capabilities are supported, the VSELx_N selections will be as follows:</p> <p>VSEL0_N = 5 V VSEL1_N = 12 V VSEL2_N = 20 V</p> <p>In another example, if only 5 and 20 V are supported, the VSELx_N selections will be as follows:</p> <p>VSEL0_N = 5 V VSEL1_N = 20 V VSEL2_N = RESERVED</p> <p>The VSELx_N pins are also used to set the overvoltage protection (OVP) voltage on the VMON pin. The OVP fault will trigger when the measured voltage on VMON is 10% above the selected voltage setting.</p> <p>For a mapping of the VSELx_N voltage assignments for each CFG_SEL1/CFG_SEL0 configuration profile, refer to Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)," on page 24.</p> <p>Note: This function is only available in specific device configurations.</p> |
| Source Voltage Select 1 | VSEL1_N | OD8 | <p>This active low signal is one in a series of output pins (VSEL0_N, VSEL1_N, and VSEL2_N) used to select the correct source voltage from the DC-to-DC solution. Each VSELx_N pin is dedicated to one voltage, assigned in order of increasing supported voltage.</p> <p>Refer to the VSEL0_N definition for additional information.</p> <p>Note: This function is only available in specific device configurations.</p> |
| Source Voltage Select 2 | VSEL2_N | OD8 | <p>This active low signal is one in a series of output pins (VSEL0_N, VSEL1_N, and VSEL2_N) used to select the correct source voltage from the DC-to-DC solution. Each VSELx_N pin is dedicated to one voltage, assigned in order of increasing supported voltage.</p> <p>Refer to the VSEL0_N definition for additional information.</p> <p>Note: This function is only available in specific device configurations.</p> |

TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

| Name | Symbol | Buffer Type | Description |
|------------------|-----------------------|-------------|---|
| VBUS Discharge | VBUS_DISCHARGE | O8 | This active high output is used to drive a power NFET to discharge VBUS during high-to-low voltage transitions in order to achieve vSafe0V. When asserted, the external MOSFET should conduct to GND through a current limiting resistor. This signal de-asserts when the VMON signal voltage reaches a preset value (a percentage of the destination voltage). |
| VBUS Out | VBUS_OUT | O8 | <p>This active high output is used on an Upstream Facing Port (UFP) to tell the hub to stay connected. This signal will remain asserted at all times that a valid VBUS level is present (VBUS minimum of 4.5 V to PD VBUS maximum 20 V+10%) on the UFP, as well as during any voltage transitions or role swaps where the voltage may drop below 4.5V.</p> <p>Note: Per the OTG specification, data connectivity roles can be swapped and a micro-AB connector with a micro-A plug inserted can operate as an “upstream” port (as a device). Therefore, VBUS_OUT assertion behavior as per above is not only valid with a micro-B cable, but also a micro-A cable so that the USB data link is not lost during PD swaps.</p> <p>Note: This function is only available in specific device configurations.</p> |
| USB ID Indicator | USB_ID_IND | O8 | This signal is used in micro-AB pinouts to indicate to the OTG host whether a micro-A plug (Legacy, Low Power or PD) is present. If a micro-A plug is present, this pin is low. Otherwise it is high. |
| Emulation Enable | CHG_EMU_EN | O8 | <p>This active high output signal can be used to drive the Emulation Enable pin of a Microchip UCS1001 or similar device that supports BC 1.2. The device will assert this signal whenever operating at VSafe5V without a PD contract. Whenever a PD contract is established (even at 5 V), this signal is de-asserted.</p> <p>Note: This function is only available in specific device configurations.</p> |

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TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

| Name | Symbol | Buffer Type | Description |
|------------------------------|------------------|-------------|---|
| Insertion Detect | INSERTION_DETECT | IS (PU) | <p>This active low input signal should be connected to the Insertion Detect pin on the USB Standard-A (STD-A) receptacle. This signal is pulled high via an internal pull-up resistor by default. Assertion (low value) qualifies a STD-A plug insertion event and triggers transition out of the “Startup” state of the Source Policy engine. The device firmware implements cold socket detection using the INSERTION_DETECT signal. Even when operating as a provider, if the signal is high, the device will not output voltage on VBUS. VSafe5V will only be output upon assertion of this signal (low).</p> <p>Note: Cold socket (insertion detect) is an optional feature in the USB PD specification. If this feature is not being used in a design, the INSERTION_DETECT signal must be grounded.</p> <p>Note: This function is only available in specific device configurations.</p> |
| Dead Battery Enable | VSAFEDB_EN | O8 | <p>This active high output signal is used to enable the dead battery supply on a USB Standard-B (STD-B) receptacle (consumer/provider) AC adapter. When no voltage has been detected on VBUS, this signal is asserted every 10 s to back power an attached provider/consumer and determine whether the attached device has specified to be powered per the dead battery mechanisms specified in the PD specification.</p> <p>Note: This function is only available in specific device configurations.</p> |
| External Power Source Detect | EXT_PWR_DET | IS | <p>This active high signal is used to indicate an external power source is installed. This input can be utilized as a standard digital input, or a resistive voltage divider can be used to determine if the wall power AC adapter or charger is plugged into the platform (i.e., a qualifying “Externally Powered” status has occurred, according to the USB Power Delivery Specification). In a typical application, this signal level will be set by a resistor divider of the DC barrel voltage to satisfy the device logic levels and level tolerance.</p> <p>When this signal is high, the “externally powered” bit of the VSafe5V Fixed Supply PDO for a provider will be set.</p> <p>This signal will also help determine the preferences on role swaps. Refer to Section 3.3.4, “USB Power Delivery Role Selection,” on page 26 for additional information.</p> <p>Note: This function is only available in specific device configurations.</p> |

TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

| Name | Symbol | Buffer Type | Description |
|------------------------------|---------------------|-------------|--|
| Hub Power Enable | HUB_PWR_EN | IS | <p>This active high signal is driven by either the PCH of a notebook or a downstream facing port (DFP) on a USB hub. The hub or USB host may request the port to be turned off by de-asserting this signal. Upon de-assertion, if the device is NOT operating as a sink under a PD contract, the device will de-assert the PD_EN signal to turn off VBUS to the port, which will remain off until HUB_PWR_EN asserts again.</p> <p>Note: In the case that the port supports insertion detect or has a micro-AB receptacle (which must support plug detection), the HUB_PWR_EN signal is ignored unless there is a STD-A or micro-A plug inserted.</p> <p>Note: This function is only available in specific device configurations.</p> |
| Port Power Controller Enable | PPC_PWR_EN | O8 | <p>This active high signal is used to enable an attached port power controller. It should only be used in cases in which the only source capability offered is 5 V.</p> <p>Note: In cases where the port power controller supports BC or other charging profiles, this single signal will be enabling both power sourcing as well as enabling the handshake emulation. BC handshaking will occur before PD negotiation and if in a headless/DCP charging mode, the handshake will persist even after a PD negotiation was completed successfully.</p> <p>Note: This function is only available in specific device configurations.</p> |
| System Reset | RESET_N | IS (PU) | System reset. This signal is active low. |
| Test | TEST | IS | Test signal. This signal is used for internal purposes only and must be connected to ground through a 1 K resistor for normal operation. |
| No Connect | NC | - | No connect. For proper operation, this signal must not be connected. |
| SPI ROM Interface | | | |
| SPI ROM Clock | SPI_ROM_CLK | O8 | SPI clock output to the serial ROM |
| SPI ROM Chip Enable | SPI_ROM_CE_N | O8 | This is the active low SPI ROM chip enable output. If the SPI ROM interface is enabled, this signal should be pulled up to the SPI ROM Vcc rail. |
| SPI ROM Data In | SPI_ROM_DI | IS | SPI ROM data in |

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TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

| Name | Symbol | Buffer Type | Description |
|---|-------------------|-------------|--|
| SPI ROM Data Out | SPI_ROM_DO | O8 (PD) | SPI ROM data out Note: This signal must be pulled-up to VDDIO with an external 10 kΩ resistor for proper operation. |
| Power/Ground | | | |
| VTR Supply Input | VTR | P | +3.3 to +5.0 V main power supply input. This signal must be connected to a 2.2 μF capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| +3.3 to +5.0 V Variable Voltage I/O Power | VDDIO | P | +3.3 V to +5.0 V variable I/O power supply input. Refer to Figure 2-6 for additional power connection information. Note: When using internal +3.3 V regulator, these pins must be externally connected to VDD33_CAP . |
| +5.0 V VBUS Input | VBUS | P | +5.0 V VBUS input. This signal provides power in the dead battery case. This signal must be connected to a 2.2 μF capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| +1.8V Power Delivery | PD_VDD18 | P | +1.8 V power for Power Delivery PHY. Refer to Figure 2-6 for additional power connection information. Note: This pin must be connected to VDD18_CAP pin externally when using the internal VDD18 regulator. |
| +1.8 V Power Capacitance | VDD18_CAP | P | This pin is used to provide capacitance for the integrated +1.8 V regulator and must be connected to a 1 μF (<100 mΩ ESR) capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| +1.8 V Analog Power Capacitance | VDD18A_CAP | P | This pin is used to provide capacitance for the integrated +1.8 V analog regulator and must be connected to a 1 μF (<100 mΩ ESR) capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| +3.3 V Power Capacitance | VDD33_CAP | P | +3.3 V regulator output. This pin must be connected to a 1 μF (<100 mΩ ESR) capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| Integrated Power Switch Capacitance | VSW_CAP | P | This pin is used to provide capacitance for the integrated power switch and must be connected to a 1 μF (<100 mΩ ESR) capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| Ground | VSS | P | Common ground. This exposed pad must be connected to the ground plane with a via array. |

2.3 Buffer Types

TABLE 2-3: BUFFER TYPES

| Buffer Type | Description |
|-------------|--|
| IS | Schmitt-triggered input |
| O8 | Output with 8 mA sink and 8 mA source |
| OD8 | Open-drain output with 8 mA sink |
| PU | 50 μ A (typical) internal pull-up. Unless otherwise noted in the signal description, internal pull-ups are always enabled. Note: Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added. |
| PD | 50 μ A (typical) internal pull-down. Unless otherwise noted in the signal description, internal pull-downs are always enabled. Note: Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added. |
| AI | Analog input |
| AIO | Analog bi-directional |
| P | Power pin |

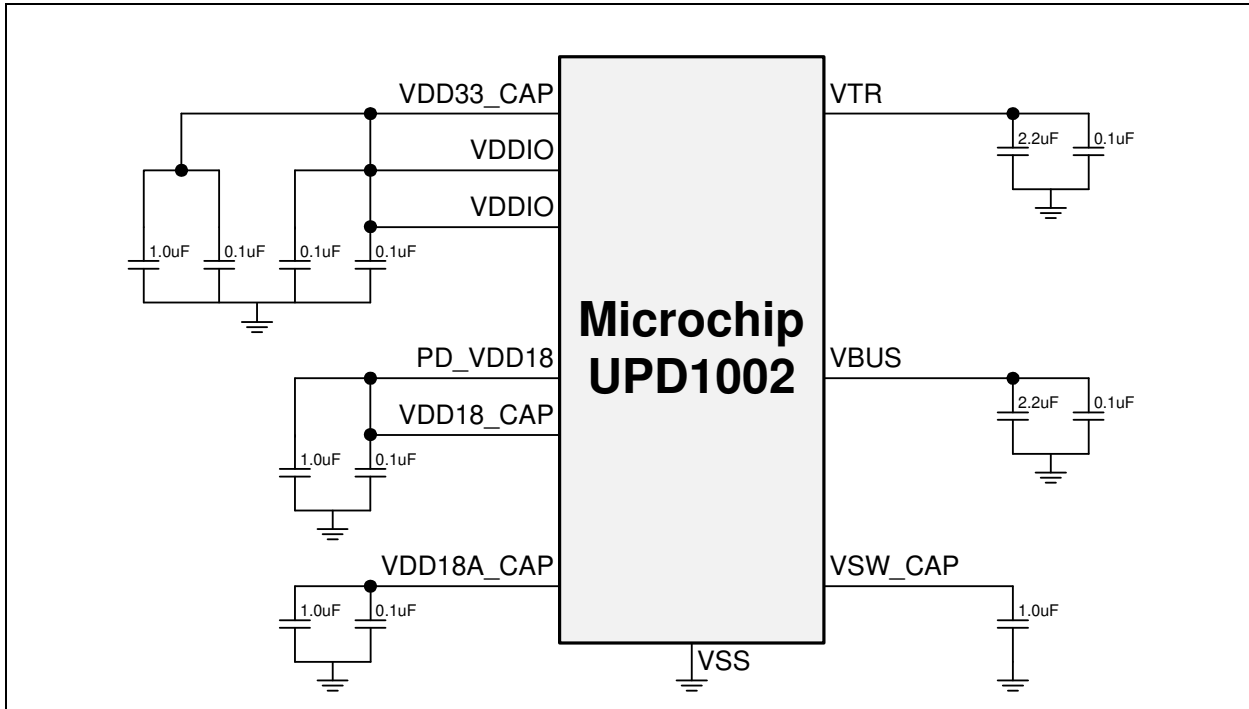
Note: All signals are 5 V tolerant.

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2.4 Power Connection Diagram

Figure 2-6 details the various power connection requirements.

FIGURE 2-6: POWER CONNECTION DIAGRAM



3.0 FUNCTIONAL DESCRIPTIONS

This chapter provides functional descriptions for the various device sub-systems:

- [Resets](#)
- [Power Management](#)
- [Configuration Selection \(CFG_SEL0/CFG_SEL1\)](#)
- [Voltage/Current Monitors \(VMON/IMON\)](#)
- [SPI ROM Controller](#)

3.1 Resets

The device includes the following reset controls:

- Power-On Reset (POR)
- External Chip Reset (**RESET_N**)

A system reset event via the external **RESET_N** pin or POR causes the following:

- All registers are set to their default values
- Pins are placed into their default state

The rising and falling Power-On Reset thresholds for each power supply are detailed in [Table 3-1](#).

TABLE 3-1: POR THRESHOLDS

| POR | Rising Threshold | Falling Threshold |
|--------------|------------------|-------------------|
| VDDIO Supply | 2.7 V | 2.35 V |
| VTR Supply | 2.85 V | 2.7 V |

After power up, the POR initially de-asserts after the Rising Threshold is passed. In the event that the supply drops below the Falling Threshold, the POR will assert. The POR stays asserted until the Rising Threshold is once again crossed.

3.2 Power Management

The device will enter low power modes based on the state of the connection to the power delivery port partner. The low power connection states are defined for the device operating as a Provider (Provider/Consumer) or a Consumer (Consumer/Provider).

The device provides the following power states:

- Provider: [Wait Insert State](#)
- Consumer: [Sink Discovery State](#)

3.2.1 PROVIDER (OR PROVIDER/CONSUMER) POWER STATE

The device Provider configuration will enter a low power mode when it is not connected to a port partner and when a Standard-A plug is not inserted in the receptacle.

3.2.1.1 Wait Insert State

In the Wait Insert State, the device utilizes the insertion detect feature to enter a standby mode when waiting for a Standard-A plug to be inserted in the receptacle. On insertion of a Standard-A plug, the device will exit from the standby mode, initiate operation by enabling the supply output to 5Vsafe, and initiate the discovery of a port partner.

3.2.2 CONSUMER (OR CONSUMER/PROVIDER) POWER STATE

The device Consumer configuration enters a standby mode when it is not connected to a provider.

3.2.2.1 Sink Discovery State

In the Sink Discovery State, the device waits for the presence of VBUS to indicate a connection to provider. The device enters a standby state when waiting for the presence of VBUS. At the presence of VBUS, the Consumer exits the standby state and resumes full operation to establish a negotiated power contract with the Provider.

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3.3 Configuration Selection (CFG_SEL0/CFG_SEL1)

The UPD1002 provides a resistor/capacitor identification detection interface which is utilized to set various device configuration parameters via the Configuration Select pins:

- CFG_SEL0
- CFG_SEL1

Each Configuration Select pin can discriminate a number of quantized RC constants. The judicious selection of RC values provides a low cost means for system element configuration identification. The Configuration Select pins measure the charge/discharge time for the RC circuit connected to it (shown in Figure 3-1), providing the ability to differentiate 16 unique “bins” for each Configuration Select pin. The resistor and capacitor values for each Configuration Select bin are defined in Table 3-2.

FIGURE 3-1: CFG_SEL0/CFG_SEL1 RESISTOR-CAPACITOR CIRCUIT CONNECTIONS

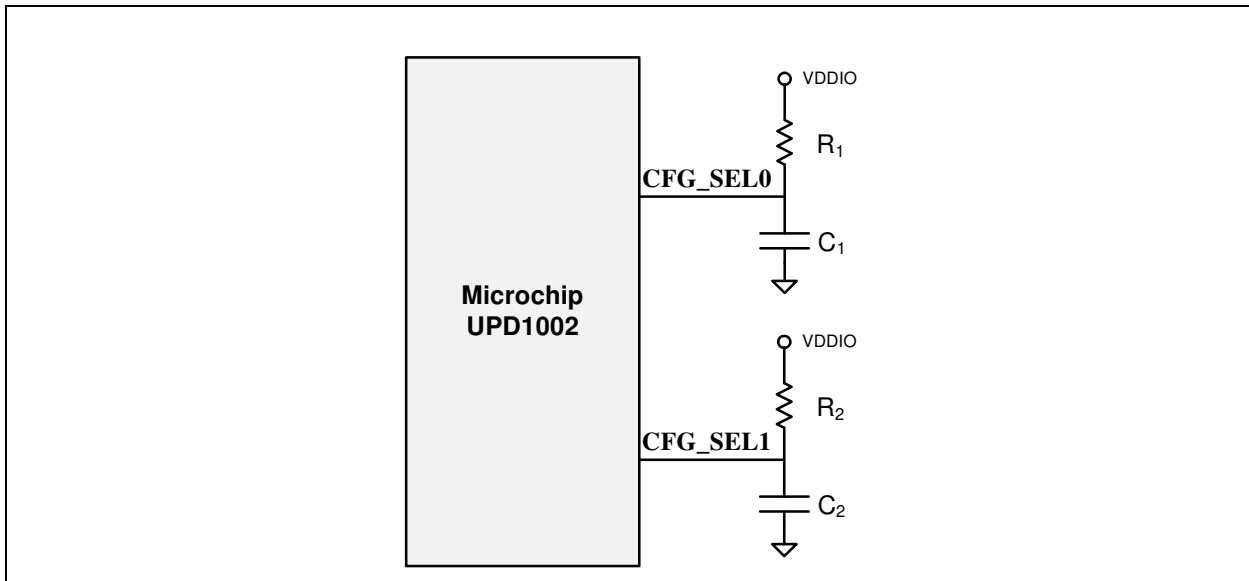


TABLE 3-2: CFG_SELX PIN RESISTOR-CAPACITOR BIN ALLOCATION

| Bin | R _x (+/-1%) | C _x (+/-5%) |
|-----|------------------------|------------------------|
| 1 | 2.70 kΩ | None |
| 2 | 2.70 kΩ | 470 pF |
| 3 | 4.87 kΩ | 470 pF |
| 4 | 8.66 kΩ | 470 pF |
| 5 | 15.40 kΩ | 470 pF |
| 6 | 2.70 kΩ | 4.7 nF |
| 7 | 4.87 kΩ | 4.7 nF |
| 8 | 8.66 kΩ | 4.7 nF |
| 9 | 15.40 kΩ | 4.7 nF |
| 10 | 2.70 kΩ | 47.0 nF |
| 11 | 4.87 kΩ | 47.0 nF |
| 12 | 8.66 kΩ | 47.0 nF |
| 13 | 15.40 kΩ | 47.0 nF |
| 14 | 2.70 kΩ | 470 nF |
| 15 | 4.87 kΩ | 470 nF |
| 16 | 8.66 kΩ | 470 nF |

Note: CFG_SEL0 and CFG_SEL1 bin definitions are identical.

By selecting specific bins on both the **CFG_SEL0** and **CFG_SEL1** pins, predefined configurations, unique to each package, may be selected. These assignments configure multiple parameters of the device, including the following:

- [Pin Configuration](#)
- [Receptacle Type](#)
- [USB Power Delivery Role Selection](#)

A list of the configuration assignments, along with the corresponding **CFG_SEL0** and **CFG_SEL1** bin settings, are detailed in the following section:

- [Section 3.3.1, "32-SQFN CFG_SELx Configuration Assignments," on page 25](#)

For details on each configurable parameter, refer to the following sub-sections.

Note: Only the bin combinations defined in the following tables are valid. All other bin combinations are reserved and must not be used.

Note: All configurations can run from either internal ROM or external SPI ROM, providing an easy design transition path from the UPD1000 with external SPI to the UPD1002 with internal ROM.

3.3.1 32-SQFN CFG_SELX CONFIGURATION ASSIGNMENTS

[Table 3-3](#) details the various 32-SQFN **CFG_SELx** configuration assignments.

TABLE 3-3: 32-SQFN CFG_SELX CONFIGURATION ASSIGNMENTS

| Config. # | Application | 32-SQFN Pin Config. | USB Receptacle Type | PD Consumer Abilities | PD Provider Abilities | VSEL0_N | VSEL1_N | VSEL2_N | CFG_SEL1 Bin | CFG_SEL0 Bin |
|-----------|-----------------------|---------------------|---------------------|-----------------------|-----------------------|---------|---------|---------|--------------|--------------|
| 1 | DFP Provider | 32-P-A | STD-A | None | Profile 1 | 5V | - | - | 3 | 1 |
| 2 | | | | | Profile 2 | 5V | 12V | - | 3 | 2 |
| 3 | | | | | Profile 3 | 5V | 12V | - | 3 | 3 |
| 4 | | | | | Profile 4 | 5V | 12V | 20V | 3 | 4 |
| 5 | | | | | Profile 5 | 5V | 12V | 20V | 3 | 5 |
| 6 | UFP Consumer/Provider | 32-CP_B | STD-B | VSafe5V-NC | 12V@1.5A | 5V | 12V | - | 3 | 6 |
| 7 | | | | | 12V@3A | 5V | 12V | - | 3 | 7 |
| 8 | | | | | 12V@5A | 5V | 12V | - | 3 | 8 |
| 9 | | | | | 20V@3A | 5V | 20V | - | 4 | 1 |
| 10 | | | | | 20V@5A | 5V | 20V | - | 4 | 2 |
| 11 | | | | | Profile 4 | 5V | 12V | 20V | 4 | 3 |
| 12 | | | | | Profile 4, PP-200 | 5V | 12V | 20V | 4 | 4 |
| 13 | | | | | Profile 5 | 5V | 12V | 20V | 4 | 5 |
| 14 | Profile 5, PP-200 | 5V | 12V | 20V | 4 | 6 | | | | |
| 15 | Provider/Consumer | 32-PC_A | STD-A | 12V@1.5A | VSafe5V-L | N/A | N/A | N/A | 1 | 1 |
| 16 | | | | 12V@3A | VSafe5V-L | N/A | N/A | N/A | 1 | 2 |
| 17 | | | | 12V@3A | Profile 1 | N/A | N/A | N/A | 1 | 3 |
| 18 | | | | 12V@3A | Profile 1, PP-200 | N/A | N/A | N/A | 1 | 4 |
| 19 | | | | 12V@5A | Profile 1 | N/A | N/A | N/A | 1 | 5 |
| 20 | | | | 12V@5A | Profile 1, PP-200 | N/A | N/A | N/A | 1 | 6 |
| 21 | | | | 20V@3A | Profile 1 | N/A | N/A | N/A | 1 | 7 |
| 22 | | | | 20V@3A | Profile 1, PP-200 | N/A | N/A | N/A | 1 | 8 |
| 23 | | | | 20V@5A | Profile 1 | N/A | N/A | N/A | 2 | 1 |
| 24 | | | | 20V@5A | Profile 1, PP-200 | N/A | N/A | N/A | 2 | 2 |