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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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User’s Manual

V850E/IF3, V850E/IG3

32-bit Single-Chip Microcontrollers

Hardware

V850E/IF3:
μPD70F3451
μPD70F3452
V850E/IG3:
μPD70F3453
μPD70F3454

Document No. U18279EJ3V0UD00 (3rd edition)
Date Published March 2010 N

[MEMO]

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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PREFACE

Readers

This manual is intended for users who wish to understand the functions of the V850E/IF3 (μPD70F3451, 70F3452) and V850E/IG3 (μPD70F3453, 70F3454) and design application systems using the V850E/IF3 and V850E/IG3.

Purpose

This manual is intended to give users an understanding of the hardware functions of the V850E/IF3 and V850E/IG3 shown in the **Organization** below.

Organization

This manual is divided into two parts: Hardware (this manual) and Architecture (**V850E1 Architecture User's Manual**).

Hardware

- Pin functions
- CPU function
- On-chip peripheral functions
- Flash memory programming
- Electrical specifications

Architecture

- Data types
- Register set
- Instruction format and instruction set
- Interrupts and exceptions
- Pipeline operation

How to Read This Manual

It is assumed that the readers of this manual have general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

To understand the overall functions of the V850E/IF3 and V850E/IG3
→ Read this manual according to the **CONTENTS**.

To find the details of a register where the name is known
→ See **APPENDIX B REGISTER INDEX**.

Register format
→ The name of the bit whose number is in angle brackets (<>) in the figure of the register format of each register is defined as a reserved word in the device file.

To understand the details of an instruction function
→ Refer to the **V850E1 Architecture User's Manual**.

To know the electrical specifications of the V850E/IF3 and V850E/IG3
→ See **CHAPTER 28 ELECTRICAL SPECIFICATIONS**.

The "yyy bit of the xxx register" is described as the "xxx.yyy bit" in this manual. Note with caution that even if "xxx.yyy" is described as is in a program, however, the compiler/assembler cannot recognize it correctly.

The mark “<R>” shows major revised points. The revised points can be easily searched by copying an “<R>” in the PDF file and specifying it in the “Find what:” field.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)	
Memory map address:	Higher addresses on the top and lower addresses on the bottom	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numeric representation:	Binary	... xxxx or xxxxB
	Decimal	... xxxx
	Hexadecimal	... xxxxH
Prefix indicating power of 2 (address space, memory capacity):		
	K (kilo):	$2^{10} = 1,024$
	M (mega):	$2^{20} = 1,024^2$
	G (giga):	$2^{30} = 1,024^3$
Data type:	Word	… 32 bits
	Halfword	… 16 bits
	Byte	… 8 bits

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850E/IF3 and V850E/IG3

Document Name	Document No.
V850E1 Architecture User's Manual	U14559E
V850E/IF3, V850E/IG3 Hardware User's Manual	This manual
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTA) Application Note	U18723E
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTB) Application Note	U18724E
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (CSIB) Application Note	U18725E
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (I^2C) Application Note	U18726E
V850E/IF3, V850E/IG3 Sample Programs for DMA Function Application Note	U18727E
V850E/IF3, V850E/IG3 Sample Programs for Timer M Application Note	U18728E
V850E/IF3, V850E/IG3 Sample Programs for Watchdog Timer Application Note	U18729E
V850E/IF3, V850E/IG3 Sample Programs for Timer AA Application Note	U18730E
V850E/IF3, V850E/IG3 Sample Programs for Timer AB Application Note	U18731E
V850E/IF3, V850E/IG3 Sample Programs for Timer T Application Note	U18732E
V850E/IF3, V850E/IG3 Sample Programs for Port Function Application Note	U18733E
V850E/IF3, V850E/IG3 Sample Programs for Clock Generator Application Note	U18734E
V850E/IF3, V850E/IG3 Sample Programs for Standby Function Application Note	U18735E
V850E/IF3, V850E/IG3 Sample Programs for Interrupt Function Application Note	U18736E
V850E/IF3, V850E/IG3 Sample Programs for A/D Converters 0 and 1 Application Note	U18737E
V850E/IF3, V850E/IG3 Sample Programs for A/D Converter 2 Application Note	U18738E
V850E/IF3, V850E/IG3 Sample Programs for Low-Voltage Detector (LVI) Function Application Note	U18739E
V850E/IF3, V850E/IG3 6-Phase PWM Output Control by Timer AB, Timer Q Option, Timer AA, A/D Converters 0, 1 Application Note	U18717E

Documents related to development tools (user's manuals)

Document Name		Document No.
QB-V850EIX3 In-Circuit Emulator		U18651E
QB-V850MINI On-Chip Debug Emulator		U17638E
QB-MINI2 On-Chip Debug Emulator with Programming Function		U18371E
QB-Programmer Programming GUI	Operation	U18527E
CA850 Ver. 3.20 C Compiler Package	Operation	U18512E
	C Language	U18513E
	Assembly Language	U18514E
	Link Directives	U18515E
PM+ Ver. 6.30 Project Manager		U18416E
ID850QB Ver. 3.40 Integrated Debugger	Operation	U18604E
TW850 Ver. 2.00 Performance Analysis Tuning Tool		U17241E
SM+ System Simulator	Operation	U18601E
	User Open Interface	U18212E
RX850 Ver. 3.20 Real-Time OS	Basics	U13430E
	Installation	U17419E
	Technical	U13431E
	Task Debugger	U17420E
RX850 Pro Ver. 3.21 Real-Time OS	Basics	U18165E
	In-Structure	U18164E
	Task Debugger	U17422E
AZ850 Ver. 3.30 System Performance Analyzer		U17423E
PG-FP4 Flash Memory Programmer		U15260E
PG-FP5 Flash Memory Programmer		U18865E

CONTENTS

CHAPTER 1 INTRODUCTION

The V850E/IF3 and V850E/IG3 are products of the NEC Electronics V850 single-chip microcontrollers. This chapter gives an outline of the V850E/IF3 and V850E/IG3.

1.1 Overview

The V850E/IF3 and V850E/IG3 are 32-bit single-chip microcontrollers that use the V850E1 CPU core and incorporate ROM/RAM and various peripheral functions such as DMA controller, timer/counter, watchdog timer, serial interfaces, A/D converter, and on-chip debug function.

In addition to high real-time response characteristics and 1-clock-pitch basic instructions, the V850E/IF3 and V850E/IG3 feature instructions such as multiply instructions, saturated operation instructions, and bit manipulation instructions realized by a hardware multiplier, as optimum instructions for digital servo control applications. Moreover, as a real-time control system, the V850E/IF3 and V850E/IG3 enable an extremely high cost-performance for applications such as motor inverter control.

Table 1-1 lists the V850E/IF3 and V850E/IG3 products.

Table 1-1. V850E/IF3, V850E/IG3 Product List

Function / Part Number		Package	ROM		RAM Size	Operating Frequency (MAX.)	Maskable Interrupt		Non-Maskable Interrupt
			Type	Size			External	Internal	
V850E/IF3	μPD70F3451	80GC	Flash memory	128 KB	8 KB	64 MHz	15	73	1
	μPD70F3452	80GC		256 KB	12 KB				
V850E/IG3	μPD70F3453	100GC		128 KB	8 KB		21	74	
	μPD70F3453	100GF		128 KB	8 KB				
	μPD70F3454	100GC		256 KB	12 KB				
	μPD70F3454	100GF		256 KB	12 KB				
	μPD70F3454	161F1		256 KB	12 KB				

Remarks 1. 80GC (V850E/IF3): 80-pin plastic LQFP (14 × 14)
100GC (V850E/IG3): 100-pin plastic LQFP (fine pitch) (14 × 14)
100GF (V850E/IG3): 100-pin plastic LQFP (14 × 20)
161F1(V850E/IG3): 161-pin plastic FBGA (10 × 10)

2. The part numbers of the V850E/IG3 are shown as follows in this manual.

- GF versions
  μPD70F3453GF-GAS-AX, 70F3454GF-GAS-AX

Table 1-2 shows the differences in functions between the V850E/IF3 and V850E/IG3.

Table 1-2. Differences in Functions Between V850E/IF3 and V850E/IG3

Item		V850E/IF3	V850E/IG3
Port function	I/O	44	56
	Input	4	8
	On-chip pull-up resistor	44	56
Interrupt source		External interrupt: 15 Internal interrupt: 74	External interrupt: 21 Internal interrupt: 75
External bus function		None	Provided (μPD70F3454GC-8EA-A and 70F3454F1-DA9-A only)
Timers AA0 to AA4		Timer AA0 (without I/O) Timer AA1 (without I/O) Timer AA2 Timer AA3 (without I/O) Timer AA4	Timer AA0 (without I/O) Timer AA1 (without I/O) Timer AA2 Timer AA3 Timer AA4
Timers T0, T1		Timer T0 (without I/O) Timer T1	Timer T0 Timer T1
Motor control function	High-impedance output control pin	TOA2OFF TOB0OFF TOB1OFF	TOA2OFF TOA3OFF TOB0OFF TOB1OFF
A/D converter 2	Analog input	4 channels	8 channels
On-chip debug function	On-chip debug emulator	NIMICUBE2	NIMICUBE NIMICUBE2
Power supply for external pin		EV_{DD0}, EV_{DD1}	EV_{DD0} to EV_{DD2}
Package		80-pin plastic LQFP (14 × 14)	100-pin plastic LQFP (14 × 14) 100-pin plastic LQFP (14 × 20) 161-pin plastic FBGA (10 × 10)

1.2 V850E/IF3

1.2.1 Features (V850E/IF3)

○ Minimum instruction execution time:
15.6 ns (at internal 64 MHz operation)

○ General-purpose registers: 32 bits × 32

○ CPU features:
Signed multiplication (16 bits × 16 bits → 32 bits or 32 bits × 32 bits → 64 bits):
1 to 2 clocks
Saturated operation instructions (with overflow/underflow detection function)
32-bit shift instructions: 1 clock
Bit manipulation instructions
Load/store instructions with long/short format
Signed load instructions

○ Internal memory:

Part Number	Internal ROM	Internal RAM
μPD70F3451	128 KB (flash memory)	8 KB
μPD70F3452	256 KB (flash memory)	12 KB

○ On-chip debug function: Supports MINICUBE®2.

○ Interrupts/exceptions:

Non-maskable interrupts:	1 source (external: none, internal: 1)
Maskable interrupts:	88 sources (external: 15, internal: 73)
Software exceptions:	32 sources
Exception traps:	2 sources

○ DMA controller:
4 channels

Transfer unit:	8 bits/16 bits
Maximum transfer count:	65536 (2^{16})
Transfer type:	2-cycle
Transfer modes:	Single/single step/block
Transfer targets:	On-chip peripheral I/O ↔ Internal RAM On-chip peripheral I/O ↔ On-chip peripheral I/O
Transfer request:	On-chip peripheral I/O/software

Next address setting function

○ I/O lines: Total: 48 (Input ports: 4, I/O ports: 44)

○ Timer/counter function: 16-bit interval timer M (TMM): 4 channels
16-bit timer/event counter AA (TAA): 5 channels
16-bit timer/event counter AB (TAB): 2 channels
16-bit timer/event counter T (TMT): 2 channels
Motor control function (uses timer TAB: 2 channels (TAB0, TAB1), TAA: 2 channels (TAA0, TAA1))
  16-bit accuracy 6-phase PWM function with deadtime: 2 channels
  High-impedance output control function
  A/D trigger generation by timer tuning operation function
  Arbitrary cycle setting function
  Arbitrary deadtime setting function
Watchdog timer: 1 channel

○ Serial interfaces: Asynchronous serial interface A (UARTA)
Asynchronous serial interface B (UARTB)
Clocked serial interface B (CSIB)
I^2C bus interface (I^2C)

UARTA0/CSIB0:	1 channel
UARTA1/I^2C:	1 channel
UARTA2/CSIB1:	1 channel
UARTB/CSIB2:	1 channel

○ A/D converter: 12-bit resolution A/D converters (A/D converters 0 and 1): 5 channels + 5 channels (2 units)
  The one A/D converter 0 channel and three A/D converter 1 channels are provided with an operational amplifier for input level amplification and a comparator for overvoltage detection.
10-bit resolution A/D converter (A/D converter 2): 4 channels

○ Clock generator: 4 to 8 MHz resonator connectable (external clock input prohibited)
Multiplication function by PLL clock synthesizer (fixed to multiplication by eight, f_{XX} = 32 to 64 MHz)
CPU clock division function (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$)

○ Power-save function: HALT/IDLE/STOP mode

○ Power-on-clear function:

○ Low-voltage detection function:

○ Package: 80-pin plastic LQFP (14 × 14)

○ Operation supply voltage: $V_{DD0} = V_{DD1} = EV_{DD0} = EV_{DD1} = AV_{DD0} = AV_{DD1} = AV_{DD2} = 4.0$ to 5.5 V
(when A/D converter 0, 1 or 2 is operating)
$V_{DD0} = V_{DD1} = EV_{DD0} = EV_{DD1} = AV_{DD0} = AV_{DD1} = AV_{DD2} = 3.5$ to 5.5 V
(when none of A/D converters 0 to 2 is operating)