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μPD70F3826, 70F3827, 70F3828, 70F3829, 70F3830, 70F3831, 70F3832, 70F3833, 70F3834, 70F3835, 70F3836, 70F3837

R01DS0029EJ0001
Rev.0.01
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–V850ES/JE3-E, V850ES/JF3-E, V850ES/JG3-E– RENESAS MCU

Description

The μPD70F3826, 70F3827, 70F3828, 70F3829 (V850ES/JF3-E), and μPD70F3830, 70F3831, 70F3832, 70F3833 (V850ES/JF3-E), and μPD70F3834, 70F3835, 70F3836, 70F3837 (V850ES/JG3-E) are products of the V850 32-bit single-chip microcontrollers, and include peripheral functions such as ROM/RAM, timer/counters, serial interfaces, an A/D converter, a DMA controller , a CAN controller , a USB function controller , and a Ethernet controller.

In addition to their high real-time responsiveness and one-clock-pitch execution of instructions, the V850ES/JE3-E, V850ES/JF3-E, and V850ES/JG3-E include instructions executed via a hardware multiplier, saturation instructions, and bit manipulation instructions.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850ES/JE3-E, V850ES/JF3-E, V850ES/JG3-E Hardware User's Manual: To be prepared
V850ES Architecture User's Manual: U15943E

Features

- Number of instructions: 83
- Minimum instruction execution time:
  20 ns (@ 50 MHz operation with main clock (f_{XX}))
- Clock
  - Main clock oscillation: f_X = 3 to 6.25 MHz
  - Subclock oscillation: f_{XT} = 32.768 kHz
  - Internal oscillation: f_R = 220 kHz (TYP.)
- General-purpose registers: 32 bits × 32 registers
- Instruction set:
  Signed multiplication, saturation operations, 32-bit shift instructions, bit manipulation instructions, load/store instructions
- Memory space:
  64 MB linear address space
- Internal memory
  Flash memory: 64/128/256 KB
  RAM: 32/48/64 KB
  (Including 16 KB of data RAM area)
- I/O lines Total: 26/42/62
- Interrupts and exceptions
  Non-maskable interrupts: 2 sources
  Maskable interrupts: 63/78/85 sources
- Timer/counters
  16-bit timer/event counter AA (TAA): 5 channels
  16-bit timer/event counter AB (TAB): 1 channel
  Motor control function supported
  16-bit interval timer M (TMM): 4 channels
  16-bit encoder timer T (TMT): 1 channel
- Real-time counter: 1 channel
- Watchdog timer: 1 channel
- Real-time output function: 6 channels
- A/D converter: 10-bit resolution × 10/10 channels
- Ethernet controller: 1 channel
- USB function controller: 1 channel
- Serial interface
  - CAN :1 channel (μPD70F3829, 70F3833, 70F3837 only)
  - Asynchronous serial interface C(UARTC): 3/4 channels
  - Clocked serial interface F(CSIF): 2/3/5 channels
  - I^2C bus interface: 2/3 channels
- DMA controller: 4 channels
- Power save function:
  HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE mode
- On-chip debug function
- Package: 64-pin LQFP (V850ES/JE3-E)
  64-pin WQFN (V850ES/JE3-E)
  80-pin LQFP (V850ES/JF3-E)
  100-pin LQFP (V850ES/JG3-E)
  113-pin FBGA (Under planing)
- Operating supply voltage: 2.85 to 3.6 V

Function list (V850ES/JE3-E)

Generic Name		V850ES/JE3-E			
Product Name		μPD70F3826	μPD70F3827	μPD70F3828	μPD70F3829
Internal memory	Flash memory	64 KB	128 KB	256 KB	256 KB
	Internal RAM	16 KB	32 KB	48 KB	48 KB
	Data RAM	16 KB	16 KB	16 KB	16 KB
Memory space		64 MB			
General-purpose register		32 bits × 32 registers			
Clocks	Main clock oscillation	PLL mode : f_X = 3 to 6.25 MHz, f_{XX} = 24 to 50 MHz (multiplication by 8) Clock through mode : f_X = 3 to 6.25 MHz (internal : f_{XX} = 3 to 6.25 MHz)			
	Subclock oscillation	f_{XT} = 32.768 kHz			
	Internal oscillation	f_R = 220 kHz (TYP.)			
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{XX}))			
I/O ports		I/O: 26 (5 V tolerant : 12)			
Timer	16-bit TAA	5 channels (among which two channels have the interval function only)			
	16-bit TAB	–			
	16-bit TMM	4 channels			
	16-bit TMT	1 channel (Interval function only)			
	Motor control	–			
	Watch timer	1 channel (RTC)			
	WDT	1 channel			
Real-time output function		6 bits × 1 channel			
10-bit A/D converter		10 channels			
Serial interface	CSIF/UARTC	1 channel			
	CSIF/UARTC/I^2C	1 channel			
	CSIF	–			
	UARTC/I^2C	1 channel			–
	UARTC/I^2C/CAN	–			1 channel
USB function		1 channel			
Ethernet controller		1 channel			
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)			
Interrupt source	External Note 1, 2	7(7)	7(7)	7(7)	7(7)
	Internal	54	54	54	58
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes			
Reset factor		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)			
On-chip debugging		MINICUBE®, MINICUBE2 supported			
Operating supply voltage		2.85 to 3.6 V			
Operating ambient temperature		–40 to +85°C			
Package		64-pin plastic LQFP (fine pitch) (10 × 10 mm), 64-pin plastic WQFN (9 × 9 mm),			

Notes 1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.

2. Include NMI.

Function list (V850ES/JF3-E)

Generic Name		V850ES/JF3-E			
Product Name		μPD70F3830	μPD70F3831	μPD70F3832	μPD70F3833
Internal memory	Flash memory	64 KB	128 KB	256 KB	256 KB
	Internal RAM	16 KB	32 KB	48 KB	48 KB
	Data RAM	16 KB	16 KB	16 KB	16 KB
Memory space		64 MB			
General-purpose register		32 bits × 32 registers			
Clocks	Main clock oscillation	PLL mode : f_X = 3 to 6.25 MHz, f_{XX} = 24 to 50 MHz (multiplication by 8) Clock through mode : f_X = 3 to 6.25 MHz (internal : f_{XX} = 3 to 6.25 MHz)			
	Subclock oscillation	f_{XT} = 32.768 kHz			
	Internal oscillation	f_R = 220 kHz (TYP.)			
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{XX}))			
I/O ports		I/O: 42 (5 V tolerant : 28)			
Timer	16-bit TAA	5 channels			
	16-bit TAB	1 channel			
	16-bit TMM	4 channels			
	16-bit TMT	1 channel			
	Motor control	1 channel			
	Watch timer	1 channel (RTC)			
	WDT	1 channel			
Real-time output function		6 bits × 1 channel			
10-bit A/D converter		10 channels			
Serial interface	CSIF/UARTC	1 channel			
	CSIF/UARTC/I²C	2 channels			
	CSIF	–			
	UARTC/I²C	1 channel			–
	UARTC/I²C/CAN	–			1 channel
USB function		1 channel			
Ethernet controller		1 channel			
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)			
Interrupt source	External Note 1, 2	19(19)	19(19)	19(19)	19(19)
	Internal	57	57	57	61
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes			
Reset factor		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)			
On-chip debugging		MINICUBE, MINICUBE2 supported			
Operating supply voltage		2.85 to 3.6 V			
Operating ambient temperature		–40 to +85°C			
Package		80-pin plastic LQFP (fine pitch) (12 × 12 mm)			

Notes 1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.

2. Include NMI.

Function list (V850ES/JG3-E)

Generic Name		V850ES/JG3-E			
Product Name		μPD70F3834	μPD70F3835	μPD70F3836	μPD70F3837
Internal memory	Flash memory	64 KB	128 KB	256 KB	256 KB
	Internal RAM	16 KB	32 KB	48 KB	48 KB
	Data RAM	16 KB	16 KB	16 KB	16 KB
Memory space		64 MB			
General-purpose register		32 bits × 32 registers			
Clocks	Main clock oscillation	PLL mode : f_X = 3 to 6.25 MHz, f_{XX} = 24 to 50 MHz (multiplication by 8) Clock through mode : f_X = 3 to 6.25 MHz (internal : f_{XX} = 3 to 6.25 MHz)			
	Subclock oscillation	f_{XT} = 32.768 kHz			
	Internal oscillation	f_R = 220 kHz (TYP.)			
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{XX}))			
I/O ports		I/O: 62 (5 V tolerant : 35)			
Timer	16-bit TAA	5 channels			
	16-bit TAB	1 channel			
	16-bit TMM	4 channels			
	16-bit TMT	1 channel			
	Motor control	1 channel			
	Watch timer	1 channel (RTC)			
	WDT	1 channel			
Real-time output function		6 bits × 1 channel			
10-bit A/D converter		10 channels			
Serial interface	CSIF/UARTC	1 channel			
	CSIF/UARTC/I²C	2 channels			
	CSIF	2 channels			
	UARTC/I²C	1 channel			–
	UARTC/I²C/CAN	–			1 channel
USB function		1 channel			
Ethernet controller		1 channel			
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)			
Interrupt source	External Note 1, 2	22(22)	22(22)	22(22)	22(22)
	Internal	61	61	61	65
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes			
Reset factor		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)			
On-chip debugging		MINICUBE, MINICUBE2 supported			
Operating supply voltage		2.85 to 3.6 V			
Operating ambient temperature		–40 to +85°C			
Package		100-pin plastic LQFP (fine pitch) (14 × 14 mm), 113-pin plastic FBGA Note3			

Notes 1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.

2. Include NMI.

3. Under planning.

APPLICATIONS

○ Applications that require Ethernet controller

Home audio, printers, and scanners.

ORDERING INFORMATION

- V850ES/JE3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3826GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	64 KB
μPD70F3827GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	128 KB
μPD70F3828GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB
μPD70F3829GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB
μPD70F3826K8-6B4-AX	64-pin plastic WQFN (9 × 9)	64 KB
μPD70F3827K8-6B4-AX	64-pin plastic WQFN (9 × 9)	128 KB
μPD70F3828K8-6B4-AX	64-pin plastic WQFN (9 × 9)	256 KB
μPD70F3829K8-6B4-AX	64-pin plastic WQFN (9 × 9)	256 KB

- V850ES/JF3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3830GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	64 KB
μPD70F3831GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	128 KB
μPD70F3832GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	256 KB
μPD70F3833GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	256 KB

- V850ES/JG3-E

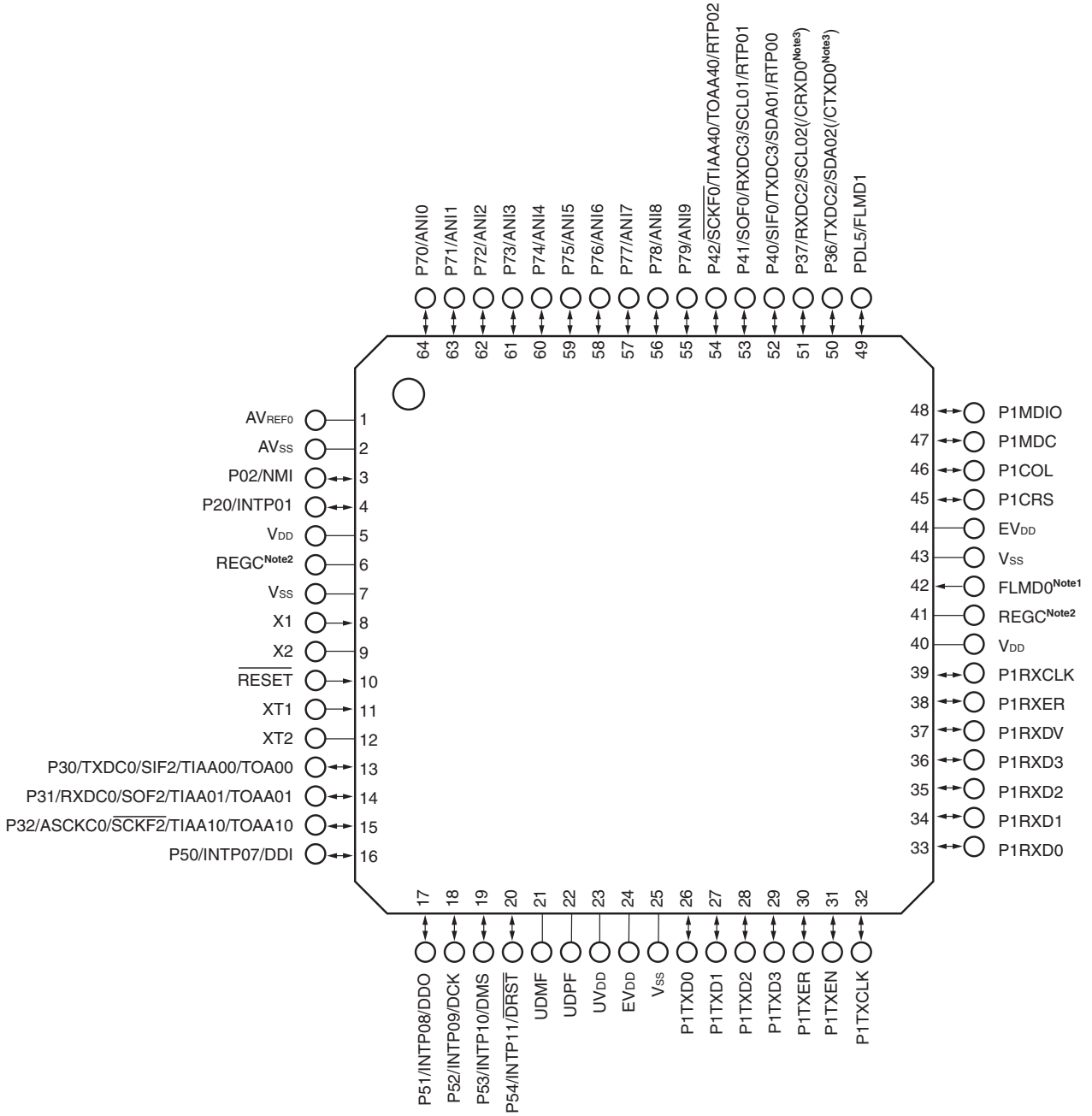
Part Number	Package	On-Chip Flash Memory
μPD70F3834GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	64 KB
μPD70F3835GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	128 KB
μPD70F3836GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB
μPD70F3837GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB
μPD70F3837F1-CAH-AX[Note]	113-pin plastic FBGA (8 × 8)	256 KB

Note Under planning

Remark The V850ES/Jx3-E microcontrollers are lead-free products.

PIN CONFIGURATION

- V850ES/JE3-E
  64-pin plastic LQFP (fine pitch) (10 × 10)
  μPD70F3826GB-GAH-AX μPD70F3827GB-GAH-AX
  μPD70F3828GB-GAH-AX μPD70F3829GB-GAH-AX

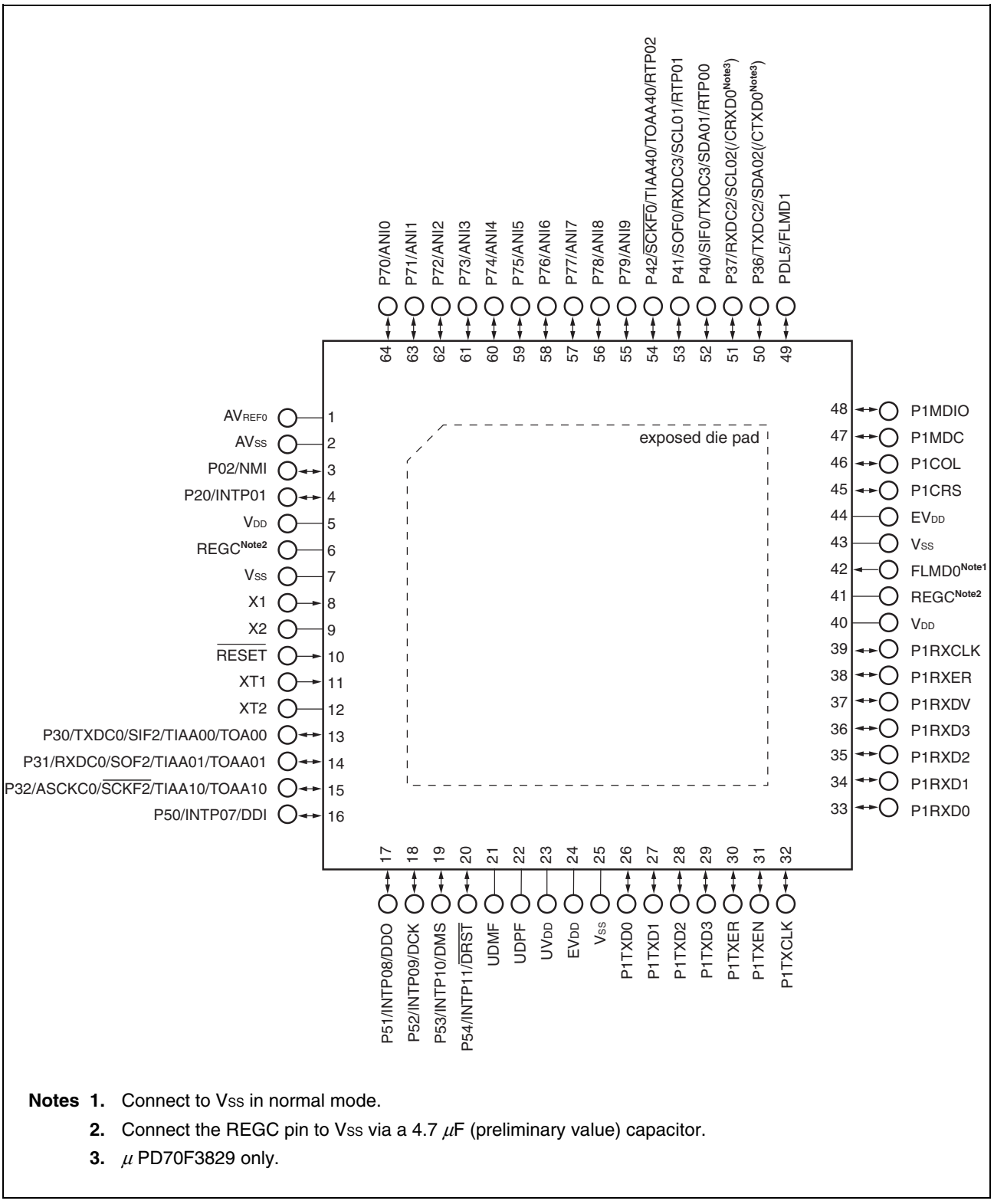


Notes 1. Connect to VSS in normal mode.

2. Connect the REGC pin to VSS via a 4.7 μF (preliminary value) capacitor.

3. μ PD70F3829 only.

- V850ES/JE3-E
  64-pin plastic WQFN (9 × 9)
  μPD70F3826K8-6B4-AX μPD70F3827K8-6B4-AX
  μPD70F3828 K8-6B4-AX μPD70F3829K8-6B4-AX



Notes 1. Connect to VSS in normal mode.

2. Connect the REGC pin to VSS via a 4.7 μF (preliminary value) capacitor.

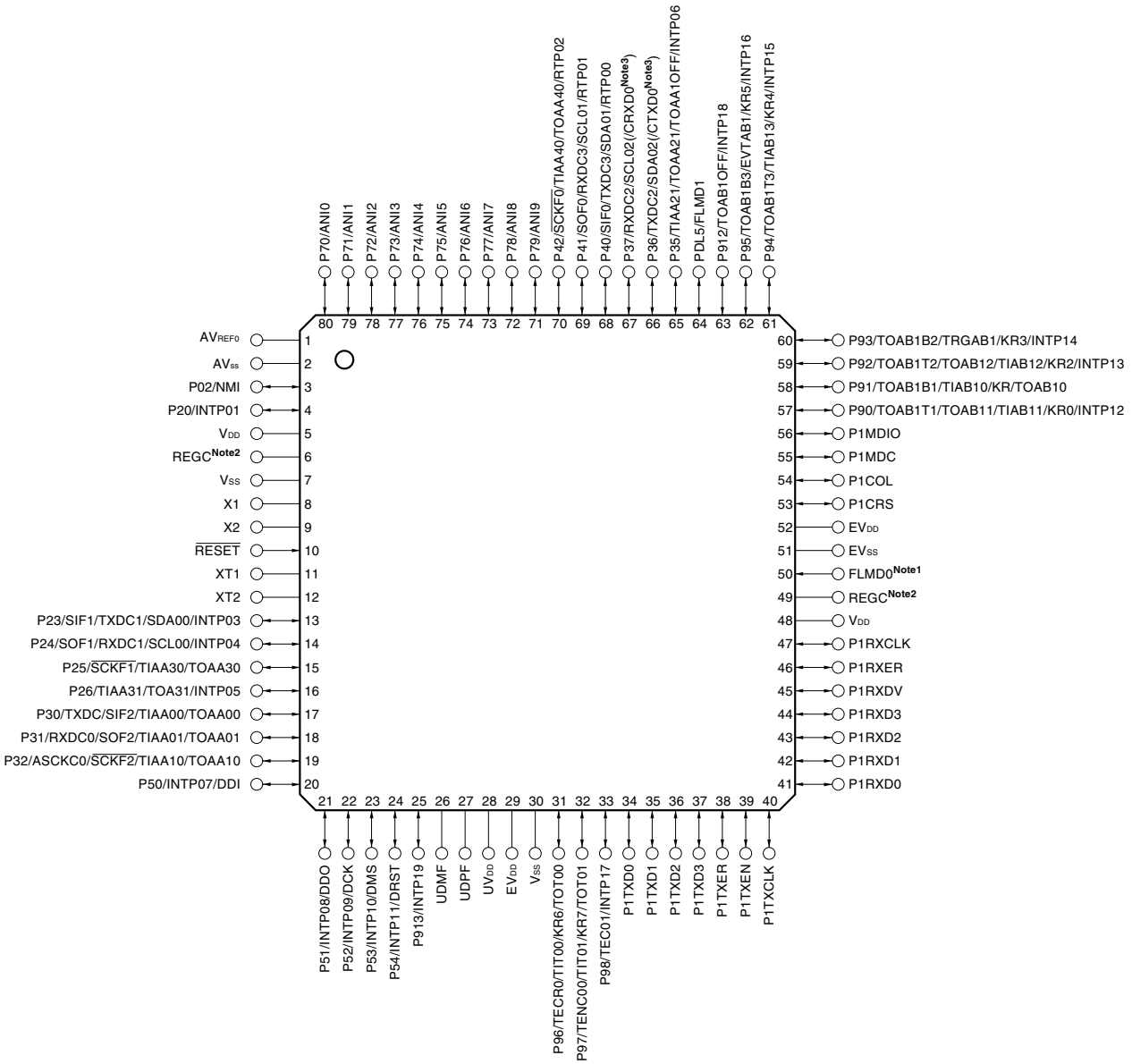
3. μ PD70F3829 only.

- V850ES/JF3-E

  80-pin plastic LQFP (fine pitch) (12 × 12)

  μPD70F3830GK-GAK-AX　　μPD70F3831GK-GAK-AX

  μPD70F3832GK-GAK-AX　　μPD70F3833GK-GAK-AX

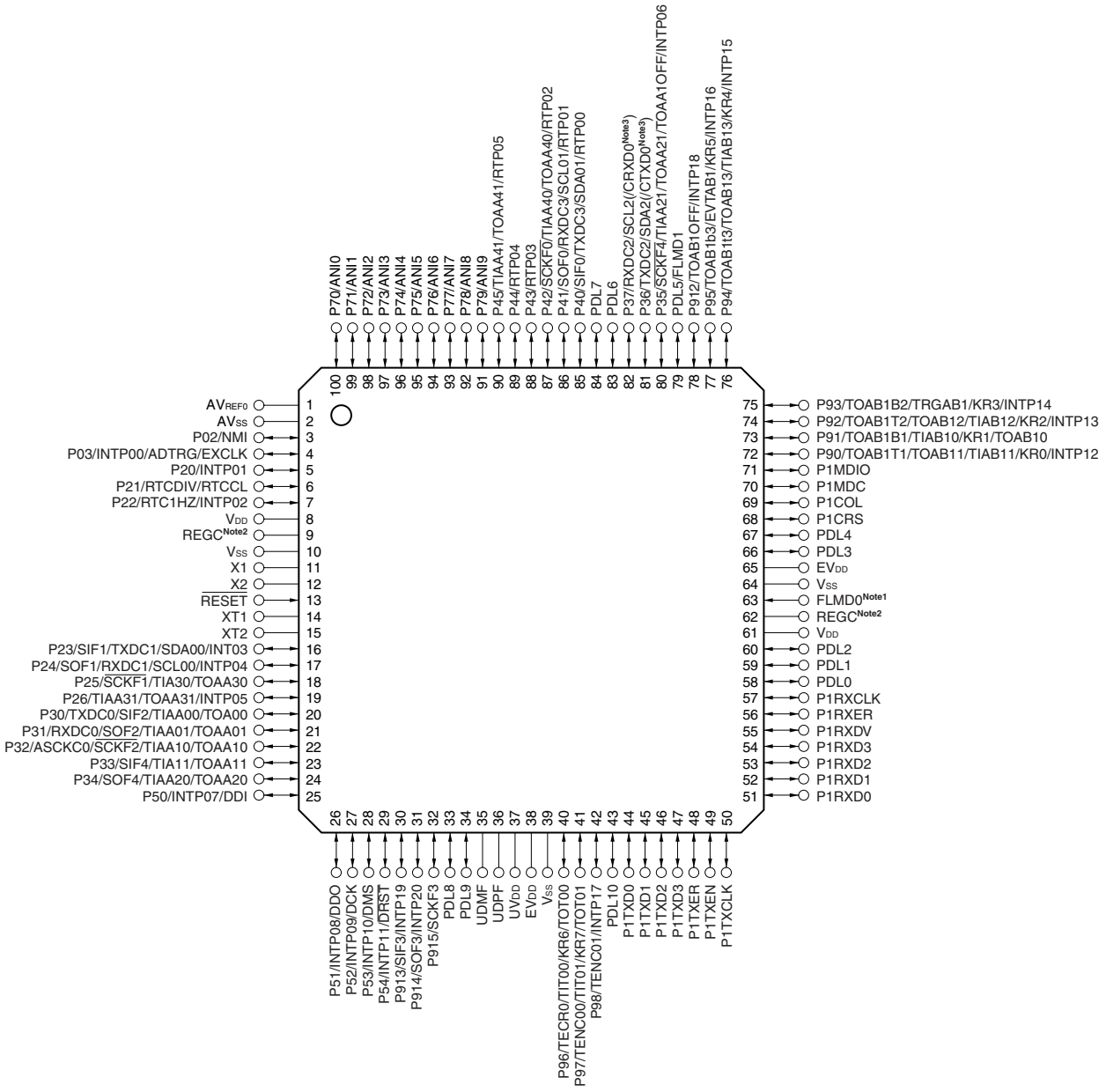


Notes 1. Connect to VSS in normal mode.

2. Connect the REGC pin to VSS via a 4.7 μF (preliminary value) capacitor.

3. μ PD70F3833 only.

- V850ES/JG3-E
  100-pin plastic LQFP (fine pitch) (14 × 14)
  μPD70F3834GC-UEU-AX μPD70F3835GC-UEU-AX
  μPD70F3836GC-UEU-AX μPD70F3837GC-UEU-AX



Notes 1. Connect to VSS in normal mode.

2. Connect the REGC pin to VSS via a 4.7 μF (preliminary value) capacitor.

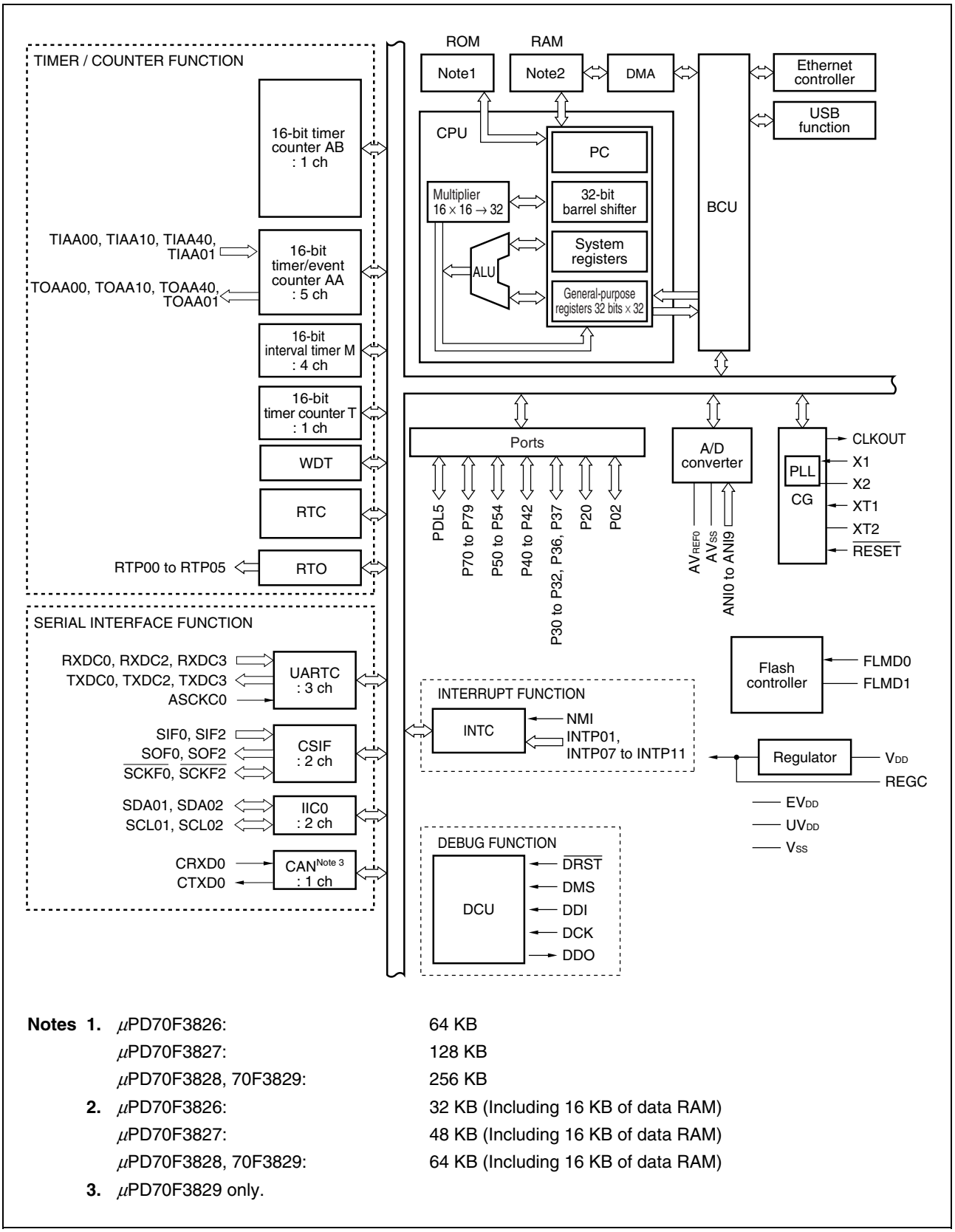
3. μ PD70F3837 only.

PIN IDENTIFICATION

ADTRG:	A/D Trigger Input
ANI0 to ANI9:	Analog Input
ASCKC0:	Asynchronous Serial Clock
AV_{REF0}:	Analog Reference Voltage
AV_{SS}:	Grand for Analog Pin
CRXD0:	CAN Receive Data
CTXD0:	CAN Transmit Data
DCK:	Debug Clock
DDI:	Debug Data Input
DDO:	Debug Data Output
DMS:	Debug Mode Select
$\overline{DRST}$:	Debug Reset
EV_{DD}:	Power Supply for External Pin
EVTAB1:	Timer Event Count Input
EXCLK	USB clock
FLMD0, FLMD1:	Flash Programming Mode
INTP00 to INTP20:	External Interrupt Input
KR0 to KR7:	Key Return
NMI:	Non-maskable Interrupt Request
P02, P03:	Port0
P1COL, P1CRS, P1MDC, P1MDIO, P1RXCLK, P1RXD0 to P1RXD3, P1RXDV, P1RXER P1TXCLK, P1TXD0 to P1TXD3, P1TXEN, P1TXER:	Ethernet PHY Interface
P20 to P26	Port2
P30 to P37:	Port3
P40 to P45:	Port4
P50 to P54:	Port5
P70 to P79:	Port7
P90 to P98, P912 to P915:	Port9
PDL0 to PDL10:	Port DL
REGC:	Regulator Control
$\overline{RESET}$:	Reset
RTC1HZ, RTCCL, RTCDIV:	Real-time Counter Clock Output
RTP00 to RTP05:	Real-time Output Port
RXDC0 to RXDC3	Receive Data
$\overline{SCKF0}$ to $\overline{SCKF4}$:	Serial Clock
SCL00 to SCL02:	Serial Clock
SDA00 to SDA02:	Serial Data
SIF0 to SIF4:	Serial Input
SOF0 to SOF4:	Serial Output
TECR0:	Timer Encoder Clear Input
TENC00, TENC01:	Timer Encoder Input
TIAA00, TIAA01, TIAA10, TIAA11, TIAA20, TIAA21, TIAA30, TIAA31, TIAA40, TIAA41, TIAB10 to TIAB13, TIT00, TIT01:	Timer Input
TOAA00, TOAA01, TOAA10, TOAA11, TOAA20, TOAA21, TOAA30, TOAA31, TOAA40, TOAA41, TOAB10 to TOAB13, TOAB1B1 to TOAB1B3, TOAB1T1 to TOAB1T3, TOT00, TOT01:	Timer Output
TOAA1OFF, TOAB1OFF	Timer Output Off
TRGAB1:	Timer Trigger Input
TXDC0 to TXDC3:	Serial Output
UDMF:	USB Data I/O (-) Function
UDPF:	USB Data I/O (+) Function
UV_{DD}:	Power Supply for External USB
V_{DD}:	Power Supply
V_{SS}:	Ground
X1, X2:	Crystal for Main Clock
XT1, XT2:	Crystal for Sub-clock

INTERNAL BLOCK DIAGRAM

- **V850ES/JE3-E**

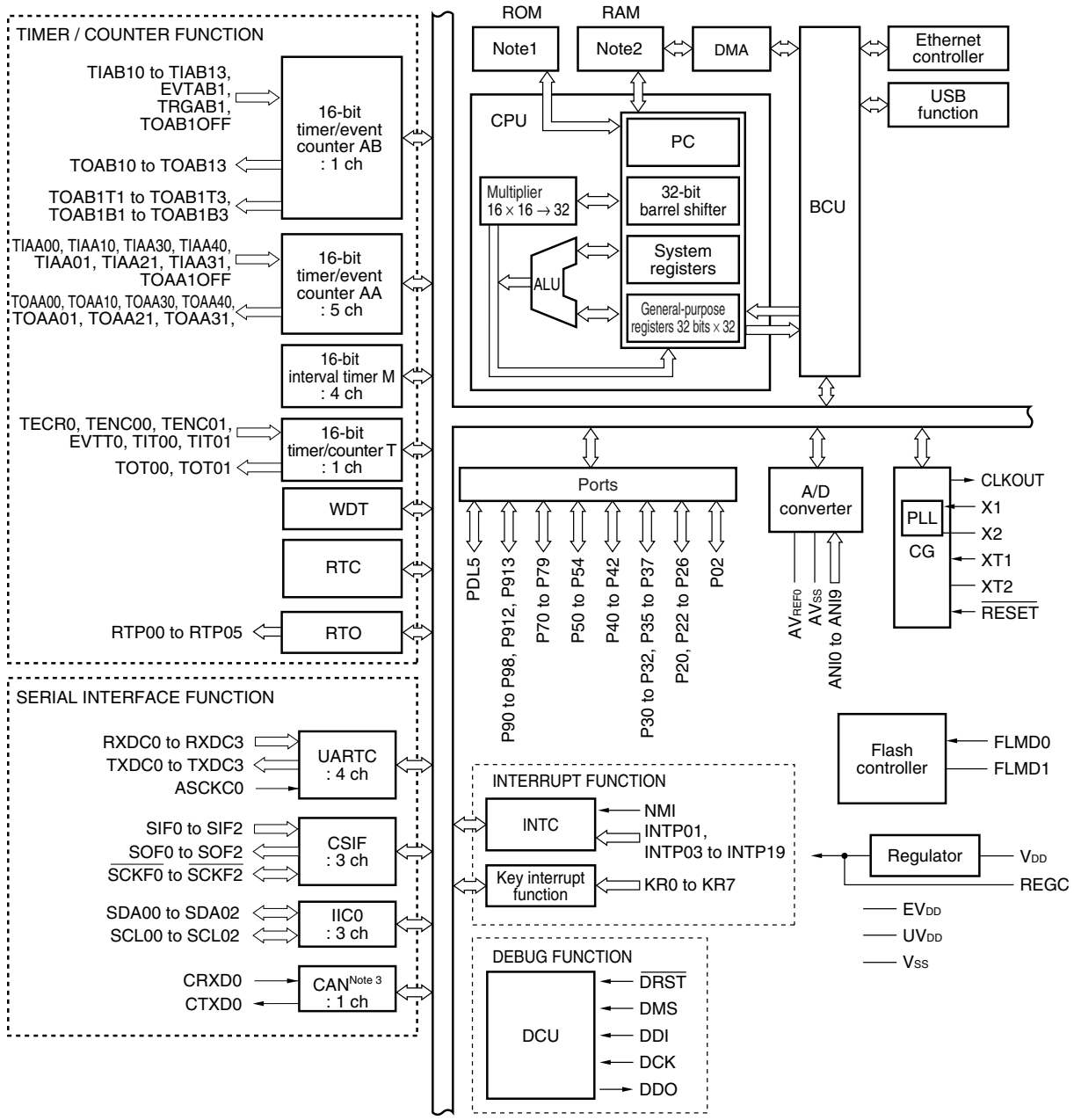


Notes 1. μPD70F3826: 64 KB
μPD70F3827: 128 KB
μPD70F3828, 70F3829: 256 KB

2. μPD70F3826: 32 KB (Including 16 KB of data RAM)
μPD70F3827: 48 KB (Including 16 KB of data RAM)
μPD70F3828, 70F3829: 64 KB (Including 16 KB of data RAM)

3. μPD70F3829 only.

- **V850ES/JF3-E**

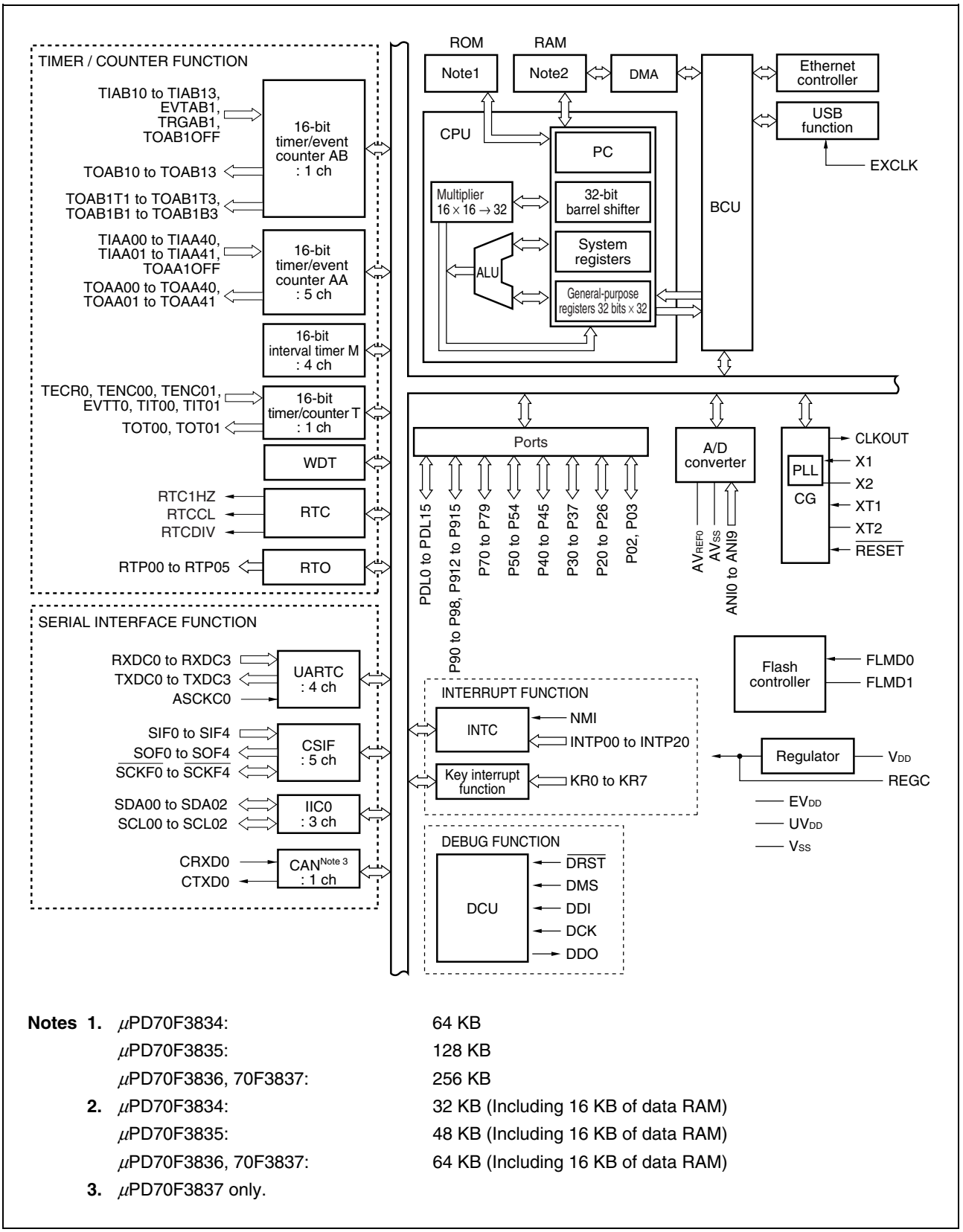


Notes 1. μPD70F3830: 64 KB
μPD70F3831: 128 KB
μPD70F3832, 70F3833: 256 KB

2. μPD70F3830: 32 KB (Including 16 KB of data RAM)
μPD70F3831: 48 KB (Including 16 KB of data RAM)
μPD70F3832, 70F3833: 64 KB (Including 16 KB of data RAM)

3. μPD70F3833 only.

- **V850ES/JG3-E**



Notes 1. μPD70F3834: 64 KB
μPD70F3835: 128 KB
μPD70F3836, 70F3837: 256 KB

2. μPD70F3834: 32 KB (Including 16 KB of data RAM)
μPD70F3835: 48 KB (Including 16 KB of data RAM)
μPD70F3836, 70F3837: 64 KB (Including 16 KB of data RAM)

3. μPD70F3837 only.

CONTENTS

1. PIN FUNCTIONS

1.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
P02	I/O	Port 0 2-bit I/O port(V850ES/JG3-E) 1-bit I/O port(V850ES/JE3-E, V850ES/JF3-E) Input/output can be specified in 1-bit units.	NMI	3	3	3
P03			INTP00/ADTRG/EXCLK	–	–	4
P20	I/O	Port 2 7-bit I/O port(V850ES/JG3-E) 5-bit I/O port(V850ES/JF3-E) 1-bit I/O port(V850ES/JE3-E) Input/output can be specified in 1-bit units.	INTP01	4	4	5
P21			RTGDIV/RTCCL	–	–	6
P22			RTC1HZ/INTP02	–	–	7
P23			SIF1/TXDC1/SDA00/INTP03	–	13	16
P24			SOF1/RXDC1/SDL00/INTP04	–	14	17
P25			$\overline{\text{SCKF}}$1/TIAA30/TOAA30	–	15	18
P26			TIAA31/TOAA31/INTP05	–	16	19
P30	I/O	Port 3 8-bit I/O port(V850ES/JG3-E) 6-bit I/O port(V850ES/JF3-E) 5-bit I/O port(V850ES/JE3-E) Input/output can be specified in 1-bit units.	TXDC0/SIF2/TIAA00/TOAA00	13	17	20
P31			RXDC0/SOF2/TIAA01/TOAA01	14	18	21
P32			ASCKC0/$\overline{\text{SCKF2}}$/TIAA10/TOAA10	15	19	22
P33			SIF4/TIAA11/TOAA11	–	–	23
P34			SOF4/TIAA20/TOAA20	–	–	24
P35			$\overline{\text{SCKF4}}$/TIAA21/TOAA21 /TOAA1OFF/INTP06	–	–	80
			TIAA21/TOAA21/TOAA1OFF/INTP06	–	65	–
P36			TXDC2/SDA02/CTXD0[Note]	50	66	81
P37			RXDC2/SCL02/CRXD0[Note]	51	67	82
P40	I/O	Port 4 6-bit I/O port(V850ES/JG3-E) 3-bit I/O port(V850ES/JE3-E, V850ES/JF3-E) Input/output can be specified in 1-bit units.	SIF0/TXDC3/SDA01/RTP00	52	68	85
P41			SOF0/RXDC3/SCL01/RTP01	53	69	86
P42			$\overline{\text{SCKF0}}$/TIAA40/TOAA40/RTP02	54	70	87
P43			RTP03	–	–	88
P44			RTP04	–	–	89
P45			TIAA41/TOAA41/RTP05	–	–	90
P50	I/O	Port 5 5-bit I/O port Input/output can be specified in 1-bit units.	INTP07/DDI	16	20	25
P51			INTP08/DDO	17	21	26
P52			INTP09/DCK	18	22	27
P53			INTP10/DMS	19	23	28
P54			INTP11/$\overline{\text{DRST}}$	20	24	29

Note Available only in on-chip CAN controller products

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

(2/2)

Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
P70	I/O	Port 7 10-bit I/O port Input/output can be specified in 1-bit units.	ANI0	64	80	100
P71			ANI1	63	79	99
P72			ANI2	62	78	98
P73			ANI3	61	77	97
P74			ANI4	60	76	96
P75			ANI5	59	75	95
P76			ANI6	58	74	94
P77			ANI7	57	73	93
P78			ANI8	56	72	92
P79			ANI9	55	71	91
P90	I/O	Port 9 13-bit I/O port(V850ES/JG3-E) 11-bit I/O port(V850ES/JF3-E) Input/output can be specified in 1-bit units.	TOAB1T1/TOAB11/TIAB11/KR0/INTP12	–	57	72
P91			TOAB1B1/TIAB10/KR1/TOAB10	–	58	73
P92			TOAB1T2/TOAB12/TIAB12/KR2/INTP13	–	59	74
P93			TOAB1B2/TRGAB1/KR3/INTP14	–	60	75
P94			TOAB1T3/TOAB13/TIAB13/KR4/INTP15	–	61	76
P95			TOAB1B3/EVTB1/KR5/INTP16	–	62	77
P96			TECR0/TIT00/KR6/TOT00	–	31	40
P97			TENC00/TIT01/KR7/TOT01	–	32	41
P98			TENC01/INTP17	–	33	42
P912			TOAB1OFF/INTP18	–	63	78
P913			SIF31/INTP19	–	–	30
			INTP19	–	25	–
P914			SOF3/INTP20	–	–	31
P915			$\overline{\text{SCKF3}}$	–	–	32
PDL0	I/O	Port DL 11-bit I/O port(V850ES/JG3-E) 1-bit I/O port(V850ES/JF3-E, V850ES/JE3-E) Input/output can be specified in 1-bit units.	–	–	–	58
PDL1			–	–	–	59
PDL2			–	–	–	60
PDL3			–	–	–	66
PDL4			–	–	–	67
PDL5			FLMD1	49	64	79
PDL6			–	–	–	83
PDL7			–	–	–	84
PDL8			–	–	–	33
PDL9			–	–	–	34
PDL10			–	–	–	43

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

1.2 Non-Port Pins

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
ADTRG	Input	External trigger input for A/D converter	P03/INTP00/EXCLK	–	–	4
ANI0	Input	Analog voltage input for A/D converter	P70	64	80	100
ANI1			P71	63	79	99
ANI2			P72	62	78	98
ANI3			P73	61	77	97
ANI4			P74	60	76	96
ANI5			P75	59	75	95
ANI6			P76	58	74	94
ANI7			P77	57	73	93
ANI8			P78	56	72	92
ANI9			P79	55	71	91
ASCKC0	Input	UARTC0 baud rate clock input	P32/$\overline{\text{SCKF2}}$/TIAA10/TOAA10	15	19	22
AV_{REF0}	–	Reference voltage input for A/D converter, and positive power supply for port 7	–	1	1	1
AV_{SS}	–	Ground voltage for A/D converter	–	2	2	2
CRXD0[Note]	Input	CAN receive data input	P37/RXDC2/SCL02	51	67	82
CTXD0[Note]	Output	CAN transmit data output	P36/TXDC2/SDA02	50	66	81
DCK	Input	Clock input for on-chip debugging	P52/INTP09	18	22	27
DDI	Input	Data input for on-chip debugging	P50/INTP07	16	20	25
DDO	Output	Data output for on-chip debugging In the on-chip debug mode, high-level output is forcibly set.	P51/INTP08	17	21	26
DMS	Input	Mode select signal input for on-chip debugging	P53/INTP10	19	23	28
$\overline{\text{DRST}}$	Input	Reset signal input for on-chip debugging	P54/INTP11	20	24	29
EV_{DD}	–	Positive power supply for external (same potential as V_{DD})	–	24, 44	29, 52	38, 65
EVTAB1	Input	External event count input of TAB1	P95/TOAB1B3/KR5/INTP16	–	62	77
EXCLK	Input	USB clock signal input	P03/INTP00/ADTRG	–	–	4
FLMD0	Input	Flash programming mode setting pins	–	42	50	63
FLMD1	Input		PDL5/AD5	49	64	79
INTP00	Input	External interrupt request input (maskable, analog noise elimination). Analog noise elimination or digital noise elimination selectable for INTP02 pin.	P03/ADTRG/EXCLK	–	–	4
INTP01			P20	4	4	5
INTP02			P22/RTC1HZ	–	–	7
INTP03			P23/SIF1/TXDC1/SDA00	–	13	16
INTP04			P24/SOF1/RXDC1/SDL00	–	14	17
INTP05			P26/TIAA31/TOAA31	–	16	19
INTP06			P35/$\overline{\text{SCKF4}}$/TIAA21/TOAA21/TOAA1OFF	–	–	80
			P35/TIAA21/TOAA21/TOAA1OFF	–	65	–
INTP07			P50/DDI	16	20	25
INTP08			P51/DDO	17	21	26
INTP09			P52/DCK	18	22	27
INTP10			P53/DMS	19	23	28

Note Available only in on-chip CAN controller products

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
INTP11	Input	External interrupt request input (maskable, analog noise elimination).	P54/$\overline{\text{DRST}}$	20	24	29
INTP12			P90/TOAB1T1/TOAB11/TIAB11/KR0	–	57	72
INTP13			P92/TOAB1T2/TOAB12/TIAB12/KR2	–	59	74
INTP14			P93/TOAB1B2/TRGAB1/KR3	–	60	75
INTP15			P94/TOAB1T3/TOAB13/TIAB13/KR4	–	61	76
INTP16			P95/TOAB1B3/EVTAB1/KR5	–	62	77
INTP17			P98/TENC01	–	33	42
INTP18			P912/TOAB1OFF	–	63	78
INTP19			P913/SIF3	–	–	30
			P913	–	25	–
INTP20			P914/SOF3	–	–	31
KR0	Input	Key interrupt input (analog noise elimination)	P90/TOAB1T1/TOAB11/TIAB11/INTP12	–	57	72
KR1			P91/TOAB1B1/TIAB10/TOAB10	–	58	73
KR2			P92/TOAB1T2/TOAB12/TIAB12/INTP13	–	59	74
KR3			P93/TOAB1B2/TRGAB1/INTP14	–	60	75
KR4			P94/TOAB1T3/TOAB13/TIAB13/INTP15	–	61	76
KR5			P95/TOAB1B3/EVTAB1/INTP16	–	62	77
KR6			P96/TECR0/TIT00/TOT00	–	31	40
KR7			P97/TENC00/TIT01/TOT01	–	32	41
NMI	Input	External interrupt (non-maskable, ananlog noise elimination)	P02	3	3	3
P1COL	Input	Collision detection input for Ethernet	–	46	54	69
P1CRS	Input	Carrier detection input for Ethernet	–	45	53	68
P1MDC	Output	Seria transmit clock output	–	32	40	50
P1MDIO	I/O	Serial I/O	–	47	55	70
P1RXCLK	Input	Receive clock input for Ethernet	–	48	56	71
P1RXD0	Input	Receive data input for Ethernet	–	39	47	57
P1RXD1	Input	Receive data input for Ethernet	–	33	41	51
P1RXD2	Input	Receive data input for Ethernet	–	34	42	52
P1RXD3	Input	Receive data input for Ethernet	–	35	43	53
P1RXDV	Input	Receive data VALID input for Ethernet	–	36	44	54
P1RXER	Input	Receive data error input for Ethernet	–	37	45	55
P1TXCLK	Output	Transmit clock output for Ethernet	–	38	46	56
P1TXD0	Output	Transmit data output for Ethernet	–	26	34	44
P1TXD1	Output	Transmit data output for Ethernet	–	27	35	45
P1TXD2	Output	Transmit data output for Ethernet	–	28	36	46
P1TXD3	Output	Transmit data output for Ethernet	–	29	37	47
P1TXEN	Output	Transmit data enable output for Ethernet	–	31	39	49
P1TXER	Output	Transmit error output for Ethernet	–	30	38	48

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
REGC	–	Connecting capacitor for regulator output stabilization (4.7 μF (preliminary value))	–	6, 41	6, 49	9, 62
$\overline{\text{RESET}}$	Input	System reset input	–	10	10	13
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	P22/INTP02	–	–	7
RTCCL	Output	Real-time counter clock (original 32 kHz clock) output	P21/RTCDIV	–	–	6
RTCDIV	Output	Real-time counter clock (divided 32 kHz clock) output	P21/RTCCL	–	–	6
RTP00	Output	Real-time output port	P40/SIF0/TXDC3/SDA01	52	68	85
RTP01		RTP00, RTP01 are N-ch open-drain output selectable.	P41/SOF0/RXDC3/SCL01	53	69	86
RTP02			P42/$\overline{\text{SCKF0}}$/TIAA40/TOAA40	54	70	87
RTP03			P43	–	–	88
RTP04			P44	–	–	89
RTP05			P45TIAA41/TOAA41	–	–	90
RXDC0	Input	Serial receive data input (UARTC0 to UARTC3)	P31/SOF2/TIAA01/TOAA01	14	18	21
RXDC1			P24/SOF1/SDL00/INTP04	–	14	17
RXDC2			P37/SCL02/CRXD0[Note]	51	67	82
RXDC3			P41/SOF0/SCL01/RTP01	53	69	86
$\overline{\text{SCKF0}}$	I/O	Serial clock I/O (CSIF0 to CSIF4)	P42/TIAA40/TOAA40/RTP02	54	70	87
$\overline{\text{SCKF1}}$			P25/TIAA30/TOAA30	–	15	18
$\overline{\text{SCKF2}}$			P32/ASCKC0/TIAA10/TOAA10	15	19	22
$\overline{\text{SCKF3}}$			P915	–	–	32
$\overline{\text{SCKF4}}$			P35/TIAA21/TOAA21/TOAA1OFF /INTP06	–	–	80
SCL00	I/O	Serial clock I/O (I^2C00 to I^2C02)	P24/SOF1/RXDC1/INTP04	–	14	17
SCL01		N-ch open-drain output selectable.	P41/SOF0/RXDC3/RTP01	53	69	86
SCL02			P37/RXDC2/CRXD0[Note]	51	67	82
SDA00	I/O	Serial transmit/receive data I/O (I^2C00 to I^2C02)	P23/SIF1/TXDC1/INTP03	–	13	16
SDA01		N-ch open-drain output selectable.	P40/SIF0/TXDC3/RTP00	52	68	85
SDA02			P36/TXDC2/CTXD0[Note]	50	66	81
SIF0	Input	Serial receive data input (CSIF0 to CSIF4)	P40/TXDC3/SDA01/RTP00	52	68	85
SIF1			P23/TXDC1/SDA00/INTP03	–	13	16
SIF2			P30/TXDC0/TIAA00/TOAA00	13	17	20
SIF3			P913/INTP19	–	–	30
SIF4			P33/TIAA11/TOAA11	–	–	23
SOF0	Output	Serial transmit data output (CSIF0 to CSIF4)	P41/RXDC3/SCL01/RTP01	53	69	86
SOF1		N-ch open-drain output selectable.	P24/RXDC1/SDL00/INTP04	–	14	17
SOF2			P31/RXDC0/TIAA01/TOAA01	14	18	21
SOF3			P914/INTP20	–	–	31
SOF4			P34/TIAA20/TOAA20	–	–	24
TECR0	Input	Encoder clear input of TMT0	P96/TIT00/KR6/TOT00	–	31	40
TENC00		Encoder input/external event input/external trigger input of TMT0	P97/TIT01/KR7/TOT01	–	32	41
TENC01		Encoder input of TMT0	P98/INTP17	–	33	42

Note Available only in on-chip CAN controller products

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
TIAA00	Input	Capture trigger input/external event input/external trigger input (TAA0)	P30/TXDC0/SIF2/TOAA00	13	17	20
TIAA01		Capture trigger input (TAA0)	P31/RXDC0/SOF2/TOAA01	14	18	21
TIAA10		Capture trigger input/external event input/external trigger input (TAA1)	P32/ASCKC0/$\overline{\text{SCKF2}}$/TOAA10	15	19	22
TIAA11		Capture trigger input (TAA1)	P33/SIF4/TXDB0/TOAA11	–	–	23
TIAA20		Capture trigger input/external event input/external trigger input (TAA2)	P34/SOF4/RXDB0/TOAA20	–	–	24
TIAA21		Capture trigger input (TAA2)	P35/$\overline{\text{SCKF4}}$/TOAA21/TOAA1OFF /INTP06	–	–	80
			TIAA21/TOAA21/TOAA1OFF/INT P06	–	65	–
TIAA30		Capture trigger input/external event input/external trigger input (TAA3)	P25/$\overline{\text{SCKF1}}$/TOAA30	–	15	18
TIAA31		Capture trigger input (TAA3)	P26/TOAA31/INTP05	–	16	19
TIAA40		Capture trigger input/external event input/external trigger input (TAA4)	P42/$\overline{\text{SCKF0}}$/TOAA40/RTP02	54	70	87
TIAA41		Capture trigger input (TAA4)	P45/$\overline{\text{SCKE0}}$/TOAA41/RTP05	–	–	90
TIAB10	Input	Capture trigger input/external event input/external trigger input (TAB1) N-ch open-drain output selectable.	P91/TOAB1B1/KR1/TOAB10	–	58	73
TIAB11		Capture trigger input (TAB1) N-ch open-drain output selectable.	P90/TOAB1T1/TOAB11/KR0/INTP12	–	57	72
TIAB12			P92/TOAB1T2/TOAB12/KR2/INTP13	–	59	74
TIAB13			P94/TOAB1T3/TOAB13/KR4/INTP15	–	61	76
TIT00	Input	Capture trigger input of TMT0 N-ch open-drain output selectable.	P96/TECR0/KR6/TOT00	–	31	40
TIT01			P97/TENC00/KR7/TOT01	–	32	41
TOAA00	Output	Timer output (TAA0) N-ch open-drain output selectable.	P30/TXDC0/SIF2/TIAA00	13	17	20
TOAA01			P31/RXDC0/SOF2/TIAA01	14	18	21
TOAA10		Timer output (TAA1) N-ch open-drain output selectable.	P32/ASCKC0/$\overline{\text{SCKF2}}$/TIAA10	15	19	22
TOAA11			P33/SIF4/TIAA11	–	–	23
TOAA1OFF	Input	TAA1 High-impedance output control signal input	P35/$\overline{\text{SCKF4}}$/TIAA21/TOAA21/INTP06	–	–	80
			P35/TIAA21/TOAA21/INTP06	–	65	–
TOAA20	Output	Timer output (TAA2) N-ch open-drain output selectable.	P34/SOF4/TIAA20	–	–	24
TOAA21			P35/$\overline{\text{SCKF4}}$/TIAA21/TOAA1OFF /INTP06	–	–	80
			P35/TIAA21/TOAA1OFF/INTP06	–	65	–
TOAA30		Timer output (TAA3) N-ch open-drain output selectable.	P25/$\overline{\text{SCKF1}}$/TIAA30/	–	15	18
TOAA31			P26/TIAA31/INTP05	–	16	19
TOAA40		Timer output (TAA4) N-ch open-drain output selectable.	P42/$\overline{\text{SCKF0}}$/TIAA40/RTP02	54	70	87
TOAA41			P45/$\overline{\text{SCKE0}}$/TIAA41/RTP05	–	–	90
TOAB10	Output	Timer output (TAB1) N-ch open-drain output selectable.	P91/TOAB1B1/TIAB10/KR1	–	58	73
TOAB11			P90/TOAB1T1/TIAB11/KR0/INTP12	–	57	72
TOAB12			P92/TOAB1T2/TIAB12/KR2/INTP13	–	59	74
TOAB13			P94/TOAB1T3/TIAB13/KR4/INTP15	–	61	76

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
TOAB1B1	Output	Pulse signal output for 6-phase PWM low arm of TAB1	P91/TIAB10/KR1/TOAB10	–	58	73
TOAB1B2			P93/TRGAB1/KR3/INTP14	–	60	75
TOAB1B3			P95/EVTAB1/KR5/INTP16	–	62	77
TOAB1OFF	Input	TAB1 High-impedance output control signal input	P912/INTP18	–	63	78
TOAB1T1	Output	Pulse signal output for 6-phase PWM high arm of TAB1. N-ch open-drain output selectable.	P90/TOAB11/TIAB11/KR0/INTP12	–	57	72
TOAB1T2			P92/TOAB12/TIAB12/KR2/INTP13	–	59	74
TOAB1T3			P94/TOAB13/TIAB13/KR4/INTP15	–	61	76
TOT00	Output	Timer output of TMT0 N-ch open-drain output selectable	P96/TECR0/TIT00/KR6	–	31	40
TOT01			P97/TENC00/TIT01/KR7	–	32	41
TRGAB1	Input	External trigger input of TAB1 N-ch open-drain output selectable	P93/TOAB1B2/KR3/INTP14	–	60	75
TXDC0	Output	Serial transmit data output (UARTC0 to UARTC3) N-ch open-drain output selectable.	P30/SIF2/TIAA00/TOAA00	13	17	20
TXDC1			P23/SIF1/SDA00/INTP03	–	13	16
TXDC2			P36/SDA02/CTXD0[Note]	50	66	81
TXDC3			P40/SIF0/SDA01/RTP00	52	68	85
UDMF	I/O	USB data I/O (–) function	–	21	26	35
UDPF		USB data I/O (+) function	–	22	27	36
UV_{DD}	–	3.3 V positive power supply for USB	–	23	28	37
V_{DD}	–	Positive power supply for internal circuit	–	5	5	8
V_{SS}	–	Ground potential for internal circuit	–	7	7	10
X1	Input	Connecting resonator for main clock	–	8	8	11
X2	–		–	9	9	12
XT1	Input	Connecting resonator for subclock	–	8	11	14
XT2	–		–	9	12	15

Note Available only in on-chip CAN controller products.

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

1.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 1-1. For the schematic circuit diagram of each type, refer to **Figure 1-1**.

Table 1-1. Types of Pin I/O Circuits (1/3)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JE3-E	JF3-E	JG3-E
P02	NMI	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	3	3	3
P03	INTP00/ADTRG/EXCLK			–	–	4
P20	TOAB02/INTP01	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	4	4	5
P21	RTCDIV/RTCCL			–	–	6
P22	RTC1HZ/INTP02			–	–	7
P23	SIF1/TXDC1/SDA00/INTP03			–	13	16
P24	SOF1/RXDC1/SCL00/INTP04			–	14	17
P25	$\overline{\text{SCKF1}}$/TIAA30/TOAA30			–	15	18
P26	TIAA31/TOAA31/INTP05			–	16	19
P27	TIAB03/TOAB03/INTP21			4	4	5
P30	TXDC0/SIF2/TIAA00/TOAA00	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	13	17	20
P31	RXDC0/SOF2/TIAA01/TOAA01			14	18	21
P32	ASCKC0/$\overline{\text{SCKF2}}$/TIAA10/TOAA10			15	19	22
P33	SIF4/TIAA11/TOAA11			–	–	23
P34	SOF4/TIAA20/TOAA20			–	–	24
P35	$\overline{\text{SCKF4}}$/TIAA21/TOAA21 /TOAA1OFF/INTP06			–	–	80
	TIAA21/TOAA21/TOAA1OFF/INTP06			–	65	–
P36	TXDC2/SDA02/CTXD0[Note]			50	66	81
P37	RXDC2/SCL02/CRXD0[Note]			51	67	82
P40	SIF0/TXDC3/SDA01/RTP00	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	52	68	85
P41	SOF0/RXDC3/SCL01/RTP01			53	69	86
P42	$\overline{\text{SCKF0}}$/TIAA40/TOAA40/RTP02			54	70	87
P43	RTP03			–	–	88
P44	RTP04			–	–	89
P45	TIAA41/TOAA41/RTP05			–	–	90
P50	INTP07/DDI	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	16	20	25
P51	INTP08/DDO			17	21	26
P52	INTP09/DCK			18	22	27
P53	INTP10/DMS			19	23	28
P54	INTP11/$\overline{\text{DRST}}$	10-N	Input: Independently connect to V_{SS} via a resistor. Fixing to V_{DD} level is prohibited. Output: Leave open. Internally pull-down after reset by $\overline{\text{RESET}}$ pin.	20	24	29
P70 to P79	ANI0 to ANI9	11-G	Input: Independently connect to AV_{REF0} or AV_{SS} via a resistor. Output: Leave open.	64 to 55	80 to 71	100 to 91

Note Available only in on-chip CAN controller products.

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Table 1-1. Types of Pin I/O Circuits (2/3)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JE3-E	JF3-E	JG3-E
P90	TOAB1T1/TOAB11/TIAB11/KR0 /INTP12	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	–	57	72
P91	TOAB1B1/TIAB10/KR1/TOAB10			–	58	73
P92	TOAB1T2/TOAB12/TIAB12/KR2 /INTP13			–	59	74
P93	TOAB1B2/TRGAB1/KR3/INTP14			–	60	75
P94	TOAB1T3/TOAB13/TIAB13/KR4 /INTP15			–	61	76
P95	TOAB1B3/EVTB1/KR5/INTP16			–	62	77
P96	TECR0/TIT00/KR6/TOT00			–	31	40
P97	TENC00/TIT01/KR7/TOT01			–	32	41
P98	TENC01/INTP17			–	33	42
P912	TOAB1OFF/INTP18			–	63	78
P913	SIF3/INTP19			–	–	30
	INTP19			–	25	–
P914	SOF3/INTP20			–	–	31
P915	$\overline{SCKF3}$			–	–	32
PDL0 to PDL4	–	5	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	–	–	58 to 67
PDL5	FLMD1	5		49	64	79
PDL6 to PDL10	–	5		–	–	83,84, 33,34, 43
AV_{REF0}	–	–	Directly connect to V_{DD} and always supply power.	1	1	1
AV_{SS}	–	–	Directly connect to V_{SS}.	2	2	2
EV_{DD}	–	–	Directly connect to V_{DD} and always supply power.	24, 44	29, 52	38, 65
FLMD0	–	–	Connect to V_{SS} in other than flash mode.	42	50	63
P1COL	–	5	Independently connect to EV_{DD} or V_{SS} via a resistor.	46	54	69
P1CRS	–	5		45	53	68
P1MDIO	–	5		47	55	70
P1RXCLK	–	5		48	56	71
P1RXD0	–	5		39	47	57
P1RXD1	–	5		33	41	51
P1RXD2	–	5		34	42	52
P1RXD3	–	5		35	43	53
P1RXDV	–	5		36	44	54
P1RXER	–	5		37	45	55
P1TXCLK	–	5		38	46	56
P1MDC	–	5	Leave open.	32	40	50
P1TXD0	–	5		26	34	44
P1TXD1	–	5		27	35	45
P1TXD2	–	5		28	36	46
P1TXD3	–	5		29	37	47
P1TXEN	–	5		31	39	49
P1TXER	–	5		30	38	48

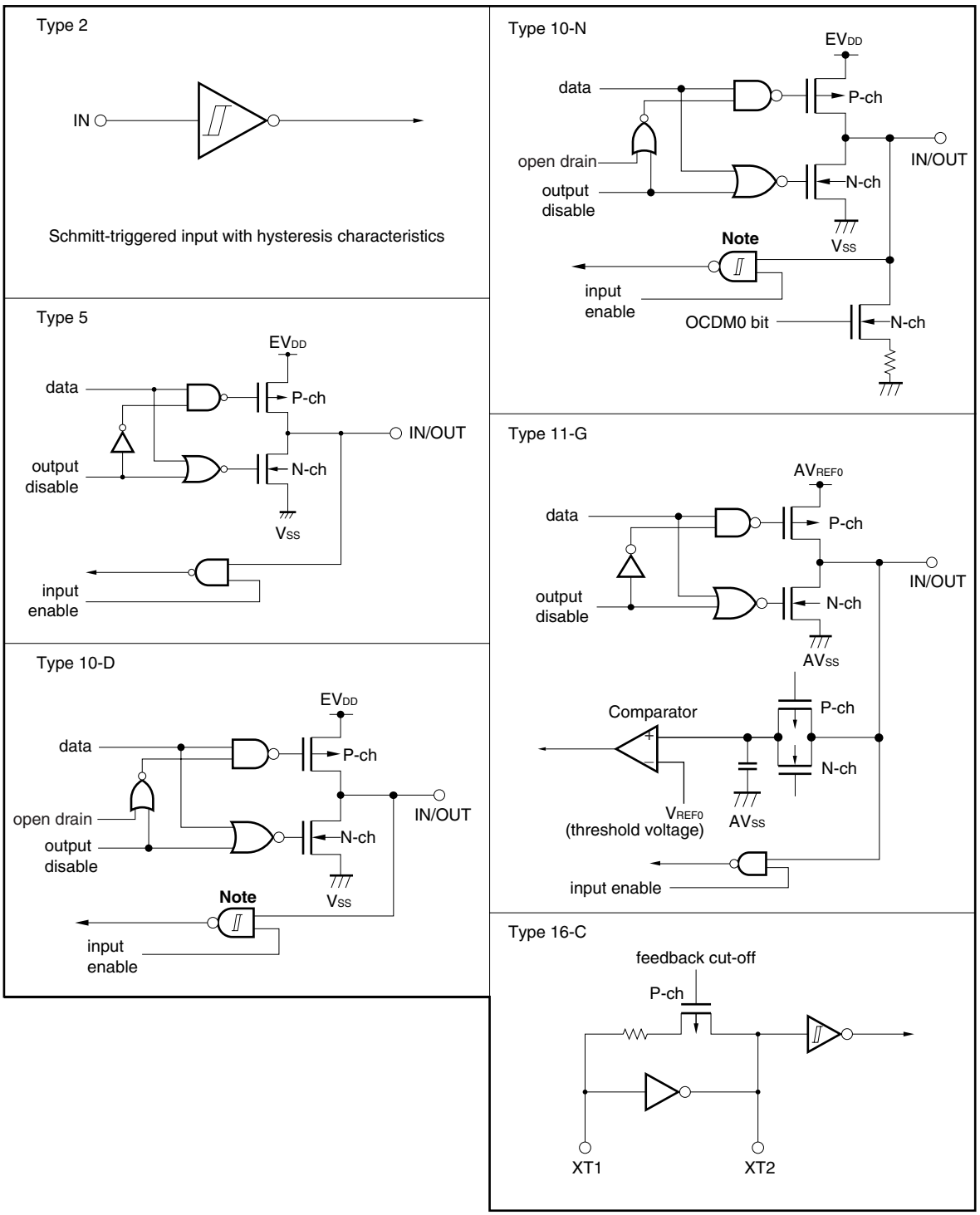
Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Table 1-1. Types of Pin I/O Circuits (3/3)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JE3-E	JF3-E	JG3-E
REGC	–	–	Connect to regulator output stabilization (4.7 μF (preliminary value)) capacitor.	6, 41	6, 49	9, 62
$\overline{\text{RESET}}$	–	2	–	10	10	13
UDMF	–	–	Leave open.	21	26	35
UDPF	–	–	Leave open.	22	27	36
UV_{DD}	–	–	Directly connect to V_{DD} and always supply power.	23	28	37
V_{DD}	–	–	–	5	5	8
V_{SS}	–	–	–	7	7	10
X1	–	–	–	8	8	11
X2	–	–	–	9	9	12
XT1	–	16-C	Connect to V_{SS} via a resistor.	8	11	14
XT2	–	16-C	Leave open.	9	12	15

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Figure 1-1. Pin I/O Circuits



Note Hysteresis characteristics are not available in port mode.