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User's Manual

32

V850ES/JC3-L, V850ES/JE3-L

User's Manual: Hardware

RENESAS MCU
V850ES/Jx3-L Microcontrollers

V850ES/JC3-L		V850ES/JE3-L
μPD70F3797	μPD70F3802	μPD70F3805
μPD70F3798	μPD70F3803	μPD70F3806
μPD70F3799	μPD70F3804	μPD70F3807
μPD70F3800	μPD70F3838	μPD70F3808
μPD70F3801	μPD70F3839	μPD70F3840

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(2012.4)

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

How to Use This Manual

Readers

This manual is intended for users who wish to understand the functions of the V850ES/JC3-L, V850ES/JE3-L and design application systems using these products.

Purpose

This manual is intended to give users an understanding of the hardware functions of the V850ES/JC3-L, V850ES/JE3-L shown in the **Organization** below.

Organization

This manual is divided into two parts: Hardware (this manual) and Architecture (**V850ES Architecture User's Manual**).

Hardware	Architecture
• Pin functions	• Data types
• CPU function	• Register set
• On-chip peripheral functions	• Instruction format and instruction set
• Flash memory programming	• Interrupts and exceptions
• Electrical specifications (Target)	• Pipeline operation

How to Read This Manual

It is assumed that the readers of this manual have general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

To understand the overall functions of the V850ES/JC3-L, V850ES/JE3-L
→Read this manual according to the **CONTENTS**.

To find the details of a register where the name is known
→Use **APPENDIX C REGISTER INDEX**.

Register format
→The name of the bit whose number is in angle brackets (<>) in the figure of the register format of each register is defined as a reserved word in the device file.

To understand the details of an instruction function
→Refer to the **V850ES Architecture User's Manual** available separately.

To know the electrical specifications of the V850ES/JC3-L (40-pin)
→ See **CHAPTER 30 ELECTRICAL SPECIFICATIONS (V850ES/JC3-L (40-pin)) (Target)**

To know the electrical specifications of the V850ES/JC3-L (48-pin)
→ See **CHAPTER 31 ELECTRICAL SPECIFICATIONS (V850ES/JC3-L (48-pin)) (Target)**

To know the electrical specifications of the V850ES/JE3-L
→ See **CHAPTER 32 ELECTRICAL SPECIFICATIONS (V850ES/JE3-L) (Target)**

The "yyy bit of the xxx register" is described as the "xxx.yyy bit" in this manual. Note with caution that if "xxx.yyy" is described as is in a program, however, the compiler/assembler cannot recognize it correctly.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Memory map address:	Higher addresses on the top and lower addresses on the bottom
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH

Prefix indicating power of 2 (address space, memory capacity):

K (kilo): $2^{10} = 1,024$

M (mega): $2^{20} = 1,024^2$

G (giga): $2^{30} = 1,024^3$

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850ES/JC3-L, V850ES/JE3-L

Document Name	Document No.
V850ES Architecture User's Manual	U15943E
V850ES/JC3-L, V850ES/JE3-L Hardware User's Manual	This manual

Documents related to development tools

Document Name		Document No.
QB-V850ESJX3L In-Circuit Emulator		To be prepared
QB-V850MINI, QB-V850MINIL On-Chip Debug Emulator		U17638E
QB-MINI2 On-Chip Debug Emulator with Programming Function		U18371E
CA850 Ver. 3.20 C Compiler Package	Operation	U18512E
	C Language	U18513E
	Assembly Language	U18514E
	Link Directives	U18415E
PM+ Ver. 6.30 Project Manager		U18416E
ID850QB Ver. 3.40 Integrated Debugger	Operation	U18604E
SM850 Ver. 2.50 System Simulator	Operation	U16218E
SM850 Ver. 2.00 or Later System Simulator	External Part User Open Interface Specification	U14873E
SM+ System Simulator	Operation	U18601E
	User Open Interface	U18212E
RX850 Ver. 3.20 Real-Time OS	Basics	U13430E
	Installation	U17419E
	Technical	U13431E
	Task Debugger	U17420E
RX850 Pro Ver. 3.21 Real-Time OS	Basics	U18165E
	Installation	U17421E
	Task Debugger	U17422E
AZ850 Ver. 3.30 System Performance Analyzer		U17423E
PG-FP5 Flash Memory Programmer		U18865E

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE − Products and Packages −	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on Renesas Semiconductor Devices	C11531E
Renesas Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the “Semiconductor Device Mount Manual” website (http://www2.renesas.com/pkg/en/mount/index.html).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

Table of Contents

CHAPTER 1 INTRODUCTION

The V850ES/JC3-L and V850ES/JE3-L are one of the products in the Renesas Electronics V850 single-chip microcontroller series designed for low-power operation for real-time control applications.

1.1 General

The V850ES/JC3-L and V850ES/JE3-L are 32-bit single-chip microcontrollers that include the V850ES CPU core and peripheral functions such as ROM/RAM, timer/counters, serial interfaces, an A/D converter, a D/A converter.

In addition to high real-time response characteristics and 1-clock-pitch basic instructions, the The V850ES/JC3-L and V850ES/JE3-L feature multiply instructions, saturated operation instructions, bit manipulation instructions, etc., realized by a hardware multiplier, as optimum instructions for digital servo control applications. Moreover, as a real-time control system, the V850ES/JC3-L and V850ES/JE3-L enable an extremely high cost-performance for applications that require super low power consumption, such as PC peripheral device, ECR peripheral device, and industrial instrument.

Table 1-1. V850ES/JC3-L Product List (1/2)

Generic Name		V850ES/JC3-L				
Part Number		μPD70F3797	μPD70F3798	μPD70F3799	μPD70F3800	μPD70F3838
Internal memory	Flash memory	16 KB	32 KB	64 KB	128 KB	256 KB
	RAM	8 KB	8 KB	8 KB	8 KB	16 KB
Memory space		64 MB				
General-purpose register		32 bits × 32 registers				
Clock	Main clock (oscillation frequency)	Ceramic/crystal (in PLL mode: f_X = 2.5 to 5 MHz (multiplied by 4), in clock through mode: f_X = 2.5 to 10 MHz) External clock (in PLL mode: f_X = 2.5 to 5 MHz (multiplied by 4), in clock through mode: f_X = 2.5 to 5 MHz				
	Subclock (oscillation frequency)	Crystal (f_{XT} = 32.768 kHz)				
	Internal oscillator	f_R = 220 kHz (TYP.)				
	Minimum instruction execution time	50 ns (main clock (f_{XX}) = 20 MHz)				
I/O port		I/O: 27 (5 V tolerant/N-ch open-drain output selectable: 17)				
Timer	16-bit TMP	6 channels				
	16-bit TMQ	1 channel				
	16-bit TMM	1 channel				
	Watch timer	1 channel				
	RTC	1 channel				
	WDT	1 channel				
Real-time output port		4 bits × 1 channel, 2 bits × 1 channel, or 6 bits × 1 channel				
10-bit A/D converter		5 channels				
8-bit D/A converter		–				
Serial interface	CSIB	1 channel				
	UARTA/CSIB	–				
	CSIB/I^2C bus	1 channel				
	UARTA/I^2C bus	1 channel				
	UARTA	1 channel				
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)				
Interrupt source	External	6 (6)[Note]				
	Internal	42				
Power save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE/ low-voltage STOP/low-voltage subclock/low-voltage sub-IDLE mode				
Reset source		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)				
CRC function		16-bit error detection code generated for 8-bit unit data				
On-chip debug		MINICUBE®, MINICUBE2 supported				
Operating power supply voltage		2.2 to 3.6 V @5 MHz, 2.7 to 3.6 V @20 MHz				
Operating ambient temperature		–40 to +85°C				
Package		40-pin WQFN (6 × 6 mm)				

Note The figure in parentheses indicates the number of external interrupts that can release STOP mode.

Table 1-1. V850ES/JC3-L Product List (2/2)

Generic Name		V850ES/JC3-L				
Part Number		μPD70F3801	μPD70F3802	μPD70F3803	μPD70F3804	μPD70F3839
Internal memory	Flash memory	16 KB	32 KB	64 KB	128 KB	256 KB
	RAM	8 KB	8 KB	8 KB	8 KB	16 KB
Memory space		64 MB				
General-purpose register		32 bits × 32 registers				
Clock	Main clock (oscillation frequency)	Ceramic/crystal (in PLL mode: f_X = 2.5 to 5 MHz (multiplied by 4), in clock through mode: f_X = 2.5 to 10 MHz) External clock (in PLL mode: f_X = 2.5 to 5 MHz (multiplied by 4), in clock through mode: f_X = 2.5 to 5 MHz				
	Subclock (oscillation frequency)	Crystal (f_{XT} = 32.768 kHz)				
	Internal oscillator	f_R = 220 kHz (TYP.)				
	Minimum instruction execution time	50 ns (main clock (f_{XX}) = 20 MHz)				
I/O port		I/O: 34 (5 V tolerant/N-ch open-drain output selectable: 20)				
Timer	16-bit TMP	6 channels				
	16-bit TMQ	1 channel				
	16-bit TMM	1 channel				
	Watch timer	1 channel				
	RTC	1 channel				
	WDT	1 channel				
Real-time output port		4 bits × 1 channel, 2 bits × 1 channel, or 6 bits × 1 channel				
10-bit A/D converter		6 channels				
8-bit D/A converter		1 channel				
Serial interface	CSIB	2 channels				
	UARTA/CSIB	1 channel				
	CSIB/I^2C bus	1 channel				
	UARTA/I^2C bus	2 channels				
	UARTA	–				
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)				
Interrupt source	External	6 (6)[Note]				
	Internal	46				
Power save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE/ low-voltage STOP/low-voltage subclock/low-voltage sub-IDLE mode				
Reset source		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)				
CRC function		16-bit error detection code generated for 8-bit unit data				
On-chip debug		MINICUBE, MINICUBE2 supported				
Operating power supply voltage		2.2 to 3.6 V @5 MHz, 2.7 to 3.6 V @20 MHz				
Operating ambient temperature		–40 to +85°C				
Package		48-pin LQFP (7 × 7 mm), 48-pin WQFN (7 × 7 mm)				

Note The figure in parentheses indicates the number of external interrupts that can release STOP mode.

Table 1-2. V850ES/JE3-L Product List

Generic Name		V850ES/JE3-L				
Part Number		μPD70F3805	μPD70F3806	μPD70F3807	μPD70F3808	μPD70F3840
Internal memory	Flash memory	16 KB	32 KB	64 KB	128 KB	256 KB
	RAM	8 KB	8 KB	8 KB	8 KB	16 KB
Memory space		64 MB				
General-purpose register		32 bits × 32 registers				
Clock	Main clock (oscillation frequency)	Ceramic/crystal (in PLL mode: f_X = 2.5 to 5 MHz (multiplied by 4), in clock through mode: f_X = 2.5 to 10 MHz) External clock (in PLL mode: f_X = 2.5 to 5 MHz (multiplied by 4), in clock through mode: f_X = 2.5 to 5 MHz)				
	Subclock (oscillation frequency)	Crystal (f_{XT} = 32.768 kHz)				
	Internal oscillator	f_R = 220 kHz (TYP.)				
	Minimum instruction execution time	50 ns (main clock (f_{XX}) = 20 MHz)				
I/O port		I/O: 50 (5 V tolerant/N-ch open-drain output selectable: 28)				
Timer	16-bit TMP	6 channels				
	16-bit TMQ	1 channel				
	16-bit TMM	1 channel				
	Watch timer	1 channel				
	RTC	1 channel				
	WDT	1 channel				
Real-time output port		4 bits × 1 channel, 2 bits × 1 channel, or 6 bits × 1 channel				
10-bit A/D converter		10 channels				
8-bit D/A converter		1 channel				
Serial interface	CSIB	3 channels				
	UARTA/CSIB	1 channel				
	CSIB/I^2C bus	1 channel				
	UARTA/I^2C bus	2 channels				
	UARTA	–				
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)				
Interrupt source	External	9 (9)[Note]				
	Internal	48				
Power save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE/ low-voltage STOP/low-voltage subclock/low-voltage sub-IDLE mode				
Reset source		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)				
CRC function		16-bit error detection code generated for 8-bit unit data				
On-chip debug		MINICUBE, MINICUBE2 supported				
Operating power supply voltage		2.2 to 3.6 V @5 MHz, 2.7 to 3.6 V @20 MHz				
Operating ambient temperature		–40 to +85°C				
Package		64-pin LQFP (10 × 10 mm)				

Notes The figure in parentheses indicates the number of external interrupts that can release STOP mode.

1.2 Features

- Minimum instruction execution time: 50 ns (operating on main clock (f_{XX}) of 20 MHz: V_{DD} = 2.7 to 3.6 V)
  200 ns (operating on main clock (f_{XX}) of 5 MHz: V_{DD} = 2.2 to 3.6 V)
  30.5 μs (operating on subclock (f_{XT}) of 32.768 kHz)
- General-purpose registers: 32 bits × 32 registers
- CPU features: Signed multiplication (16 × 16 → 32): 1 to 2 clocks
  Signed multiplication (32 × 32 → 64): 1 to 5 clocks
  Saturated operations (overflow and underflow detection functions included)
  Most instructions can be executed in 1 clock cycle by using 32-bit RISC-based 5-stage pipeline architecture
  Instruction fetching from internal ROM and accessing internal RAM for data can be executed separately, by using Harvard architecture
  High code efficiency achieved by using variable length instructions
  32-bit shift instruction: 1 clock cycle
  Bit manipulation instructions
  Load/store instructions with long/short format
- Memory space: 64 MB of linear address space (for programs and data)
  - Internal memory: RAM: 8/16 KB (see **Tables 1-1** and **1-2**)
    Flash memory: 16/32/64/128/256 KB (see **Tables 1-1** and **1-2**)
- Interrupts and exceptions:

		Internal			external:		
		maskable	Non-maskable	total	maskable	Non-maskable	total
V850ES/JC3-L (40-pin)	μPD70F3797	1	42	43	1	5	6
	μPD70F3798						
	μPD70F3799						
	μPD70F3800						
	μPD70F3838						
V850ES/JC3-L (48-pin)	μPD70F3801	1	46	47	1	5	6
	μPD70F3802						
	μPD70F3803						
	μPD70F3804						
	μPD70F3839						
V850ES/JE3-L	μPD70F3805	1	48	49	1	8	9
	μPD70F3806						
	μPD70F3807						
	μPD70F3808						
	μPD70F3840						

  Software exceptions: 32 sources
  Exception trap: 2 sources
- Ports: I/O ports: 27/34/50 (see **Tables 1-1** and **1-2**)

- Timer function: 16-bit interval timer M (TMM): 1 channel
  16-bit timer/event counter P (TMP): 6 channels
  16-bit timer/event counter Q (TMQ): 1 channel
  Watch timer: 1 channel
  Watchdog timer: 1 channel

  Note The available functions differ for each product. For details, see **CHAPTER 6 16-BIT TIMER/EVENT COUNTER P (TMP)**.

- Real-time counter: 1 channel
- Real-time output port: 6 bits × 1 channel
- Serial interface: For details about the number of incorporated channels, see **Tables 1-1** and **1-2**.
  Asynchronous serial interface A (UARTA)
  Clocked serial interface B (CSIB)
  I^2C bus interface (I^2C)
- A/D converter: 10-bit resolution: 5/6/10 channels (see **Tables 1-1** and **1-2**)
- D/A converter: 8-bit resolution: 0/1 channels (see **Tables 1-1** and **1-2**)
- DMA controller: 4 channels
- DCU (debug control unit): JTAG interface
- Clock generator: During main clock or subclock operation
  7-level CPU clock (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, f_{XT})
  Clock-through mode/PLL mode selectable
- Internal oscillator clock: 220 kHz (TYP.)
- Power-save functions: HALT/IDLE1/IDLE2/STOP/low-voltage STOP/subclock/sub-IDLE/low-voltage subclock/low-voltage sub-IDLE mode
- Package: V850ES/JC3-L
  40-pin plastic WQFN (6 × 6)
  48-pin plastic LQFP (fine pitch) (7 × 7)
  48-pin plastic WQFN (7 × 7)
  V850ES/JE3-L
  64-pin plastic LQFP (fine pitch) (8 × 8)
- Power supply voltage: V_{DD} = 2.2 V to 3.6 V (5 MHz)
  V_{DD} = 2.7 V to 3.6 V (20 MHz)

1.3 Application Fields

Digital cameras, electrical power meters, mobile terminals, digital home electronics, other consumer devices

.

1.4 Ordering Information

1.4.1 V850ES/JC3-L

Part Number	Package	Internal Flash Memory
μPD70F3797K8-4B4-AX	40-pin plastic WQFN (6 × 6)	16 KB
μPD70F3798K8-4B4-AX	40-pin plastic WQFN (6 × 6)	32 KB
μPD70F3799K8-4B4-AX	40-pin plastic WQFN (6 × 6)	64 KB
μPD70F3800K8-4B4-AX	40-pin plastic WQFN (6 × 6)	128 KB
μPD70F3838K8-4B4-AX	40-pin plastic WQFN (6 × 6)	256 KB
μPD70F3801GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	16 KB
μPD70F3802GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	32 KB
μPD70F3803GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	64 KB
μPD70F3804GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	128 KB
μPD70F3839GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	256 KB
μPD70F3801K8-5B4-AX	48-pin plastic WQFN (7 × 7)	16 KB
μPD70F3802K8-5B4-AX	48-pin plastic WQFN (7 × 7)	32 KB
μPD70F3803K8-5B4-AX	48-pin plastic WQFN (7 × 7)	64 KB
μPD70F3804K8-5B4-AX	48-pin plastic WQFN (7 × 7)	128 KB
μPD70F3839K8-5B4-AX	48-pin plastic WQFN (7 × 7)	256 KB

Remark The V850ES/JC3-L is a lead-free product.

1.4.2 V850ES/JE3-L

Part Number	Package	Internal Flash Memory
μPD70F3805GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	16 KB
μPD70F3806GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	32 KB
μPD70F3807GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	64 KB
μPD70F3808GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	128 KB
μPD70F3840GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB

Remark The V850ES/JE3-L is a lead-free product.