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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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RENESAS

User's Manual

78K0/LE3

8-Bit Single-Chip Microcontrollers

μPD78F0441	μPD78F0451	μPD78F0461
μPD78F0442	μPD78F0452	μPD78F0462
μPD78F0443	μPD78F0453	μPD78F0463
μPD78F0444	μPD78F0454	μPD78F0464
μPD78F0445	μPD78F0455	μPD78F0465

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[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

INTRODUCTION

Readers

This manual is intended for user engineers who wish to understand the functions of the 78K0/LE3 and design and develop application systems and programs for these devices. The target products are as follows.

78K0/LE3: μPD78F0441, 78F0442, 78F0443, 78F0444, 78F0445,
μPD78F0451, 78F0452, 78F0453, 78F0454, 78F0455,
μPD78F0461, 78F0462, 78F0463, 78F0464, 78F0465

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The 78K0/LE3 manual is separated into two parts: this manual and the instructions edition (common to the 78K0 microcontrollers).

78K0/LE3 User's Manual (This Manual)	**78K/0 Series User's Manual Instructions**
• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.
- How to interpret the register format:
  → For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.
- To know details of the 78K0 microcontroller instructions:
  → Refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
78K0/LE3 User's Manual	This manual
78K/0 Series Instructions User's Manual	U12326E
78K0 Microcontrollers Self Programming Library Type01 User's Manual[Note]	U18274E
78K0 Microcontrollers EEPROM™ Emulation Library Type01 User's Manual[Note]	U18275E

Note This document is under engineering management. For details, consult an NEC Electronics sales representative.

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0 Ver. 3.80 Assembler Package	Operation	U17199E
	Language	U17198E
	Structured Assembly Language	U17197E
CC78K0 Ver. 3.70 C Compiler	Operation	U17201E
	Language	U17200E
ID78K0-QB Ver. 3.00 Integrated Debugger	Operation	U18492E
PM+ Ver. 6.30		U18416E

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
QB-78K0LX3 In-Circuit Emulator	U18511E
QB-MINI2 On-Chip Debug Emulator with Programming Function	U18371E

Documents Related to Flash Memory Programming

Document Name	Document No.
PG-FP5 Flash Memory Programme	U18865E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE − Products and Packages −	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the “Semiconductor Device Mount Manual” website (http://www.necel.com/pkg/en/mount/index.html).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

CONTENTS

CHAPTER 1 OUTLINE

1.1 Features

- Minimum instruction execution time can be changed from high speed (0.2 μs: @ 10 MHz operation with high-speed system clock) to ultra low-speed (122 μs: @ 32.768 kHz operation with subsystem clock)
- General-purpose register: 8 bits × 32 registers (8 bits × 8 registers × 4 banks)
- ROM, RAM capacities

Item / Part Number	Program Memory (ROM)		Data Memory		
			Internal High-Speed RAM[Note 1]	Internal Expansion RAM[Note 1]	LCD Display RAM
μPD78F0441, 78F0451, 78F0461	Flash memory[Note 1]	16 KB	768 bytes	–	<μPD78F044x, 78F045x> 32 × 4 bits (28 × 8 bits) [28 × 4 bits (24 × 8 bits)][Note 2]
μPD78F0442, 78F0452, 78F0462		24 KB	1 KB		
μPD78F0443, 78F0453, 78F0463		32 KB			
μPD78F0444, 78F0454, 78F0464		48 KB		1 KB	<μPD78F046x> 24 × 4 bits (20 × 8 bits) [20 × 4 bits (16 × 8 bits)][Note 2]
μPD78F0445, 78F0455, 78F0465		60 KB			

Notes 1. The internal flash memory, internal high-speed RAM capacities, and internal expansion RAM capacities can be changed using the internal memory size switching register (IMS) and the internal expansion RAM size switching register (IXS).

<R> **2.** The items in parentheses are applicable when 8com is used.
The items in square brackets are applicable when using the UART6 pins (RxD6, TxD6) on the bottom side.

- On-chip single-power-supply flash memory
- Self-programming (with boot swap function)
- On-chip debug function
- On-chip power-on-clear (POC) circuit and low-voltage detector (LVI)
- On-chip watchdog timer (operable with internal low-speed oscillation clock)
- LCD controller/driver (external resistance division and internal resistance division are switchable)

μPD78F044x: Segment signals: 28, Common signals: 8 (1/4 bias)
: Segment signals: 32, Common signals: 4 (1/3 bias)
: Segment signals: 32, Common signals: 3 (1/3, 1/2 bias)
: Segment signals: 32, Common signals: 2 (1/2 bias)
: Segment signals: 32, Common signals: 1 (Static)

μPD78F045x: Segment signals: 28, Common signals: 8 (1/4 bias)
: Segment signals: 32, Common signals: 4 (1/3 bias)
: Segment signals: 32, Common signals: 3 (1/3, 1/2 bias)
: Segment signals: 32, Common signals: 2 (1/2 bias)
: Segment signals: 32, Common signals: 1 (Static)

μPD78F046x: Segment signals: 20, Common signals: 8 (1/4 bias)
: Segment signals: 24, Common signals: 4 (1/3 bias)
: Segment signals: 24, Common signals: 3 (1/3, 1/2 bias)
: Segment signals: 24, Common signals: 2 (1/2 bias)
: Segment signals: 24, Common signals: 1 (Static)

<R> ○ On-chip segment key scan function: 8 channels
○ On-chip key interrupt function: 5 channels
○ On-chip buzzer output controller
○ I/O ports: 46
○ Timer: 9 channels
- 16-bit timer/event counter: 1 channel
- 8-bit timer/event counter: 3 channels
- 8-bit timer: 3 channels
- Real-time counter (RTC): 1 channel
- Watchdog timer: 1 channel

○ Serial interface: 2 channels
- UART (LIN (Local Interconnect Network)-bus supported): 1 channel
- CSI/UART[Note]: 1 channel

Note Select either of the functions of these alternate-function pins.

○ 16-bit ΔΣ type A/D converter[Note]: 3 channels (μPD78F046x only)
○ 10-bit successive approximation type A/D converter: 8 channels (μPD78F045x and 78F046x only)
○ Remote controller receiver
○ Manchester code generator
○ Power supply voltage: V_{DD} = 1.8 to 5.5 V
○ Operating ambient temperature: T_A = −40 to +85°C

Note The specifications of the 16-bit ΔΣ A/D converter may have been changed.
For details of the specifications, contact an NEC Electronics sales representative or authorized dealer.

1.2 Applications

Digital cameras, AV equipments, household electrical appliances, utility meters, health care equipments, and measurement equipment, etc.

1.3 Ordering Information

- **Flash memory version (Lead-free products)**

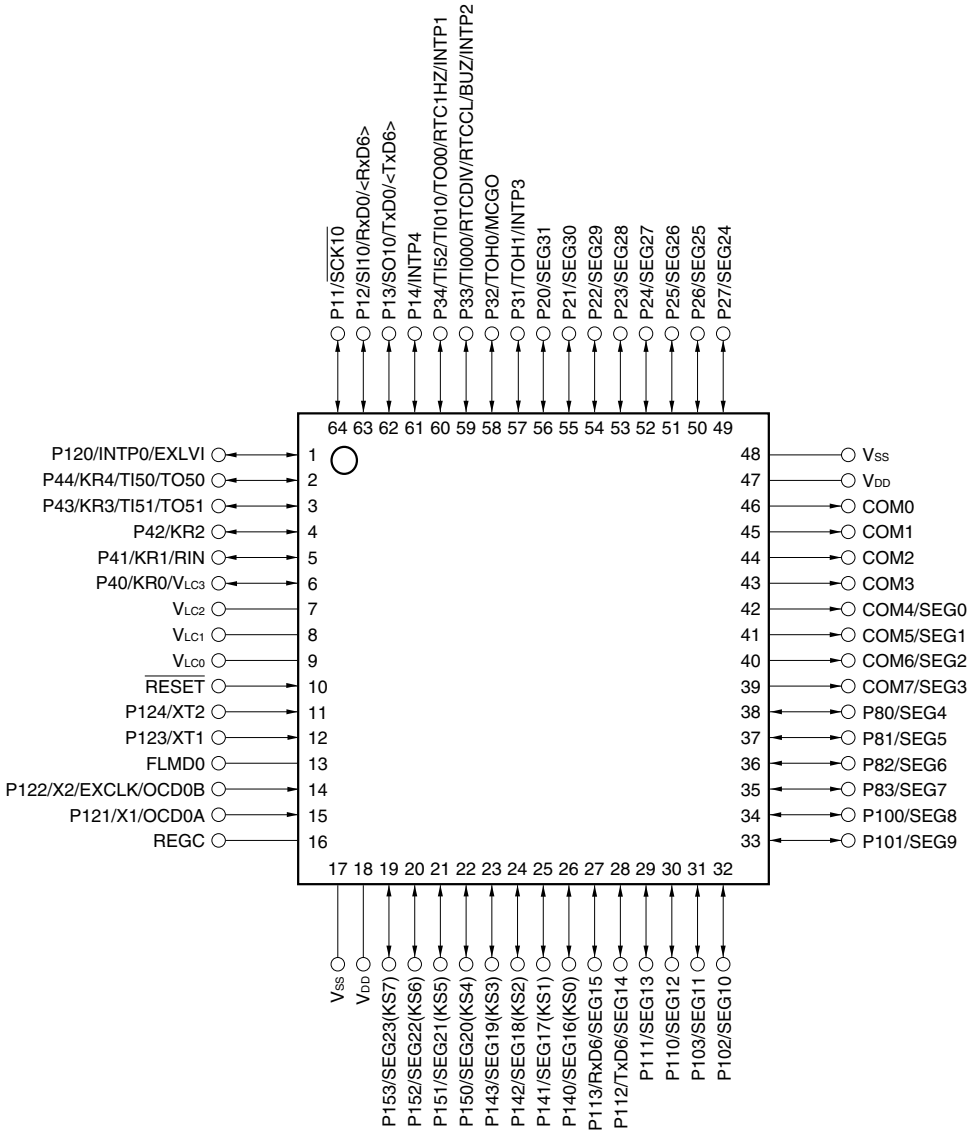
Part Number	Package
μPD78F0441GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0442GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0443GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0444GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0445GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0441GK-GAJ-AX	64-pin plastic LQFP (12 × 12)
μPD78F0442GK-GAJ-AX	64-pin plastic LQFP (12 × 12)
μPD78F0443GK-GAJ-AX	64-pin plastic LQFP (12 × 12)
μPD78F0444GK-GAJ-AX	64-pin plastic LQFP (12 × 12)
μPD78F0445GK-GAJ-AX	64-pin plastic LQFP (12 × 12)
μPD78F0451GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0452GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0453GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0454GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0455GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0451GK-GAJ-AX	64-pin plastic LQFP (12 × 12)
μPD78F0452GK-GAJ-AX	64-pin plastic LQFP (12 × 12)
μPD78F0453GK-GAJ-AX	64-pin plastic LQFP (12 × 12)
μPD78F0454GK-GAJ-AX	64-pin plastic LQFP (12 × 12)
μPD78F0455GK-GAJ-AX	64-pin plastic LQFP (12 × 12)
μPD78F0461GB-GAH-AX[Note]	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0462GB-GAH-AX[Note]	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0463GB-GAH-AX[Note]	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0464GB-GAH-AX[Note]	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0465GB-GAH-AX[Note]	64-pin plastic LQFP (fine pitch) (10 × 10)
μPD78F0461GK-GAJ-AX[Note]	64-pin plastic LQFP (12 × 12)
μPD78F0462GK-GAJ-AX[Note]	64-pin plastic LQFP (12 × 12)
μPD78F0463GK-GAJ-AX[Note]	64-pin plastic LQFP (12 × 12)
μPD78F0464GK-GAJ-AX[Note]	64-pin plastic LQFP (12 × 12)
μPD78F0465GK-GAJ-AX[Note]	64-pin plastic LQFP (12 × 12)

Note Under development

1.4 Pin Configuration (Top View)

(1) μPD78F0441, 78F0442, 78F0443, 78F0444, 78F0445

- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic LQFP (12 × 12)



Cautions 1. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF: recommended).

2. Only the bottom side pins (pin numbers 27 and 28) correspond to the UART6 pins (RxD6 and TxD6) when writing by a flash memory programmer. Writing cannot be performed by the top side pins (pin numbers 63 and 62).

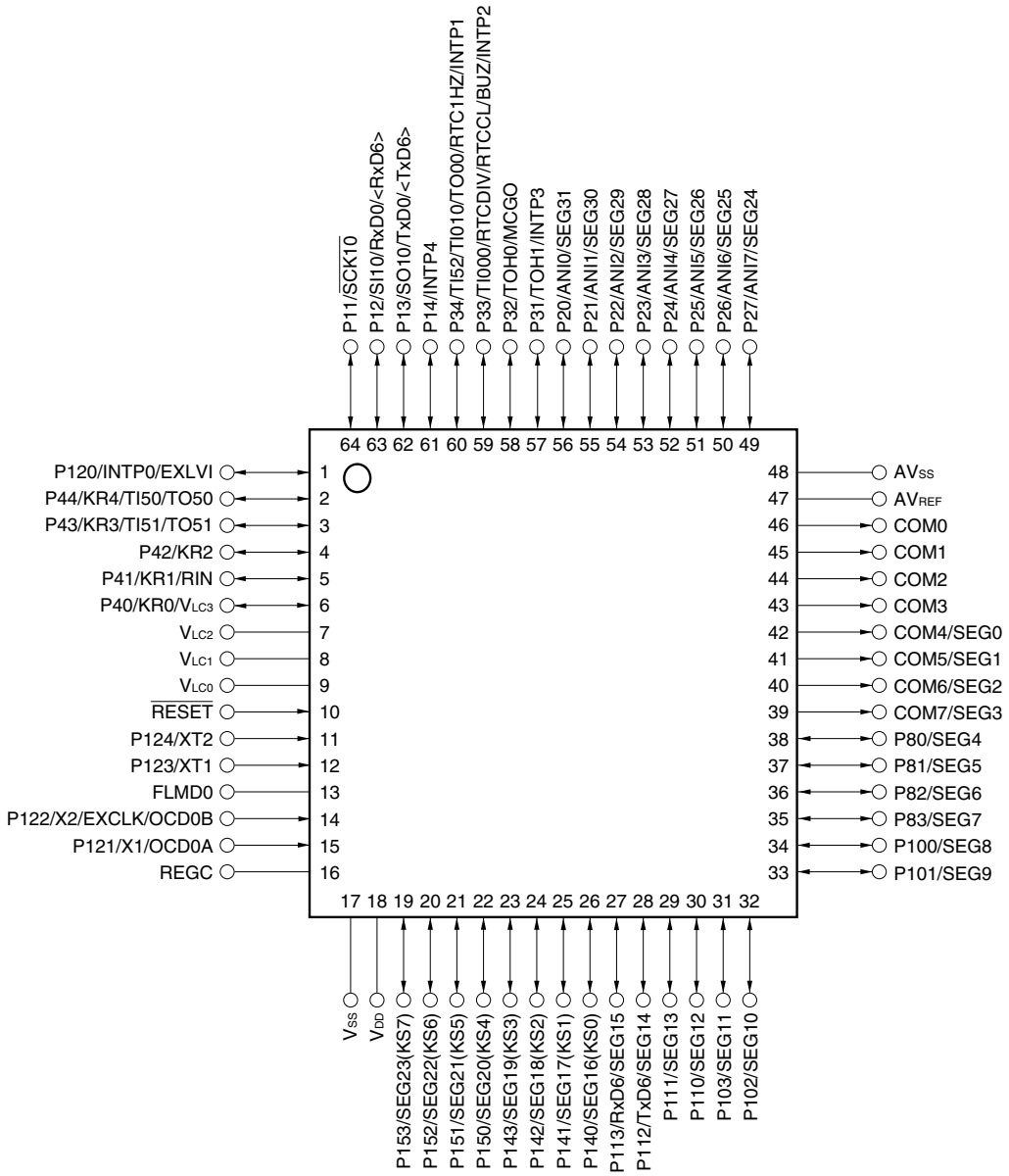
3. Make VDD (pin number 18) and VDD (pin number 47), VSS (pin number 17) and VSS (pin number 48) the same potential.

Remarks 1. The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

<R> **2.** The functions within parentheses can be used by setting the LCD mode register (LCDMD).

(2) μPD78F0451, 78F0452, 78F0453, 78F0454, 78F0455

- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic LQFP (12 × 12)



Cautions 1. Connect the AVSS pin to VSS.

2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF: recommended).

3. ANI0/P20 to ANI7/P27 are set in the analog input mode after release of reset.

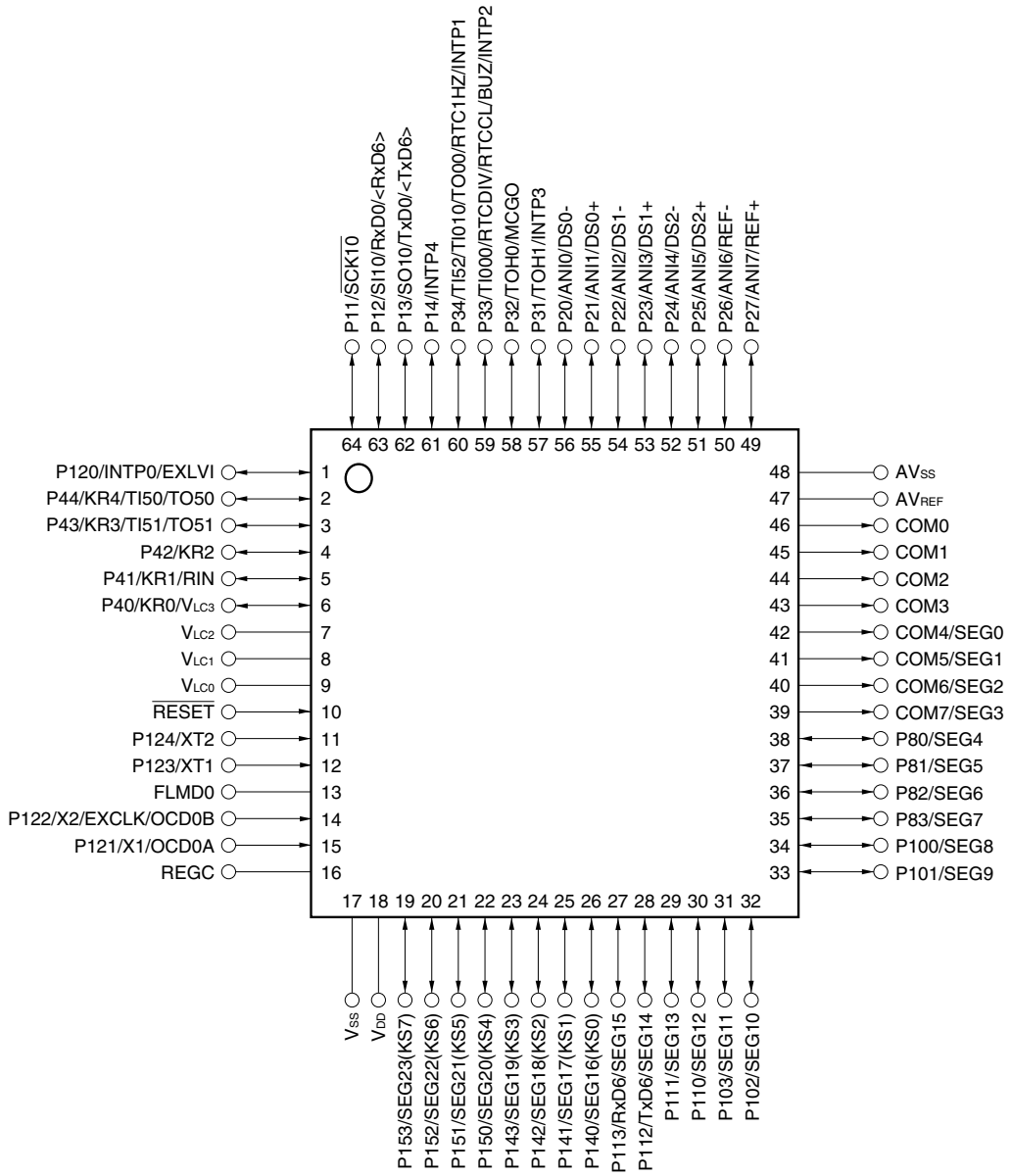
4. Only the bottom side pins (pin numbers 27 and 28) correspond to the UART6 pins (RxD6 and TxD6) when writing by a flash memory programmer. Writing cannot be performed by the top side pins (pin numbers 63 and 62).

Remarks 1. The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

<R> **2.** The functions within parentheses can be used by setting the LCD mode register (LCDMD).

(3) μPD78F0461, 78F0462, 78F0463, 78F0464, 78F0465

- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic LQFP (12 × 12)



Cautions 1. Connect the AVSS pin to VSS.

2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF: recommended).

3. ANI0/P20 to ANI7/P27 are set in the analog input mode after release of reset.

4. Only the bottom side pins (pin numbers 27 and 28) correspond to the UART6 pins (RxD6 and TxD6) when writing by a flash memory programmer. Writing cannot be performed by the top side pins (pin numbers 63 and 62).

Remarks 1. The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

<R> **2.** The functions within parentheses can be used by setting the LCD mode register (LCDMD).

Pin Identification

ANI0 to ANI7[Note 1]: Analog input
AV_{REF}[Note 1]: Analog reference voltage
AV_{SS}[Note 1]: Analog ground
BUZ: Buzzer output
COM0 to COM7: Common output
DS0+ to DS2+[Note 2]: ΔΣ Analog input (+)
DS0− to DS2−[Note 2]: ΔΣ Analog input (−)
EXCLK: External clock input (main system clock)
EXLVI: External potential input for low-voltage detector
FLMD0: Flash programming mode
INTP0 to INTP4: External interrupt input
KR0 to KR4: Key return
MCGO: Manchester code generator output
OCD0A, OCD0B: On chip debug input/output
P11 to P14: Port 1
P20 to P27: Port 2
P31 to P34: Port 3
P40 to P44: Port 4
P80 to P83: Port 8
P100 to P103: Port 10
P110 to P113: Port 11
P120 to P124: Port 12
P140 to P143: Port 14
P150 to P153: Port 15
REGC: Regulator capacitance
$\overline{RESET}$: Reset
RxD0, RxD6: Receive data
REF+[Note 2]: ΔΣ Analog reference voltage (+)
REF−[Note 2]: ΔΣ Analog reference voltage (−)
RIN: Remote control input
RTC1HZ: Real-time counter correction clock (1 Hz) output
RTCCL: Real-time counter clock (32.768 kHz original oscillation) output
RTCDIV: Real-time counter clock (32.768 kHz divided frequency) output
SEG0 to SEG23: Segment output
SEG24 to SEG31[Note 3]: Segment output
SEG16 (KS0) to SEG23 (KS7): Segment key scan
$\overline{SCK10}$: Serial clock input/output
SI10: Serial data input
SO10: Serial data output
TI000, TI010: Timer input
TI50, TI51, TI52: Timer input
TO00: Timer output
TO50, TO51: Timer output
TOH0, TOH1: Timer output
TxD0, TxD6: Transmit data
V_{DD}: Power supply
V_{SS}: Ground
V_{LC0} to V_{LC3}: LCD power supply
X1, X2: Crystal oscillator (main system clock)
XT1, XT2: Crystal oscillator (subsystem clock)

Notes 1. μPD78F045x and 78F046x only.
2. μPD78F046x only.
3. μPD78F044x and 78F045x only.