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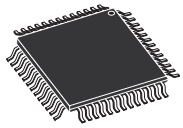
UPSD33xx

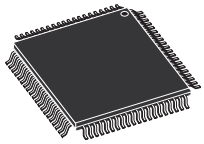
Turbo series
fast 8032 MCU with programmable logic

Features

- Fast 8-bit Turbo 8032 MCU, 40 MHz
  - Advanced core, 4-clocks per instruction
  - 10 MIPs, peak performance at 40 MHz (5 V)
  - JTAG debug and in-system programming
  - Branch cache and6 instruction prefetch queue
  - Dual XDATA pointers with auto increment and decrement
  - Compatible with 3rd party 8051 tools
- Dual Flash memories with memory management
  - Place either memory into 8032 program address space or data address space
  - Read-while-write operation for in-application programming and EEPROM emulation
  - Single voltage program and erase
  - 100K guaranteed erase cycles, 15-year retention
- Clock, reset, and supply management
  - Flexible 8-level CPU clock divider register
  - Normal, Idle, and Power-down modes
  - Power-on and low voltage reset supervisor
  - Programmable watchdog timer
- Programmable logic, general purpose
  - 16 macrocells
  - Create shifters, state machines, chip-selects, glue-logic to keypads, panels, LCDs, others



LQFP52 (T) 52-lead, thin, quad, Flat



LQFP80 (U) 80-lead, thin, quad, flat

- Packages are ECOPACK®
- Communication interfaces
  - I^2C master/slave controller, 833 kHz
  - SPI master controller, 10 MHz
  - Two UARTs with independent baud rate
  - IrDA protocol support up to 115 Kbaud
  - Up to 46 I/O, 5 V tolerant on 3.3 V UPSD33xxV
- A/D converter
  - Eight channels, 10-bit resolution, 6 µs
- Timers and interrupts
  - Three 8032 standard 16-bit timers
  - Programmable counter array (PCA), six 16-bit modules for PWM/CAPCOM/timers
  - 8/10/16-bit PWM operation
  - 11 interrupt sources with two external interrupt pins
- Operating voltage source (±10%)
  - 5 V devices use both 5.0 V and 3.3 V
  - 3.3 V devices use only 3.3 V source

Table 1. Device summary

Reference	Part number
UPSD33xx	UPSD3312D, UPSD3333D, UPSD3334D, UPSD3354D
	UPSD3312DV, UPSD3333DV, UPSD3334DV, UPSD3354DV

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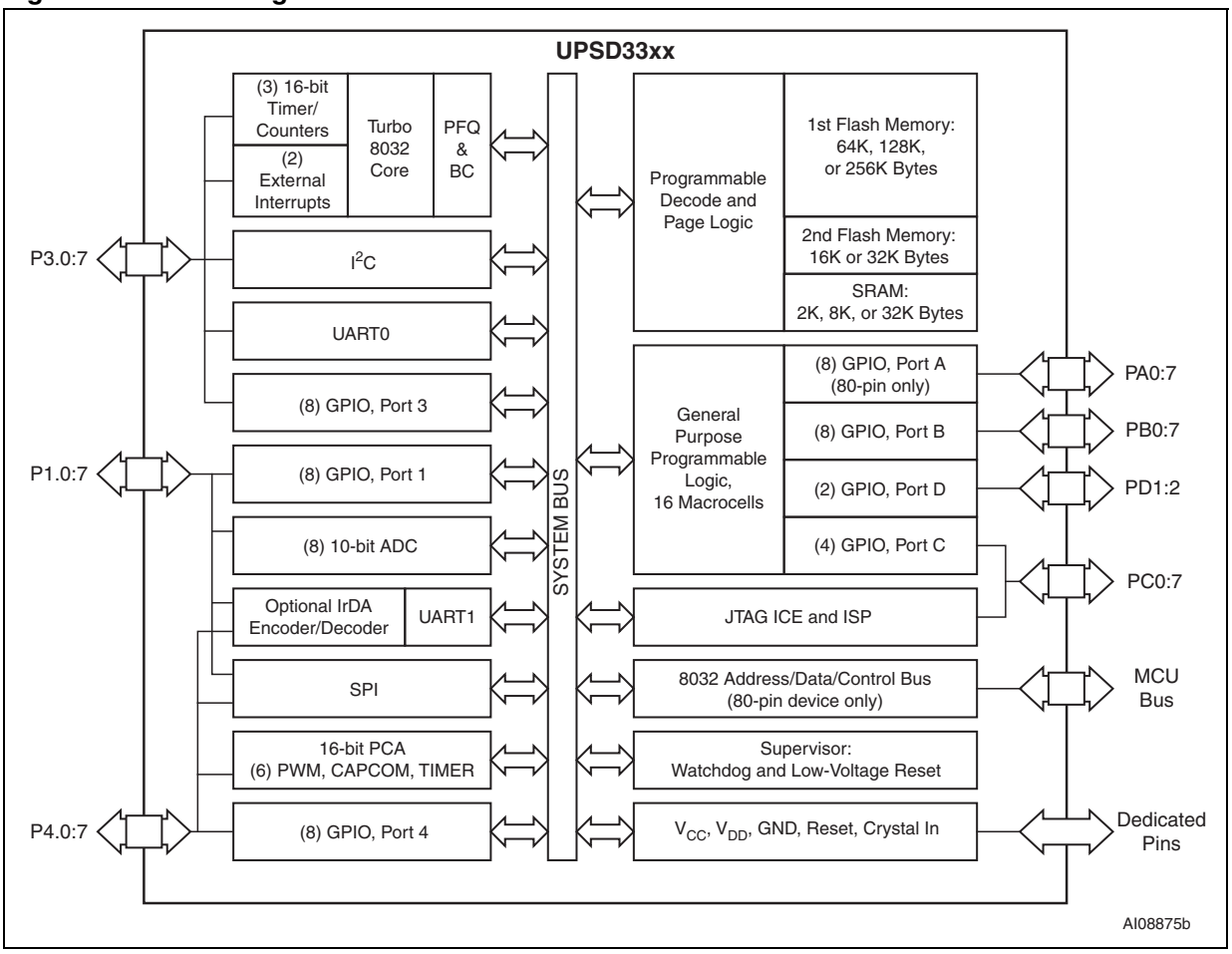
1 Description

The Turbo UPSD33xx series combines a powerful 8051-based microcontroller with a flexible memory structure, programmable logic, and a rich peripheral mix to form an ideal embedded controller. At its core is a fast 4-cycle 8032 MCU with a 6-byte instruction prefetch queue (PFQ) and a 4-entry fully associative branching cache (BC) to maximize MCU performance, enabling loops of code in smaller localities to execute extremely fast.

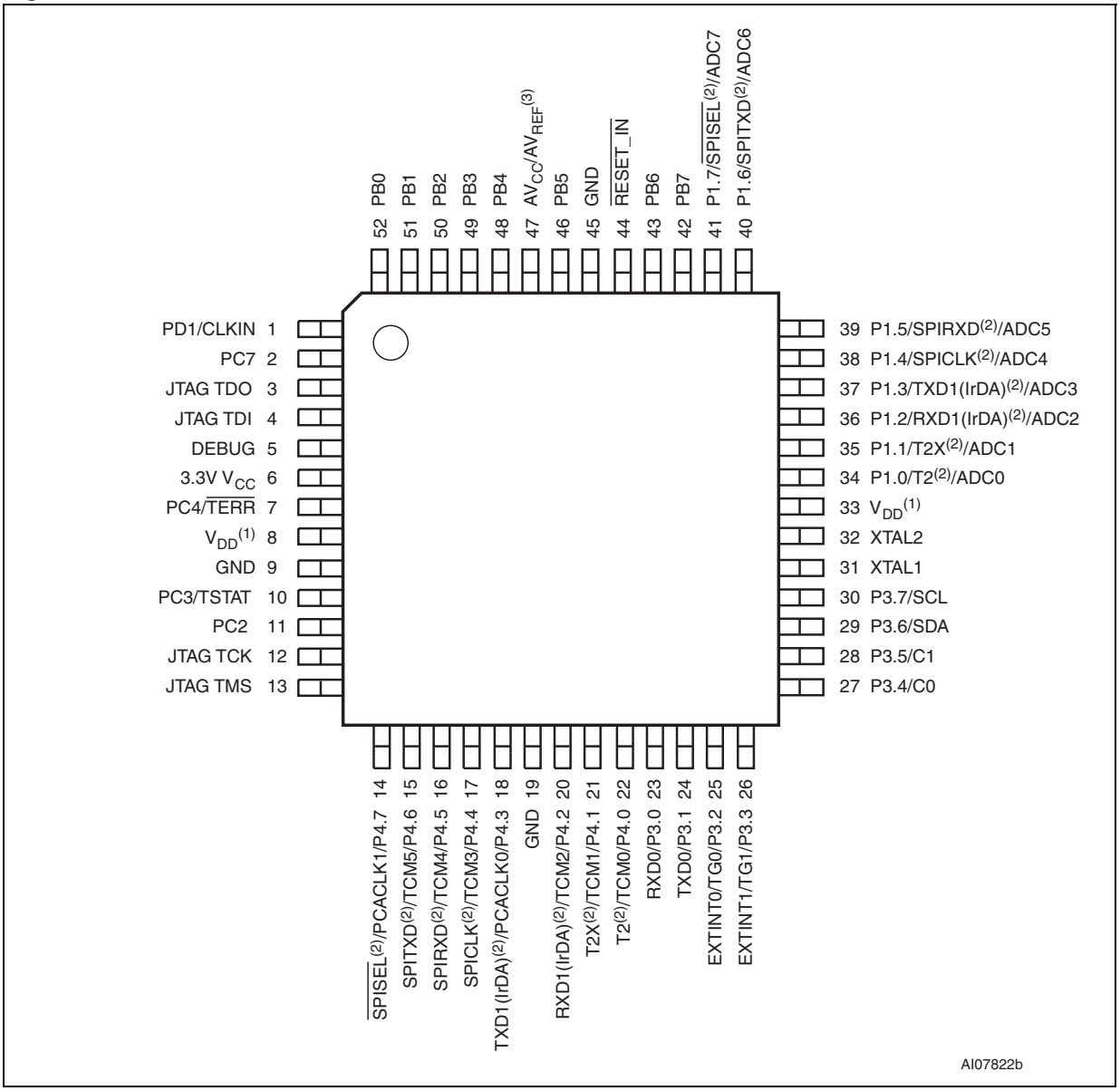
Code development is easily managed without a hardware in-circuit emulator by using the serial JTAG debug interface. JTAG is also used for in-system programming (ISP) in as little as 10 seconds, perfect for manufacturing and lab development. The 8032 core is coupled to programmable system device (PSD) architecture to optimize the 8032 memory structure, offering two independent banks of Flash memory that can be placed at virtually any address within 8032 program or data address space, and easily paged beyond 64 Kbytes using on-chip programmable decode logic. Dual Flash memory banks provide a robust solution for remote product updates in the field through in-application programming (IAP). Dual Flash banks also support EEPROM emulation, eliminating the need for external EEPROM chips. General purpose programmable logic (PLD) is included to build an endless variety of glue-logic, saving external logic devices. The PLD is configured using the software development tool, PSDsoft™ Express, available from the web at *www.st.com*, at no charge. The UPSD33xx also includes supervisor functions such as a programmable watchdog timer and low-voltage reset.

Figure 1. Block diagram



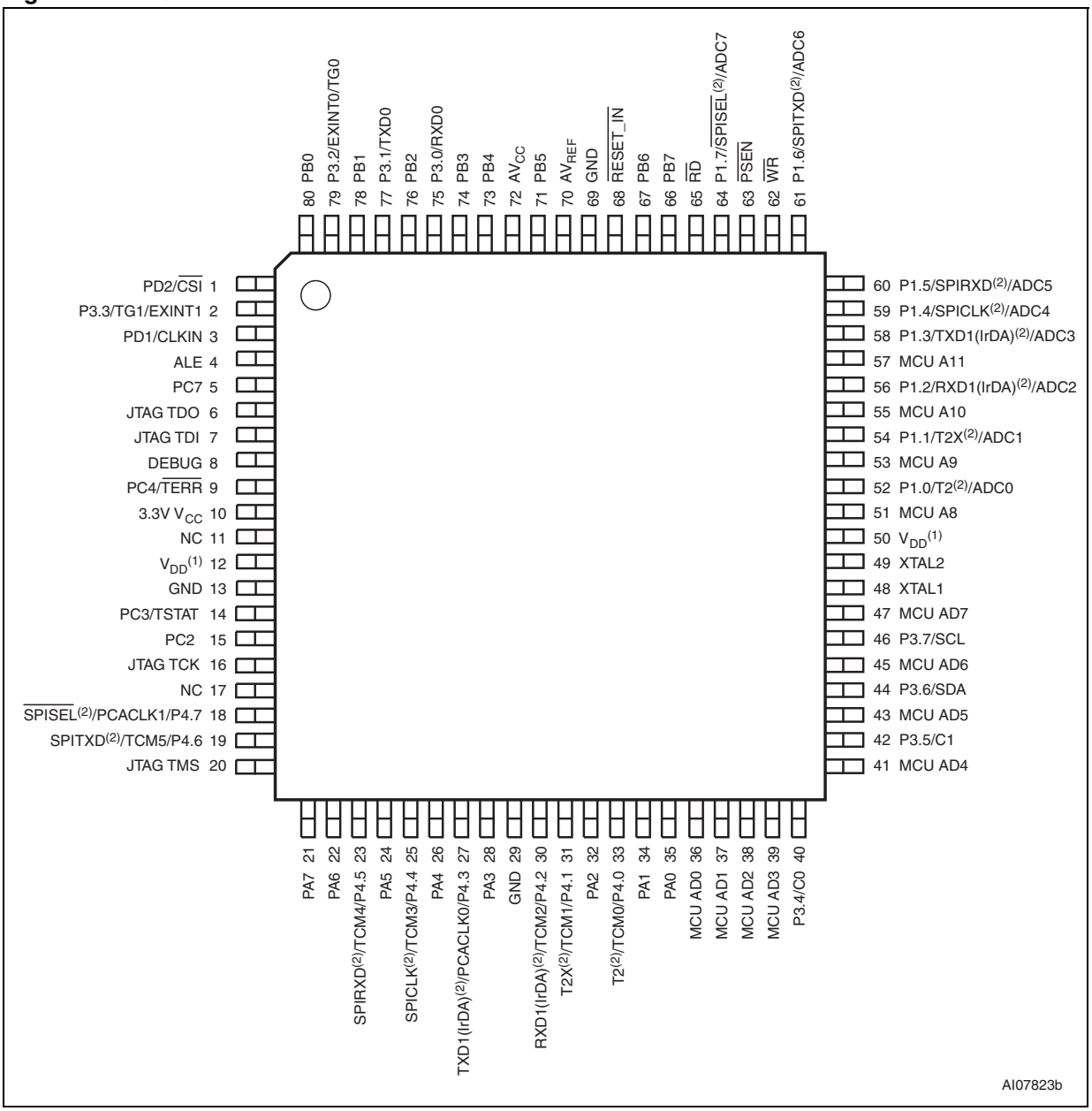
2 Pin descriptions

Figure 2. LQFP52 connections



1. For 5 V applications, V_{DD} must be connected to a 5.0 V source. For 3.3 V applications, V_{DD} must be connected to a 3.3 V source.
2. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port1.
3. AV_{REF} and 3.3 V AV_{CC} are shared in the 52-pin package only. ADC channels must use AV_{CC} as AV_{REF} for the 52-pin package.

Figure 3. LQFP80 connections



1. For 5 V applications, V_{DD} must be connected to a 5.0 V source. For 3.3 V applications, V_{DD} must be connected to a 3.3 V source.
2. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port1.
3. NC = Not Connected

Table 2. Pin definitions

Port pin	Signal name	80-Pin num.	52-Pin num.(1)	In/Out	Function		
					Basic	Alternate 1	Alternate 2
MCUAD0	AD0	36	N/A	I/O	External bus Multiplexed address/data bus A0/D0		
MCUAD1	AD1	37	N/A	I/O	Multiplexed address/data bus A1/D1		
MCUAD2	AD2	38	N/A	I/O	Multiplexed address/data bus A2/D2		
MCUAD3	AD3	39	N/A	I/O	Multiplexed address/data bus A3/D3		
MCUAD4	AD4	41	N/A	I/O	Multiplexed address/data bus A4/D4		
MCUAD5	AD5	43	N/A	I/O	Multiplexed address/data bus A5/D5		
MCUAD6	AD6	45	N/A	I/O	Multiplexed address/data bus A6/D6		
MCUAD7	AD7	47	N/A	I/O	Multiplexed address/data bus A7/D7		
MCUA8	A8	51	N/A	O	External bus, Addr A8		
MCUA9	A9	53	N/A	O	External bus, Addr A9		
MCUA10	A10	55	N/A	O	External bus, Addr A10		
MCUA11	A11	57	N/A	O	External bus, Addr A11		
P1.0	T2 ADC0	52	34	I/O	General I/O port pin	Timer 2 Count input (T2)	ADC Channel 0 input (ADC0)
P1.1	T2X ADC1	54	35	I/O	General I/O port pin	Timer 2 Trigger input (T2X)	ADC Channel 1 input (ADC1)
P1.2	RxD1 ADC2	56	36	I/O	General I/O port pin	UART1 or IrDA Receive (RxD1)	ADC Channel 2 input (ADC2)
P1.3	TXD1 ADC3	58	37	I/O	General I/O port pin	UART or IrDA Transmit (TxD1)	ADC Channel 3 input (ADC3)

Table 2. Pin definitions (continued)

Port pin	Signal name	80-Pin num.	52-Pin num.(1)	In/Out	Function		
					Basic	Alternate 1	Alternate 2
P1.4	SPICLK ADC4	59	38	I/O	General I/O port pin	SPI Clock Out (SPICLK)	ADC Channel 4 input (ADC4)
P1.5	SPIRxD ADC6	60	39	I/O	General I/O port pin	SPI Receive (SPIRxD)	ADC Channel 5 input (ADC5)
P1.6	SPITXD ADC6	61	40	I/O	General I/O port pin	SPI Transmit (SPITxD)	ADC Channel 6 input (ADC6)
P1.7	SPISEL ADC7	64	41	I/O	General I/O port pin	SPI Slave Select ($\overline{\text{SPISEL}}$)	ADC Channel 7 input (ADC7)
P3.0	RxD0	75	23	I/O	General I/O port pin	UART0 Receive (RxD0)	
P3.1	TXD0	77	24	I/O	General I/O port pin	UART0 Transmit (TxD0)	
P3.2	EXINT0 TGO	79	25	I/O	General I/O port pin	Interrupt 0 input (EXTINT0)/Timer 0 gate control (TG0)	
P3.3	INT1	2	26	I/O	General I/O port pin	Interrupt 1 input (EXTINT1)/Timer 1 gate control (TG1)	
P3.4	C0	40	27	I/O	General I/O port pin	Counter 0 input (C0)	
P3.5	C1	42	28	I/O	General I/O port pin	Counter 1 input (C1)	
P3.6	SDA	44	29	I/O	General I/O port pin	I^2C Bus serial data (I^2CSDA)	
P3.7	SCL	46	30	I/O	General I/O port pin	I^2C Bus clock (I^2CSCL)	
P4.0	T2 TCM0	33	22	I/O	General I/O port pin	Program Counter Array0 PCA0-TCM0	Timer 2 Count input (T2)
P4.1	T2X TCM1	31	21	I/O	General I/O port pin	PCA0-TCM1	Timer 2 Trigger input (T2X)
P4.2	RXD1 TCM2	30	20	I/O	General I/O port pin	PCA0-TCM2	UART1 or IrDA Receive (RxD1)
P4.3	TXD1 PCACLK0	27	18	I/O	General I/O port pin	PCACLK0	UART1 or IrDA Transmit (TxD1)
P4.4	SPICLK TCM3	25	17	I/O	General I/O port pin	Program Counter Array1 PCA1-TCM3	SPI Clock Out (SPICLK)
P4.5	SPIRXD TCM4	23	16	I/O	General I/O port pin	PCA1-TCM4	SPI Receive (SPIRxD)

Table 2. Pin definitions (continued)

Port pin	Signal name	80-Pin num.	52-Pin num.(1)	In/Out	Function		
					Basic	Alternate 1	Alternate 2
P4.6	SPITXD TCM5	19	15	I/O	General I/O port pin	PCA1-TCM5	SPI Transmit (SPITxD)
P4.7	SPISEL PCACLK1	18	14	I/O	General I/O port pin	PCACLK1	SPI Slave Select ($\overline{\text{SPISEL}}$)
AV_{REF}		70	N/A	I	Reference voltage input for ADC. Connect AV_{REF} to V_{CC} if the ADC is not used.		
$\overline{RD}$		65	N/A	O	READ Signal, external bus		
$\overline{WR}$		62	N/A	O	WRITE Signal, external bus		
$\overline{PSEN}$		63	N/A	O	$\overline{PSEN}$ Signal, external bus		
ALE		4	N/A	O	Address Latch signal, external bus		
$\overline{RESET\_IN}$		68	44	I	Active low reset input		
XTAL1		48	31	I	Oscillator input pin for system clock		
XTAL2		49	32	O	Oscillator output pin for system clock		
DEBUG		8	5	I/O	I/O to the MCU debug unit		

Table 2. Pin definitions (continued)

Port pin	Signal name	80-Pin num.	52-Pin num.(1)	In/Out	Function		
					Basic	Alternate 1	Alternate 2
PA0		35	N/A	I/O	General I/O port pin		All Port A pins support: – PLD Macro-cell outputs, or – PLD inputs, or – Latched Address Out (A0-A7), or – Peripheral I/O mode
PA1		34	N/A	I/O	General I/O port pin		
PA2		32	N/A	I/O	General I/O port pin		
PA3		28	N/A	I/O	General I/O port pin		
PA4		26	N/A	I/O	General I/O port pin		
PA5		24	N/A	I/O	General I/O port pin		
PA6		22	N/A	I/O	General I/O port pin		
PA7		21	N/A	I/O	General I/O port pin		

1. N/A = Signal Not Available on 52-pin package.