



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



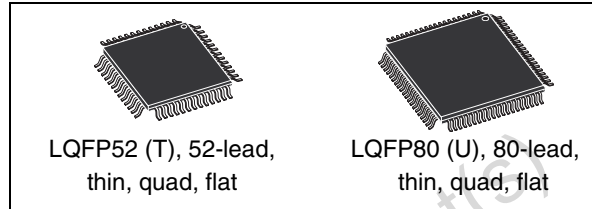


# UPSD3422 UPSD3433 UPSD3434 UPSD3454

Turbo Plus series  
Fast Turbo 8032 MCU with USB and programmable logic

## Features

- Fast 8-bit Turbo 8032 MCU, 40 MHz
  - Advanced core, 4-clocks per instruction
  - 10 MIPs peak performance at 40 MHz (5 V)
  - JTAG debug and in-system programming
  - 16-bit internal instruction path fetches double-byte instruction in a single memory cycle
  - Branch cache & 4 instruction prefetch queue
  - Dual XDATA pointers with automatic increment and decrement
  - Compatible with 3rd party 8051 tools
- Dual Flash memories with memory management
  - Place either memory into 8032 program address space or data address space
  - READ-while-WRITE operation for in-application programming and EEPROM emulation
  - Single voltage program and erase
  - 100 000 guaranteed erase cycles, 15-year retention
- Clock, reset, and power supply management
  - Flexible 8-level CPU clock divider register
  - Normal, Idle, and power-down modes
  - Power-on-reset and low-voltage-reset supervisor
  - Programmable watchdog timer
- Programmable logic, general purpose
  - 16 macrocells for logic applications (e.g., shifters, state machines, chip-selects, glue-logic to keypads, and LCDs)
- A/D converter
  - Eight channels, 10-bit resolution, 6  $\mu$ s
- Operating voltage source ( $\pm 10\%$ )
  - 5 V devices: 5.0 V and 3.3 V sources
  - 3.3 V devices: 3.3 V source



- Communication interfaces
  - USB v2.0 Full Speed (12Mbps)
  - 10 endpoint pairs (In/Out), each endpoint with 64-byte FIFO (supports Control, In, and Bulk transfer types)
  - I<sup>2</sup>C Master/Slave controller, 933kHz
  - SPI Master controller, 10MHz
  - Two UARTs with independent baud rate
  - IrDA protocol: up to 115 kbaud
  - Up to 43 V<sub>IO</sub>, 5 V tolerant uPSD34xxV
- Timers and interrupts
  - Three 8032 standard 16-bit timers
  - Programmable counter array (PCA), six 16-bit modules for PWM, CAPCOM, and timers
  - 8/10/16-bit PWM operation
  - 12 Interrupt sources with two external interrupt pins
- Packages
  - ECOPACK<sup>®</sup> compliant

Table 1. Device summary

Reference	Part number
uPSD3422	UPSD3422E, UPSD3422EV
uPSD3433E	UPSD3433E, UPSD3433EV
uPSD3434	UPSD3434E, UPSD3434EV
uPSD3454	UPSD3454E, UPSD3454EV

# Contents

<b>1</b>	<b>Description</b> .....	<b>20</b>
<b>2</b>	<b>Pin descriptions</b> .....	<b>22</b>
<b>3</b>	<b>Hardware description</b> .....	<b>28</b>
<b>4</b>	<b>Memory organization</b> .....	<b>30</b>
4.1	Internal memory (MCU module, standard 8032 memory: DATA, IDATA, SFR) .....	31
4.1.1	DATA memory .....	31
4.1.2	IDATA memory .....	31
4.1.3	SFR memory .....	31
4.2	External memory (PSD module: program memory, data memory) .....	31
4.2.1	Program memory .....	32
4.2.2	Data memory .....	32
4.2.3	Memory placement .....	32
<b>5</b>	<b>8032 MCU core performance enhancements</b> .....	<b>33</b>
5.1	Pre-fetch queue (PFQ) and branch cache (BC) .....	34
5.2	PFQ example, multi-cycle instructions .....	35
5.3	Aggregate performance .....	35
<b>6</b>	<b>MCU module description</b> .....	<b>37</b>
<b>7</b>	<b>8032 MCU registers</b> .....	<b>38</b>
7.1	Stack pointer (SP) .....	38
7.2	Data pointer (DPTR) .....	38
7.3	Program counter (PC) .....	38
7.4	Accumulator (ACC) .....	39
7.5	B register (B) .....	39
7.6	General purpose registers (R0 - R7) .....	39
7.7	Program status word (PSW) .....	39
7.7.1	Carry flag (CY) .....	39
7.7.2	Auxiliary carry flag (AC) .....	39



7.7.3	General purpose flag (F0)	39
7.7.4	Register bank select flags (RS1, RS0)	39
7.7.5	Overflow flag (OV)	40
7.7.6	Parity flag (P)	40
<b>8</b>	<b>Special function registers (SFR)</b>	<b>41</b>
<b>9</b>	<b>8032 addressing modes</b>	<b>48</b>
9.1	Register addressing	48
9.2	Direct addressing	48
9.3	Register indirect addressing	48
9.4	Immediate addressing	49
9.5	External direct addressing	49
9.6	External indirect addressing	49
9.7	Indexed addressing	50
9.8	Relative addressing	50
9.9	Absolute addressing	50
9.10	Long addressing	50
9.11	Bit addressing	51
<b>10</b>	<b>UPSD34xx instruction set summary</b>	<b>52</b>
<b>11</b>	<b>Dual data pointers</b>	<b>57</b>
11.1	Data pointer control register, DPTC (85h)	57
11.2	Data pointer mode register, DPTM (86h)	58
11.2.1	Firmware example	58
<b>12</b>	<b>Debug unit</b>	<b>60</b>
<b>13</b>	<b>Interrupt system</b>	<b>62</b>
13.1	Individual interrupt sources	64
13.1.1	External interrupts Int0 and Int1	64
13.1.2	Timer 0 and 1 overflow interrupt	65
13.1.3	Timer 2 overflow interrupt	65
13.1.4	UART0 and UART1 interrupt	65
13.1.5	SPI interrupt	65

13.1.6	I <sup>2</sup> C interrupt	65
13.1.7	ADC interrupt	65
13.1.8	PCA interrupt	65
13.1.9	USB interrupt	66
<b>14</b>	<b>MCU clock generation</b>	<b>68</b>
14.1	MCU_CLK	68
14.2	PERIPH_CLK	68
14.2.1	JTAG interface clock	68
14.2.2	USB_CLK	69
<b>15</b>	<b>Power saving modes</b>	<b>72</b>
15.1	Idle mode	72
15.2	Power-down mode	73
15.3	Reduced frequency mode	73
<b>16</b>	<b>Oscillator and external components</b>	<b>76</b>
<b>17</b>	<b>I/O ports of mcu module</b>	<b>78</b>
17.1	MCU port operating modes	78
17.1.1	GPIO function	79
17.1.2	GPIO output	79
17.1.3	GPIO input	79
17.1.4	Alternate functions	83
<b>18</b>	<b>MCU bus interface</b>	<b>86</b>
18.1	PSEN bus cycles	86
18.2	READ or WRITE bus cycles	86
18.3	Connecting external devices to the MCU bus	86
18.4	Programmable bus timing	87
18.5	Controlling the PFQ and BC	88
<b>19</b>	<b>Supervisory functions</b>	<b>91</b>
19.1	External reset input pin, RESET_IN	91
19.2	Low V <sub>CC</sub> voltage detect, LVD	92
19.3	Power-up reset	92

19.4	JTAG debug reset . . . . .	92
19.5	Watchdog timer, WDT . . . . .	92
19.5.1	Firmware example . . . . .	94
<b>20</b>	<b>Standard 8032 timer/counters . . . . .</b>	<b>96</b>
20.1	Standard timer SFRs . . . . .	96
20.2	Clock sources . . . . .	96
20.3	SFR, TCON . . . . .	97
20.4	SFR, TMOD . . . . .	98
20.5	Timer 0 and Timer 1 operating modes . . . . .	98
20.5.1	Mode 0 . . . . .	98
20.5.2	Mode 1 . . . . .	98
20.5.3	Mode 2 . . . . .	98
20.5.4	Mode 3 . . . . .	98
20.6	Timer 2 . . . . .	100
20.6.1	Capture mode . . . . .	101
20.6.2	Auto-reload mode . . . . .	101
20.6.3	Baud rate generator mode . . . . .	103
<b>21</b>	<b>Serial UART interfaces . . . . .</b>	<b>107</b>
21.1	UART operation modes . . . . .	107
21.1.1	Mode 0 . . . . .	107
21.1.2	Mode 1 . . . . .	107
21.1.3	Mode 2 . . . . .	108
21.1.4	Mode 3 . . . . .	108
21.1.5	Multiprocessor communications . . . . .	108
21.2	Serial port control registers . . . . .	109
21.3	UART baud rates . . . . .	110
21.3.1	Using timer 1 to generate baud rates . . . . .	111
21.3.2	Using timer/counter 2 to generate baud rates . . . . .	111
21.4	More about UART mode 0 . . . . .	112
21.5	More about UART mode 1 . . . . .	114
21.6	More about UART modes 2 and 3 . . . . .	116
<b>22</b>	<b>IrDA interface . . . . .</b>	<b>119</b>
22.1	Baud rate selection . . . . .	120

22.2	Pulse width selection .....	121
<b>23</b>	<b>I<sup>2</sup>C interface .....</b>	<b>123</b>
23.1	I2C interface main features .....	123
23.2	Communication flow .....	124
23.3	Operating modes .....	125
23.4	Bus arbitration .....	126
23.5	Clock synchronization .....	126
23.5.1	Clock sync during arbitration .....	126
23.5.2	Clock sync during handshaking .....	126
23.6	General call address .....	127
23.7	Serial I/O engine (SIOE) .....	127
23.8	I <sup>2</sup> C interface control register (S1CON) .....	129
23.9	I <sup>2</sup> C interface status register (S1STA) .....	130
23.9.1	Interrupt conditions .....	130
23.10	I2C data shift register (S1DAT) .....	131
23.10.1	Bus wait condition .....	132
23.11	I <sup>2</sup> C address register (S1ADR) .....	132
23.12	I <sup>2</sup> C Start sample setting (S1SETUP) .....	133
23.13	I <sup>2</sup> C operating sequences .....	135
23.13.1	Interrupt service routine (ISR) .....	138
<b>24</b>	<b>SPI (synchronous peripheral interface) .....</b>	<b>142</b>
24.1	SPI bus features and communication flow .....	143
24.2	Full-duplex operation .....	143
24.3	Bus-level activity .....	143
24.4	SPI SFR registers .....	145
24.5	SPI configuration .....	146
24.6	Dynamic control .....	147
<b>25</b>	<b>USB interface .....</b>	<b>150</b>
25.1	Basic USB concepts .....	151
25.1.1	Communication flow .....	151
25.1.2	Endpoints .....	152
25.1.3	Packets .....	152

25.1.4	Data transfers with the host	153
25.2	Types of transfers	154
25.2.1	Enumeration	155
25.3	Endpoint FIFOs	156
25.3.1	Busy bit (BSY) operation	156
25.3.2	Busy bit and interrupts	156
25.3.3	FIFO pairing	157
25.3.4	Reading and writing FIFOs	159
25.3.5	Accessing FIFO control registers, UCON, and USIZE	159
25.3.6	Accessing the setup command buffer	160
25.4	USB registers	160
25.4.1	USB device address register	161
25.4.2	Endpoint FIFO pairing	162
25.4.3	USB interrupts	163
25.5	Typical connection to USB	177
<b>26</b>	<b>Analog-to-digital convertor (ADC)</b>	<b>178</b>
26.1	Port 1 ADC channel selects	178
<b>27</b>	<b>Programmable counter array (PCA) with PWM</b>	<b>181</b>
27.1	PCA block	181
27.2	PCA clock selection	182
27.3	Operation of TCM modes	183
27.4	Capture mode	183
27.5	Timer mode	183
27.6	Toggle mode	184
27.7	PWM mode - (x8), fixed frequency	184
27.8	PWM mode - (x8), programmable frequency	185
27.9	PWM mode - fixed frequency, 16-bit	186
27.10	PWM mode - fixed frequency, 10-bit	187
27.11	Writing to capture/compare registers	187
27.12	Control register bit definition	187
27.13	TCM interrupts	189
<b>28</b>	<b>PSD module</b>	<b>191</b>



28.1	PSD module functional description	192
28.1.1	8032 address/data/control interface	192
28.1.2	Dual Flash memories and IAP	192
28.1.3	Main Flash memory	192
28.1.4	Secondary Flash memory	193
28.1.5	SRAM	193
28.1.6	Runtime control registers, csiop	193
28.1.7	Memory page register	193
28.1.8	Programmable logic (PLDs)	194
28.1.9	PLD #1, decode PLD (DPLD)	194
28.1.10	PLD #2, general PLD (GPLD)	194
28.1.11	OMCs	195
28.1.12	OMC allocator	195
28.1.13	IMCs	195
28.1.14	I/O ports	195
28.1.15	JTAG port	196
28.1.16	Power management	197
28.1.17	Security and NVM sector protection	197
28.2	Memory mapping	197
28.2.1	8032 program address space	198
28.2.2	8032 data address space (XDATA)	198
28.2.3	Specifying the memory map with PSDsoft express	198
28.2.4	EEPROM emulation	199
28.2.5	Alternative mapping schemes	200
28.2.6	Memory sector select rules	202
28.2.7	The VM register	203
28.3	PSD module data bus width	204
28.4	Runtime control register definitions (csiop)	205
28.5	PSD module detailed operation	207
28.5.1	Flash memory operation	207
28.5.2	Flash memory instruction sequences	208
28.5.3	Reading Flash memory	210
28.5.4	Read memory contents	210
28.5.5	Reading the erase/program status bits	210
28.5.6	Data polling flag (DQ7)	210
28.5.7	Toggle flag (DQ6)	211

28.5.8	Error flag (DQ5)	211
28.5.9	Erase time-out flag (DQ3)	212
28.5.10	Programming Flash memory	212
28.5.11	Data polling	213
28.5.12	Data toggle	214
28.5.13	Ready/Busy (PC3)	215
28.5.14	Bypassed unlock sequence	215
28.5.15	Erasing Flash memory	216
28.5.16	Flash bulk erase	216
28.5.17	Flash sector erase	216
28.5.18	Suspend sector erase	217
28.5.19	Resume sector erase	217
28.5.20	Reset Flash	218
28.5.21	Reset signal applied to Flash memory	218
28.5.22	Flash memory sector protection	218
28.5.23	Flash memory protection during power-up	218
28.5.24	PSD module security bit	218
28.5.25	PLDs	219
28.5.26	Turbo bit and PLDs	220
28.5.27	Decode PLD (DPLD)	222
28.5.28	General PLD (GPLD)	223
28.5.29	Output macrocell	225
28.5.30	OMC allocator	226
28.5.31	Product term allocator	226
28.5.32	Loading and reading OMCs	228
28.5.33	OMC mask registers	229
28.5.34	Input macrocells	229
28.5.35	I/O ports	231
28.5.36	General port architecture	231
28.5.37	Port operating modes	231
28.5.38	MCU I/O mode	233
28.5.39	PLD I/O mode	236
28.5.40	Latched address output mode	238
28.5.41	Peripheral I/O mode	239
28.5.42	JTAG ISP mode	240
28.5.43	Other port capabilities	240
28.5.44	Port pin drive options	240

28.5.45	Drive select registers	240
28.5.46	Enable out registers	240
28.5.47	Individual port structures	243
28.5.48	Port A structure	243
28.5.49	Port B structure	244
28.5.50	Port C structure	245
28.5.51	Port D structure	246
28.5.52	Power management	248
28.5.53	Automatic power-down (APD)	250
28.5.54	Forced power-down (FDP)	251
28.5.55	Chip select input (CSI)	253
28.5.56	PLD non-turbo mode	253
28.5.57	PLD current consumption	254
28.5.58	Turbo mode current consumption	254
28.5.59	Non-turbo mode current consumption	254
28.5.60	PLD blocking bits	255
28.5.61	Blocking 8032 bus control signals	255
28.5.62	Blocking common clock, CLKIN	255
28.6	PSD module reset conditions	255
28.6.1	JTAG ISP and JTAG debug	257
28.6.2	JTAG chaining inside the package	257
28.6.3	In-system programming	258
28.6.4	4-pin JTAG ISP (default)	259
28.6.5	6-pin JTAG ISP (optional)	260
28.6.6	Recommended JTAG connector	261
28.6.7	Chaining UPSD34xx devices	262
28.6.8	Debugging the 8032 MCU module	263
28.6.9	JTAG security setting	264
28.6.10	Initial delivery state	264
<b>29</b>	<b>AC/DC parameters</b>	<b>265</b>
<b>30</b>	<b>Maximum rating</b>	<b>268</b>
<b>31</b>	<b>DC and AC parameters</b>	<b>269</b>
<b>32</b>	<b>Package mechanical information</b>	<b>289</b>

<b>33</b>	<b>Part numbering</b> .....	<b>292</b>
<b>34</b>	<b>Important notes</b> .....	<b>294</b>
	34.1 USB interrupts with idle mode .....	294
	34.2 USB reset interrupt .....	294
	34.3 USB reset .....	294
	34.4 Data toggle .....	295
	34.5 USB FIFO accessibility .....	295
	34.6 Erroneous resend of data packet .....	295
	34.7 IN FIFO pairing operation .....	296
	34.8 OUT FIFO pairing operation .....	296
	34.9 Missing ACK to host retransmission of SETUP packet .....	296
	34.10 MCU JTAG ID .....	297
	34.11 Port 1 not 5-volt IO tolerant .....	297
	34.12 Incorrect code execution when code banks are switched .....	298
	34.13 9 <sup>th</sup> received data bit corrupted in UART modes 2 and 3 .....	298
<b>35</b>	<b>Revision history</b> .....	<b>299</b>

Obsolete Product(s) - Obsolete Product(s)  
 Obsolete Product(s) - Obsolete Product(s)

## List of tables

Table 1.	Device summary . . . . .	1
Table 2.	Pin definitions . . . . .	24
Table 3.	Port type and voltage source combinations . . . . .	28
Table 4.	Register bank select addresses . . . . .	40
Table 5.	SFR memory map with direct address and reset value . . . . .	42
Table 6.	Arithmetic instruction set. . . . .	52
Table 7.	Logical instruction set . . . . .	53
Table 8.	Data transfer instruction set . . . . .	54
Table 9.	Boolean variable manipulation instruction set . . . . .	55
Table 10.	Program branching instruction set . . . . .	55
Table 11.	Miscellaneous instruction set . . . . .	56
Table 12.	Notes on instruction set and addressing modes. . . . .	56
Table 13.	DPTC: data pointer control register (SFR 85h, reset value 00h) . . . . .	57
Table 14.	DPTC register bit definition. . . . .	57
Table 15.	DPTM: data pointer mode register (SFR 86h, reset value 00h) . . . . .	58
Table 16.	DPTM register bit definition . . . . .	58
Table 17.	Interrupt summary. . . . .	63
Table 18.	IE: interrupt enable register (SFR A8h, reset value 00h) . . . . .	66
Table 19.	IE register bit definition . . . . .	66
Table 20.	IEA: interrupt enable addition register (SFR A7h, reset value 00h) . . . . .	66
Table 21.	IEA register bit definition. . . . .	66
Table 22.	IP: interrupt priority register (SFR B8h, reset value 00h) . . . . .	67
Table 23.	IP register bit definition . . . . .	67
Table 24.	IPA: Interrupt Priority Addition register (SFR B7h, reset value 00h) . . . . .	67
Table 25.	IPA register bit definition. . . . .	67
Table 26.	PLLM and PLLD values for different $f_{OSC}$ frequencies . . . . .	69
Table 27.	CCON0: clock control register (SFR F9h, reset value 50h) . . . . .	70
Table 28.	CCON0 register bit definition . . . . .	70
Table 29.	CCON1 PLL control register (SFR FAh, reset value 00h) . . . . .	71
Table 30.	CCON1 register bit definition . . . . .	71
Table 31.	MCU module port and peripheral status during reduced power modes . . . . .	74
Table 32.	State of 8032 MCU bus signals during power-down and idle modes . . . . .	74
Table 33.	PCON: power control register (SFR 87h, reset value 00h) . . . . .	74
Table 34.	PCON register bit definition . . . . .	74
Table 35.	P1: I/O port 1 register (SFR 90h, reset value FFh) . . . . .	81
Table 36.	P1 register bit definition . . . . .	81
Table 37.	P3: I/O port 3 register (SFR B0h, reset value FFh) . . . . .	82
Table 38.	P3 register bit definition . . . . .	82
Table 39.	P4: I/O port 4 register (SFR C0h, reset value FFh) . . . . .	82
Table 40.	P4 register bit definition . . . . .	82
Table 41.	P3SFS: Port 3 special function select register (SFR 91h, reset value 00h) . . . . .	84
Table 42.	P3SFS register bit definition . . . . .	84
Table 43.	P1SFS0: Port 1 special function select 0 register (SFR 8Eh, reset value 00h) . . . . .	84
Table 44.	P1SFS1: Port 1 special function select 1 register (SFR 8Fh, reset value 00h) . . . . .	84
Table 45.	P1SFS0 and P1SFS1 details . . . . .	84
Table 46.	P4SFS0: Port 4 special function select 0 register (SFR 92h, reset value 00h) . . . . .	85
Table 47.	P4SFS1: Port 4 special function select 1 register (SFR 93h, reset value 00h) . . . . .	85
Table 48.	P4SFS0 and P4SFS1 details . . . . .	85



Table 49.	BUSCON: bus control register (SFR 9Dh, reset value EBh) . . . . .	88
Table 50.	BUSCON register bit definition . . . . .	89
Table 51.	Number of MCU_CLK periods required to optimize bus transfer rate . . . . .	90
Table 52.	WDKEY: Watchdog timer key register (SFR AEh, reset value 55h) . . . . .	94
Table 53.	WDKEY register bit definition . . . . .	94
Table 54.	WDRST: Watchdog timer reset counter register (SFR A6h, reset value 00h) . . . . .	94
Table 55.	WDRST register bit definition . . . . .	95
Table 56.	TCON: Timer control register (SFR 88h, reset value 00h) . . . . .	97
Table 57.	TCON register bit definition . . . . .	97
Table 58.	TMOD: Timer mode register (SFR 89h, reset value 00h) . . . . .	99
Table 59.	TMOD register bit definition . . . . .	99
Table 60.	T2CON: Timer 2 control register (SFR C8h, reset value 00h) . . . . .	101
Table 61.	T2CON register bit definition . . . . .	101
Table 62.	Timer/counter 2 operating modes . . . . .	102
Table 63.	Commonly used baud rates generated from timer2 (T2CON = 34h) . . . . .	104
Table 64.	UART operating modes . . . . .	108
Table 65.	SCON0: serial port UART0 control register (SFR 98h, reset value 00h) . . . . .	109
Table 66.	SCON0 register bit definition . . . . .	109
Table 67.	SCON1: serial port UART1 control register (SFR D8h, reset value 00h) . . . . .	109
Table 68.	SCON1 register bit definition . . . . .	110
Table 69.	Commonly used baud rates generated from timer 1 . . . . .	111
Table 70.	IRDACON register bit definition (SFR CEh, reset value 0Fh) . . . . .	120
Table 71.	IRDACON register bit definition . . . . .	120
Table 72.	Baud rate selection register (SFR xxh, reset value xxh) . . . . .	120
Table 73.	Baud rate of UART#1 for IrDA interface . . . . .	121
Table 74.	Recommended CDIV[4:0] values to generate SIRCk (default CDIV[4:0] = 0Fh, 15 decimal) . . . . .	122
Table 75.	Serial control register S1CON (SFR DCh, reset value 00h) . . . . .	129
Table 76.	S1CON register bit definition . . . . .	129
Table 77.	Selection of the SCL frequency in Master mode based on f <sub>OSC</sub> examples . . . . .	130
Table 78.	S1STA: I <sup>2</sup> C interface status register (SFR DDh, reset value 00h) . . . . .	130
Table 79.	S1STA register bit definition . . . . .	131
Table 80.	S1DAT: I2C data shift register (SFR DEh, reset value 00h) . . . . .	132
Table 81.	S1DAT register bit definition . . . . .	132
Table 82.	S1ADR: I2C address register (SFR DFh, reset value 00h) . . . . .	132
Table 83.	S1ADR register bit definition . . . . .	132
Table 84.	S1SETUP: I <sup>2</sup> C Start condition sample setup register (SFR DBh, reset value 00h) . . . . .	133
Table 85.	S1SETUP register bit definition . . . . .	133
Table 86.	Number of I <sup>2</sup> C bus samples taken after 1-to-0 transition on SDA (Start condition) . . . . .	134
Table 87.	Start condition hold time . . . . .	134
Table 88.	S1SETUP examples for various I <sup>2</sup> C bus speeds and oscillator frequencies . . . . .	134
Table 89.	SPICON0: control register 0 (SFR D6h, reset value 00h) . . . . .	147
Table 90.	SPICON0 register bit definition . . . . .	147
Table 91.	SPICON1: SPI interface control register 1 (SFR D7h, reset value 00h) . . . . .	148
Table 92.	SPICON1 register bit definition . . . . .	148
Table 93.	SPICLKD: SPI prescaler (clock divider) register (SFR D2h, reset value 04h) . . . . .	148
Table 94.	SPICLKD register bit definition . . . . .	149
Table 95.	SPISTAT: SPI interface status register (SFR D3h, reset value 02h) . . . . .	149
Table 96.	SPISTAT register bit definition . . . . .	149
Table 97.	Types of packet IDs . . . . .	152

Table 98.	UPSD34xx supported endpoints. . . . .	157
Table 99.	UPSD34xx USB SFR register map. . . . .	160
Table 100.	USB device address register (UADDR 0E2h, reset value 00h) . . . . .	162
Table 101.	UADDR register bit definition . . . . .	162
Table 102.	Pairing control register (UPAIR 0E3h, reset value 00h) . . . . .	162
Table 103.	UPAIR register bit definition . . . . .	162
Table 104.	USB global interrupt enable register (UIE0 0E4h, reset value 00h) . . . . .	163
Table 105.	UIE0 register bit definition. . . . .	164
Table 106.	USB IN FIFO interrupt enable register (UIE1 0E5h, reset value 00h) . . . . .	164
Table 107.	UIE1 register bit definition. . . . .	164
Table 108.	USB OUT FIFO interrupt enable register (UIE2 0E6h, reset value 00h) . . . . .	164
Table 109.	UIE2 register bit definition. . . . .	165
Table 110.	USB IN FIFO NAK interrupt enable register (UIE3 0E7h, reset value 00h) . . . . .	165
Table 111.	UIE3 register bit definition. . . . .	165
Table 112.	USB global interrupt flag register (UIF0 0E8h, reset value 00h). . . . .	166
Table 113.	UIF0 register bit definition. . . . .	166
Table 114.	USB IN FIFO interrupt flag (UIF1 0E9h, reset value 00h). . . . .	167
Table 115.	UIF1 register bit definition. . . . .	167
Table 116.	USB OUT FIFO interrupt flag (UIF2 0EAh, reset value 00h) . . . . .	168
Table 117.	UIF2 register bit definition. . . . .	168
Table 118.	USB IN FIFO NAK interrupt flag (UIF3 0EBh, reset value 00h) . . . . .	169
Table 119.	UIF3 register bit definition. . . . .	169
Table 120.	USB control register (UCTL 0ECh, reset value 00h) . . . . .	170
Table 121.	UCTL register bit definition . . . . .	170
Table 122.	USB endpoint0 status (USTA 0EDh, reset value 00h) . . . . .	171
Table 123.	USTA register bit definition . . . . .	171
Table 124.	USB endpoint select register (USEL 0EFh, reset value 00h) . . . . .	172
Table 125.	USEL register bit definition . . . . .	172
Table 126.	USB endpoint control register (UCON 0F1h, reset value 08h) . . . . .	173
Table 127.	UCON register bit definition . . . . .	173
Table 128.	USB FIFO valid size (USIZE 0F2h, reset value 00h) . . . . .	174
Table 129.	USIZE register bit definition . . . . .	174
Table 130.	USB FIFO base address high register (UBASEH 0F3h, reset value 00h) . . . . .	175
Table 131.	UBASEH register bit definition . . . . .	175
Table 132.	USB FIFO base address low register (UBASEL 0F4h, reset value 00h) . . . . .	175
Table 133.	UBASEL register bit definition . . . . .	175
Table 134.	USB setup command index register (USCI 0F5h, reset value 00h) . . . . .	176
Table 135.	USCI register bit definition . . . . .	176
Table 136.	USB setup command value register (USCV 0F6h, reset value 00h) . . . . .	176
Table 137.	USCV register bit definition. . . . .	176
Table 138.	ACON register (SFR 97h, reset value 00h) . . . . .	179
Table 139.	ACON register bit definition . . . . .	179
Table 140.	ADCPS register details (SFR 94h, Reset Value 00h) . . . . .	180
Table 141.	ADAT0 register (SFR 95h, reset value 00h) . . . . .	180
Table 142.	ADAT1 register (SFR 96h, reset value 00h) . . . . .	180
Table 143.	PCA0 and PCA1 registers . . . . .	182
Table 144.	CCON2 register bit definition (SFR 0FBh, reset value 10h) . . . . .	183
Table 145.	CCON2 register bit definition . . . . .	183
Table 146.	CCON3 register bit definition (SFR 0FCh, reset value 10h) . . . . .	183
Table 147.	CCON3 register bit definition . . . . .	183
Table 148.	PCA0 control register PCACON0 (SFR 0A4h, reset value 00h) . . . . .	187
Table 149.	PCA0 register bit definition . . . . .	187

Table 150.	PCA1 control register PCACON1 (SFR 0BCh, reset value 00h) . . . . .	188
Table 151.	PCA1 register bit definition . . . . .	188
Table 152.	PCA status register PCASTA (SFR 0A5h, reset value 00h) . . . . .	188
Table 153.	PCASTA register bit definition . . . . .	188
Table 154.	TCMMODE0 - TCMMODE5 (6 registers, reset value 00h) . . . . .	189
Table 155.	TCMMODE0 - TCMMODE5 register bit definition . . . . .	189
Table 156.	TCMMODE register configurations . . . . .	190
Table 157.	UPSD34xx memory configuration . . . . .	193
Table 158.	General I/O pins on PSD module . . . . .	196
Table 159.	HDL statement example generated from PSDsoft express for memory map . . . . .	199
Table 160.	VM register (address = csiop + offset E2h) . . . . .	203
Table 161.	Data width in different bus cycles . . . . .	205
Table 162.	CSIOP registers and their offsets (in hexadecimal) . . . . .	205
Table 163.	Flash memory instruction sequences . . . . .	209
Table 164.	Flash memory status bit definition . . . . .	212
Table 165.	Main Flash memory protection register definition (address = csiop + offset C0h) . . . . .	219
Table 166.	Secondary Flash memory protection/security register definition (csiop + offset C2h) . . . . .	219
Table 167.	DPLD and GPLD inputs . . . . .	220
Table 168.	OMC port and data bit assignments . . . . .	227
Table 169.	Output macrocell MCELLAB (address = csiop + offset 20h) . . . . .	228
Table 170.	Output macrocell MCELLBC (address = csiop + offset 21h) . . . . .	228
Table 171.	Output macrocell MCELLAB mask register (address = csiop + offset 22h) . . . . .	229
Table 172.	Output macrocell MCELLBC mask register (address = csiop + offset 23h) . . . . .	229
Table 173.	Input macrocell port A (address = csiop + offset 0Ah) . . . . .	230
Table 174.	Input macrocell port B (address = csiop + offset 0Bh) . . . . .	230
Table 175.	Input macrocell port C (address = csiop + offset 18h) . . . . .	230
Table 176.	Port operating modes . . . . .	232
Table 177.	Port configuration setting requirements . . . . .	233
Table 178.	MCU I/O mode port A data in register (address = csiop + offset 00h) . . . . .	234
Table 179.	MCU I/O mode port B data in register (address = csiop + offset 01h) . . . . .	234
Table 180.	MCU I/O mode port C data in register (address = csiop + offset 10h) . . . . .	234
Table 181.	MCU I/O mode port D Data in register (address = csiop + offset 11h) . . . . .	234
Table 182.	MCU I/O mode port A data out register (address = csiop + offset 04h) . . . . .	234
Table 183.	MCU I/O mode port B data out register (address = csiop + offset 05h) . . . . .	235
Table 184.	MCU I/O mode port C data out register (address = csiop + offset 12h) . . . . .	235
Table 185.	MCU I/O mode port D data out register (address = csiop + offset 13h) . . . . .	235
Table 186.	MCU I/O mode port A direction register (address = csiop + offset 06h) . . . . .	235
Table 187.	MCU I/O mode port B direction in register (address = csiop + offset 07h) . . . . .	235
Table 188.	MCU I/O mode port C direction register (address = csiop + offset 14h) . . . . .	235
Table 189.	MCU I/O mode port D direction register (address = csiop + offset 15h) . . . . .	236
Table 190.	Latched address output, port A contro register(address = csiop + offset 02h)  . . . . .	238
Table 191.	Latched address output, port B contro register (address = csiop + offset 03h)  . . . . .	239
Table 192.	Port A pin drive select register (address = csiop + offset 08h) . . . . .	241
Table 193.	Port B pin drive select register (address = csiop + offset 09h) . . . . .	242
Table 194.	Port C pin drive select register (address = csiop + offset 16h) . . . . .	242
Table 195.	Port D pin drive select register (address = csiop + offset 17h) . . . . .	242
Table 196.	Port A enable out register (address = csiop + offset 0Ch) . . . . .	242
Table 197.	Port B enable out register (address = csiop + offset 0Dh) . . . . .	242
Table 198.	Port C enable out register (address = csiop + offset 1Ah) . . . . .	242
Table 199.	Port D enable out register (address = csiop + offset 1Bh) . . . . .	242
Table 200.	Power management mode register PMMR0 (address = csiop + offset B0h) . . . . .	249
Table 201.	Power management mode register PMMR2 (address = csiop + offset B4h) . . . . .	249

Table 202.	Power management mode register PMMR3 (address = csiop + offset C7h) . . . . .	250
Table 203.	Function status during power-up reset, warm reset, power-down mode . . . . .	256
Table 204.	PSD module example, typ. power calculation at $V_{CC} = 5.0\text{ V}$ (turbo mode off) . . . . .	266
Table 205.	Absolute maximum ratings . . . . .	268
Table 206.	Operating conditions (5 V devices) . . . . .	269
Table 207.	Operating conditions (3.3 V devices) . . . . .	269
Table 208.	AC signal letters for timing . . . . .	269
Table 209.	AC signal behavior symbols for timing . . . . .	270
Table 210.	Major parameters . . . . .	271
Table 211.	MCU module DC characteristics . . . . .	271
Table 212.	PSD module DC characteristics (with 5 V $V_{DD}$ ) . . . . .	273
Table 213.	PSD module DC characteristics (with 3.3 V $V_{DD}$ ) . . . . .	274
Table 214.	External READ cycle AC characteristics (3 V or 5 V device) . . . . .	275
Table 215.	n, m, and x, y values . . . . .	275
Table 216.	External WRITE cycle AC characteristics (3 V or 5 V device) . . . . .	276
Table 217.	External clock drive . . . . .	277
Table 218.	A/D analog specification . . . . .	277
Table 219.	USB transceiver specification . . . . .	277
Table 220.	CPLD combinatorial timing (5 V PSD module) . . . . .	279
Table 221.	CPLD combinatorial timing (3 V PSD module) . . . . .	279
Table 222.	CPLD macrocell synchronous clock mode timing (5 V PSD module) . . . . .	280
Table 223.	CPLD macrocell synchronous clock mode timing (3 V PSD module) . . . . .	281
Table 224.	CPLD macrocell asynchronous clock mode timing (5 V PSD module) . . . . .	282
Table 225.	CPLD macrocell asynchronous clock mode timing (3 V PSD module) . . . . .	282
Table 226.	Input macrocell timing (5 V PSD module) . . . . .	283
Table 227.	Input macrocell timing (3 V PSD module) . . . . .	283
Table 228.	Program, WRITE and erase times (5 V, 3 V PSD modules) . . . . .	283
Table 229.	Port A peripheral data mode READ timing (5 V PSD module) . . . . .	284
Table 230.	Port A peripheral data mode READ timing (3 V PSD module) . . . . .	285
Table 231.	Port A peripheral data mode WRITE timing (5 V PSD module) . . . . .	285
Table 232.	Port A peripheral data mode WRITE timing (3 V PSD module) . . . . .	285
Table 233.	Supervisor reset and LVD . . . . .	286
Table 234.	ISC timing (5 V PSD module) . . . . .	286
Table 235.	ISC timing (3 V PSD module) . . . . .	287
Table 236.	I/O pin capacitance . . . . .	288
Table 237.	LQFP52 – 52-lead plastic thin, quad, flat package mechanical data . . . . .	290
Table 238.	LQFP80 – 80-lead plastic thin, quad, flat package mechanical data . . . . .	291
Table 239.	Ordering information scheme . . . . .	292
Table 240.	Order codes . . . . .	293
Table 241.	Document revision history . . . . .	299

## List of figures

Figure 1.	Block diagram . . . . .	21
Figure 2.	LQFP52 connections . . . . .	22
Figure 3.	LQFP80 connections . . . . .	23
Figure 4.	Functional modules . . . . .	29
Figure 5.	UPSD34xx memories . . . . .	30
Figure 6.	Comparison of UPSD34xx with standard 8032 performance . . . . .	33
Figure 7.	Instruction pre-fetch queue and branch cache . . . . .	34
Figure 8.	PFQ operation on multi-cycle instructions . . . . .	35
Figure 9.	UPSD34xx multi-cycle instructions compared to standard 8032 . . . . .	36
Figure 10.	8032 MCU registers . . . . .	38
Figure 11.	Program status word (PSW) register . . . . .	40
Figure 12.	Enabling and polling interrupts . . . . .	64
Figure 13.	Clock generation logic . . . . .	70
Figure 14.	Oscillator and clock connections . . . . .	77
Figure 15.	MCU module port pin function routing . . . . .	80
Figure 16.	MCU I/O cell block diagram for port 1 . . . . .	80
Figure 17.	MCU I/O cell block diagram for port 3 . . . . .	81
Figure 18.	MCU I/O cell block diagram for port 4 . . . . .	81
Figure 19.	Connecting external devices using ports A and B for address AD[15:0] . . . . .	87
Figure 20.	Connecting external devices using port A and an external latch for address AD[15:0] . . . . .	87
Figure 21.	A RD or PSEN bus cycle set to 5 MCU_CLK . . . . .	88
Figure 22.	Supervisor reset generation . . . . .	91
Figure 23.	Watchdog counter . . . . .	93
Figure 24.	Timer/counter mode 0: 13-bit counter . . . . .	100
Figure 25.	Timer/counter mode 2: 8-bit Auto-reload . . . . .	100
Figure 26.	Timer/counter mode 3: two 8-bit counters . . . . .	100
Figure 27.	Timer 2 in capture mode . . . . .	105
Figure 28.	Timer 2 in auto-reload mode . . . . .	106
Figure 29.	Timer 2 in baud rate generator mode . . . . .	106
Figure 30.	UART mode 0, block diagram . . . . .	113
Figure 31.	UART mode 0, timing diagram . . . . .	113
Figure 32.	UART mode 1, block diagram . . . . .	115
Figure 33.	UART mode 1, timing diagram . . . . .	115
Figure 34.	UART mode 2, block diagram . . . . .	117
Figure 35.	UART mode 2, timing diagram . . . . .	117
Figure 36.	UART mode 3, block diagram . . . . .	118
Figure 37.	UART mode 3, timing diagram . . . . .	118
Figure 38.	IrDA interface . . . . .	119
Figure 39.	Pulse shaping by the IrDA interface . . . . .	119
Figure 40.	Typical I2C bus configuration . . . . .	123
Figure 41.	Data transfer on an I <sup>2</sup> C bus . . . . .	125
Figure 42.	I <sup>2</sup> C interface SIOE block diagram . . . . .	128
Figure 43.	SPI device connection examples . . . . .	142
Figure 44.	SPI full-duplex data exchange . . . . .	144
Figure 45.	SPI receive operation example . . . . .	144
Figure 46.	SPI transmit operation example . . . . .	145
Figure 47.	SPI interface, master mode only . . . . .	146
Figure 48.	USB module block diagram . . . . .	151



Figure 49.	USB packets in a USB transfer example	153
Figure 50.	IN and OUT bulk transfers	154
Figure 51.	Interrupt transfer	155
Figure 52.	Control transfer	156
Figure 53.	FIFOs with no pairing	158
Figure 54.	FIFO pairing example (1/2 IN paired and 3/4 OUT paired)	159
Figure 55.	Typical self powered example	177
Figure 56.	10-bit ADC	179
Figure 57.	PCA0 block diagram	181
Figure 58.	Timer mode	184
Figure 59.	PWM mode - (x8), fixed frequency	185
Figure 60.	PWM mode - (x8) programmable frequency	186
Figure 61.	PSD module block diagram	191
Figure 62.	Memory page register	194
Figure 63.	Typical system memory map	198
Figure 64.	PSDsoft express memory mapping	199
Figure 65.	Mapping: split second Flash in half	200
Figure 66.	Mapping: all Flash in code space	201
Figure 67.	Mapping: small code / big data	201
Figure 68.	PSD module memory priority	202
Figure 69.	VM register control of memories	204
Figure 70.	VM register example corresponding to memory map example	204
Figure 71.	Data polling flowchart	214
Figure 72.	Data toggle flowchart	215
Figure 73.	DPLD and GPLD	221
Figure 74.	DPLD logic array	223
Figure 75.	GPLD: one OMC, one IMC, and one I/O port (typical pin, port A, B, or C)	224
Figure 76.	Detail of a single OMC	226
Figure 77.	OMC allocator	227
Figure 78.	Detail of a single IMC	230
Figure 79.	Detail of a single I/O port (typical of ports A, B, C)	232
Figure 80.	Simple PLD logic example	237
Figure 81.	Pin declarations in PSDsoft express for simple PLD example	237
Figure 82.	Using the design assistant in PSDsoft Express for simple PLD example	238
Figure 83.	Peripheral I/O mode	239
Figure 84.	Port A structure	243
Figure 85.	Port B structure	244
Figure 86.	Port C structure	246
Figure 87.	Port D structure	247
Figure 88.	Automatic power-down (APD) unit	252
Figure 89.	Power-down mode flowchart	253
Figure 90.	JTAG chain in UPSD34xx package	258
Figure 91.	Recommended 4-pin JTAG connections	259
Figure 92.	Recommended 6-pin JTAG connections	261
Figure 93.	Recommended JTAG connector	262
Figure 94.	Example of chaining UPSD34xx devices	263
Figure 95.	PLD ICC / frequency consumption (5 V range)	265
Figure 96.	PLD ICC / frequency consumption (3 V range)	266
Figure 97.	Switching waveforms – key	270
Figure 98.	External READ cycle (80-pin device only)	275
Figure 99.	External WRITE cycle (80-pin device only)	276
Figure 100.	Input to output disable / enable	278

Figure 101. Synchronous Clock mode timing – PLD .....	280
Figure 102. Asynchronous RESET / Preset .....	281
Figure 103. Asynchronous clock mode timing (product term clock) .....	281
Figure 104. Input macrocell timing (product term clock) .....	283
Figure 105. Peripheral I/O READ timing .....	284
Figure 106. Peripheral I/O WRITE timing .....	285
Figure 107. ISC timing .....	286
Figure 108. MCU module AC measurement I/O waveform .....	287
Figure 109. PSD module AC float I/O waveform .....	287
Figure 110. External clock cycle .....	288
Figure 111. PSD module AC measurement I/O waveform .....	288
Figure 112. PSD module AC measurement load circuit .....	288
Figure 113. LQFP52 – 52-lead plastic thin, quad, flat package outline .....	290
Figure 114. LQFP80 – 80-lead plastic thin, quad, flat package outline .....	291

Obsolete Product(s) - Obsolete Product(s)  
Obsolete Product(s) - Obsolete Product(s)

# 1 Description

The *Turbo Plus* UPSD34xx Series combines a powerful 8051-based microcontroller with a flexible memory structure, programmable logic, and a rich peripheral mix to form an ideal embedded controller. At its core is a fast 4-cycle 8032 MCU with a 4-byte instruction prefetch queue (PFQ) and a 4-entry fully associative branching cache (BC). The MCU is connected to a 16-bit internal instruction path to maximize performance, enabling loops of code in smaller localities to execute extremely fast. The 16-bit wide instruction path in the *Turbo Plus* Series allows double-byte instructions to be fetched from memory in a single memory cycle. This keeps the average performance near its peak performance (peak performance for 5 V, 40 MHz *Turbo Plus* UPSD34xx is 10 MIPS for single-byte instructions, and average performance will be approximately 9 MIPS for mix of single- and multi-byte instructions).

USB 2.0 (full speed, 12Mbps) is included, providing 10 endpoints, each with its own 64-byte FIFO to maintain high data throughput. Endpoint 0 (control endpoint) uses two of the 10 endpoints for In and Out directions, the remaining eight endpoints may be allocated in any mix to either type of transfers: Bulk or Interrupt.

Code development is easily managed without a hardware in-circuit emulator by using the serial JTAG debug interface. JTAG is also used for in-system programming (ISP) in as little as 10 seconds, perfect for manufacturing and lab development. The 8032 core is coupled to programmable system device (PSD) architecture to optimize the 8032 memory structure, offering two independent banks of Flash memory that can be placed at virtually any address within 8032 program or data address space, and easily paged beyond 64 Kbytes using on-chip programmable decode logic.

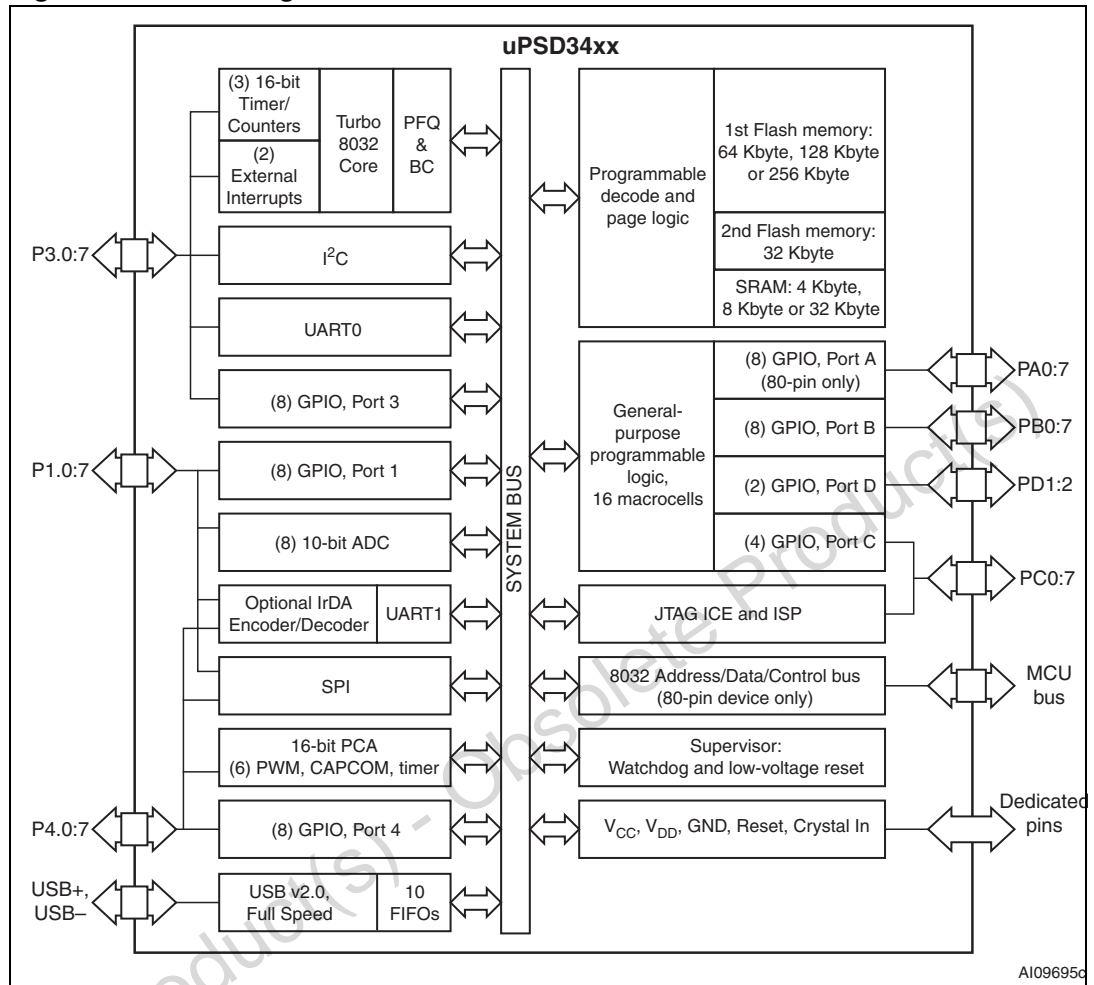
Dual Flash memory banks provide a robust solution for remote product updates in the field through in-application programming (IAP). Dual Flash banks also support EEPROM emulation, eliminating the need for external EEPROM chips.

General-purpose programmable logic (PLD) is included to build an endless variety of glue-logic, saving external logic devices. The PLD is configured using the software development tool, PSDsoft Express, available from the web at [www.st.com/psm](http://www.st.com/psm), at no charge.

The UPSD34xx also includes supervisor functions such as a programmable watchdog timer and low-voltage reset.

*Note:* For a list of known limitations of the UPSD34xx devices, please refer to [Section 34: Important notes](#).

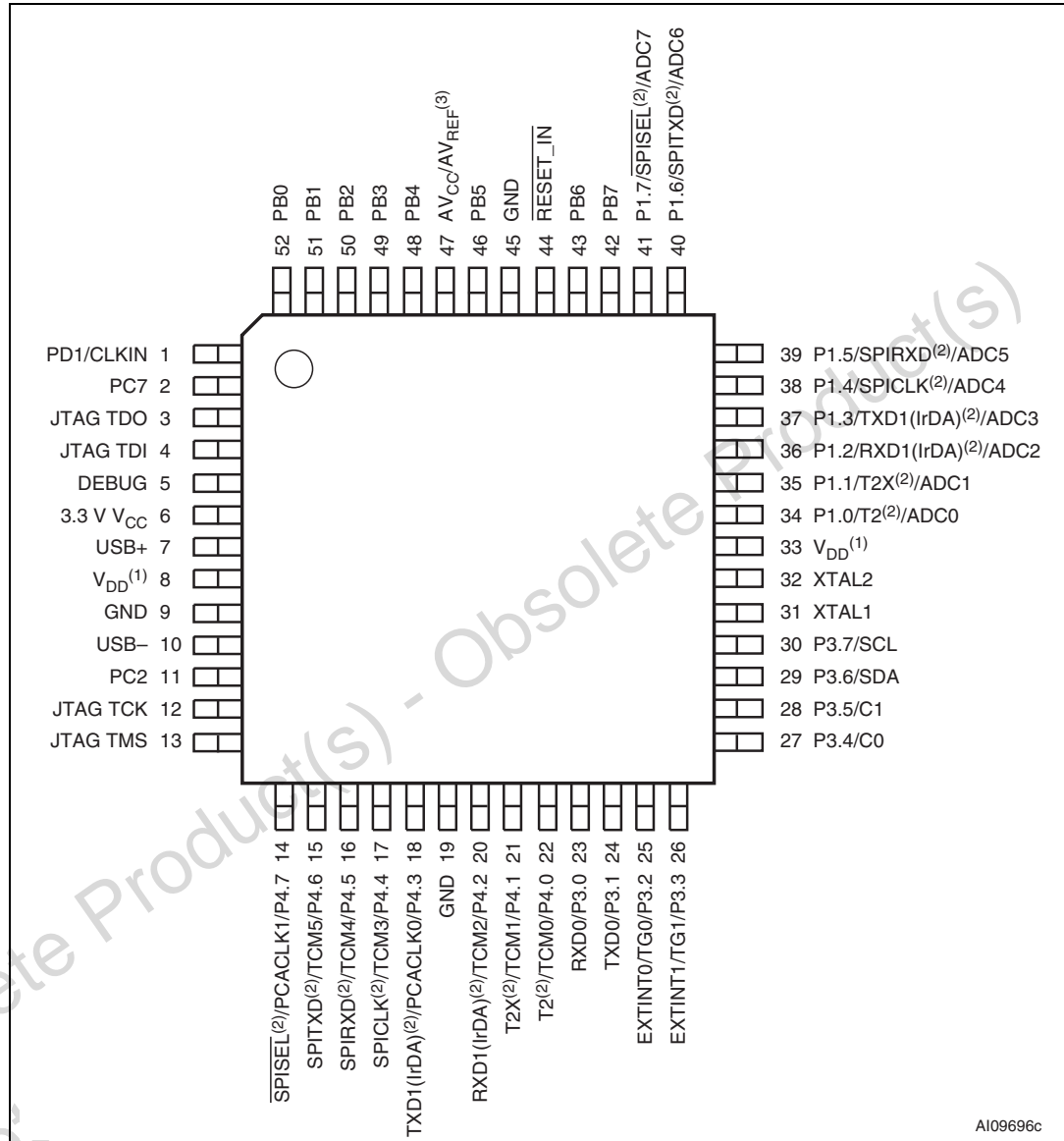
Figure 1. Block diagram



Obsolete Product(s)  
Obsolete Product(s)

## 2 Pin descriptions

Figure 2. LQFP52 connections

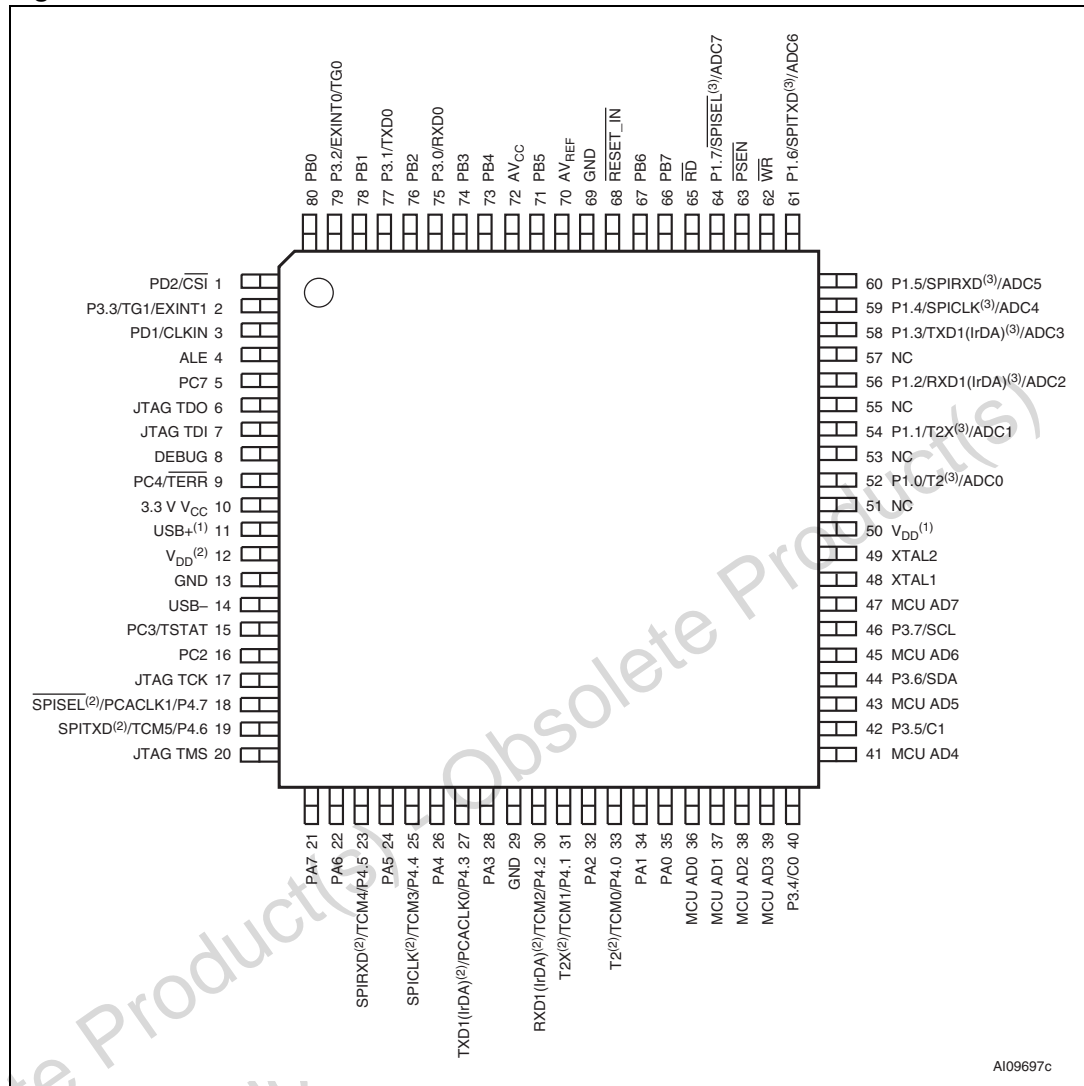


AI09696c

1. For 5 V applications,  $V_{DD}$  must be connected to a 5.0 V source. For 3.3 V applications,  $V_{DD}$  must be connected to a 3.3 V source.
2. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port1.
3.  $AV_{REF}$  and 3.3 V  $AV_{CC}$  are shared in the 52-pin package only. ADC channels must use 3.3 V as  $AV_{REF}$  for the 52-pin package.



Figure 3. LQFP80 connections



1. NC = Not connected
2. The USB+ pin needs a 1.5 kΩ pull-up resistor.
3. For 5 V applications, V<sub>DD</sub> must be connected to a 5.0 V source. For 3.3 V applications, V<sub>DD</sub> must be connected to a 3.3 V source.
4. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port1.

Table 2. Pin definitions

Port pin	Signal name	80-pin No.	52-pin No. <sup>(1)</sup>	In/out	Function		
					Basic	Alternate 1	Alternate 2
MCUAD0	AD0	36	N/A	I/O	External bus multiplexed address/data bus A0/D0		
MCUAD1	AD1	37	N/A	I/O	Multiplexed address/data bus A1/D1		
MCUAD2	AD2	38	N/A	I/O	Multiplexed address/data bus A2/D2		
MCUAD3	AD3	39	N/A	I/O	Multiplexed address/data bus A3/D3		
MCUAD4	AD4	41	N/A	I/O	Multiplexed address/data bus A4/D4		
MCUAD5	AD5	43	N/A	I/O	Multiplexed address/data bus A5/D5		
MCUAD6	AD6	45	N/A	I/O	Multiplexed address/data bus A6/D6		
MCUAD7	AD7	47	N/A	I/O	Multiplexed address/data bus A7/D7		
P1.0	T2 ADC0	52	34	I/O	General I/O port pin	Timer 2 Count input (T2)	ADC Channel 0 input (ADC0)
P1.1	T2X ADC1	54	35	I/O	General I/O port pin	Timer 2 Trigger input (T2X)	ADC Channel 1 input (ADC1)
P1.2	RxD1 ADC2	56	36	I/O	General I/O port pin	UART1 or IrDA Receive (RxD1)	ADC Channel 2 input (ADC2)
P1.3	TxD1 ADC3	58	37	I/O	General I/O port pin	UART or IrDA Transmit (TxD1)	ADC Channel 3 input (ADC3)
P1.4	SPICLK ADC4	59	38	I/O	General I/O port pin	SPI Clock Out (SPICLK)	ADC Channel 4 input (ADC4)
P1.5	SPIRxD ADC5	60	39	I/O	General I/O port pin	SPI Receive (SPIRxD)	ADC Channel 5 input (ADC5)
P1.6	SPITxD ADC6	61	40	I/O	General I/O port pin	SPI Transmit (SPITxD)	ADC Channel 6 input (ADC6)
P1.7	SPISEL ADC7	64	41	I/O	General I/O port pin	SPI Slave Select (SPISEL)	ADC Channel 7 input (ADC7)
P3.0	RxD0	75	23	I/O	General I/O port pin	UART0 Receive (RxD0)	

Table 2. Pin definitions (continued)

Port pin	Signal name	80-pin No.	52-pin No. <sup>(1)</sup>	In/out	Function		
					Basic	Alternate 1	Alternate 2
P3.1	TXD0	77	24	I/O	General I/O port pin	UART0 Transmit (TxD0)	
P3.2	EXINT0 TGO	79	25	I/O	General I/O port pin	Interrupt 0 input (EXTINT0)/Timer 0 gate control (TG0)	
P3.3	INT1	2	26	I/O	General I/O port pin	Interrupt 1 input (EXTINT1)/Timer 1 gate control (TG1)	
P3.4	C0	40	27	I/O	General I/O port pin	Counter 0 input (C0)	
P3.5	C1	42	28	I/O	General I/O port pin	Counter 1 input (C1)	
P3.6	SDA	44	29	I/O	General I/O port pin	I <sup>2</sup> C bus serial data (I <sup>2</sup> CSDA)	
P3.7	SCL	46	30	I/O	General I/O port pin	I <sup>2</sup> C bus clock (I <sup>2</sup> CSCL)	
P4.0	T2 TCM0	33	22	I/O	General I/O port pin	Program counter array0 PCA0-TCM0	Timer 2 count input (T2)
P4.1	T2X TCM1	31	21	I/O	General I/O port pin	PCA0-TCM1	Timer 2 trigger input (T2X)
P4.2	RXD1 TCM2	30	20	I/O	General I/O port pin	PCA0-TCM2	UART1 or IrDA Receive (RxD1)
P4.3	TXD1 PCACLK0	27	18	I/O	General I/O port pin	PCACLK0	UART1 or IrDA Transmit (TxD1)
P4.4	SPICLK TCM3	25	17	I/O	General I/O port pin	Program counter Array1 PCA1-TCM3	SPI clock out (SPICLK)
P4.5	SPIRXD TCM4	23	16	I/O	General I/O port pin	PCA1-TCM4	SPI Receive (SPIRXD)
P4.6	SPITXD	19	15	I/O	General I/O port pin	PCA1-TCM5	SPI Transmit (SPITXD)
P4.7	SPISEL PCACLK1	18	14	I/O	General I/O port pin	PCACLK1	SPI Slave Select (SPISEL)
AV <sub>REF</sub>		70	N/A	I	Reference Voltage input for ADC. Connect AV <sub>REF</sub> to V <sub>CC</sub> if the ADC is not used.		
RD		65	N/A	O	READ signal, external bus		
WR		62	N/A	O	WRITE signal, external bus		
PSEN		63	N/A	O	PSEN signal, external bus		