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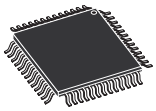
UPSD3422 UPSD3433 UPSD3434 UPSD3454

Turbo Plus series

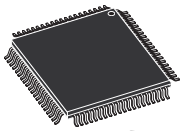
Fast Turbo 8032 MCU with USB and programmable logic

Features

- Fast 8-bit Turbo 8032 MCU, 40 MHz
  - Advanced core, 4-clocks per instruction
  - 10 MIPs peak performance at 40 MHz (5 V)
  - JTAG debug and in-system programming
  - 16-bit internal instruction path fetches double-byte instruction in a single memory cycle
  - Branch cache & 4 instruction prefetch queue
  - Dual XDATA pointers with automatic increment and decrement
  - Compatible with 3rd party 8051 tools
- Dual Flash memories with memory management
  - Place either memory into 8032 program address space or data address space
  - READ-while-WRITE operation for in-application programming and EEPROM emulation
  - Single voltage program and erase
  - 100 000 guaranteed erase cycles, 15-year retention
- Clock, reset, and power supply management
  - Flexible 8-level CPU clock divider register
  - Normal, Idle, and power-down modes
  - Power-on-reset and low-voltage-reset supervisor
  - Programmable watchdog timer
- Programmable logic, general purpose
  - 16 macrocells for logic applications (e.g., shifters, state machines, chip-selects, glue-logic to keypads, and LCDs)
- A/D converter
  - Eight channels, 10-bit resolution, 6 µs
- Operating voltage source (±10%)
  - 5 V devices: 5.0 V and 3.3 V sources
  - 3.3 V devices: 3.3 V source



LQFP52 (T), 52-lead, thin, quad, flat



LQFP80 (U), 80-lead, thin, quad, flat

- Communication interfaces
  - USB v2.0 Full Speed (12Mbps)
  - 10 endpoint pairs (In/Out), each endpoint with 64-byte FIFO (supports Control, Int., and Bulk transfer types)
  - I^2C Master/Slave controller, 333kHz
  - SPI Master controller, 10MHz
  - Two UARTs with independent baud rate
  - IrDA protocol: up to 115 kbaud
  - Up to 43 I/O, 5 V tolerant uPSD34xxV
- Timers and interrupts
  - Three 8032 standard 16-bit timers
  - Programmable counter array (PCA), six 16-bit modules for PWM, CAPCOM, and timers
  - 8/10/16-bit PWM operation
  - 12 Interrupt sources with two external interrupt pins
- Packages
  - ECOPACK® compliant

Table 1. Device summary

Reference	Part number
uPSD3422	UPSD3422E, UPSD3422EV
uPSD3433E	UPSD3433E, UPSD3433EV
uPSD3434	UPSD3434E, UPSD3434EV
uPSD3454	UPSD3454E, UPSD3454EV

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1 Description

The *Turbo Plus* UPSD34xx Series combines a powerful 8051-based microcontroller with a flexible memory structure, programmable logic, and a rich peripheral mix to form an ideal embedded controller. At its core is a fast 4-cycle 8032 MCU with a 4-byte instruction prefetch queue (PFQ) and a 4-entry fully associative branching cache (BC). The MCU is connected to a 16-bit internal instruction path to maximize performance, enabling loops of code in smaller localities to execute extremely fast. The 16-bit wide instruction path in the *Turbo Plus* Series allows double-byte instructions to be fetched from memory in a single memory cycle. This keeps the average performance near its peak performance (peak performance for 5 V, 40 MHz Turbo *Plus* UPSD34xx is 10 MIPS for single-byte instructions, and average performance will be approximately 9 MIPS for mix of single- and multi-byte instructions).

USB 2.0 (full speed, 12Mbps) is included, providing 10 endpoints, each with its own 64-byte FIFO to maintain high data throughput. Endpoint 0 (control endpoint) uses two of the 10 endpoints for In and Out directions, the remaining eight endpoints may be allocated in any mix to either type of transfers: Bulk or Interrupt.

Code development is easily managed without a hardware in-circuit emulator by using the serial JTAG debug interface. JTAG is also used for in-system programming (ISP) in as little as 10 seconds, perfect for manufacturing and lab development. The 8032 core is coupled to programmable system device (PSD) architecture to optimize the 8032 memory structure, offering two independent banks of Flash memory that can be placed at virtually any address within 8032 program or data address space, and easily paged beyond 64 Kbytes using on-chip programmable decode logic.

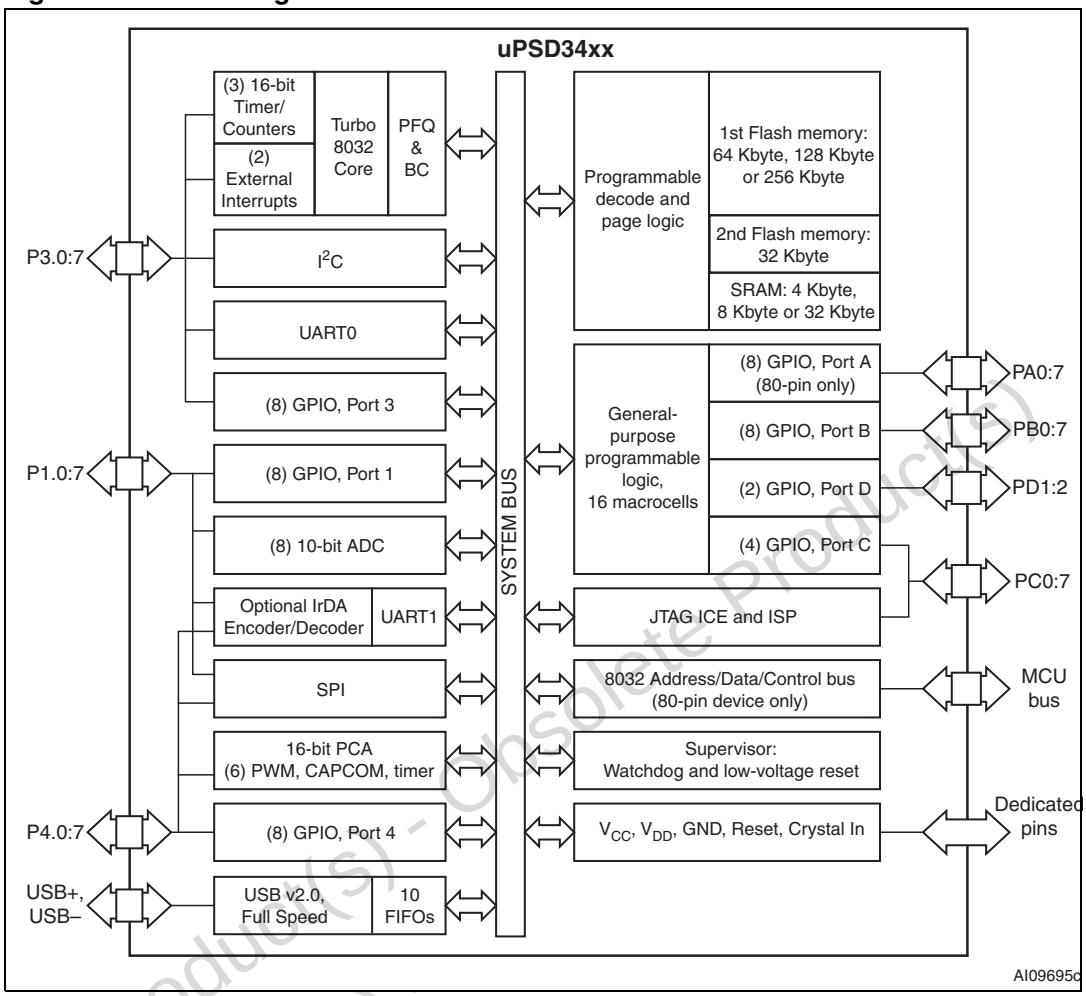
Dual Flash memory banks provide a robust solution for remote product updates in the field through in-application programming (IAP). Dual Flash banks also support EEPROM emulation, eliminating the need for external EEPROM chips.

General-purpose programmable logic (PLD) is included to build an endless variety of glue-logic, saving external logic devices. The PLD is configured using the software development tool, PSDsoft Express, available from the web at **www.st.com/psm**, at no charge.

The UPSD34xx also includes supervisor functions such as a programmable watchdog timer and low-voltage reset.

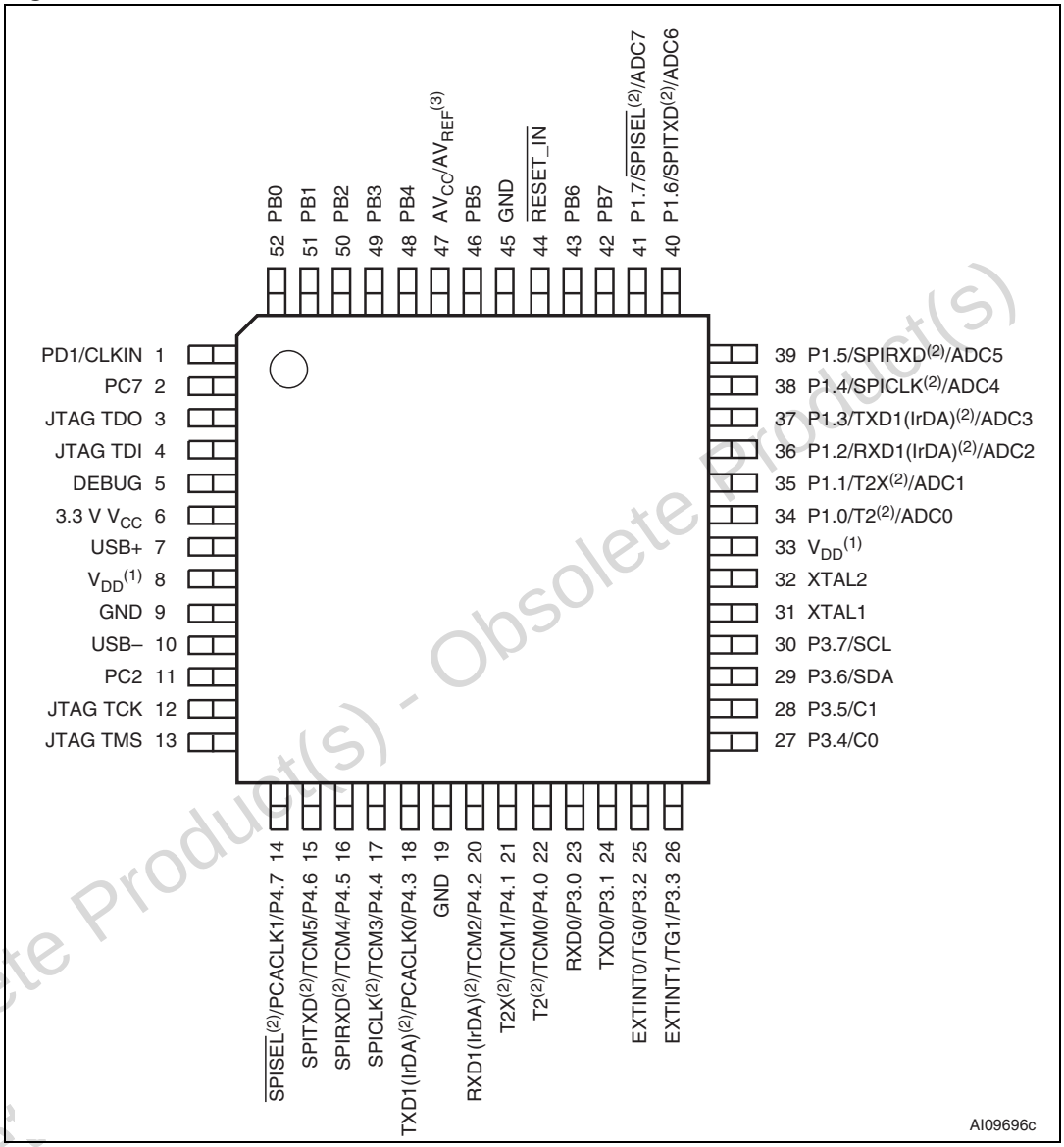
Note: For a list of known limitations of the UPSD34xx devices, please refer to Section 34: Important notes.

Figure 1. Block diagram



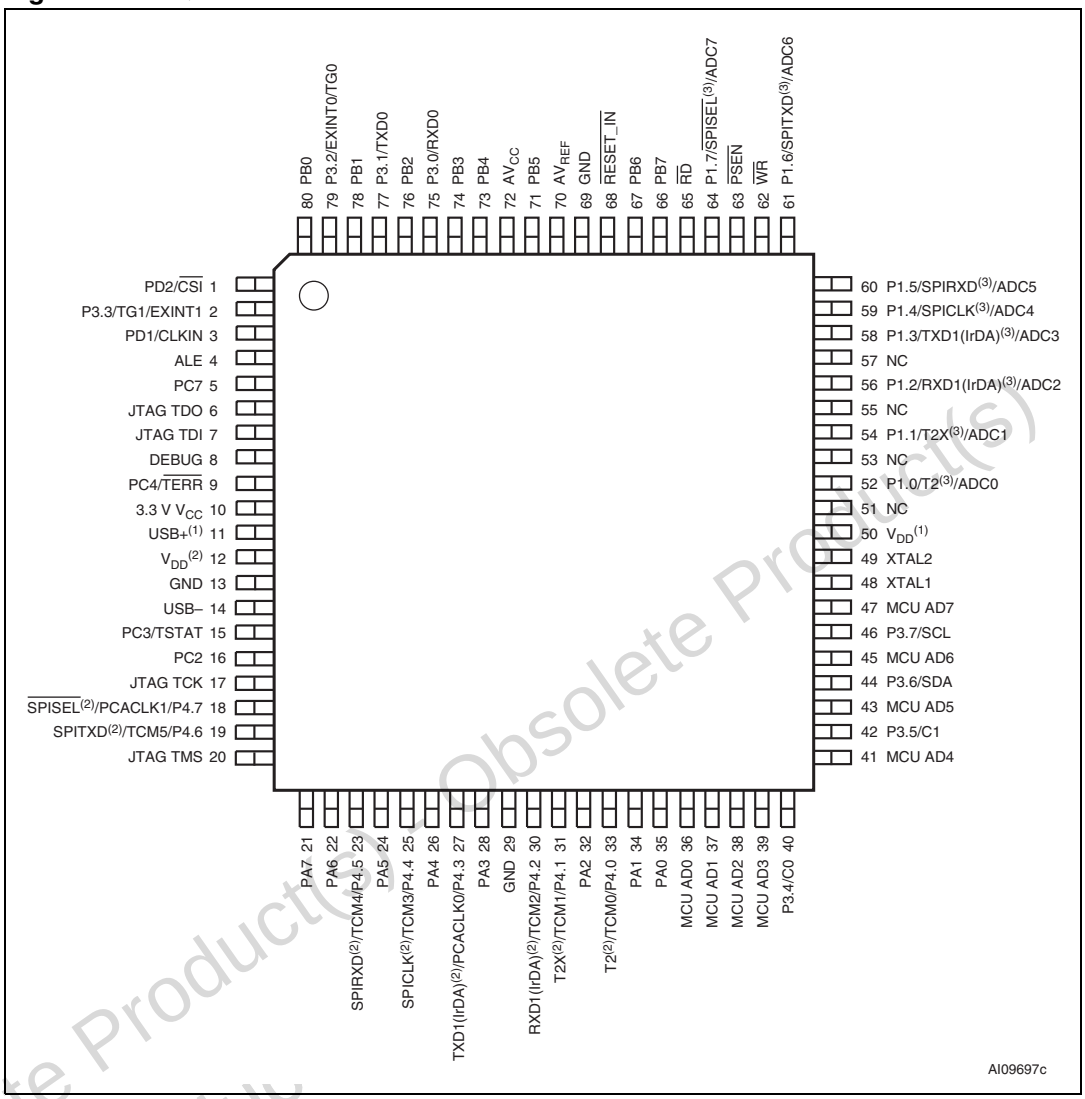
2 Pin descriptions

Figure 2. LQFP52 connections



1. For 5 V applications, V_{DD} must be connected to a 5.0 V source. For 3.3 V applications, V_{DD} must be connected to a 3.3 V source.
2. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port1.
3. AV_{REF} and 3.3 V AV_{CC} are shared in the 52-pin package only. ADC channels must use 3.3 V as AV_{REF} for the 52-pin package.

Figure 3. LQFP80 connections



1. NC = Not connected
2. The USB+ pin needs a 1.5 kΩ pull-up resistor.
3. For 5 V applications, V_{DD} must be connected to a 5.0 V source. For 3.3 V applications, V_{DD} must be connected to a 3.3 V source.
4. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port1.

Table 2. Pin definitions

Port pin	Signal name	80-pin No.	52-pin No.(1)	In/out	Function		
					Basic	Alternate 1	Alternate 2
MCUAD0	AD0	36	N/A	I/O	External bus multiplexed address/data bus A0/D0		
MCUAD1	AD1	37	N/A	I/O	Multiplexed address/data bus A1/D1		
MCUAD2	AD2	38	N/A	I/O	Multiplexed address/data bus A2/D2		
MCUAD3	AD3	39	N/A	I/O	Multiplexed address/data bus A3/D3		
MCUAD4	AD4	41	N/A	I/O	Multiplexed address/data bus A4/D4		
MCUAD5	AD5	43	N/A	I/O	Multiplexed address/data bus A5/D5		
MCUAD6	AD6	45	N/A	I/O	Multiplexed address/data bus A6/D6		
MCUAD7	AD7	47	N/A	I/O	Multiplexed address/data bus A7/D7		
P1.0	T2 ADC0	52	34	I/O	General I/O port pin	Timer 2 Count input (T2)	ADC Channel 0 input (ADC0)
P1.1	T2X ADC1	54	35	I/O	General I/O port pin	Timer 2 Trigger input (T2X)	ADC Channel 1 input (ADC1)
P1.2	RxD1 ADC2	56	36	I/O	General I/O port pin	UART1 or IrDA Receive (RxD1)	ADC Channel 2 input (ADC2)
P1.3	TXD1 ADC3	58	37	I/O	General I/O port pin	UART or IrDA Transmit (TxD1)	ADC Channel 3 input (ADC3)
P1.4	SPICLK ADC4	59	38	I/O	General I/O port pin	SPI Clock Out (SPICLK)	ADC Channel 4 input (ADC4)
P1.5	SPIRxD ADC5	60	39	I/O	General I/O port pin	SPI Receive (SPIRxD)	ADC Channel 5 input (ADC5)
P1.6	SPITXD ADC6	61	40	I/O	General I/O port pin	SPI Transmit (SPITxD)	ADC Channel 6 input (ADC6)
P1.7	SPISEL ADC7	64	41	I/O	General I/O port pin	SPI Slave Select (SPISEL)	ADC Channel 7 input (ADC7)
P3.0	RxD0	75	23	I/O	General I/O port pin	UART0 Receive (RxD0)	

Table 2. Pin definitions (continued)

Port pin	Signal name	80-pin No.	52-pin No.(1)	In/out	Function		
					Basic	Alternate 1	Alternate 2
P3.1	TXD0	77	24	I/O	General I/O port pin	UART0 Transmit (TxD0)	
P3.2	EXINT0 TGO	79	25	I/O	General I/O port pin	Interrupt 0 input (EXTINT0)/Timer 0 gate control (TG0)	
P3.3	INT1	2	26	I/O	General I/O port pin	Interrupt 1 input (EXTINT1)/Timer 1 gate control (TG1)	
P3.4	C0	40	27	I/O	General I/O port pin	Counter 0 input (C0)	
P3.5	C1	42	28	I/O	General I/O port pin	Counter 1 input (C1)	
P3.6	SDA	44	29	I/O	General I/O port pin	I^2C bus serial data (I^2CSDA)	
P3.7	SCL	46	30	I/O	General I/O port pin	I^2C bus clock (I^2CSCL)	
P4.0	T2 TCM0	33	22	I/O	General I/O port pin	Program counter array0 PCA0-TCM0	Timer 2 count input (T2)
P4.1	T2X TCM1	31	21	I/O	General I/O port pin	PCA0-TCM1	Timer 2 trigger input (T2X)
P4.2	RXD1 TCM2	30	20	I/O	General I/O port pin	PCA0-TCM2	UART1 or IrDA Receive (RxD1)
P4.3	TXD1 PCACLK0	27	18	I/O	General I/O port pin	PCACLK0	UART1 or IrDA Transmit (TxD1)
P4.4	SPICLK TCM3	25	17	I/O	General I/O port pin	Program counter Array1 PCA1-TCM3	SPI clock out (SPICLK)
P4.5	SPIRXD TCM4	23	16	I/O	General I/O port pin	PCA1-TCM4	SPI Receive (SPIRxD)
P4.6	SPITXD	19	15	I/O	General I/O port pin	PCA1-TCM5	SPI Transmit (SPITxD)
P4.7	SPISEL PCACLK1	18	14	I/O	General I/O port pin	PCACLK1	SPI Slave Select (SPISEL)
AV_{REF}		70	N/A	I	Reference Voltage input for ADC. Connect AV_{REF} to V_{CC} if the ADC is not used.		
RD		65	N/A	O	READ signal, external bus		
WR		62	N/A	O	WRITE signal, external bus		
PSEN		63	N/A	O	PSEN signal, external bus		