



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## 2-Port USB 2.0 Hi-Speed Hub Controller

### PRODUCT FEATURES

Datasheet

#### General Description

The SMSC USB2412 hub is a low-power, single transaction translator (STT) hub controller IC with two downstream ports for embedded USB applications. The SMSC hub controller supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

#### Features

- Fully integrated USB termination and pull-up/pull-down resistors
- Supports a single external 3.3 V supply source; internal regulators provide 1.2 V internal core voltage
- On-chip 24 MHz crystal driver or external 24 MHz clock input
- ESD protection up to 4 kilovolts on all USB pins
- Supports self-powered operation
- Contains a built-in default configuration; no external configuration options or components are required
- Downstream ports as optional non-removable ports
- Supports compound devices on a port-by-port basis
- 28-pin QFN (5 x 5 mm) lead-free RoHS compliant package
- Supports the commercial temperature range: 0°C to +70°C

#### Highlights

- High performance, low-power, small footprint hub controller IC with two downstream ports
- Fully compliant with the *USB 2.0 Specification 1*.
- 28QFN low pin count package
- Optimized for minimal bill-of-materials and low cost designs

#### Applications

- Automobile/home audio systems
- Cable/DSL modems
- Embedded systems
- Gaming consoles
- HDD enclosures
- IP telephony
- KVM switches
- LCD monitors and TVs
- Multi-function USB peripherals
- Mobile PC docking
- PC motherboards
- PC media drive bay
- Portable hub boxes
- Point-of-Sale (POS) systems
- Printers and scanners
- Server front panels
- Set-top boxes, DVD players, DVR/PVR
- Thin client terminals

**Order Numbers:**

| ORDER NUMBERS* | LEAD-FREE<br>ROHS COMPLIANT<br>PACKAGE   | PACKAGE SIZE   | REEL SIZE |
|----------------|--|----------------|-----------|
| USB2412-DZK    | 28-Pin QFN Lead-Free, RoHS<br>Compliant Package<br>(includes tape and reel option) | 5 x 5 x 0.5 mm | -         |
| USB2412-DZK-TR |  |                |           |

This product meets the halogen maximum concentration values per IEC61249-2-21  
 For RoHS compliance and environmental information, please visit [www.smsc.com/rohs](http://www.smsc.com/rohs)



80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000 or 1 (800) 443-SEMI

Copyright © 2011 SMSC or its subsidiaries. All rights reserved.

Circuit diagrams and other information relating to SMSC products are included as a means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. Although the information has been checked and is believed to be accurate, no responsibility is assumed for inaccuracies. SMSC reserves the right to make changes to specifications and product descriptions at any time without notice. Contact your local SMSC sales office to obtain the latest specifications before placing your product order. The provision of this information does not convey to the purchaser of the described semiconductor devices any licenses under any patent rights or other intellectual property rights of SMSC or others. All sales are expressly conditional on your agreement to the terms and conditions of the most recently dated version of SMSC's standard Terms of Sale Agreement dated before the date of your order (the "Terms of Sale Agreement"). The product may contain design defects or errors known as anomalies which may cause the product's functions to deviate from published specifications. Anomaly sheets are available upon request. SMSC products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of SMSC and further testing and/or modification will be fully at the risk of the customer. Copies of this document or other SMSC literature, as well as the Terms of Sale Agreement, may be obtained by visiting SMSC's website at <http://www.smsc.com>. SMSC is a registered trademark of Standard Microsystems Corporation ("SMSC"). Product names and company names are the trademarks of their respective holders.

**SMSC DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT AND THE LIKE, AND ANY AND ALL WARRANTIES ARISING FROM ANY COURSE OF DEALING OR USAGE OF TRADE. IN NO EVENT SHALL SMSC BE LIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES; OR FOR LOST DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND; REGARDLESS OF THE FORM OF ACTION, WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF SMSC OR OTHERS; STRICT LIABILITY; BREACH OF WARRANTY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER OR NOT SMSC HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.**

## Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

| Example             | Description   |
|---------------------|---|
| <b>BIT</b>          | Name of a single bit within a field   |
| <b>FIELD.BIT</b>    | Name of a single bit (BIT) in FIELD   |
| x...y               | Range from x to y, inclusive  |
| <b>BITS[m:n]</b>    | Groups of bits from m to n, inclusive   |
| <b>PIN</b>          | Pin Name  |
| zzzzb               | Binary number (value zzzz)  |
| 0zzzz               | Hexadecimal number (value zzz)  |
| zzh                 | Hexadecimal number (value zz)   |
| rsvd                | Reserved memory location. Must write 0, read value indeterminate  |
| code                | Instruction code, or API function or parameter  |
| <i>Section Name</i> | Section or Document name  |
| x                   | Don't care  |
| <Parameter>         | <> indicate a Parameter is optional or is only used under some conditions   |
| {,Parameter}        | Braces indicate Parameter(s) that repeat one or more times  |
| [Parameter]         | Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters. |



## Table of Contents

---

|                  |                      |          |
|------------------|----------------------|----------|
| <b>Chapter 1</b> | <b>Block Diagram</b> | <b>7</b> |
|------------------|----------------------|----------|

---

|                  |  |          |
|------------------|--|----------|
| <b>Chapter 2</b> | <b>Pin Descriptions</b>                | <b>8</b> |
| 2.1              | Pin Configuration                      | 8        |
| 2.2              | 28-Pin Table                           | 9        |
| 2.3              | Pin Descriptions (Grouped by Function) | 10       |
| 2.4              | Buffer Type Descriptions               | 12       |
| 2.5              | Strap Option Pins                      | 12       |

---

|                  |                                       |           |
|------------------|---------------------------------------|-----------|
| <b>Chapter 3</b> | <b>Internal Default Configuration</b> | <b>14</b> |
| 3.1              | Hub Configuration                     | 14        |
| 3.2              | Reset                                 | 14        |
| 3.2.1            | External Hardware RESET_N             | 14        |
| 3.2.2            | USB Bus Reset                         | 15        |

---

|                  |                                |           |
|------------------|--------------------------------|-----------|
| <b>Chapter 4</b> | <b>DC Parameters</b>           | <b>16</b> |
| 4.1              | Maximum Guaranteed Ratings     | 16        |
| 4.2              | Operating Conditions           | 16        |
| 4.2.1            | Pin Capacitance                | 19        |
| 4.2.2            | Package Thermal Specifications | 19        |

---

|                  |                          |           |
|------------------|--------------------------|-----------|
| <b>Chapter 5</b> | <b>AC Specifications</b> | <b>20</b> |
| 5.1              | Oscillator/Crystal       | 20        |
| 5.2              | External Clock           | 21        |
| 5.2.1            | USB 2.0                  | 21        |

---

|                  |                             |           |
|------------------|-----------------------------|-----------|
| <b>Chapter 6</b> | <b>Package Outline</b>      | <b>22</b> |
| 6.1              | Tape and Reel Specification | 24        |

## List of Figures

|            |   |    |
|------------|---|----|
| Figure 1.1 | USB2412 Block Diagram   | 7  |
| Figure 2.1 | USB2412 28-Pin QFN  | 8  |
| Figure 2.2 | Non-Removable Pin Strap Example                                       | 12 |
| Figure 2.3 | LED Pin Strap Example   | 13 |
| Figure 3.1 | Reset_N Timing  | 15 |
| Figure 4.1 | Supply Rise Time Model  | 17 |
| Figure 5.1 | Typical Crystal Circuit   | 20 |
| Figure 5.2 | Formula to Find the Value of C1 and C2                                | 20 |
| Figure 6.1 | USB2412 28-Pin QFN Package Outline (5x5 mm Body, 0.5 Pitch, 3.1 ePad) | 22 |
| Figure 6.2 | Recommended Printed Circuit Board (PCB) Land Pattern                  | 23 |
| Figure 6.3 | 28-Pin Package Tape Dimensions and Part Orientation (mm)              | 24 |
| Figure 6.4 | 28-Pin Package Tape Length and Part Quantity                          | 24 |
| Figure 6.5 | Package Reel Specifications   | 25 |

## List of Tables

|           |                                       |    |
|-----------|---------------------------------------|----|
| Table 2.1 | USB2412 28-Pin Table                  | 9  |
| Table 2.2 | USB2412 Pin Descriptions              | 10 |
| Table 2.3 | Buffer Type Descriptions              | 12 |
| Table 3.1 | Reset_N Timing                        | 15 |
| Table 4.1 | DC Electrical Characteristics         | 17 |
| Table 4.2 | Pin Capacitance                       | 19 |
| Table 4.3 | 28-Pin QFN Package Thermal Parameters | 19 |
| Table 5.1 | Crystal Circuit Legend                | 20 |
| Table 6.1 | Package Parameters                    | 22 |

# Chapter 1 Block Diagram

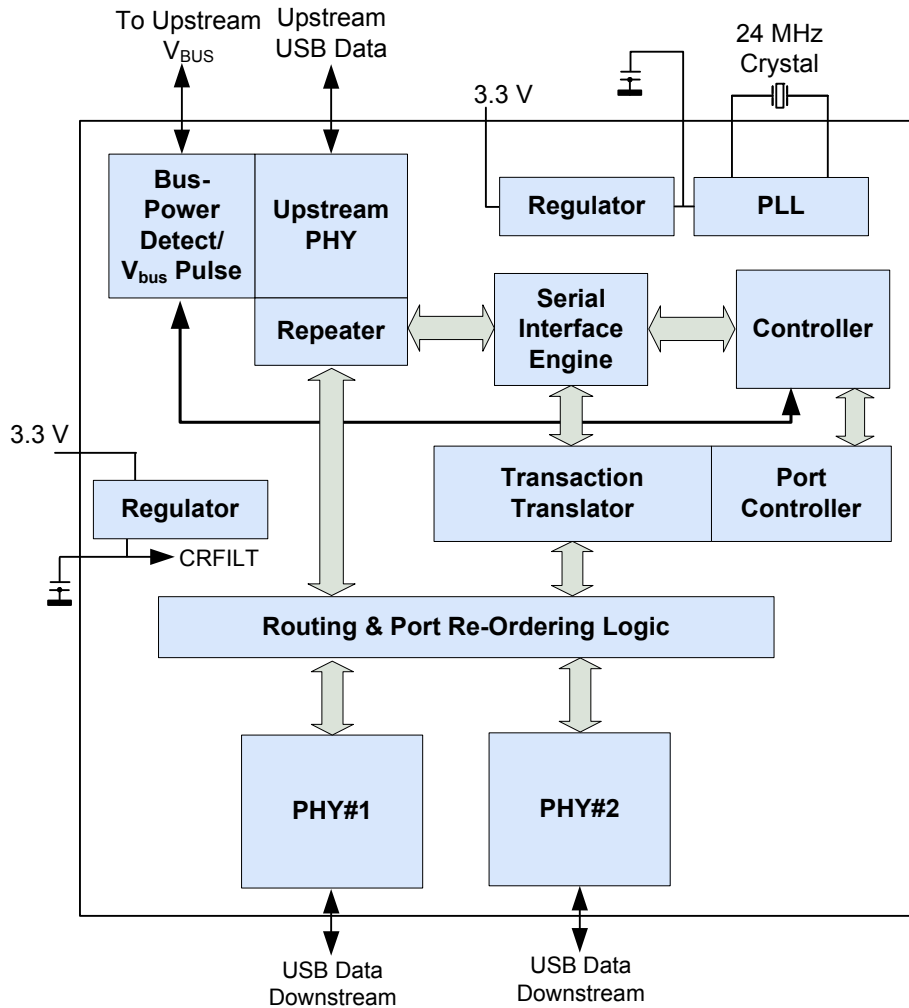


Figure 1.1 USB2412 Block Diagram



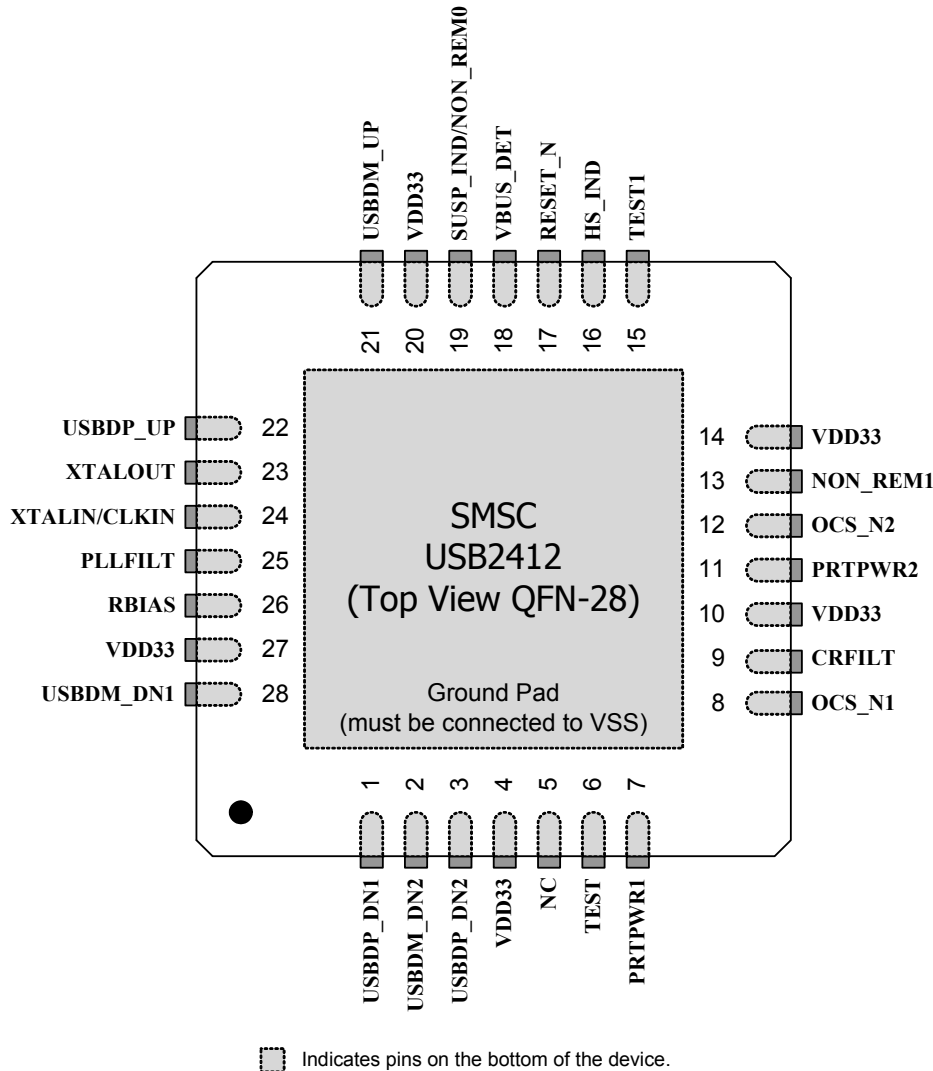
## Chapter 2 Pin Descriptions

This chapter is organized by a set of pin configurations followed by a corresponding pin list organized by function according to their associated interface. A detailed description list of each signal (named in the pin list) is organized by function in [Table 2.2, “USB2412 Pin Descriptions,” on page 10](#). Refer to [Table 2.3, “Buffer Type Descriptions,” on page 12](#) for a list of buffer types.

The “N” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “N” is not present after the signal name, the signal is asserted when it is at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

### 2.1 Pin Configuration



**Figure 2.1 USB2412 28-Pin QFN**

## 2.2 28-Pin Table

Table 2.1 USB2412 28-Pin Table

| <b>UPSTREAM USB 2.0 INTERFACES (3 PINS)</b>          |                     |                |           |
|--|---------------------|----------------|-----------|
| USBDP_UP   | USBDM_UP            | VBUS_DET       |           |
| <b>DOWNSTREAM 2-PORT USB 2.0 INTERFACES (9 PINS)</b> |                     |                |           |
| USBDP_DN1  | USBDM_DN1           | USBDP_DN2      | USBDM_DN2 |
| PRT_PWR1   | PRT_PWR2            | OCS_N1         | OCS_N2    |
| RBIAS  |                     |                |           |
| <b>MISC (7 PINS)</b>                                 |                     |                |           |
| RESET_N  | TEST                | XTALIN / CLKIN | XTALOUT   |
| NON_REM1   | SUSP_IND / NON_REM0 | HS_IND         |           |
| <b>POWER, GROUND, AND NO CONNECTS (9 PINS)</b>       |                     |                |           |
| (5) VDD33  | CRFILT              | PLLFILT        | VSS       |
| NC   |                     |                |           |
| <b>TOTAL 28</b>                                      |                     |                |           |

## 2.3 Pin Descriptions (Grouped by Function)

**Table 2.2 USB2412 Pin Descriptions**

| PIN #                                | SYMBOL   | BUFFER TYPE | DESCRIPTION  |
|--------------------------------------|--|-------------|--|
| <b>UPSTREAM USB 2.0 INTERFACES</b>   |  |             |  |
| 21<br>22                             | USBDM_UP<br>USBDP_UP                             | IO-U        | USB Bus Data: connect to the upstream USB bus data signals (host, port, or upstream hub).  |
| 18                                   | VBUS_DET   | I/O12       | <p>Detect Upstream VBUS Power: detects the state of upstream VBUS power. The SMSC hub monitors <b>VBUS_DET</b> to determine when to assert the internal D+ pull-up resistor which signals a connect event.</p> <p>When designing a detachable hub, this pin should be connected to VBUS on the upstream port via a 2 to 1 voltage divider.</p> <p>For self-powered applications with a permanently attached host, this pin must be connected to a dedicated host control output, or connected to 3.3 V domain that powers the host.'</p> <p>According to Section 7.2.1 of the <i>USB 2.0 Specification 1.</i>, a downstream port can never provide power to its D+ or D- pull-up resistors unless the upstream port's VBUS is in the asserted (powered) state.</p> <p><b>VBUS_DET</b> monitors the state of the upstream VBUS signal and will not pull-up the D+ resistor if VBUS is not active. If VBUS goes from an active to an inactive state (Not Powered), the hub will remove power from the D+ pull-up resistor within 10 seconds.</p> |
| <b>DOWNSTREAM USB 2.0 INTERFACES</b> |  |             |  |
| 1<br>3<br>28<br>2                    | USBDP_DN1<br>USBDP_DN2<br>USBDM_DN1<br>USBDM_DN2 | IO-U        | Hi-Speed USB Data: connect to the downstream USB peripheral devices attached to the hub's ports.   |
| 7<br>11                              | PRTPOWER1<br>PRTPOWER2                           | I/O12       | USB Power Enable: enables power to USB peripheral devices that are downstream, where the hub supports active high power controllers only.  |
| 8<br>12                              | OCS_N1<br>OCS_N2                                 | IPU         | Over-Current Sense: input from external current monitor indicating an over-current condition. This pin contains an internal pull-up to the 3.3 V supply.   |
| 26                                   | RBIAS  | I-R         | USB Transceiver Bias: a 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.   |
| <b>MISC</b>                          |  |             |  |
| 13                                   | NON_REM1   | I/O         | <p>Non-removable Port Strap Option: this pin is sampled (in conjunction with <b>SUSP_IND/NON_REM0</b>) at <b>RESET_N</b> negation to determine if ports [2:1] contain permanently attached (non-removable) devices:</p> <p>NON_REM[1:0] = 00: all ports are removable<br/>                     NON_REM[1:0] = 01: port 1 is non-removable<br/>                     NON_REM[1:0] = 10 and 11: ports 1 and 2 are non-removable</p> <p>See <a href="#">Section 2.5, "Strap Option Pins"</a> for details.</p>  |

Table 2.2 USB2412 Pin Descriptions (continued)

| PIN #                                 | SYMBOL     | BUFFER TYPE | DESCRIPTION  |
|---------------------------------------|------------|-------------|--|
| 19                                    | SUSP_IND / | I/O         | Active/Suspend Status LED (suspend indicator): indicates the USB hub state. See <a href="#">Section 2.5, "Strap Option Pins"</a> for details.<br><br>NON_REM0 = 0: <b>SUSP_IND</b> is active high<br>NON_REM0 = 1: <b>SUSP_IND</b> is active low<br><br>negated = unconfigured, or configured and in USB suspend<br>asserted = hub is configured and is active (i.e., not in suspend)  |
|                                       | NON_REM0   |             | Non-removable Port Strap Option: this pin is sampled (in conjunction with <b>NON_REM1</b> ) at <b>RESET_N</b> negation to determine if ports [2:1] contain permanently attached (non-removable) devices:<br><br>NON_REM[1:0] = 00: all ports are removable<br>NON_REM[1:0] = 01: port 1 is non-removable<br>NON_REM[1:0] = 10 and 11: ports 1 and 2 are non-removable<br><br>See <a href="#">Section 2.5, "Strap Option Pins"</a> for details. |
| 16                                    | HS_IND     | I/O12       | Hi-Speed Upstream Port Indicator<br><br><b>Note:</b> An LED can be attached for visual indication. See <a href="#">Section 2.5, "Strap Option Pins"</a> for details. When an LED is not used, this pin requires a 50 k $\Omega$ or higher resistor to ground.<br><br>negated = the hub is connected at FS<br>asserted = the hub is connected at HS   |
| 24                                    | XTALIN     | ICLKx       | 24 MHz Crystal Input: this pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.   |
|                                       | CLKIN      |             | External Clock Input: this pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.   |
| 23                                    | XTALOUT    | OCLKx       | 24 MHz Crystal Output: this is the other terminal of the crystal circuit with 1.2 V p-p output and a weak (< 1mA) driving strength. When an external clock source is used to drive <b>XTALIN/CLKIN</b> , leave this pin unconnected, or use with appropriate caution.  |
| 6                                     | TEST       | IPD         | Treat as a no connect pin or connect to ground. No trace or signal should be routed or attached to this pin.   |
| 17                                    | RESET_N    | IS          | RESET Input: the system can reset the chip by driving this input low, where the minimum active low pulse is 1 $\mu$ s.   |
| <b>POWER, GROUND, and NO CONNECTS</b> |            |             |  |
| 9                                     | CRFILT     |             | VDD Core Regulator Filter Capacitor: this pin can have up to 0.1 $\mu$ F low-ESR capacitor to VSS, or be left unconnected.   |
| 4<br>10<br>14<br>20<br>27             | VDD33      |             | 3.3 V Power  |
| 25                                    | PLLFILT    |             | PLL Regulator Filter Capacitor: this pin can have up to 0.1 $\mu$ F low-ESR capacitor to VSS, or be left unconnected.  |
| 15                                    | TEST1      |             | This pin must be connected to VSS.   |

**Table 2.2 USB2412 Pin Descriptions (continued)**

| PIN # | SYMBOL | BUFFER TYPE | DESCRIPTION   |
|-------|--------|-------------|---|
| 29    | ePAD   |             | Ground Pad/ePad: this pin must be connected to VSS for the device and must be tied to ground with multiple vias |
| 5     | NC     |             | No Connect: no signal or trace should be routed or attached to these pins.                                      |

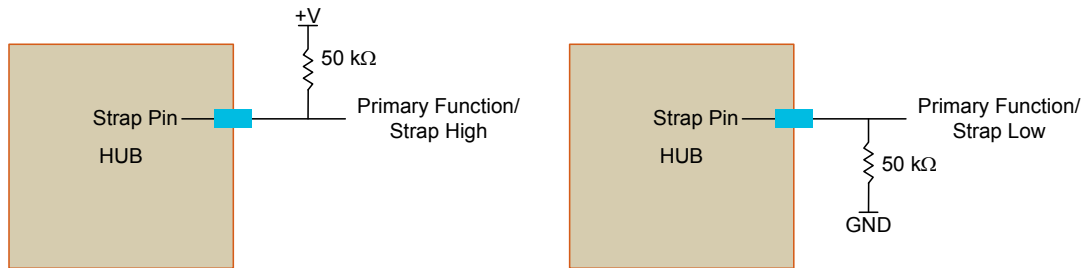
## 2.4 Buffer Type Descriptions

**Table 2.3 Buffer Type Descriptions**

| BUFFER | DESCRIPTION  |
|--------|--|
| I/O    | Input/Output   |
| IPD    | Input with internal weak pull-down resistor          |
| IPU    | Input with internal weak pull-up resistor            |
| IS     | Input with Schmitt trigger                           |
| I/O12  | Input/Output buffer with 12 mA sink and 12 mA source |
| ICLKx  | XTAL clock input                                     |
| OCLKx  | XTAL clock output                                    |
| I-R    | RBIAS  |
| I/O-U  | Analog Input/Output defined in USB specification     |

## 2.5 Strap Option Pins

The NON\_REM[1:0] strap option pins can be enabled using the internal default configuration. The driver type of each strap pin is I/O (no internal pull-up or pull-down for the input function). [Figure 2.2](#) shows an example of Strap High and Strap Low configurations, where Strap High sets the strap option to a 1 and Strap Low sets the strap option value to 0. To use an external LED indicator, the options outlined in [Figure 2.3](#) should be implemented.


**Figure 2.2 Non-Removable Pin Strap Example**

Datasheet

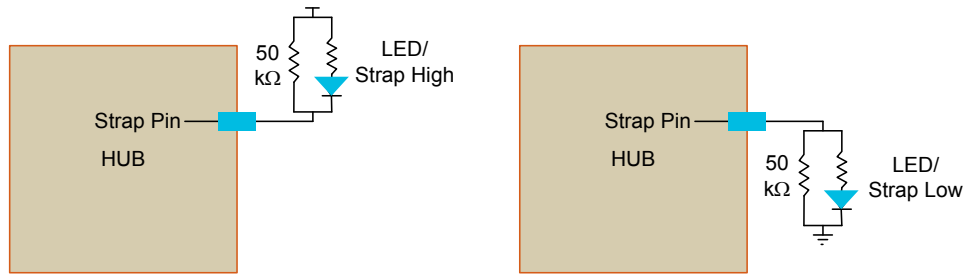


Figure 2.3 LED Pin Strap Example



## Chapter 3 Internal Default Configuration

SMSC's USB 2.0 hub is fully compliant with the *USB Specification*<sup>1</sup>. Refer to Chapter 10 (Hub Specification) for general details regarding hub operation and functionality.

The hub provides one Transaction Translator (TT) that is shared by both downstream ports (defined as Single-TT configuration). The TT contains 4 non-periodic buffers.

### 3.1 Hub Configuration

The USB2412 only supports internal defaults with the exception of the non-removable strap option (using **NON\_REM[1:0]**). The hub internal default settings are as follows:

- Internal Default Configuration without over-rides
- Strap options enabled
- Self-powered operation enabled
- Individual power switching
- Individual over-current sensing

### 3.2 Reset

There are two different resets that the hub experiences. One is a hardware reset via **RESET\_N** and the second is a USB Bus Reset.

#### 3.2.1 External Hardware RESET\_N

A valid hardware reset is defined as assertion of **RESET\_N** for a minimum of 1  $\mu$ s after all power supplies are within operating range. While reset is asserted, the hub (and its associated external circuitry) consumes less than 500  $\mu$ A of current from the upstream USB power source.

Assertion of **RESET\_N** causes the following:

1. All downstream ports are disabled, and **PRT\_PWR** power to downstream devices is removed.
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00h).
5. The external crystal oscillator is halted.
6. The PLL is halted.
7. The hub is "operational" 500  $\mu$ s after **RESET\_N** is negated.

## Datasheet

## 3.2.1.1 RESET\_N

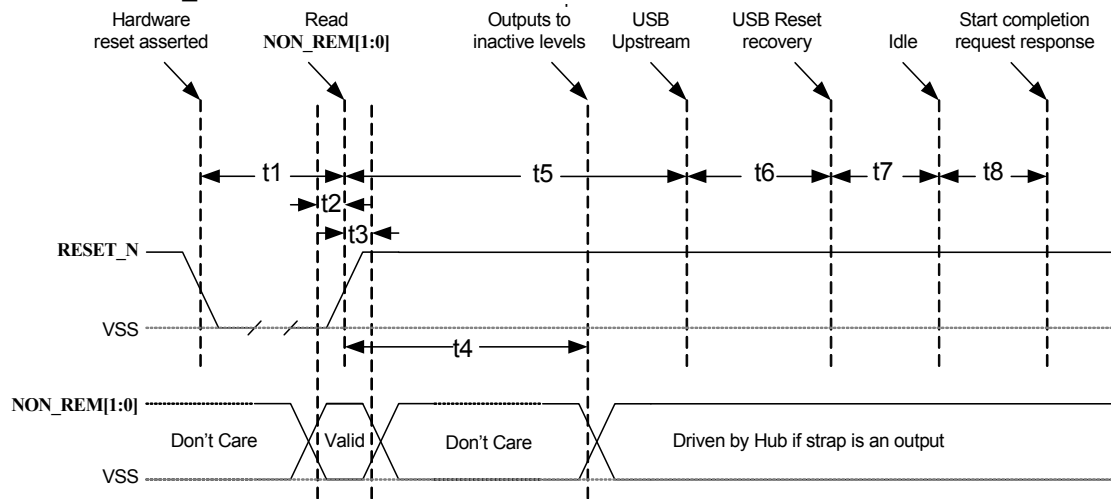


Figure 3.1 Reset\_N Timing

Table 3.1 Reset\_N Timing

| NAME | DESCRIPTION   | MIN  | TYP       | MAX  | UNITS |
|------|---|------|-----------|------|-------|
| t1   | RESET_N asserted  | 1    |           |      | μsec  |
| t2   | Strap setup time  | 16.7 |           |      | nsec  |
| t3   | Strap hold time   | 16.7 |           | 1400 | nsec  |
| t4   | Hub outputs driven to inactive logic states               |      | 1.5       | 2    | μsec  |
| t5   | USB attach (See Note)                                     |      |           | 100  | msec  |
| t6   | Host acknowledges attach and signals USB reset            | 100  |           |      | msec  |
| t7   | USB idle  |      | undefined |      | msec  |
| t8   | Completion time for requests (with or without data stage) |      |           | 5    | msec  |

**Note:** All power supplies must have reached the operating levels mandated in [Chapter 4, DC Parameters](#), prior to (or coincident with) the assertion of RESET\_N.

## 3.2.2 USB Bus Reset

In response to the upstream port signaling a reset to the hub, the hub does the following:

1. Sets default address to 0.
2. Sets configuration to unconfigured.
3. Negates **PRT\_PWR[2:1]** to all downstream ports.
4. Clears all TT buffers.
5. Moves device from suspended to active (if suspended).
6. Complies with Section 11.10 of the *USB 2.0 Specification* for behavior after completion of the reset sequence. The host then configures the hub and the hub's downstream port devices in accordance with the specification.

**Note:** The hub does not propagate the upstream USB reset to downstream devices.

## Chapter 4 DC Parameters

### 4.1 Maximum Guaranteed Ratings

| PARAMETER              | SYMBOL                   | MIN  | MAX | UNITS |
|------------------------|--------------------------|------|-----|-------|
| Storage Temperature    | $T_{\text{STOR}}$        | -55  | 150 | °C    |
| Lead Temperature       |                          |      |     | °C    |
| 3.3 V supply voltage   | VDD33<br>PLLFLT<br>CRFLT |      | 4.6 | V     |
| Voltage on any I/O pin |                          | -0.5 | 5.5 | V     |
| Voltage on XTALIN      |                          | -0.5 | 4.0 | V     |
| Voltage on XTALOUT     |                          | -0.5 | 2.5 | V     |

**Note 4.1** Refer to JEDEC Specification J-STD-020D 5..

**Note 4.2** Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

**Note 4.3** When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

### 4.2 Operating Conditions

| PARAMETER              | SYMBOL          | MIN  | MAX   | UNITS | COMMENTS   |
|------------------------|-----------------|------|-------|-------|--|
| Operating Temperature  | $T_A$           | 0    | 70    | °C    | Ambient temperature in still air.  |
| 3.3 V supply voltage   | VDD33           | 3.0  | 3.6   | V     |  |
| 3.3 V supply rise time | $t_{\text{RT}}$ | 0    | 400   | μs    | See <a href="#">Figure 4.1</a>   |
| Voltage on any I/O pin |                 | -0.3 | 5.5   | V     | If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes:<br>(3.3 V supply voltage) + 0.5 |
| Voltage on XTALIN      |                 | -0.3 | VDD33 | V     |  |

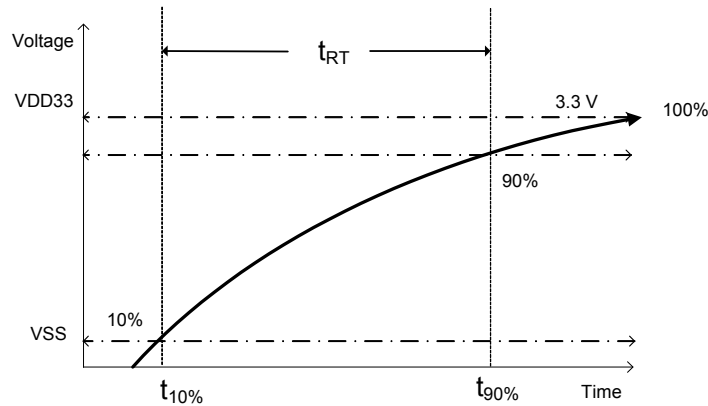


Figure 4.1 Supply Rise Time Model

Table 4.1 DC Electrical Characteristics

| PARAMETER                                | SYMBOL     | MIN | TYP | MAX | UNITS   | COMMENTS              |
|--|------------|-----|-----|-----|---------|-----------------------|
| <b>I, IS Type Input Buffer</b>           |            |     |     |     |         |                       |
| Low Input Level                          | $V_{ILI}$  |     |     | 0.8 | V       | TTL Levels            |
| High Input Level                         | $V_{IHI}$  | 2.0 |     |     | V       |                       |
| Input Leakage                            | $I_{IL}$   | -10 |     | +10 | $\mu A$ | $V_{IN} = 0$ to VDD33 |
| Hysteresis ('IS' Only)                   | $V_{HYSI}$ | 250 |     | 350 | mV      |                       |
| <b>Input Buffer with Pull-Up (IPU)</b>   |            |     |     |     |         |                       |
| Low Input Level                          | $V_{ILI}$  |     |     | 0.8 | V       | TTL Levels            |
| High Input Level                         | $V_{IHI}$  | 2.0 |     |     | V       |                       |
| Low Input Leakage                        | $I_{ILL}$  | +35 |     | +90 | $\mu A$ | $V_{IN} = 0$          |
| High Input Leakage                       | $I_{IHL}$  | -10 |     | +10 | $\mu A$ | $V_{IN} = VDD33$      |
| <b>Input Buffer with Pull-Down (IPD)</b> |            |     |     |     |         |                       |
| Low Input Level                          | $V_{ILI}$  |     |     | 0.8 | V       | TTL Levels            |
| High Input Level                         | $V_{IHI}$  | 2.0 |     |     | V       |                       |
| Low Input Leakage                        | $I_{ILL}$  | +10 |     | -10 | $\mu A$ | $V_{IN} = 0$          |
| High Input Leakage                       | $I_{IHL}$  | -35 |     | -90 | $\mu A$ | $V_{IN} = VDD33$      |
| <b>ICLK Input Buffer</b>                 |            |     |     |     |         |                       |
| Low Input Level                          | $V_{ILCK}$ |     |     | 0.5 | V       |                       |
| High Input Level                         | $V_{IHCK}$ | 1.4 |     |     | V       |                       |
| Input Leakage                            | $I_{IL}$   | -10 |     | +10 | $\mu A$ | $V_{IN} = 0$ to VDD33 |

**Table 4.1 DC Electrical Characteristics (continued)**

| PARAMETER   | SYMBOL        | MIN | TYP                       | MAX                       | UNITS         | COMMENTS   |
|---|---------------|-----|---------------------------|---------------------------|---------------|--|
| <b>O12, I/O12 &amp;I/OSD12 Type Buffer</b>  |               |     |                           |                           |               |  |
| Low Output Level  | $V_{OL}$      |     |                           | 0.4                       | V             | $I_{OL} = 12 \text{ mA @ } V_{DD33} = 3.3 \text{ V}$<br>$I_{OH} = -12 \text{ mA @ } V_{DD33} = 3.3 \text{ V}$<br>$V_{IN} = 0 \text{ to } V_{DD33}$<br>(Note 4.1) |
| High Output Level   | $V_{OH}$      | 2.4 |                           |                           | V             |  |
| Output Leakage  | $I_{OL}$      | -10 |                           | +10                       | $\mu\text{A}$ |  |
| Hysteresis ('SD' pad only)  | $V_{HYSC}$    | 250 |                           | 350                       | mV            |  |
|   |               |     |                           |                           |               |  |
| <b>Supply Current Unconfigured Hi-Speed Host</b>                                  | $I_{CCINTHS}$ |     | 40                        | 45                        | mA            |  |
| <b>Supply Current Unconfigured Full-Speed Host</b>                                | $I_{CCINTFS}$ |     | 35                        | 40                        | mA            |  |
| <b>Supply Current Configured Hi-Speed Host, 1 downstream port</b>                 | $I_{HCH1}$    |     | 60                        | 65                        | mA            |  |
| <b>Supply Current Configured Hi-Speed Host, each additional downstream port</b>   |               |     | 1 port base<br>+<br>25 mA | 1 port base<br>+<br>25 mA | mA            |  |
| <b>Supply Current Configured Full-Speed Host, 1 downstream port</b>               | $I_{FCC1}$    |     | 45                        | 50                        | mA            | There is no additional current for additional ports.   |
| <b>Supply Current Configured Full-Speed Host, each additional downstream port</b> |               |     | 1 port base<br>+<br>8 mA  | 1 port base<br>+<br>8 mA  | mA            |  |
| <b>Supply Current Suspend</b>   | $I_{CSBY}$    |     | 475                       | 1000                      | $\mu\text{A}$ | All supplies combined  |
| <b>Supply Current Reset</b>   | $I_{CRST}$    |     | 550                       | 1100                      | $\mu\text{A}$ | All supplies combined  |

**Note 4.4** Output leakage is measured with the current pins in high impedance.

**Note 4.5** See *USB 2.0 Specification 1*. for USB DC electrical characteristics.

## 4.2.1 Pin Capacitance

Table 4.2 Pin Capacitance

| PARAMETER               | SYMBOL     | LIMITS |     |     | UNIT | TEST CONDITION   |
|-------------------------|------------|--------|-----|-----|------|--|
|                         |            | MIN    | TYP | MAX |      |  |
| Clock Input Capacitance | $C_{XTAL}$ |        |     | 6   | pF   | All pins except USB pins and the pins under the test tied to AC ground.  |
| Input Capacitance       | $C_{IN}$   |        |     | 6   | pF   | Capacitance $T_A = 25^\circ\text{C}$<br>$f_c = 1\text{ MHz}$<br>$V_{DD33} = 3.3\text{ V}$                                  |
| Output Capacitance      | $C_{OUT}$  |        |     | 6   | pF   | The maximum capacitance values include the full length of the pin pad. See the Y dimension in <a href="#">Figure 6.2</a> . |

## 4.2.2 Package Thermal Specifications

Thermal parameters are measured or estimated for devices with the exposed pad soldered to thermal vias in a multilayer 2S2P PCB per JESD51. Thermal resistance is measured from the die to the ambient air.

Table 4.3 28-Pin QFN Package Thermal Parameters

| PARAMETER                  | VELOCITY (meters/sec) | SYMBOL        | VALUE | UNIT               |
|----------------------------|-----------------------|---------------|-------|--------------------|
| Thermal Resistance         | 0                     | $\Theta_{JA}$ | 40.3  | $^\circ\text{C/W}$ |
|                            | 1                     |               | 35.2  |                    |
| Junction-to-Top-of-Package | 0                     | $\Psi_{JT}$   | 0.5   | $^\circ\text{C/W}$ |
|                            | 1                     |               | 0.6   |                    |



## Chapter 5 AC Specifications

### 5.1 Oscillator/Crystal

Parallel Resonant, Fundamental Mode, 24 MHz ± 350 ppm.

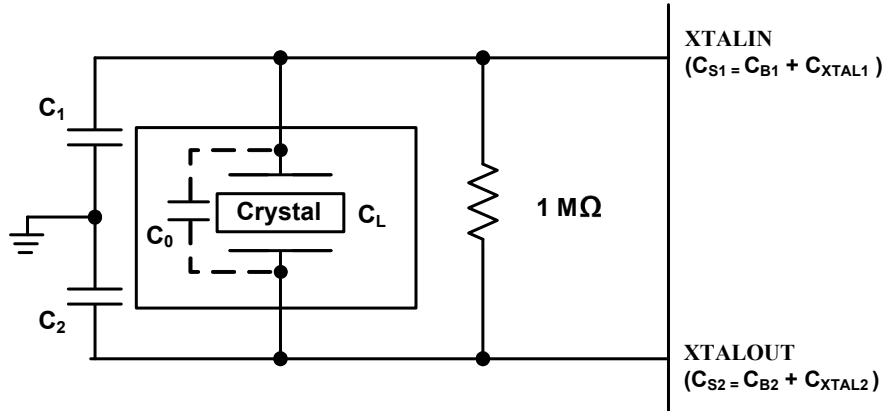


Figure 5.1 Typical Crystal Circuit

Table 5.1 Crystal Circuit Legend

| SYMBOL     | DESCRIPTION                            | IN ACCORDANCE WITH   |
|------------|--|--|
| $C_0$      | Crystal shunt capacitance              | Crystal manufacturer's specification (See <a href="#">Note 5.1</a> )   |
| $C_L$      | Crystal load capacitance               |  |
| $C_B$      | Total board or trace capacitance       | OEM board design   |
| $C_S$      | Stray capacitance                      | SMSC IC and OEM board design   |
| $C_{XTAL}$ | XTAL pin input capacitance             | SMSC IC  |
| $C_1$      | Load capacitors installed on OEM board | Calculated values based on <a href="#">Figure 5.2</a> , "Formula to Find the Value of C1 and C2" (See <a href="#">Note 5.2</a> ) |
| $C_2$      |  |  |

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

Figure 5.2 Formula to Find the Value of  $C_1$  and  $C_2$

**Note 5.1**  $C_0$  is usually included (subtracted by the crystal manufacturer) in the specification for  $C_L$  and should be set to 0 for use in the calculation of the capacitance formulas in [Figure 5.2](#), "Formula to Find the Value of C1 and C2". However, the PCB itself may present a parasitic capacitance between **XTALIN** and **XTALOUT**. For an accurate calculation of  $C_1$  and  $C_2$ , take the parasitic capacitance between traces **XTALIN** and **XTALOUT** into account.

**Note 5.2** Each of these capacitance values is typically approximately 18 pF.

## 5.2 External Clock

50% Duty cycle  $\pm$  10%, 24 MHz  $\pm$  350 ppm, Jitter < 100 ps rms.

The external clock is recommended to conform to the signaling level designated in the JESD76-2 specification on 1.2 V CMOS Logic. **XTALOUT** should be treated as a no connect.

### 5.2.1 USB 2.0

The SMSC hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the *USB 2.0 Specification 1*. See the *USB Specification* for more information.

## Chapter 6 Package Outline

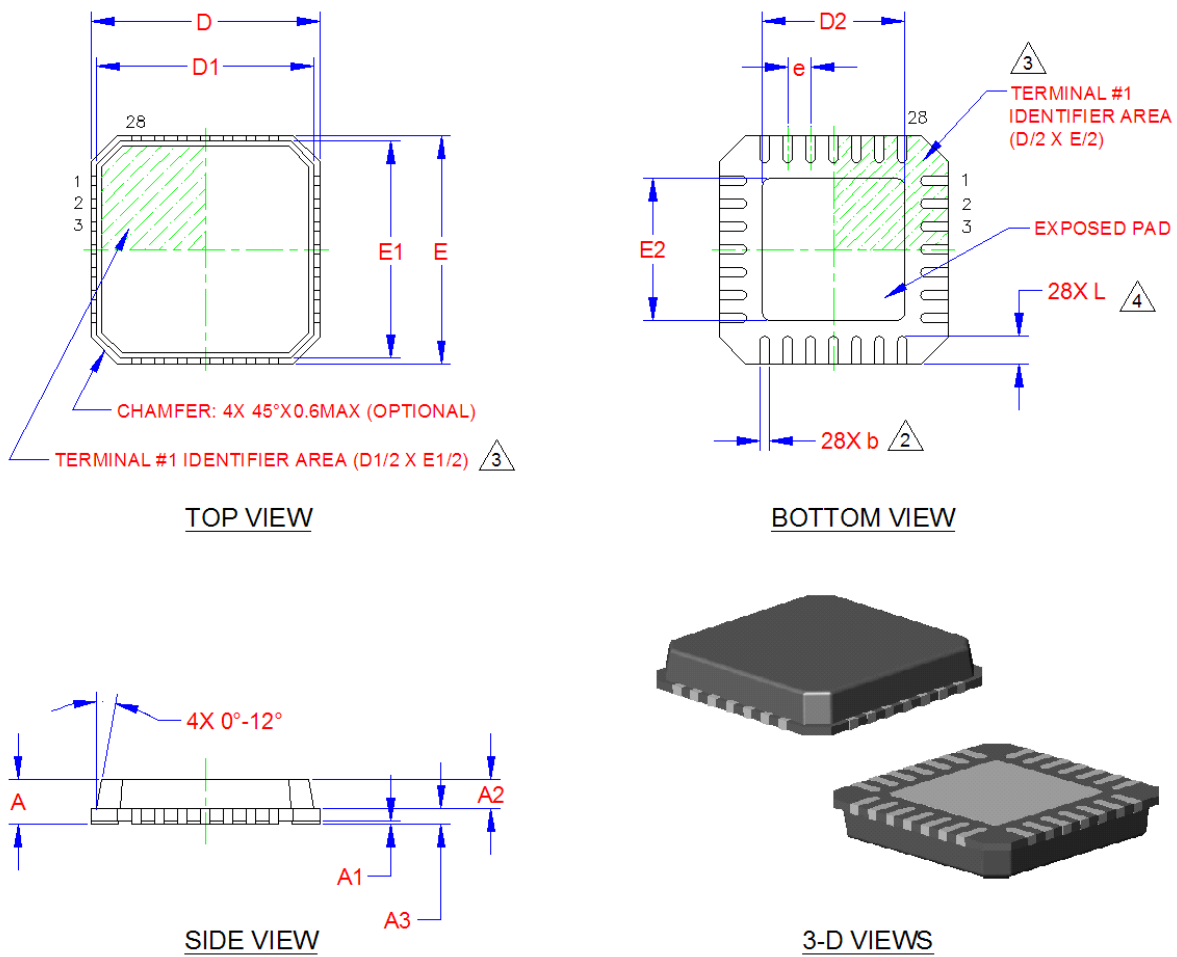


Figure 6.1 USB2412 28-Pin QFN Package Outline (5x5 mm Body, 0.5 Pitch, 3.1 ePad)

Table 6.1 Package Parameters

|       | MIN      | NOMINAL | MAX  | NOTE | REMARKS                    |
|-------|----------|---------|------|------|----------------------------|
| A     | 0.80     | 0.85    | 1.00 | -    | Overall Package Height     |
| A1    | 0        | 0.02    | 0.05 | -    | Standoff                   |
| A2    | 0.60     | -       | 0.80 | -    | Mold Cap Thickness         |
| D/E   | 4.90     | 5.00    | 5.10 | -    | X/Y Overall Body Size      |
| D1/E1 | 4.55     | 4.75    | 4.95 | -    | X/Y Mold Cap Size          |
| D2/E2 | 3.00     | 3.10    | 3.20 | -    | X/Y Exposed Pad Size       |
| L     | 0.30     | 0.40    | 0.50 | -    | Terminal Length            |
| b     | 0.18     | 0.25    | 0.30 | 2    | Terminal Width             |
| K     | 0.45     | 0.55    | -    | -    | Terminal to ePad Clearance |
| e     | 0.50 BSC |         |      | -    | Terminal Pitch             |

**Notes:**

- All dimensions are in millimeters.
- Position tolerance of each terminal and exposed pad is  $\pm 0.05$  mm at maximum material condition. Instances of dimension "b" apply to plated terminals and is measured between 0.15 and 0.33 mm from the terminal tip.
- Details of terminal #1 identifier are optional. However, they must be located within the area indicated.
- Coplanarity zone applies to exposed pad and terminals.

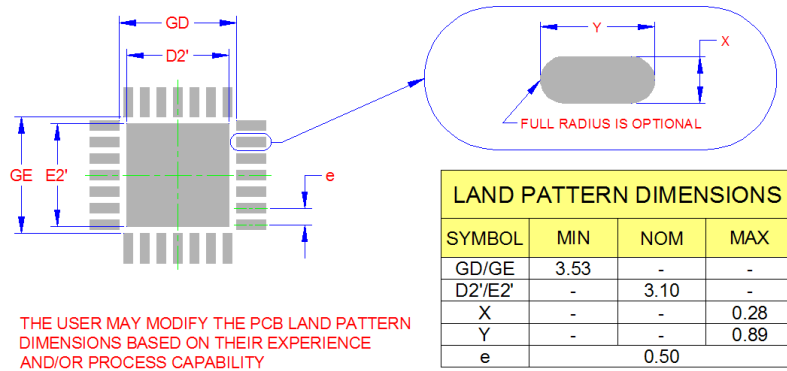


Figure 6.2 Recommended Printed Circuit Board (PCB) Land Pattern

## 6.1 Tape and Reel Specification

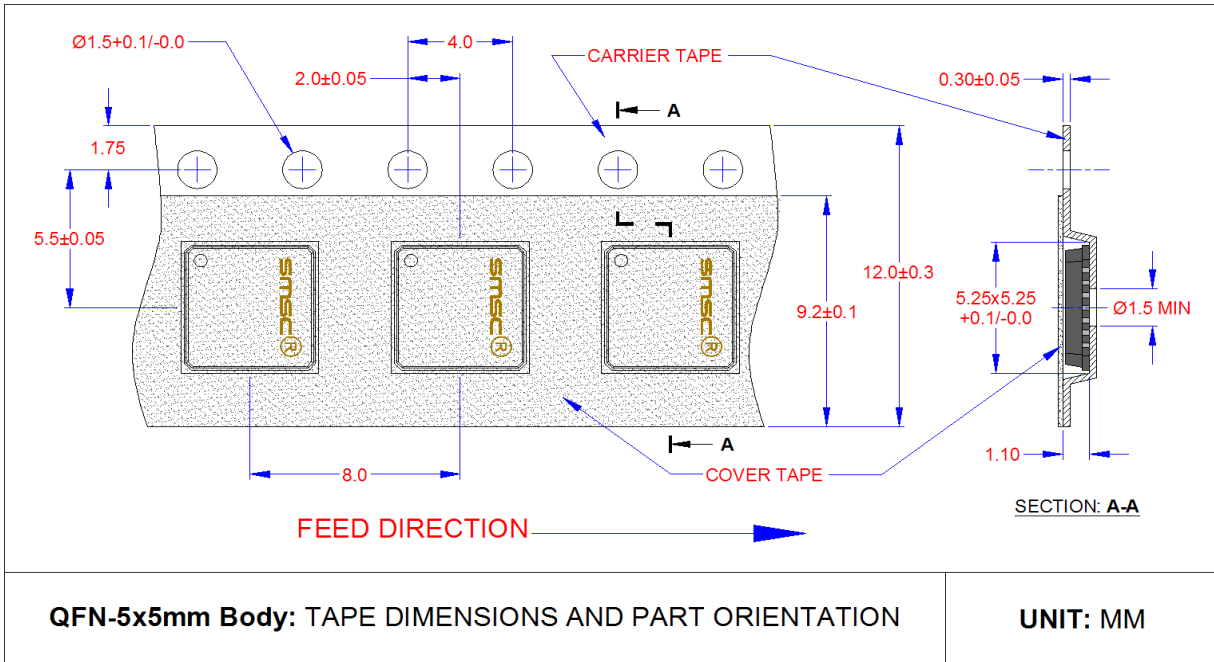


Figure 6.3 28-Pin Package Tape Dimensions and Part Orientation (mm)

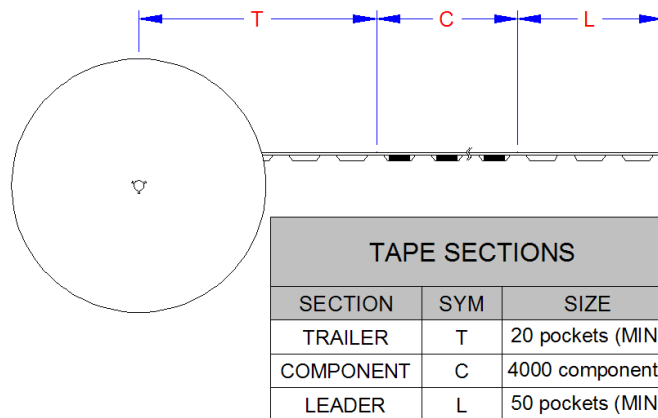
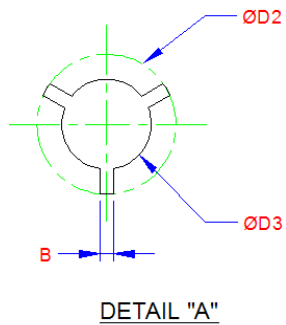
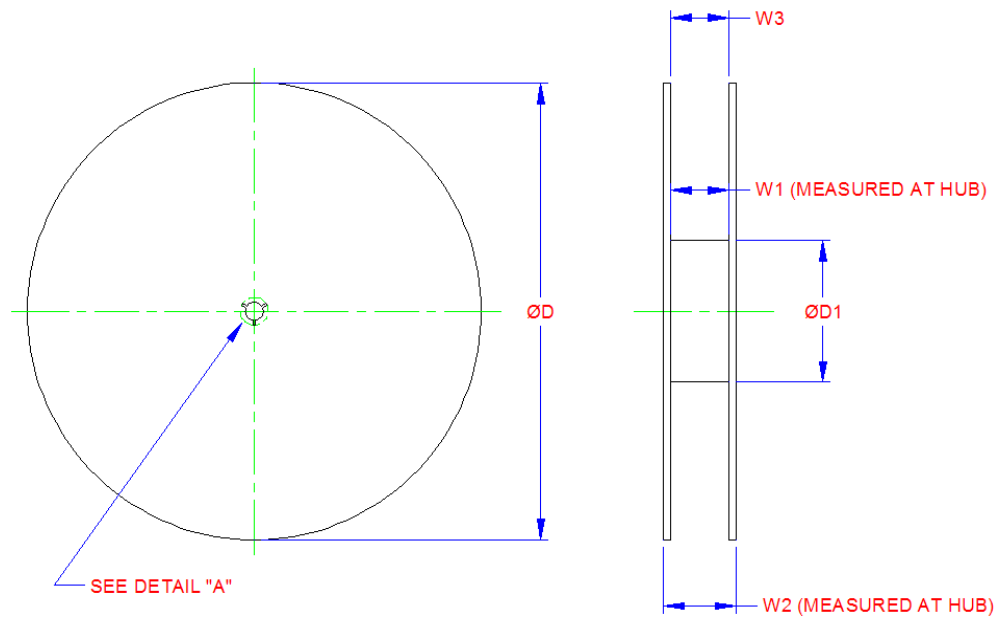


Figure 6.4 28-Pin Package Tape Length and Part Quantity



| REEL DIMs for 12mm CARRIER TAPE |                               |     |                   |
|---------------------------------|-------------------------------|-----|-------------------|
| PART                            | FEATURE                       | SYM | SIZE (mm)         |
| FLANGE                          | DIAMETER                      | D   | 330 (+0.25/-4.00) |
|                                 | SPACE between FLANGES         | W1  | 12.4 (+2.0/-0.0)  |
|                                 | OVERALL WITH                  | W2  | 18.4 (MAX)        |
|                                 | MIN SPACE "W1" AT FLANGE EDGE | W3  | 12.3 (MIN)        |
| HUB                             | OUTER DIAMETER                | D1  | 102 REF           |
|                                 | KEY SLIT DIAMETER             | D2  | 20.2 (MIN)        |
|                                 | ARBOR HOLE DIAMETER           | D3  | 13.0 (+0.5/-0.2)  |
|                                 | KEY SLIT WIDTH                | B   | 2.0 (±0.5)        |

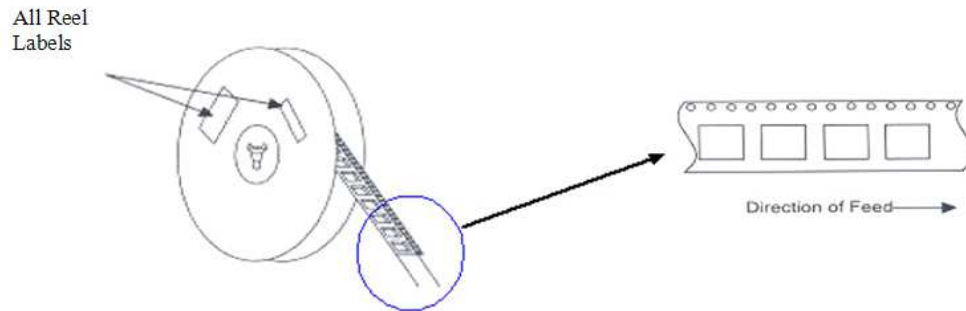


Figure 6.5 Package Reel Specifications