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2-Port USB 2.0 Hi-Speed Hub Controller

General Description

The Microchip USB2422 hub is a low-power, single transaction translator, hub controller IC with two downstream ports for embedded USB solutions. The hub controller can attach to an upstream port as a Hi-Speed and Full-Speed hub or as a Full-Speed only hub. The hub supports Low-Speed, Full-Speed, and Hi-Speed (when configured as a Hi-Speed hub) downstream devices on the enabled downstream ports.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D- pins and all required pull-down and pull-up resistors on D+ and D- pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

Features

- Supports the *USB Battery Charging Specification, Revision 1.1*
- Fully integrated USB termination and pull-up/pull-down resistors
- Supports a single external 3.3 V supply source; internal regulators provide 1.2 V internal core voltage
- On-chip driver for 24 MHz crystal resonator or external 24 MHz clock input
- ESD protection up to 6 kV on all USB pins
- Supports self-powered operation
- The hub contains a built-in default configuration; no external configuration options or components are required
- Downstream ports as non-removable ports
- Downstream port power control and over-current detection on an individual or ganged basis
- Supports compound devices on a port-by-port basis
- 24-pin SQFN (4x4 mm), RoHS-compliant package
- Commercial temperature range support: 0°C to +70°C
- Industrial temperature range support: -40°C to +85°C

Highlights

- High performance, low-power, small footprint hub controller IC with two downstream ports
- Fully compliant with the *USB 2.0 Specification*
- Optimized for minimal bill-of-materials and low-cost designs

Applications

- LCD monitors and TVs
- Multi-function USB peripherals
- PC motherboards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems
- Gaming consoles
- Cable/DSL modems
- HDD enclosures
- KVM switches
- Server front panels
- Point-of-Sale (POS) systems
- IP telephony
- Automobile/home audio systems
- Thin client terminals

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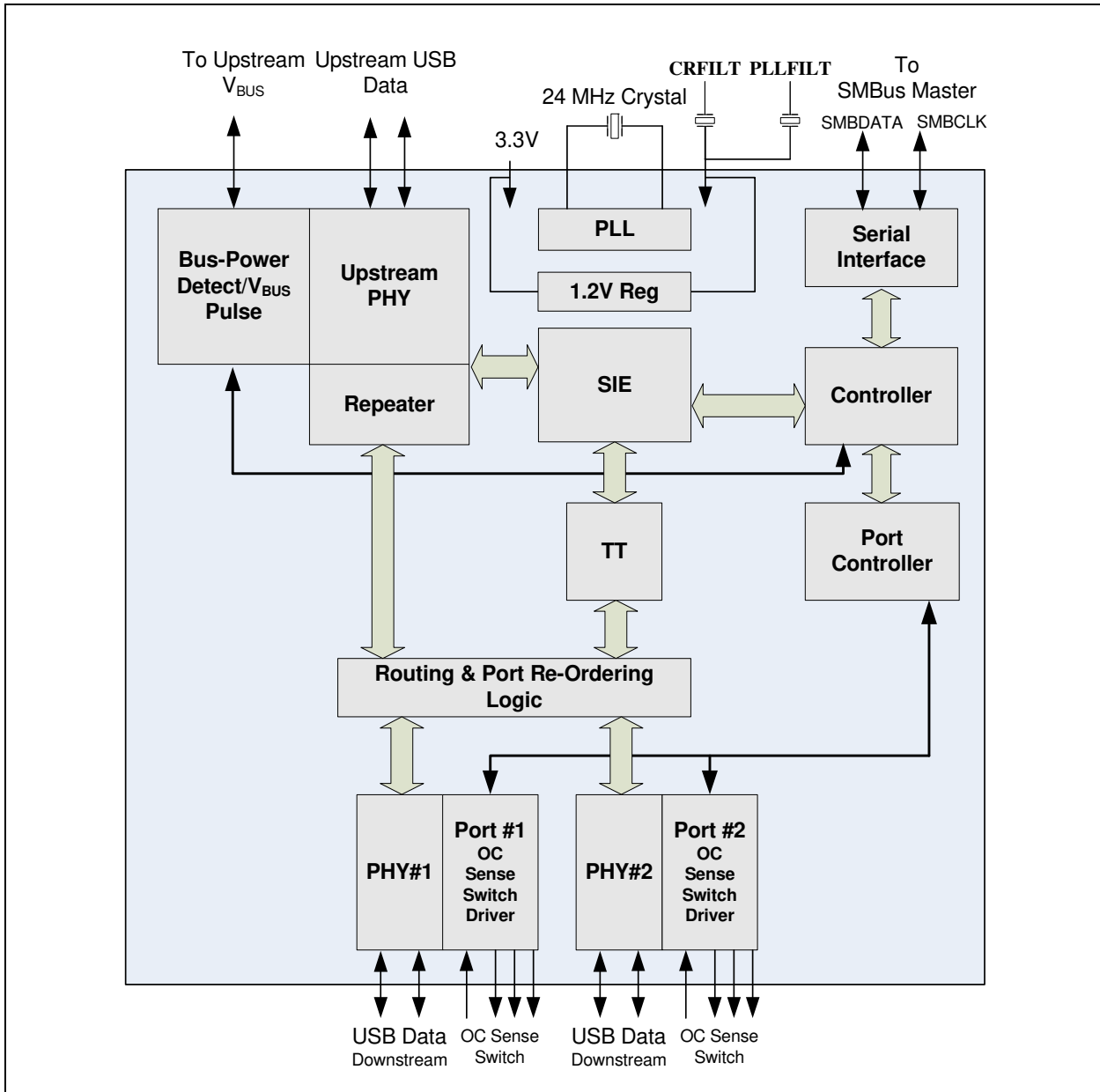
Table of Contents

1.0 Block Diagram	4
2.0 Pin Descriptions	6
3.0 Battery Charging Support	14
4.0 Configuration Options	16
5.0 DC Parameters	35
6.0 AC Specifications	38
7.0 Package Outline	40
Appendix A: Acronyms	41
Appendix B: References	42
Appendix C: Data Sheet Revision History	43
The Microchip Web Site	44
Customer Change Notification Service	44
Customer Support	44
Product Identification System	45

USB2422

1.0 BLOCK DIAGRAM

FIGURE 1-1: USB2422 BLOCK DIAGRAM



Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x...y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
code	Instruction code, or API function or parameter
<i>Multi Word Name</i>	Used for multiple words that are considered a single unit, such as: <i>Resource Allocate</i> message, or <i>Connection Label</i> , or <i>Decrement Stack Pointer</i> instruction.
<i>Section Name</i>	Section or Document name.
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times.
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

USB2422

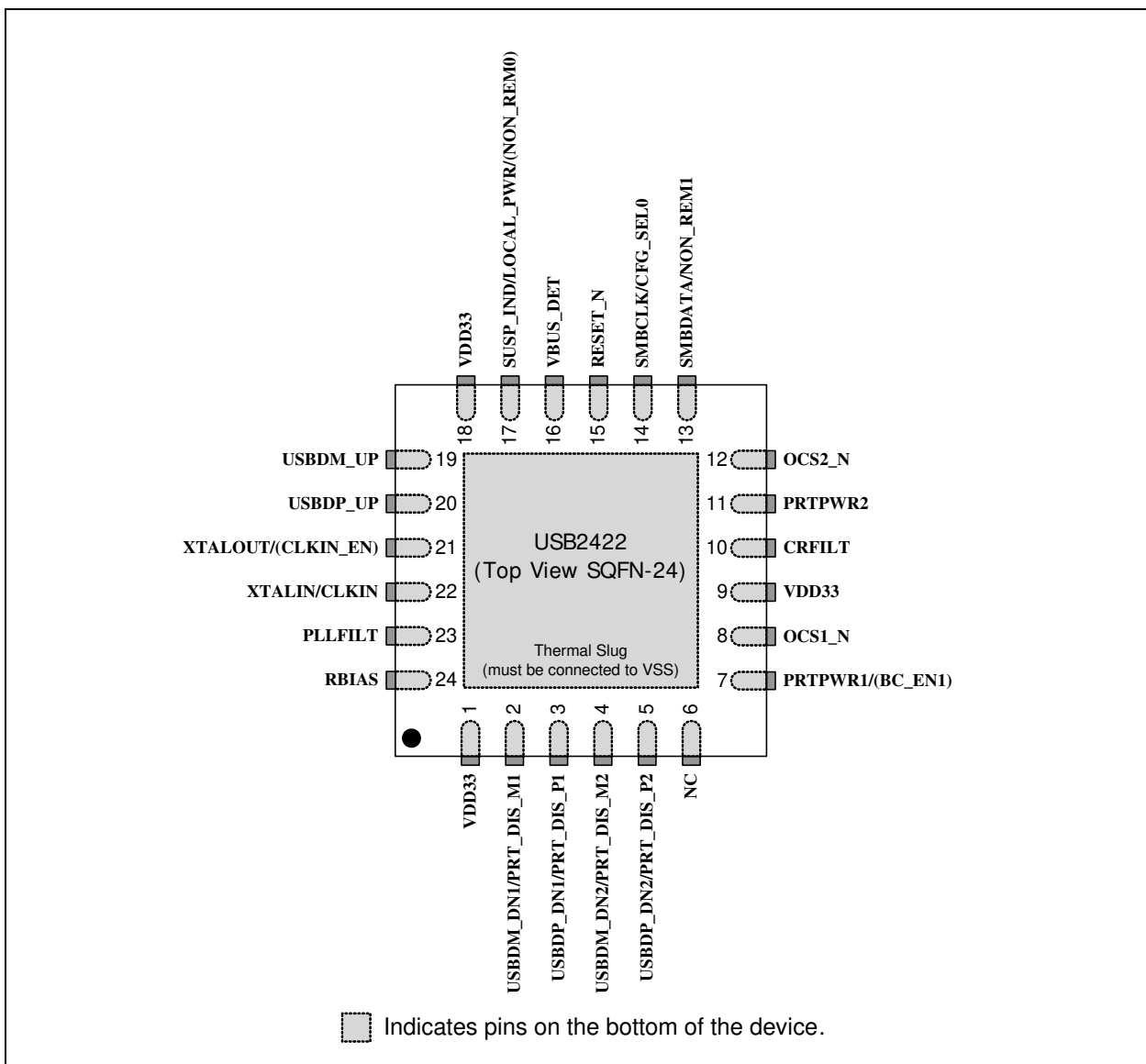
2.0 PIN DESCRIPTIONS

This chapter is organized by a set of pin configurations followed by a corresponding pin list organized by function according to their associated interface. A detailed description list of each signal (named in the pin list) is organized by function in [Table 2-2, “USB2422 Pin Descriptions,”](#) on page 7. Refer to [Table 2-3, “Buffer Type Descriptions,”](#) on page 10 for a list of buffer types.

An *N* at the end of a signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *N* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

2.1 Pin Configuration

FIGURE 2-1: USB2422 24-Pin SQFN



2.2 Pin Table

TABLE 2-1: USB2422 PIN TABLE

UPSTREAM USB 2.0 INTERFACES (3 PINS)			
USBDM_UP	usbDM_UP	VBUS_DET	
DOWNSTREAM 2-PORT USB 2.0 INTERFACES (9 PINS)			
USBDP_DN1/ PRT_DIS_P1	USBDM_DN1/ PRT_DIS_M1	USBDP_DN2/ PRT_DIS_P2	USBDM_DN2/ PRT_DIS_M2
P RTPWR1/ BC_EN1	P RTPWR2	OCS1_N	OCS2_N
RBIAS			
SERIAL PORT INTERFACE (2 PINS)			
SMBDATA/ NON_REM1	SMBCLK/ CFG_SEL		
MISC (5 PINS)			
XTALIN/ CLKIN	XTALOUT/ CLKIN_EN	RESET_N	SUSP_IND/ LOCAL_PWR/ NON_REM0
NC			
POWER, GROUND, AND NO CONNECTS (5 PINS)			
(3) VDD33	CRFILT	PLLFILT	VSS
TOTAL 24			

2.3 Pin Descriptions (Grouped by Function)

TABLE 2-2: USB2422 PIN DESCRIPTIONS

Pin #	Symbol	Buffer Type	Description
UPSTREAM USB 2.0 INTERFACES			
19 20	USBDM_UP USBDP_UP	IO-U	USB Bus Data: Connect to the upstream USB bus data signals (host, port, or upstream hub).
16	VBUS_DET	I	Detect Upstream VBUS Power: Detects the state of upstream VBUS power. The hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor (signalling a connect event) When designing a detachable hub, this pin should be connected to VBUS on the upstream port via a 2:1 voltage divider. Two 100 kΩ resistors are suggested. For self-powered applications with a permanently attached host, this pin must be connected to a dedicated host control output, or connected to the 3.3 V domain that powers the host (typically VDD33).

USB2422

TABLE 2-2: USB2422 PIN DESCRIPTIONS (CONTINUED)

Pin #	Symbol	Buffer Type	Description
DOWNSTREAM USB 2.0 INTERFACES			
5 3 and 4 2	USBDP_DN[2:1]/ PRT_DIS_P[2:1] and USBDN_DN[2:1]/ PRT_DIS_M[2:1]	IO-U	<p>Hi-Speed USB Data:</p> <p>Connect to the downstream USB peripheral devices attached to the hub's ports.</p> <p>Port Disable Strap Option:</p> <p>If this strap is enabled by package and configuration settings (see Table 4-1, "Hub Configuration Options"), this pin will be sampled at RESET_N negation to determine if the port is disabled.</p> <p>Both USB data pins for the corresponding port must be tied to VDD33 to disable the associated downstream port.</p>
7	PRT_PWR1/ BC_EN1	O12 IPD	<p>USB Power Enable:</p> <p>Enables power to USB peripheral devices that are downstream, where the hub supports active high power controllers only.</p> <p>Battery Charging Strap Option:</p> <p>Port 1 pin will be sampled at RESET_N negation to determine if port 1 supports the battery charging protocol (and thus the supporting external port power controllers) that would enable a device to draw the currents per the <i>USB Battery Charging Specification</i>.</p> <p>This pin has an internal pull-down that will be removed after the strap option hold time is completed.</p> <p>BC_EN1= 1: Battery charging feature is supported for port 1 BC_EN1= 0: Battery charging feature is not supported for port 1</p>
11	PRT_PWR2	O12	<p>USB Power Enable:</p> <p>Enables power to USB peripheral devices that are downstream, where the hub supports active high power controllers only.</p>
8 12	OCS1_N OCS2_N	IPU	<p>Over-Current Sense:</p> <p>Input from external current monitor indicating an over-current condition. This pin contains an internal pull-up to the 3.3 V supply.</p>
24	RBIAS	I-R	<p>USB Transceiver Bias:</p> <p>A12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.</p>
SERIAL PORT INTERFACE			
13	SMBDATA NON_REM1	I/OSD12	<p>System Management Bus Data</p> <p>Non-removable Port Strap Option:</p> <p>This pin is sampled (in conjunction with SUSP_IND/NON_REM0) at RESET_N negation to determine if ports [2:1] contain permanently attached (non-removable) devices:</p> <p>NON_REM[1:0] = 00: all ports are removable NON_REM[1:0] = 01: port 1 is non-removable NON_REM[1:0] = 10: ports 1 and 2 are non-removable NON_REM[1:0] = 11: reserved</p> <p>See Section 2.5, "Strap Pin Configuration" for details.</p>
14	SMBCLK/ CFG_SEL	I/OSD12	<p>System Management Bus Clock</p> <p>Configuration Select:</p> <p>The logic state of this multifunction pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 4-1.</p>

TABLE 2-2: USB2422 PIN DESCRIPTIONS (CONTINUED)

Pin #	Symbol	Buffer Type	Description
MISC			
22	XTALIN/ CLKIN	ICLKx	24 MHz Crystal or External Clock Input: This pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.
21	XTALOUT	OCLKx	Crystal Output: This is the other terminal of the crystal circuit with 1.2 V p-p output and a weak (< 1 mA) driving strength. When an external clock source is used to drive XTALIN/CLKIN, leave this pin unconnected, or use with appropriate caution.
15	RESET_N	IS	RESET Input: The system must reset the chip by driving this input low. The minimum active low pulse is 1 μ s.
6	NC	IPD	Treat as a no connect pin or connect to ground. No trace or signal should be routed or attached to this pin.
17	SUSP_IND	I/O12	Suspend Indicator: Indicates the USB state of the hub. negated : unconfigured, or configured and in USB Suspend asserted : Hub is configured, and is active (i.e., not in suspend)
	LOCAL_PWR		Local Power: This input selects whether the hub reports itself as bus or self-powered when dynamic power switching is enabled via the Dynamic Power Enable (DYNAMIC) bit of the Configuration Data Byte 2 Register (CFG2) . This pin is sampled at POR/Reset before the USB Hub Attach command is sent. Once the hub has entered the attach state (as indicated by the USB Attach and Write Protect (USB_ATTACH) bit of the Status/Command Register (STCD)), this pin cannot be changed. Low : self/local power source is not available (i.e., the Hub gets all power from the upstream USB VBus). High : self/local power source is available. Note: Never tie this pin directly to VDD33, as doing so may cause it to act as SUSP_IND. Note: This pin assumes the meaning of local power input only if properly configured via SMBus. If the hub is configured via straps, it is NON_REM0 at reset and SUSP_IND after reset.
	(NON_REM0)		Non-Removable Port Strap Option: This pin is sampled (in conjunction with SUSP_IND/NON_REM0) at RESET_N negation to determine if ports [2:1] contain permanently attached (non-removable) devices: NON_REM[1:0] = 00: all ports are removable NON_REM[1:0] = 01: port 1 is non-removable NON_REM[1:0] = 10: ports 1 and 2 are non-removable NON_REM[1:0] = 11: reserved See Section 2.5, "Strap Pin Configuration" for details.

USB2422

TABLE 2-2: USB2422 PIN DESCRIPTIONS (CONTINUED)

Pin #	Symbol	Buffer Type	Description
POWER, GROUND, and NO CONNECTS			
1 9 18	VDD33		3.3 V power to the chip. A 1.0 μ F low-ESR capacitor to VSS is required on pin 9 as close as possible to the pin. A 0.1 μ F low-ESR capacitor to VSS is required on pin 1 as close as possible to the pin.
10	CRFILT		VDD Core Regulator Filter Capacitor: This pin requires a 1.0 μ F low-ESR capacitor to VSS for proper operation.
23	PLLFILT		PLL Regulator Filter Capacitor: This pin can have up to a 0.1 μ F low-ESR capacitor to VSS, or be left unconnected.
	VSS		Ground Pad/ePad: The package slug is the only VSS for the device and must be tied to ground with multiple vias.

2.4 Buffer Type Descriptions

TABLE 2-3: BUFFER TYPE DESCRIPTIONS

Buffer	Description
I/O	Input/Output
IPD	Input with internal weak pull-down resistor
IPU	Input with internal weak pull-up resistor
IS	Input with Schmitt trigger
I/O12	Input/Output buffer with 12 mA sink and 12 mA source
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I-R	RBIAS
I/O-U	Analog Input/Output defined in USB specification

2.5 Strap Pin Configuration

If a pin's strap function is enabled through hub configuration selection ([Table 4-1](#)), the strap pins must be pulled either high or low using the values provided in [Table 2-4](#). Each strap option is dependent on the pin's buffer type, as outlined in the sections that follow.

TABLE 2-4: STRAP OPTION SUMMARY

Strap Option	Resistor Value	Buffer Type	Notes
Non-Removable	47 - 100 k Ω	I/O	
Internal Pull-Down (IPD)	10 k Ω	IPD	<ul style="list-style-type: none"> • Only applicable to port power pins • Contains a built-in resistor
LED	47 - 100 k Ω	I/O	

2.5.1 NON-REMOVABLE

If a strap pin's buffer type is I/O, an external pull-up or pull-down must be implemented as shown in [Figure 2-2](#). Use Strap High to set the strap option to 1 and Strap Low to set the strap option to 0. When implementing the Strap Low option, no additional components are needed (i.e., the internal pull-down provides the resistor).

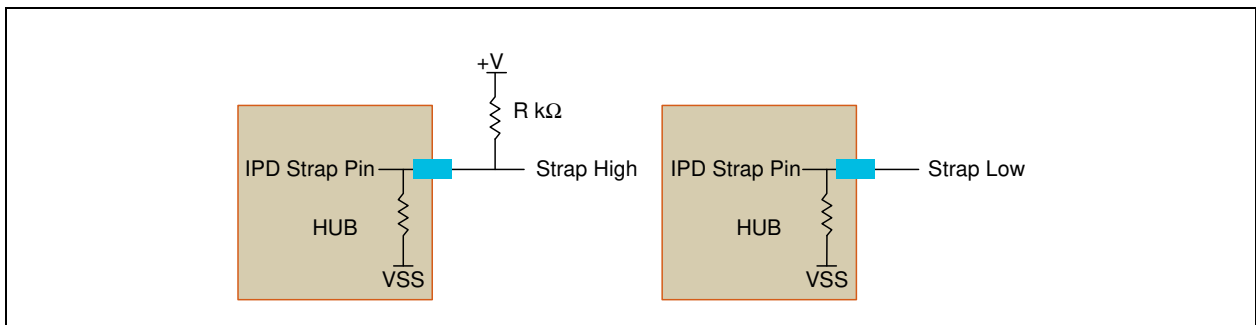
FIGURE 2-2: NON-REMOVABLE PIN STRAP EXAMPLE



2.5.2 INTERNAL PULL-DOWN (IPD)

If a strap pin's buffer type is IPD, one of the two hardware configurations outlined in [Figure 2-3](#) must be implemented. Use the Strap High configuration to set the strap option value to 1 and Strap Low to set the strap option value to 0.

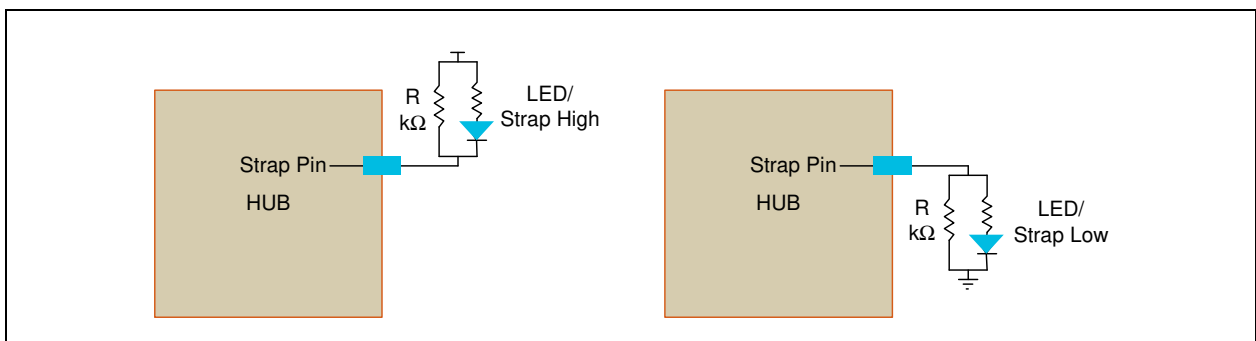
FIGURE 2-3: IPD PIN STRAP EXAMPLE



2.5.3 LED

If a strap pin's buffer type is I/O and shares functionality with an LED, the hardware configuration outlined below must be implemented. The internal logic will drive the LED appropriately (active high or low) depending on the sampled strap option. Use the Strap High configuration to set the strap option value to 1 and Strap Low to set the strap option to 0.

FIGURE 2-4: LED PIN STRAP EXAMPLE



USB2422

2.6 Example Applications

Figure 2-5 and Figure 2-6 depict example applications for an SoC based design and a non-SoC based design, respectively. The corresponding resistor and capacitor values for these examples are provided in Table 2-5.

FIGURE 2-5: EXAMPLE APPLICATION - SOC BASED DESIGN

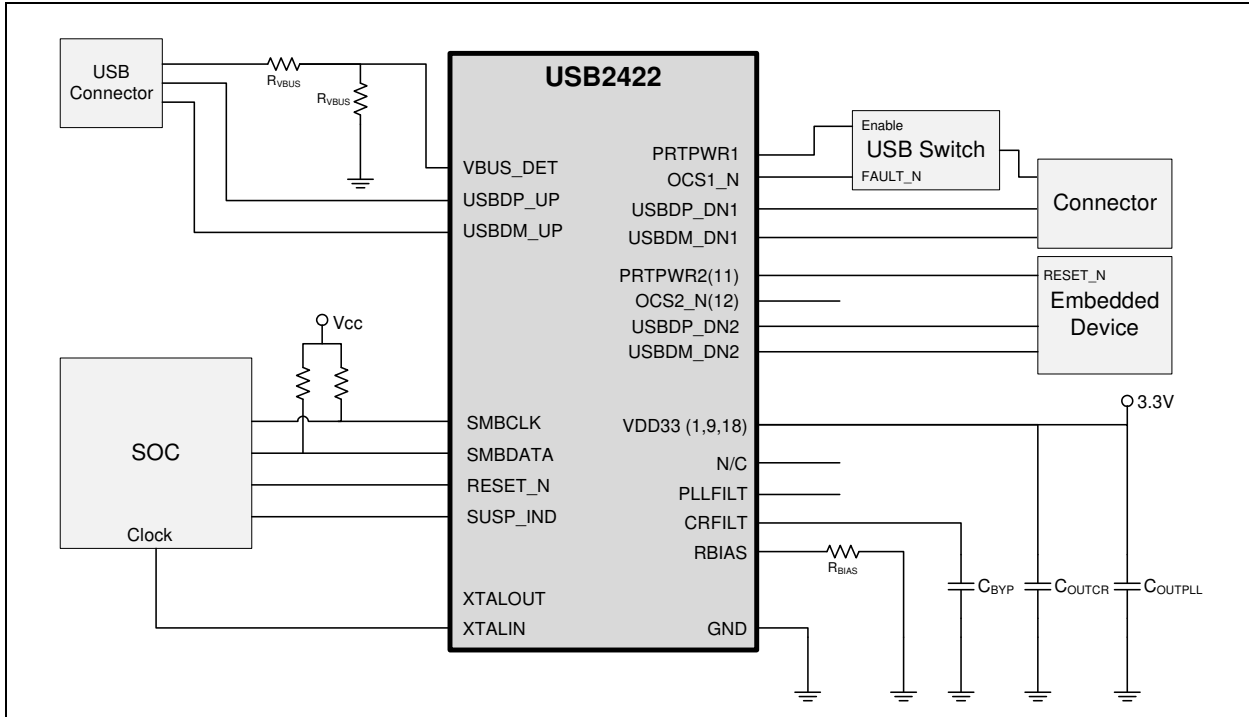


FIGURE 2-6: EXAMPLE APPLICATION - NON-SOC BASED DESIGN

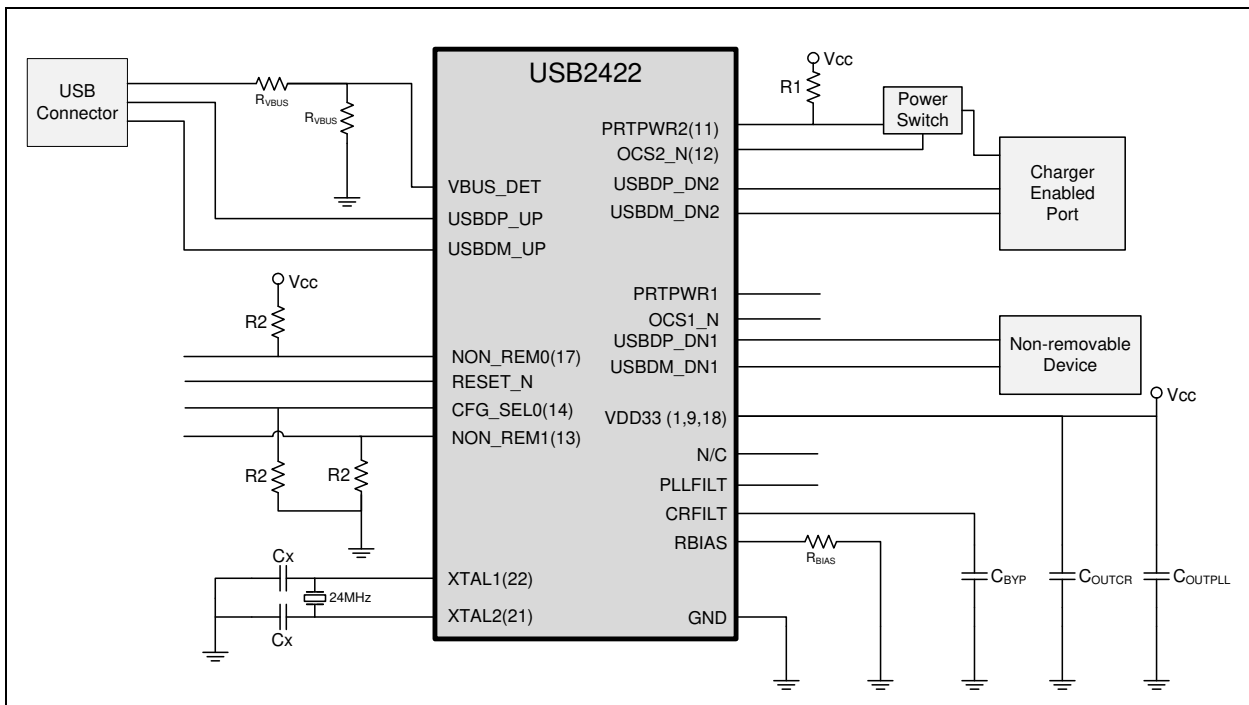


TABLE 2-5: EXAMPLE APPLICATIONS - RESISTOR/CAPACITOR VALUES

Designator	Value
R1	20 k Ω
R2	50 k Ω
Cx	18 pF
C _{BYP}	1.0 μ F
C _{OUTCR}	1.0 μ F (Note 2-1)
C _{OUTPLL}	0.1 μ F (Note 2-2)
R _{BIAS}	12 k Ω
R _{VBUS}	100 k Ω

Note 2-1 C_{OUTCR} should be placed as close as possible to pin 9

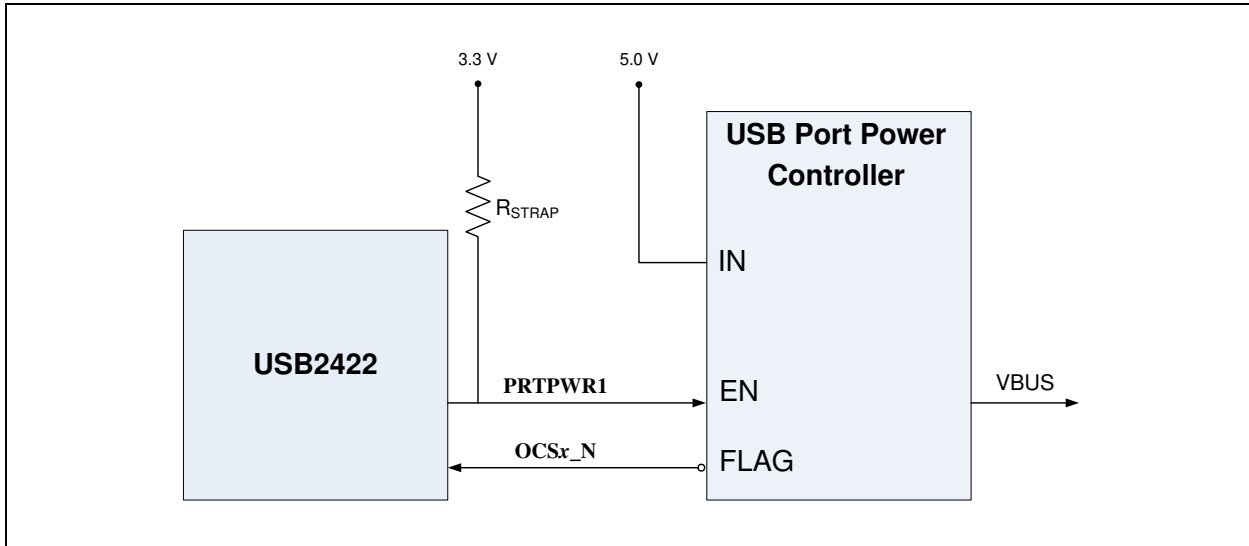
Note 2-2 C_{OUTPLL} should be placed as close as possible to pin 1

USB2422

3.0 BATTERY CHARGING SUPPORT

The USB2422 hub provides support for battery charging devices on a per port basis in compliance with the *USB Battery Charging Specification, Revision 1.1*. The hub can be configured to individually enable each downstream port for battery charging support either via pin strapping (Port 1 only) as illustrated in [Figure 3-1](#) or by setting the corresponding configuration bits via SMBus ([Section 4.1 on page 16](#)).

FIGURE 3-1: BATTERY CHARGING VIA EXTERNAL POWER SUPPLY



Note: R_{STRAP} enables battery charging.

3.1 USB Battery Charging

A downstream port enabled for battery charging turns on port power as soon as the power on reset and hardware configuration process has completed. The hub does not need to be enumerated nor does **VBUS_DET** need to be asserted for the port power to be enabled. These conditions allow battery charging in S3, S4, and S5 system power states as well as in the fully operational state. The *USB Battery Charging Specification* does not interfere with standard USB operation, which allows a device to perform battery charging at any time.

A port that supports battery charging must be able to support 1.5 amps of current on VBUS. Standard USB port power controllers typically only allow for 0.8 amps of current before detecting an over-current condition. Therefore, the 5 volt power supply, port power controller, or over-current protection devices must be chosen to handle the larger current demand compared to standard USB hub designs.

3.1.1 SPECIAL BEHAVIOR OF P RTPWR PINS

The USB2422 enables VBUS by asserting the port power (**P RTPWR[2:1]**) as soon as the hardware configuration process has completed. If the port detects an over-current condition, **P RTPWR[2:1]** will be turned off to protect the circuitry from overloading. If an over-current condition is detected when the hub is not enumerated, **P RTPWR[2:1]** can only be turned on from the host or if **RESET_N** is toggled. These behaviors provide battery charging even when the hub is not enumerated and protect the hub from sustained short circuit conditions. If the short circuit condition persists when the hub is plugged into a host system the user is notified that a port has an over-current condition. Otherwise **P RTPWR[2:1]** turned on by the host system and the ports operate normally.

3.2 Battery Charging Configuration

The battery charging option can be configured in one of two ways:

- When the hub is brought up in the default configuration with strapping options enabled, with the **PRTP-WR1/BC_EN1** pin configured (Port 1 only). See the following sections for details:
 - [Section 2.3, "Pin Descriptions \(Grouped by Function\)," on page 7](#)
 - [Section 2.5, "Strap Pin Configuration," on page 10](#)
- When the hub is initialized for configuration over SMBus.

3.2.1 BATTERY CHARGING ENABLED VIA SMBUS

Register memory map location 0xD0 is allocated for battery charging support. The Battery Charging register at location 0xD0 starting from bit 1 enables battery charging for each downstream port when asserted. Bit 1 represents port 1, and bit 2 represents port 2. Each port that has battery charging enabled asserts the corresponding **PRTPW[2:1]** pin.

USB2422

4.0 CONFIGURATION OPTIONS

Microchip's USB 2.0 hub is fully compliant with the *USB Specification* [1]. Refer to Chapter 10 (Hub Specification) for general details regarding hub operation and functionality.

The hub provides one Transaction Translator (TT) that is shared by both downstream ports (defined as Single-TT configuration). The TT contains 4 non-periodic buffers.

4.1 Hub Configuration

The USB2422 only supports internal defaults with the exception of the non-removable strap option (using **NON_REM[1:0]**). The hub internal default settings are as follows:

- Internal Default Configuration without over-rides
- Strap options enabled
- Self-powered operation enabled
- Individual power switching
- Individual over-current sensing

TABLE 4-1: HUB CONFIGURATION OPTIONS

CFG_SEL	Description
0	Default configuration: <ul style="list-style-type: none">• Strap options enabled• Hub descriptors indicate the hub as “self-powered”
1	The hub is configured externally over SMBus (as an SMBus slave device with address 0101100b): <ul style="list-style-type: none">• Strap options disabled• Self-powered or bus-powered depending on register settings• All registers configured over SMBus

4.2 Resets

There are two device resets: a hardware reset via **RESET_N**, and a USB Bus Reset.

4.2.1 EXTERNAL HARDWARE RESET_N

A valid hardware reset is defined as assertion of **RESET_N** for a minimum of 1 μ s after all power supplies are within operating range. While reset is asserted, the hub (and its associated external circuitry) consumes less than 500 μ A of current from the upstream USB power source.

Assertion of **RESET_N** causes the following:

1. All downstream ports are disabled.
2. The **PRTPWR** power to downstream devices is turned on when battery charging is enabled for a specific port, and removed when battery charging is disabled for a specific port.
3. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
4. All transactions immediately terminate; no states are saved.
5. All internal registers return to the default state (in most cases, 00h).
6. The external crystal oscillator is halted.
7. The PLL is halted.

4.2.1.1 Hub Configuration Timing for Strapping Option

FIGURE 4-1: HUB CONFIGURATION TIMING

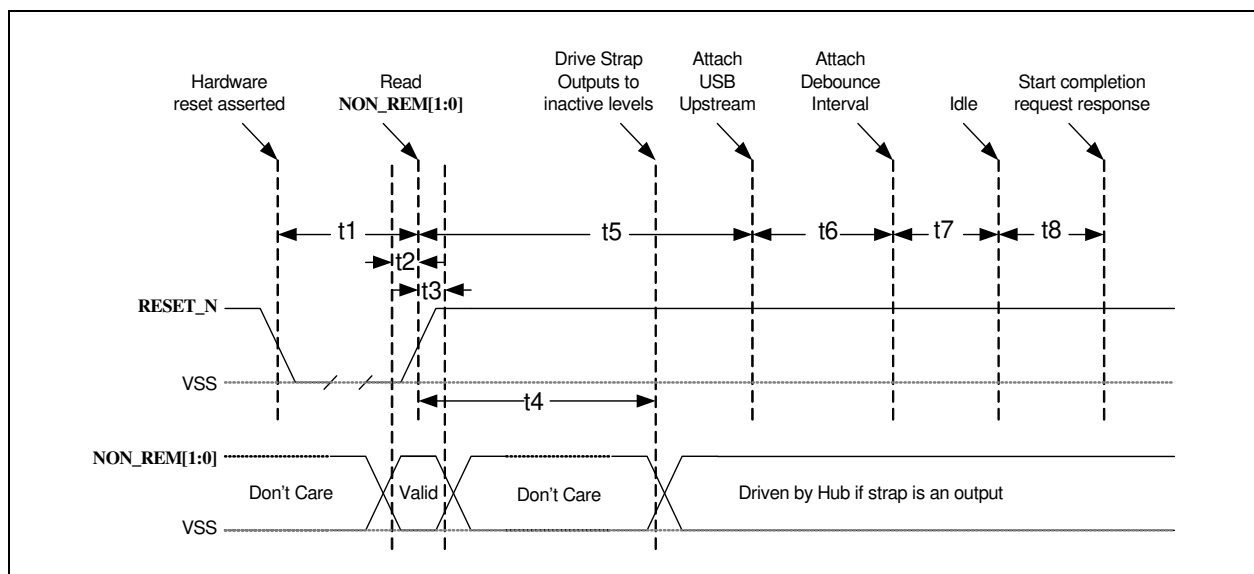


TABLE 4-2: HUB CONFIGURATION TIMING

Name	Description	MIN	TYP	MAX	Units
t1	RESET_N asserted	1			μsec
t2	Strap setup time	16.7			nsec
t3	Strap hold time	16.7		1400	nsec
t4	Hub outputs driven to inactive logic states		1.5	2	μsec
t5	USB attach (See Note)		3		μsec
t6	Host acknowledges attach and signals USB reset	100			msec
t7	USB idle		undefined		msec
t8	Completion time for requests (with or without data stage)			5	msec

Note: All power supplies must have reached the operating levels mandated in [Section 5.0, "DC Parameters"](#), prior to (or coincident with) the assertion of **RESET_N**.

4.2.2 USB BUS RESET

In response to the upstream port signaling a reset to the hub, the hub does the following:

1. Sets default address to 0.
2. Sets configuration to unconfigured.
3. The **PRTPWR** power to downstream devices is turned on when battery charging is enabled for a specific port, and removed when battery charging is disabled for a specific port.
4. Clears all TT buffers.
5. Moves device from suspended to active (if suspended).
6. Complies with Section 11.10 of the *USB 2.0 Specification* for behavior after completion of the reset sequence. The host then configures the hub and the hub's downstream port devices in accordance with the specification.

The hub does not propagate the upstream USB reset to downstream devices.

USB2422

4.3 SMBus

The Microchip hub can be configured by an external processor via an SMBus interface (see [Table 4-1](#) for details on enabling the SMBus interface). The Microchip hub waits indefinitely for the SMBus code load to complete and only appears as a newly connected device on USB after the code load is complete.

The hub's SMBus acts as a slave-only SMBus device. The implementation only supports block write ([Section 4.3.2.1](#)) and block read ([Section 4.3.2.2](#)) protocols. Reference the *System Management Bus Specification* [2] for additional information.

Refer to [Section 4.4, "SMBus Registers," on page 20](#) for details on all SMBus accessible registers.

4.3.1 SMBUS SLAVE ADDRESS

The 7-bit slave address is 0101100b. The hub will not respond to the general call address of 0000000b.

4.3.2 PROTOCOL IMPLEMENTATION

Typical block write and block read protocols are shown in figures [4-2](#) and [4-3](#). Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading shown in the figures during a read or write indicates the hub is driving data on the **SMBDATA** line; otherwise, host data is on the **SMBDATA** line.

The SMBus slave address assigned to the hub (0101100b) allows it to be identified on the SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

Note: Data bytes are transferred MSB first.

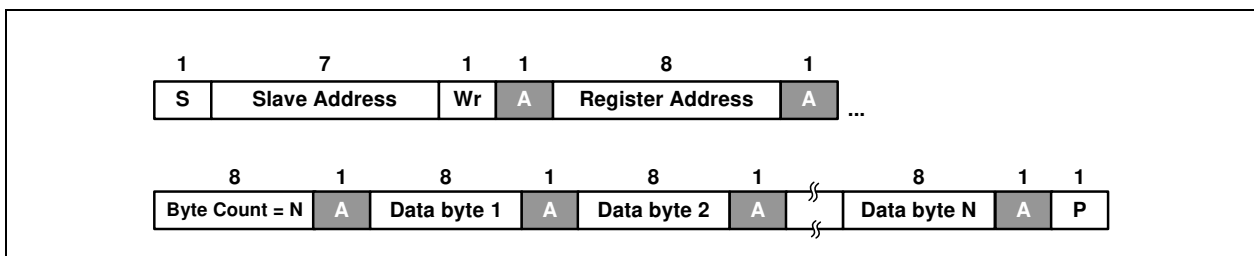
4.3.2.1 Block Write/Read

The block write begins with a slave address and a write condition. After the command code, the host issues a byte count which describes how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be zero. A block write or read allows a transfer maximum of 32 data bytes.

Note: For the following SMBus tables:

Denotes Master-to-Slave
 Denotes Slave-to-Master

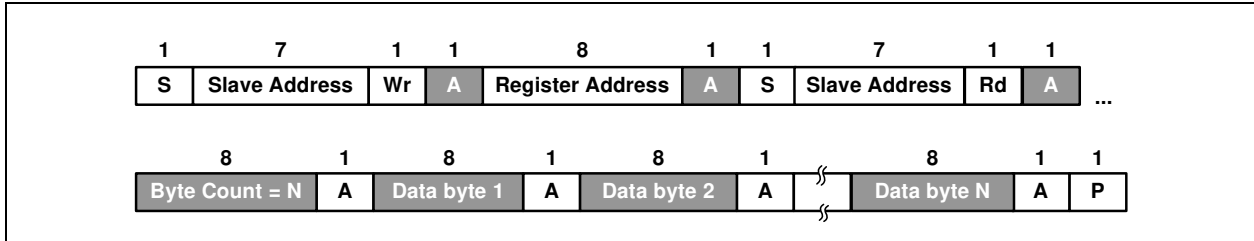
FIGURE 4-2: BLOCK WRITE



4.3.2.2 Block Read

A block read differs from a block write in that the repeated start condition exists to satisfy the SMBus specification's requirement for a change in the transfer direction.

FIGURE 4-3: BLOCK READ



4.3.2.3 Invalid Protocol Response Behavior

Note that any attempt to update registers with an invalid protocol will not be updated. The only valid protocols are write block and read block (described above), where the hub only responds to the 7-bit hardware selected slave address (0101100b).

4.3.3 SLAVE DEVICE TIMEOUT

Devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25 ms ($T_{\text{TIMEOUT, MIN}}$). The master must detect this condition and generate a stop condition within or after the transfer of the interrupted data byte. Slave devices must reset their communication and be able to receive a new START condition no later than 35 ms ($T_{\text{TIMEOUT, MAX}}$).

Note: Some simple devices do not contain a clock low drive circuit; this simple kind of device typically resets its communications port after a start or stop condition. The slave device timeout must be implemented.

4.3.4 STRETCHING THE SCLK SIGNAL

The hub supports stretching of the SCLK by other devices on the SMBus. However, the hub does not stretch the SCLK.

4.3.5 SMBUS TIMING

The SMBus slave interface complies with the *SMBus Specification Revision 1.02*. See Section 2.1, *AC Specifications* on page 3 for more information.

4.3.6 BUS RESET SEQUENCE

The SMBus slave interface resets and returns to the idle state upon a START condition followed immediately by a STOP condition.

4.3.7 SMBUS ALERT RESPONSE ADDRESS

The SMBALERT# signal is not supported by the hub.

USB2422

4.4 SMBus Registers

This section details the device SMBus registers.

Note: Internal Default ROM values are not visible to THE SMBus interface and cannot be read. When the hub is configured for SMBus register load, the entire register set must be written.

TABLE 4-3: INTERNAL DEFAULT AND SMBUS REGISTER MEMORY MAP

Reg. Address	Type	Register Name	Internal Default ROM	SMBus & EEPROM Default
00h	R/W	Vendor ID Least Significant Bit Register (VIDL)	24h	00h
01h	R/W	Vendor ID Most Significant Bit Register (VIDM)	04h	00h
02h	R/W	Product ID Least Significant Bit Register (PIDL)	22h	00h
03h	R/W	Product ID Most Significant Bit Register (PIDM)	24h	00h
04h	R/W	Device ID Least Significant Bit Register (DIDL)	A0h	00h
05h	R/W	Device ID Most Significant Bit Register (DIDM)	00h	00h
06h	R/W	Configuration Data Byte 1 Register (CFG1)	8Bh	00h
07h	R/W	Configuration Data Byte 2 Register (CFG2)	20h	00h
08h	R/W	Configuration Data Byte 3 Register (CFG3)	02h	00h
09h	R/W	Non-Removable Device Register (NRD)	00h	00h
0Ah	R/W	Port Disable for Self-Powered Operation Register (PDS)	00h	00h
0Bh	R/W	Port Disable for Bus-Powered Operation Register (PDB)	00h	00h
0Ch	R/W	Max Power for Self-Powered Operation Register (MAXPS)	01h	00h
0Dh	R/W	Max Power for Bus-Powered Operation Register (MAXPB)	32h	00h
0Eh	R/W	Hub Controller Max Current for Self-Powered Operation Register (HCMCS)	01h	00h
0Fh	R/W	Hub Controller Max Power for Bus-Powered Operation Register (HCMCB)	32h	00h
10h	R/W	Power-On Time Register (PWRT)	32h	00h
11h	R/W	Language ID High Register (LANGIDH)	00h	00h
12h	R/W	Language ID Low Register (LANGIDL)	00h	00h
13h	R/W	Manufacturer String Length Register (MFRSL)	00h	00h
14h	R/W	Product String Length Register (PRDSL)	00h	00h
15h	R/W	Serial String Length Register (SERSL)	00h	00h
16h-53h	R/W	Manufacturer String Registers (MANSTR)	00h	00h
54h-91h	R/W	Product String Registers (PRDSTR)	00h	00h
92h-CFh	R/W	Serial String Registers (SERSTR)	00h	00h
D0h	R/W	Battery Charging Enable Register (BC_EN)	00h	00h
E0h-F5h	-	RESERVED	-	-
F6h	R/W	Boost Upstream Register (BOOSTUP)	00h	00h
F7h	-	RESERVED	-	-
F8h	R/W	Boost Downstream Register (BOOST40)	00h	00h
F9h	-	RESERVED	-	-
FAh	R/W	Port Swap Register (PRTSP)	00h	00h
FBh	R/W	Port 1/2 Remap Register (PRTR12)	00h	00h
FCh-FEh	-	RESERVED	-	-
FFh	R/W	Status/Command Register (STCD)	00h	00h

4.4.1 VENDOR ID LEAST SIGNIFICANT BIT REGISTER (VIDL)

Offset: 00h Size: 8 bits

Bits	Description	Type	Default
7:0	Least Significant Byte of the Vendor ID (VID_LSB) This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the OEM using the SMBus interface option.	R/W	00h

4.4.2 VENDOR ID MOST SIGNIFICANT BIT REGISTER (VIDM)

Address: 01h Size: 8 bits

Bits	Description	Type	Default
7:0	Most Significant Byte of the Vendor ID (VID_LSB) This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the OEM using the SMBus interface options.	R/W	00h

4.4.3 PRODUCT ID LEAST SIGNIFICANT BIT REGISTER (PIDL)

Address: 02h Size: 8 bits

Bits	Description	Type	Default
7:0	Least Significant Byte of the Product ID (PID_LSB) This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by OEM). This field is set by the OEM using the SMBus interface options.	R/W	00h

4.4.4 PRODUCT ID MOST SIGNIFICANT BIT REGISTER (PIDM)

Address: 03h Size: 8 bits

Bits	Description	Type	Default
7:0	Most Significant Byte of the Product ID (PID_LSB) This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by OEM). This field is set by the OEM using either SMBus interface options.	R/W	00h

USB2422

4.4.5 DEVICE ID LEAST SIGNIFICANT BIT REGISTER (DIDL)

Address: 04h Size: 8 bits

Bits	Description	Type	Default
7:0	Least Significant Byte of the Device ID (DID_LSB) This is a 16-bit device release number in BCD format (assigned by OEM). This field is set by the OEM using either the SMBus interface options.	R/W	00h

4.4.6 DEVICE ID MOST SIGNIFICANT BIT REGISTER (DIDM)

Address: 05h Size: 8 bits

Bits	Description	Type	Default
7:0	Most Significant Byte of the Device ID (DID_LSB) This is a 16-bit device release number in BCD format (assigned by OEM). This field is set by the OEM using the SMBus interface options.	R/W	00h

4.4.7 CONFIGURATION DATA BYTE 1 REGISTER (CFG1)

Address: 06h Size: 8 bits

Bits	Description	Type	Default
7	<p>Self or Bus Power (SELF_BUS_PWR) Selects between Self- and Bus-Powered operation.</p> <p>The Hub is either Self-Powered (draws less than 2mA of upstream bus power) or Bus-Powered (limited to a 100mA maximum of upstream power prior to being configured by the host controller).</p> <p>When configured as a Bus-Powered device, the Hub consumes less than 100mA of current prior to being configured. After configuration, the Bus-Powered Hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100mA per externally available downstream port) must consume no more than 500mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB2.0 specifications are not violated.</p> <p>When configured as a Self-Powered device, <1mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500mA of current.</p> <p>This field is set by the OEM using the SMBus interface option. Please see the description under Dynamic Power for the self/bus power functionality when dynamic power switching is enabled.</p> <p>0 = Bus-Powered operation 1 = Self-Powered operation</p> <p>Note: If Dynamic Power Switching is enabled, this bit is ignored and the LOCAL_PWR pin is used to determine if the hub is operating from self or bus power.</p>	R/W	0b
6	RESERVED	-	-
5	<p>High Speed Disable (HS_DISABLE) Disables the capability to attach as either a High/Full- speed device, and forces attachment as Full-speed only i.e. (no High-Speed support).</p> <p>0 = High-/Full-Speed 1 = Full-Speed-Only (High-Speed disabled)</p>	R/W	0b
4	<p>Multi-TT Enable (MTT_ENABLE) Enables one transaction translator per port operation.</p> <p>Selects between a mode where only one transaction translator is available for all ports (Single-TT), or each port gets a dedicated transaction translator (Multi-TT)</p> <p>Note: The host may force Single-TT mode only</p> <p>0 = Single TT for all ports. Default to STT if MTT still exists 1 = One TT per port (multiple TT's supported)</p>	R/W	0b

USB2422

Bits	Description	Type	Default
3	EOP Disable (EOP_DISABLE) Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the Hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification for additional details. Note: generation of an EOP at the EOF1 point may prevent a Host controller (operating in FS mode) from placing the USB bus in suspend. 0 = An EOP is generated at the EOF1 point if no traffic is detected 1 = EOP generation at EOF1 is disabled (Note: This is normal USB operation) Note: This is a rarely used feature in the PC environment. It is included because it is a permitted feature in Chapter 11 of the USB specification.	R/W	0b
2:1	Over Current Sense (CURRENT_SNS) Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs) The ability to support current sensing on a port or ganged basis is hardware implementation dependent. 00 = Ganged sensing (all ports together) 01 = Individual port-by-port 1x = Over current sensing not supported (Must only be used with Bus-Powered configurations)	R/W	00b
0	Port Power Switching (PORT_PWR) Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port-by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. 0 = Ganged switching (all ports together) 1 = Individual port-by-port switching	R/W	0b

4.4.8 CONFIGURATION DATA BYTE 2 REGISTER (CFG2)

Address: 07h Size: 8 bits

Bits	Description	Type	Default
7	<p>Dynamic Power Enable (DYNAMIC) Controls the ability of the Hub to automatically change from Self-Powered operation to Bus-Powered operation if the local power source is removed or is unavailable (and from Bus-Powered to Self-Powered if the local power source is restored).</p> <p>Note: If the local power source is available, the Hub will always switch to Self-Powered operation.</p> <p>When Dynamic Power switching is enabled, the Hub detects the availability of a local power source by monitoring the external LOCAL_PWR pin. If the Hub detects a change in power source availability, the Hub immediately disconnects and removes power from all downstream devices and disconnects the upstream port. The Hub will then re-attach to the upstream port as either a Bus-Powered Hub (if local-power is unavailable) or a Self-Powered Hub (if local power is available).</p> <p>0 = No Dynamic auto-switching (pin becomes SUSP_IND) and the hub controller will utilize the inverse of the SELF_BUS_PWR bit for 'Hub_Status_Field' bit '0' (local power source) 1 = Dynamic Auto-switching capable (pin becomes LOCAL_PWR) and the hub controller will utilize the LOCAL_PWR pin for 'Hub_Status_Field' bit '0' (local power source)</p>	R/W	0b
6	RESERVED	-	-
5:4	<p>Over Current Timer Delay (OC_TIMER)</p> <p>00 = 0.1ms 01 = 4ms 10 = 8ms 11 = 16ms</p>	R/W	00b
3	<p>Compound Device (COMPOUND) Allows the OEM to indicate that the Hub is part of a compound (see the USB Specification for definition) device. The applicable port(s) must also be defined as having a "Non-Removable Device".</p> <p>Note: When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device.</p> <p>0 = No 1 = Yes, Hub is part of a compound device</p>	R/W	0b
2:0	RESERVED	-	-