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USB2512/12A/12B
USB2513/13B
USB2514/14B
USB2517

USB 2.0 Hi-Speed Hub Controller

PRODUCT FEATURES

Datasheet

General Description

The SMSC USB251x hub is a family of low-power, OEM configurable, MTT (multi transaction translator)[1] hub controller IC products for embedded USB solutions. The "x" in the part number indicates the number of downstream ports available. The SMSC hub supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

For a summary of the products documented in this datasheet, please refer to the Chapter 1, "USB251x Hub Family Differences Overview," on page 7.

Highlights

- High performance, low-power, small footprint hub controller IC with 2, 3, 4, or 7 downstream ports (indicated by the "x" in the part number)
- Fully compliant with the USB 2.0 specification
- Enhanced OEM configuration options available through either a single serial I²C® EEPROM, or SMBus slave port
- **MultiTRAK™**
  - High-performance multiple transaction translator which provides one transaction translator per port
- **PortMap**
  - Flexible port mapping and disable sequencing
- **PortSwap**
  - Programmable USB differential-pair pin locations ease PCB design by aligning USB signal lines directly to connectors
- **PHYBoost**
  - Programmable USB signal drive strength for recovering signal integrity using 4-level driving strength resolution

Features

- USB251xB/xBi products are fully footprint compatible with USB251x/xi/xA/xAi products as direct drop-in replacements
  - Cost savings include using the same PCB components and application of USB-IF Compliance by Similarity
- Full power management with individual or ganged power control of each downstream port
- Fully integrated USB termination and pull-up/pull-down resistors
- Supports a single external 3.3 V supply source; internal regulators provide 1.2 V or 1.8 V internal core voltage
- Onboard 24 MHz crystal driver, ceramic resonator, or external 24/48 MHz clock input
- Customizable vendor ID, product ID, and device ID
- 4 kilovolts of HBM JESD22-A114F ESD protection (powered and unpowered)
- Supports self- or bus-powered operation
- USB251xB and USB251xBi products support the USB Battery Charging specification Rev. 1.1 for Charging Downstream Ports (CDP)
- Lead-free RoHS compliant packages:
  - 36-pin QFN (6x6 mm)
  - 48-pin QFN (7x7 mm)
  - 64-pin QFN (9x9 mm)
- USB251xi, USB2512Ai, and USB251xBi products support the industrial temperature range of -40ºC to +85ºC
- USB251xB products support the extended commercial temperature range of 0ºC to +85ºC

Applications

- LCD monitors and TVs
- Multi-function USB peripherals
- PC motherboards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems

1.USB2512A/Ai only uses a single transaction translator.

ORDER NUMBERS:

ORDER NUMBERS	LEAD-FREE ROHS COMPLIANT PACKAGE	PACKAGE SIZE	TEMPERATURE RANGE
USB2512-AEZG USB2512A-AEZG USB2513-AEZG USB2514-AEZG	36QFN	6 x 6 x 0.5 mm	0ºC to 70ºC
USB2512B-AEZG USB2513B-AEZG USB2514B-AEZG			0ºC to 85ºC
USB2512i-AEZG USB2512Ai-AEZG USB2512Bi-AEZG USB2513i-AEZG USB2513Bi-AEZG USB2514i-AEZG USB2514Bi-AEZG			-40ºC to 85ºC
USB2513-HZH USB2514-HZH	48QFN	7 x 7 x 0.5 mm	0ºC to 70ºC
USB2513i-HZH USB2514i-HZH			-40ºC to 85ºC
USB2517-JZX	64QFN	9 x 9 x 0.5 mm	0ºC to 70ºC
USB2517i-JZX			-40ºC to 85ºC

THIS PRODUCT MEETS THE HALOGEN MAXIMUM CONCENTRATION VALUES PER IEC61249-2-21.

FOR ROHS COMPLIANCE AND ENVIRONMENTAL INFORMATION, PLEASE VISIT WWW.SMSC.COM/ROHS.

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Chapter 1 USB251x Hub Family Differences Overview

Table 1.1 36-pin QFN (6x6x0.5 mm) RoHS Compliant Part Numbers

Part Number	Down-stream ports	True Speed	Battery Charging	Lower Power Consumption	LED Port Indicators	Clock (MHz)	0ºC to 70ºC	0ºC to 85ºC	-40ºC to 85ºC
USB2512 USB2512A*	2					24	✓		
USB2512i USB2512Ai*	2					24			✓
USB2512B	2		✓	✓		24		✓	
USB2512Bi	2		✓	✓		24			✓
USB2513	3					24	✓		
USB2513i	3					24			✓
USB2513B	3		✓	✓		24		✓	
USB2513Bi	3		✓	✓		24			✓
USB2514	4					24	✓		
USB2514i	4					24			✓
USB2514B	4		✓	✓		24		✓	
USB2514Bi	4		✓	✓		24			✓

Table 1.2 48-pin QFN (7x7x0.5 mm) RoHS Compliant Part Numbers

Part Number	Down-stream ports	True Speed	Battery Charging	Lower Power Consumption	LED Port Indicators	Clock (MHz)	0ºC to 70ºC	0ºC to 85ºC	-40ºC to 85ºC
USB2513	3	✓			✓	24/48	✓		
USB2513i	3	✓			✓	24/48			✓
USB2514	4	✓			✓	24/48	✓		
USB2514i	4	✓			✓	24/48	✓		✓

Table 1.3 64-pin QFN (9x9x0.5 mm) RoHS Compliant Part Numbers

Part Number	Down-stream ports	True Speed	Battery Charging	Lower Power Consumption	LED Port Indicators	Clock (MHz)	0ºC to 70ºC	0ºC to 85ºC	-40ºC to 85ºC
USB2517	7	✓			✓	24	✓		
USB2517i	7	✓			✓	24			✓

Note 1.1 *USB2512A/Ai only uses a single transaction translator, whereas all other parts use a multi transactions translator.

Chapter 2 General Description

The SMSC USB251x hub family is a group of low-power, OEM configurable, MTT (multi transaction translator)[1] hub controller IC's with downstream ports for embedded USB solutions. The SMSC USB251x hub family is fully compliant with the USB 2.0 specification. Each of the SMSC hub controllers can attach to an upstream port as a full-speed hub or as a full-/hi-speed hub. The SMSC hub controllers support low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors on D+ and D– pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB251x hub family includes programmable features such as:

MultiTRAK™ Technology which utilizes a dedicated TT per port to maintain consistent full-speed data throughput regardless of the number of active downstream connections. MultiTRAK™ outperforms conventional USB 2.0 hubs with a single TT in USB full-speed data transfers.

PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB251x hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB251x hub controllers automatically reorder the remaining ports to match the USB host controller's port numbering scheme.

PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost which enables 4 programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost attempts to restore USB signal integrity.

OEM Selectable Features

A default configuration is available in each of the SMSC USB251x hub controllers following a reset. This configuration may be sufficient for most applications. Strapping option pins make it possible to modify a sub-set of the configuration options.

The USB251x hub controllers may be configured by an external EEPROM or a microcontroller. When using the microcontroller interface, the hub appears as an SMBus slave device. If the hub is pin-strapped for external EEPROM configuration but no external EEPROM is present, then a value of '0' will be written to all configuration data bit fields (the hub will attach to the host with all '0' values).

The USB251x hub family supports OEM selectable features including:

- Optional OEM configuration via I^2C EEPROM or via the industry standard SMBus interface from an external SMBus host or microcontroller.
- Supports compound devices on a port-by-port basis.
- Selectable over-current sensing and port power control on an individual or ganged basis to match the OEM's choice of circuit board component selection.
- Customizable vendor ID, product ID, and device ID.
- Configurable delay time for filtering the over-current sense inputs.
- Configurable downstream port power-on time reported to the host.
- Supports indication of the maximum current that the hub consumes from the USB upstream port.
- Supports Indication of the maximum current required for the hub controller.

1.USB2512A/2Ai only uses a single transaction translator.

- Supports custom string descriptors (up to 31 characters):
  - Product string
  - Manufacturer string
  - Serial number string
- When available, pin selectable options for default configuration may include:
  -Downstream ports as non-removable ports
  -Downstream ports as disabled ports
  -Downstream port power control and over-current detection on a ganged or individual basis
  -USB signal drive strength
  -USB differential pair pin location
- For more information, please contact your sales representative to obtain a copy of the latest Battery Charging white paper.
- USB251xB/xBi products are fully footprint compatible with USB251x/xi/xA/xAi products:
  -pin-compatible
  -direct drop-in replacement
  -use the same PCB components
  -USB-IF Compliance by Similarity for ease of use and a complete cost reduction solution
  -PIDs, DIDs, and other register defaults may differ and can be configured to match the OEM's needs. Please see Table 8.2, "Internal Default, EEPROM and SMBus Register Memory Map" for details.

Table 2.1 Summary of Compatibilities between USB251xB/xBi and USB251x/xi/xA/xAi Products

Part Number	Drop-in Replacement	PACKAGE
USB2512	USB2512B	36QFN
USB2512i	USB2512Bi	
USB2512A	USB2512B	
USB2512Ai	USB2512Bi	
USB2513	USB2513B	
USB2513i	USB2513Bi	
USB2514	USB2514B	
USB2514i	USB2514Bi	

Chapter 3 Acronyms

I^2C®: Inter-Integrated Circuit[1]

OCS: Over-Current Sense

PCB: Printed Circuit Board

PHY: Physical Layer

PLL: Phase-Locked Loop

QFN: Quad Flat No Leads

RoHS: Restriction of Hazardous Substances Directive

SCL: Serial Clock

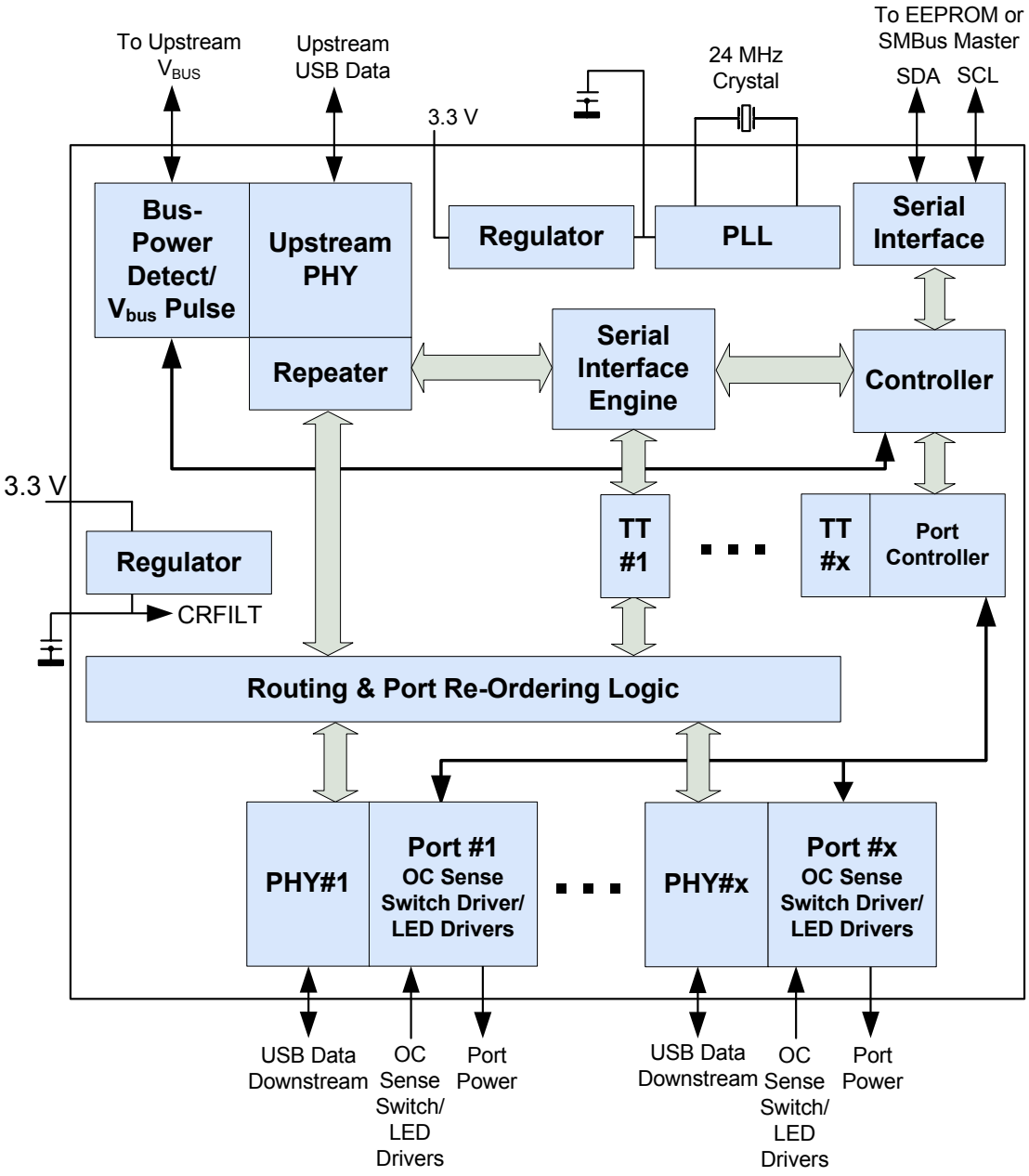
SIE: Serial Interface Engine

SMBus: System Management Bus

TT: Transaction Translator

1.I^2C is a registered trademark of Philips Corporation.

Chapter 4 Block Diagram



The 'x' indicates the number of available downstream ports: 2, 3, 4, or 7.

Figure 4.1 USB251x Hub Family Block Diagram

Note 4.1 USB2512A/USB2512Ai only supports a single transaction translator.

Note 4.2 The LED port indicators only apply to USB2513/13i/14/14i (48QFN only) and USB2517/17i.

Chapter 5 Pin Descriptions

This chapter is organized by a set of pin configurations (organized by package type) followed by a corresponding pin list organized alphabetically. A comprehensive and detailed description list of each signal (named in the pin list) is organized by function in Table 5.2, “USB251x Pin Descriptions,” on page 22. Please refer to Table 5.3, “Buffer Type Descriptions,” on page 27 for a list of buffer types.

The “N” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “N” is not present after the signal name, the signal is asserted when it is at the high voltage level. The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

5.1 Pin Configurations and Lists (Organized by Package Type)

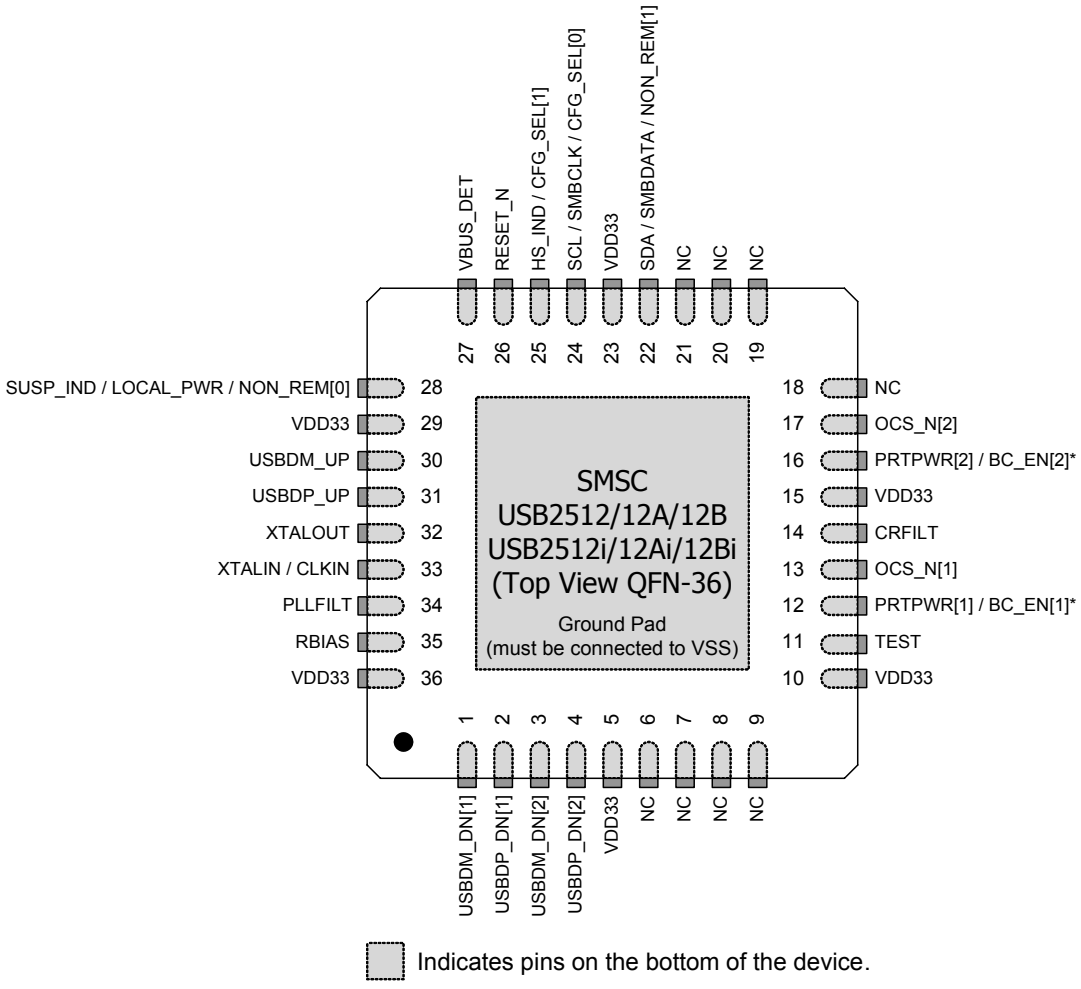


Figure 5.1 2-Port 36-Pin QFN

Note: *Battery charging enable (BC_EN) is only available in the USB251xB/Bi.

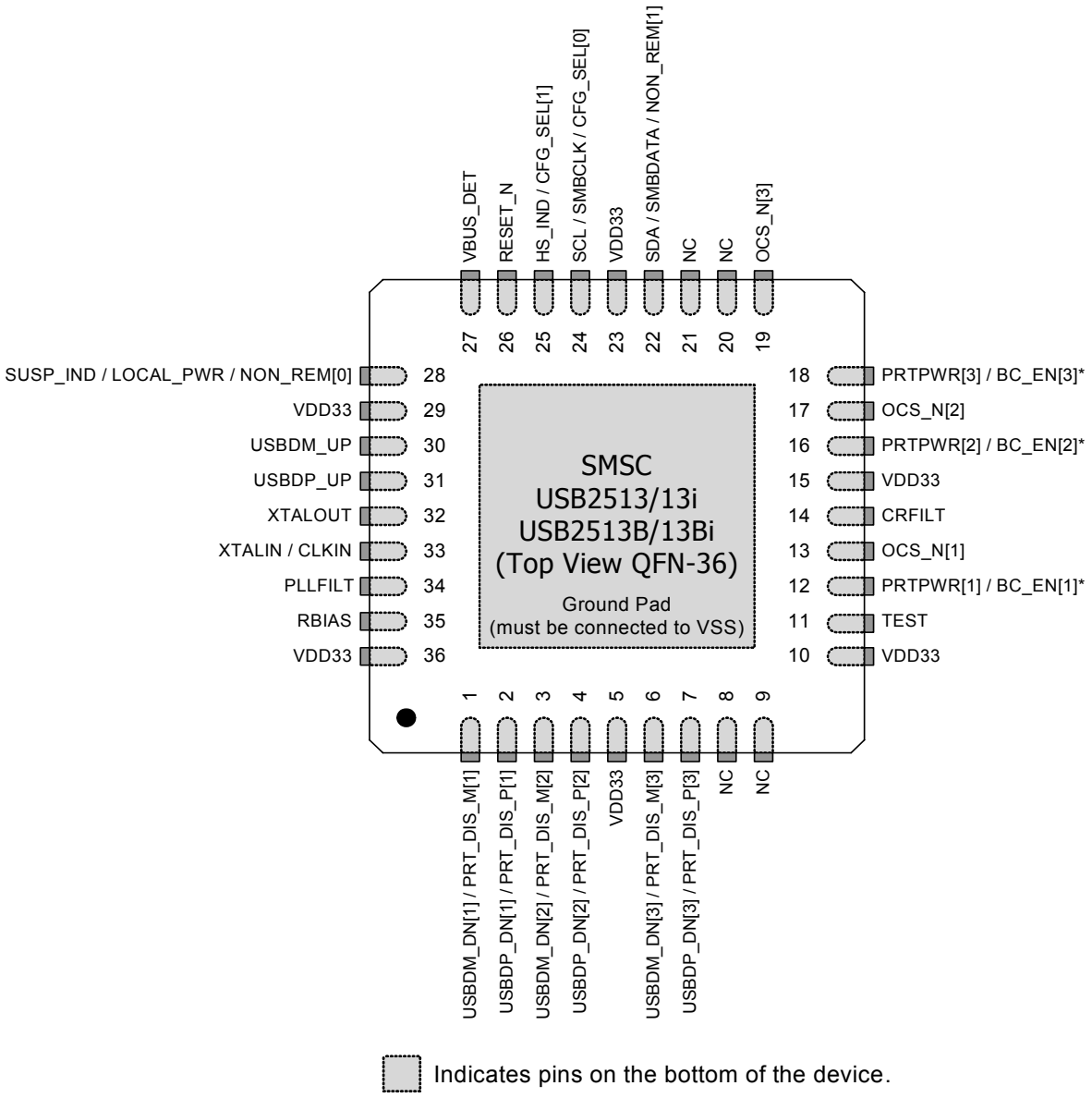


Figure 5.2 3-Port 36-pin QFN

Note: *Battery charging enable (BC_EN) is only available in the USB251xB/Bi.

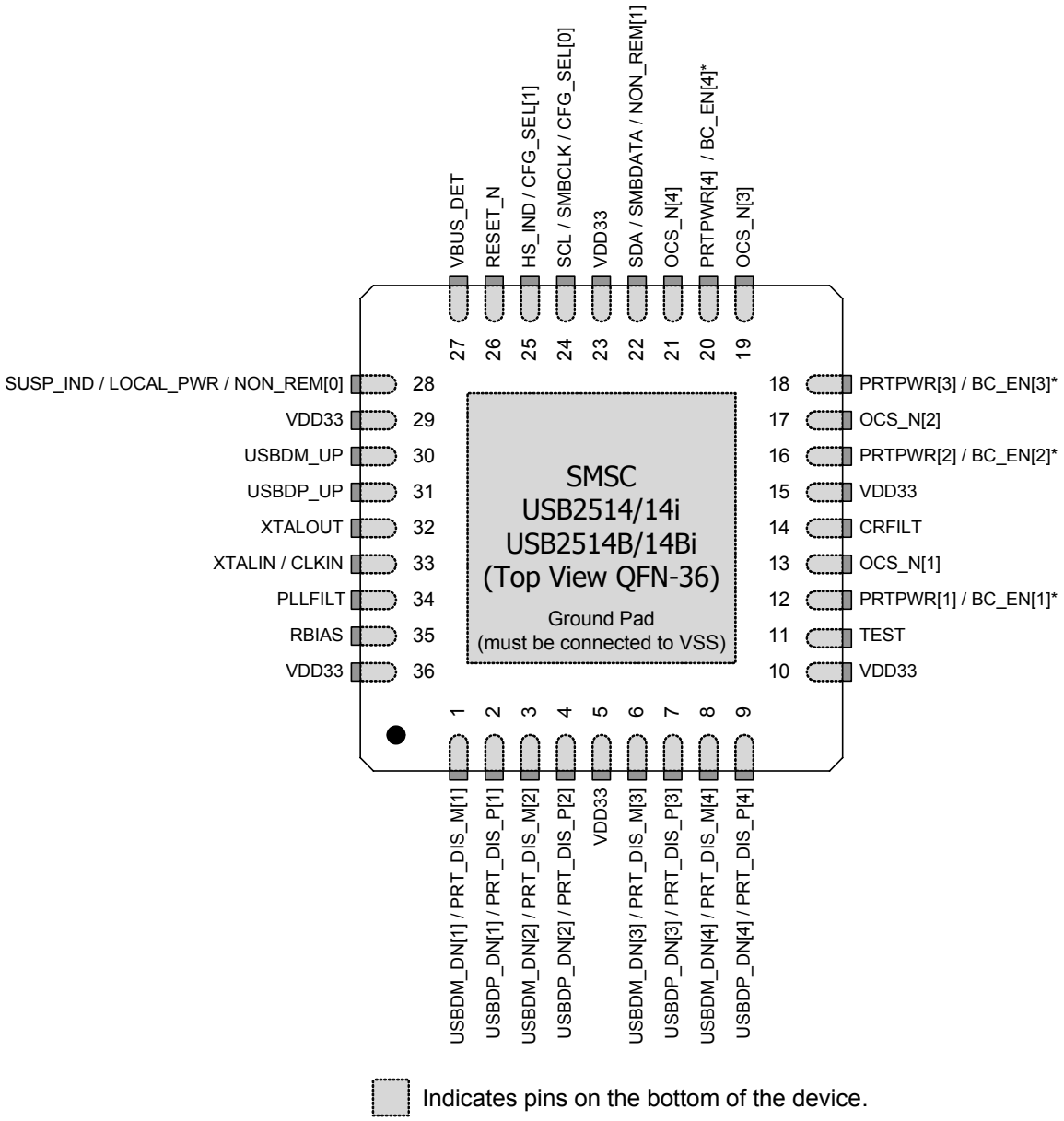


Figure 5.3 4-Port 36-pin QFN

Note: *Battery charging enable (BC_EN) is only available in the USB251xB/Bi.

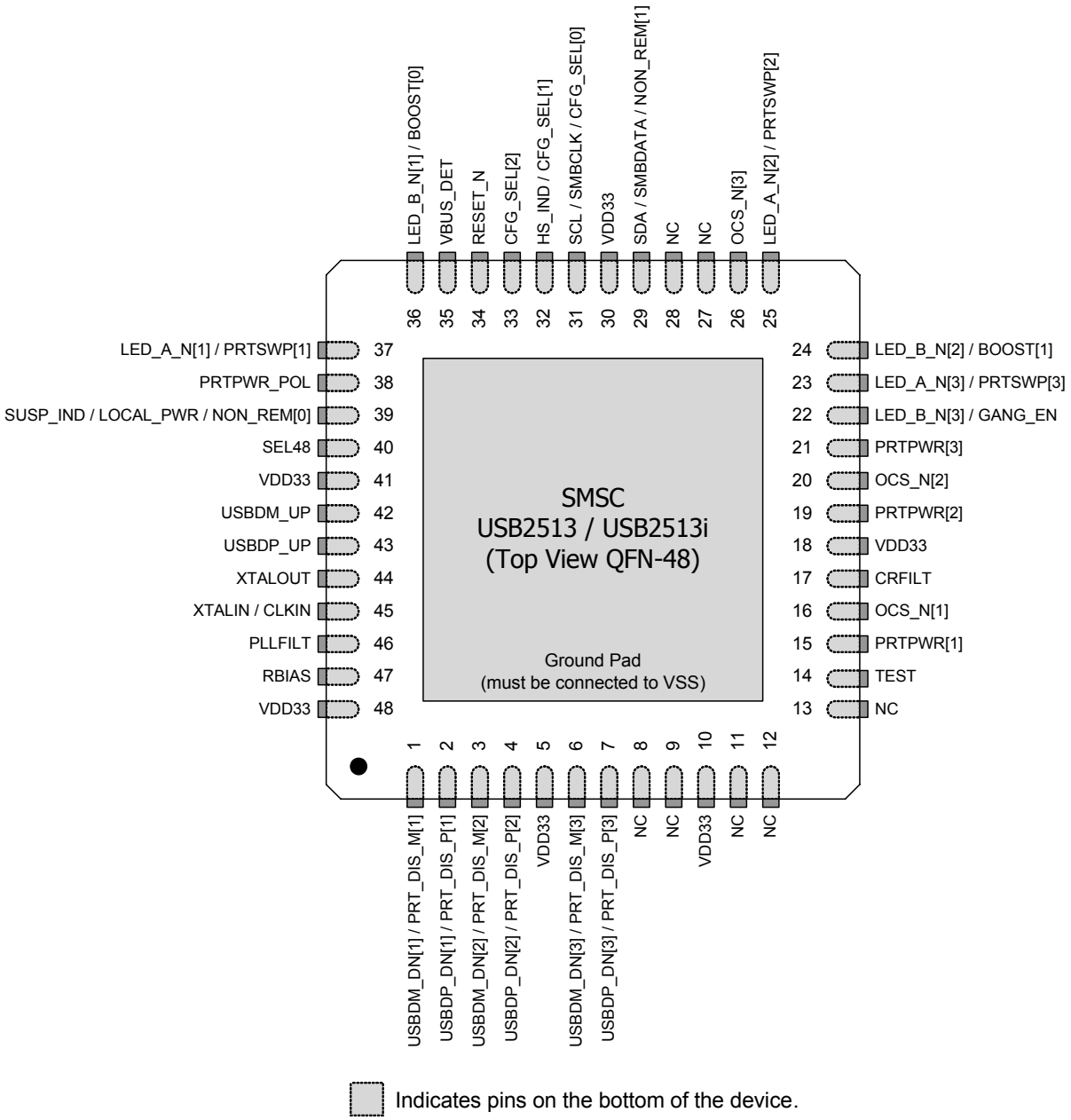


Figure 5.4 3-Port 48-Pin QFN

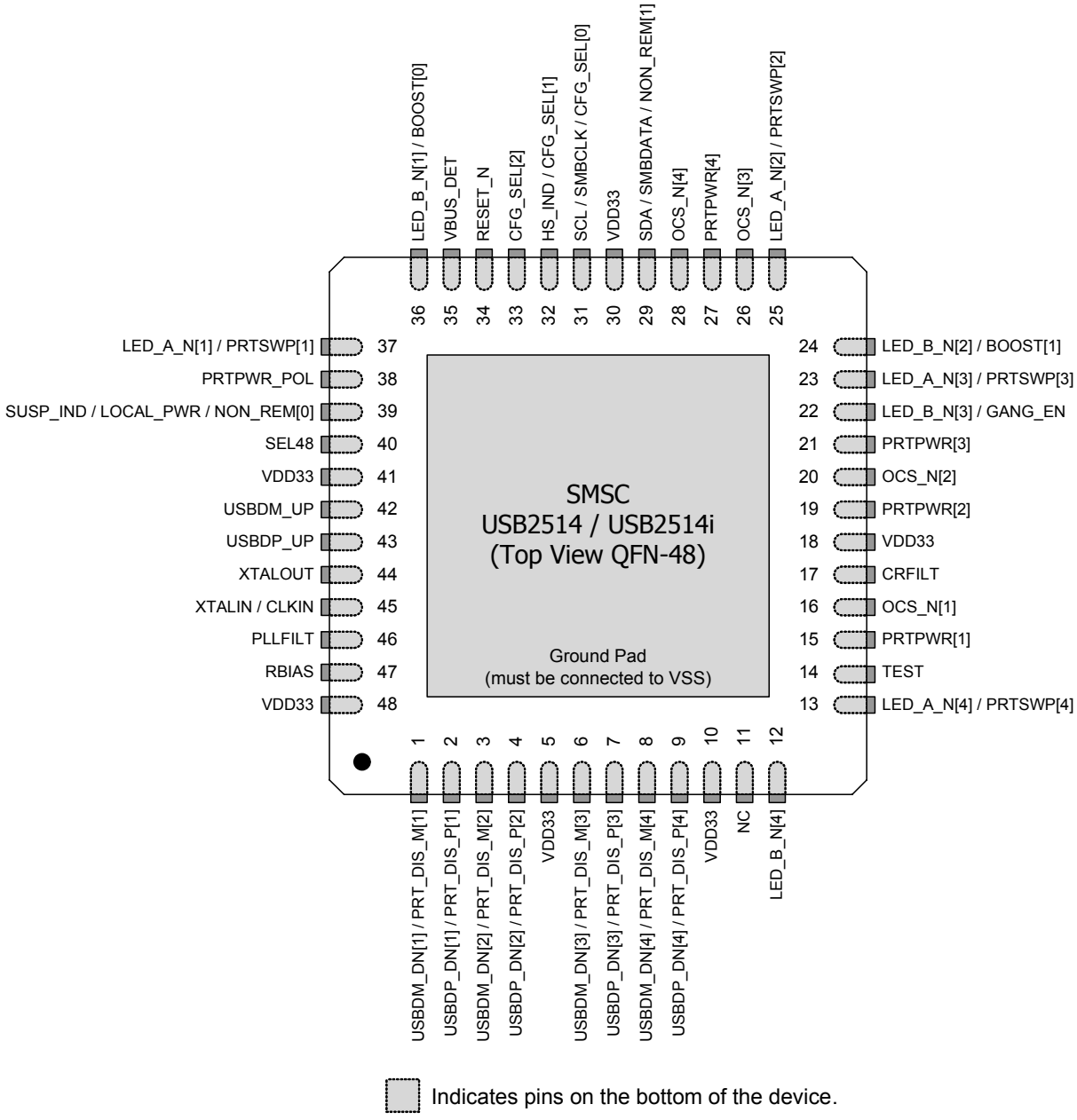


Figure 5.5 4-Port 48-Pin QFN

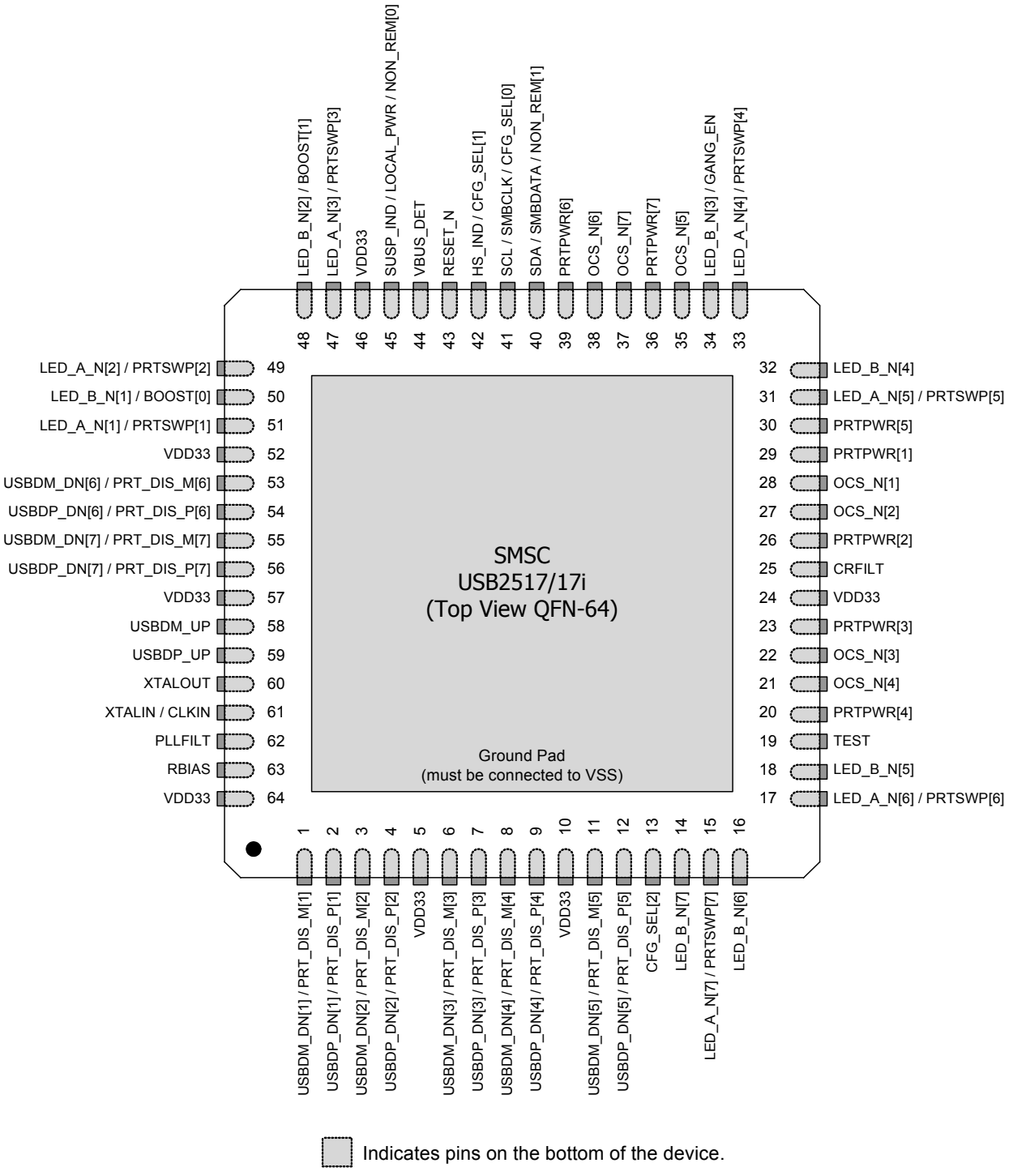


Figure 5.6 7-Port 64-Pin QFN

Table 5.1 Pin List in Alphabetical Order

SYMBOL	NAME	PIN NUMBERS								
		36 QFN						48QFN		64 QFN
		USB2512 USB2512i USB2512A USB2512Ai	USB2512B USB2512Bi	USB2513 USB2513i	USB2513B USB2513Bi	USB2514 USB2514i	USB2514B USB2514Bi	USB2513 USB22513i	USB2514 USB22514i	USB2517 USB2517i
BC_EN[1]	Battery Charging Strap Option	-	12	-	12	-	12	-		
BC_EN[2]		-	16	-	16	-	16	-		
BC_EN[3]		-			18	-	18	-		
BC_EN[4]		-					20	-		
BOOST[0]	PHY Boost Strapping Option	-						36		50
BOOST[1]		-						24		48
CFG_SEL[0]	Configuration Programming Selection	24						31		41
CFG_SEL[1]		25						32		42
CFG_SEL[2]		-						33		13
CLKIN	External Clock Input	33						45		61
CRFILT	Core Regulator Filter Capacitor	14						17		25
GANG_EN	Ganged Port Power Strap Option	-						22		34
Ground Pad	Exposed Pad Tied to Ground (VSS)	ePad								
HS_IND	Hi-Speed Upstream Port Indicator	25						32		42
LED_A_N[1]	Port LED Indicator	-						37		51
LED_A_N[2]		-						25		49
LED_A_N[3]		-						23		47
LED_A_N[4]		-							13	33
LED_A_N[5]		-								31
LED_A_N[6]		-								17
LED_A_N[7]		-								15
LED_B_N[1]	Enhanced Indicator Port LED	-						36		50
LED_B_N[2]		-						24		48
LED_B_N[3]		-						22		34
LED_B_N[4]		-							12	32
LED_B_N[5]		-								18
LED_B_N[6]		-								16
LED_B_N[7]		-								14
LOCAL_PWR	Local Power Detection	28						39		45

Table 5.1 Pin List in Alphabetical Order (continued)

SYMBOL	NAME	PIN NUMBERS								
		36 QFN						48QFN		64 QFN
		USB2512 USB2512i USB2512A USB2512Ai	USB2512B USB2512Bi	USB2513 USB2513i	USB2513B USB2513Bi	USB2514 USB2514i	USB2514B USB2514Bi	USB2513 USB22513i	USB2514 USB22514i	USB2517 USB2517i
NC	No Connect	6		-				8	11	-
NC		7		-				9	-	
NC		18		-				11	-	
NC		19		-				12	-	
NC		8				-		13	-	
NC		9				-		27	-	
NC		20				-		28	-	
NC		21				-				
NON_REM[0]	Non-Removable Port Strap Option	28						39		45
NON_REM[1]		22						29		40
OCS_N[1]	Over-Current Sense	13						16		28
OCS_N[2]		17						20		27
OCS_N[3]		-		19				26		22
OCS_N[4]		-				21		-	28	21
OCS_N[5]		-								35
OCS_N[6]		-								38
OCS_N[7]		-								37
PLLFILT	PLL Regulator Filter Capacitor	34						46		62
PRT_DIS_M[1]	Downstream Port Disable Strap Option	-		1						
PRT_DIS_M[2]		-		3						
PRT_DIS_M[3]		-		6						
PRT_DIS_M[4]		-				8		-	8	
PRT_DIS_M[5]		-								11
PRT_DIS_M[6]		-								53
PRT_DIS_M[7]		-								55
PRT_DIS_P[1]	Port Disable	-		2						
PRT_DIS_P[2]		-		4						
PRT_DIS_P[3]		-		7						
PRT_DIS_P[4]		-				9		-	9	
PRT_DIS_P[5]		-								12
PRT_DIS_P[6]		-								54
PRT_DIS_P[7]		-								56

Table 5.1 Pin List in Alphabetical Order (continued)

SYMBOL	NAME	PIN NUMBERS								
		36 QFN						48QFN		64 QFN
		USB2512 USB2512i USB2512A USB2512Ai	USB2512B USB2512Bi	USB2513 USB2513i	USB2513B USB2513Bi	USB2514 USB2514i	USB2514B USB2514Bi	USB2513 USB22513i	USB2514 USB22514i	USB2517 USB2517i
PRTPWR[1]	USB Port Power Enable	12						15		29
PRTPWR[2]		16						19		26
PRTPWR[3]		-		18				21		23
PRTPWR[4]		-				20		-	27	20
PRTPWR[5]		-								30
PRTPWR[6]		-								39
PRTPWR[7]		-								36
PRTPWR_POL	Port Power Polarity Strapping	-						38		-
PRTSWP[1]	Port Swap Strapping Option	-						37		51
PRTSWP[2]		-						25		49
PRTSWP[3]		-						23		47
PRTSWP[4]		-							13	33
PRTSWP[5]		-								31
PRTSWP[6]		-								17
PRTSWP[7]		-								15
RBIAS	USB Transceiver Bias	35						47		63
RESET_N	Reset Input	26						34		43
SCL	Serial Clock	24						31		41
SDA	Serial Data Signal	22						29		40
SEL48	Select 48 MHz Clock Input	-						40		-
SMBCLK	System Management Bus Clock	24						31		41
SMBDATA	Server Message Block Data Signal	22						29		40
SUSP_IND	Active/Suspend Status Indicator	28						39		45
TEST	Test Pin	11						14		19
USBDM_UP	USB Bus Data	30						42		58
USBDP_UP		31						43		59

Table 5.1 Pin List in Alphabetical Order (continued)

SYMBOL	NAME	PIN NUMBERS								
		36 QFN						48QFN		64 QFN
		USB2512 USB2512i USB2512A USB2512Ai	USB2512B USB2512Bi	USB2513 USB2513i	USB2513B USB2513Bi	USB2514 USB2514i	USB2514B USB2514Bi	USB2513 USB22513i	USB2514 USB22514i	USB2517 USB2517i
USBDM_DN[1]	Hi-Speed USB Data	1								
USBDM_DN[2]		3								
USBDM_DN[3]		-	6							
USBDM_DN[4]		-				8		-	8	
USBDM_DN[5]		-								11
USBDM_DN[6]		-								53
USBDM_DN[7]		-								55
USBDP_DN[1]		2								
USBDP_DN[2]		4								
USBDP_DN[3]		-	7							
USBDP_DN[4]		-				9		-	9	
USBDP_DN[5]		-								12
USBDP_DN[6]		-								54
USBDP_DN[7]		-								56
VBUS_DET	Upstream VBUS Power Detection	27						35		44
VDD33	3.3 V Power	5								
VDD33		10								
VDD33		15						18		24
VDD33		23						30		46
VDD33		29						41		52
VDD33		36						48		57
VDD33		-								64
XTALIN	Crystal Input	33						45		61
XTALOUT	Crystal Output	32						44		60

5.2 USB251x Pin Descriptions (Grouped by Function)

Table 5.2 USB251x Pin Descriptions

SYMBOL	BUFFER TYPE	DESCRIPTION
UPSTREAM USB 2.0 INTERFACES		
USBDM_UP USBDP_UP	IO-U	USB Data These pins connect to the upstream USB bus data signals (host, port, or upstream hub).
VBUS_DET	I/O12	Detect Upstream VBUS Power Detects the state of Upstream VBUS power. The SMSC hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor which signals a connect event. When designing a detachable hub, this pin should be connected to VBUS on the upstream port via a 2 to 1 voltage divider. For self-powered applications with a permanently attached host, this pin must be connected to 3.3 V (typically VDD33).
DOWNSTREAM USB 2.0 INTERFACES		
USBDP_DN[x:1]/ PRT_DIS_P[x:1]	IO-U	Hi-Speed USB Data These pins connect to the downstream USB peripheral devices attached to the hub's port. To disable, pull up with a 10 K resistor to 3.3 V.
USBDM_DN[x:1]/ PRT_DIS_M[x:1]		Downstream Port Disable Strap Option If this strap is enabled by package and configuration settings (see Table 8.1, "Hub Configuration Options"), then this pin will be sampled at RESET_N negation to determine if the port is disabled. To disable a port, pull up both PRT_DIS_M[x:1] and PRT_DIS_P[x:1] pins corresponding to the port numbers.
PRTPWR[x:1] /	O12	USB Power Enable Enables power to USB peripheral devices downstream. When PRTPWR_POL pin is unavailable, the hub supports active high power controllers only. When PRTPWR_POL pin is available, the active signal level of the PRTPWR pins is determined by the power polarity strapping function of the PRTPWR_POL pin.
BC_EN[x]	IPD	Battery Charging Strap Option *This feature is only available on USB251xB/Bi. If this strap is enabled by package and configuration settings, (see Table 8.1, "Hub Configuration Options"), this pin will be sampled at RESET_N negation to determine if ports [x:1] support the battery charging protocol (and thus the supporting external port power controllers) that would enable a device to draw the currents per the USB battery charging specification. BC_EN[x] = 1: Battery charging feature is supported for port x BC_EN[x] = 0: Battery charging feature is not supported for port x

Table 5.2 USB251x Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
DOWNSTREAM USB 2.0 INTERFACES (continued)		
LED_A_N[x:1] /	I/O12	Port LED Indicators This pin will be active low when LED support is enabled via EEPROM or SMBus.
PRTSWP[x:1]		Port Swap Strapping Option If this strap is enabled by package and configuration settings (see Table 8.1, "Hub Configuration Options"), this pin will be sampled at RESET_N negation to determine the electrical connection polarity of the downstream USB port pins (USB_DP and USB_DM). Also, the active state of the LED will be determined as follows: ‘0’ = Port polarity is normal, LED is active high. ‘1’ = Port polarity (USB_DP and USB_DM) is swapped, LED is active low.
LED_B_N[7:4]	I/O12	Enhanced Indicator Port LED for ports 4-7 Enhanced indicator LED for ports 4-7. This pin will be active low when LED support is enabled via EEPROM or SMBus.
LED_B_N[3] /	I/O12	Enhanced Indicator Port LED for port 3 This pin will be active low when LED support is enabled via EEPROM or SMBus.
GANG_EN		Ganged Power and Over-current strap option This signal selects between ganged or individual port power and over-current sensing. If this strap is enabled by package and configuration settings (see Table 8.1, "Hub Configuration Options"), this pin will be sampled at RESET_N negation to determine the mode as follows: ‘0’ = Individual sensing and switching, LED_B_N[3] is active high. ‘1’ = Ganged sensing and switching, LED_B_N[3] is active low.

Table 5.2 USB251x Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
DOWNSTREAM USB 2.0 INTERFACES (continued)		
LED_B_N[2:1] / BOOST[1:0]	I/O12	Enhanced Indicator Port LED for ports 1 and 2 Enhanced indicator LED for ports 1 and 2. This pin will be active low when LED support is enabled via EEPROM or SMBus. If this strap option is enabled by package and configuration settings (see Table 8.1, "Hub Configuration Options"), this pin will be sampled at RESET_N negation to determine if all PHY ports (upstream and downstream) operate at a normal or boosted electrical level. Also, the active state of the LEDs will be determined as follows: See Section 8.2.1.27, "Register F6h: Boost_Up," on page 45 and Section 8.2.1.29, "Register F8h: Boost_4:0," on page 46 for more information. BOOST[1:0] = BOOST_IOUT[1:0] BOOST[1:0] = ‘00’, LED_B_N[2] is active high, LED_B_N[1] is active high. BOOST[1:0] = ‘01’, LED_B_N[2] is active high, LED_B_N[1] is active low. BOOST[1:0] = ‘10’, LED_B_N[2] is active low, LED_B_N[1] is active high. BOOST[1:0] = ‘11’, LED_B_N[2] is active low, LED_B_N[1] is active low.
PRTPWR_POL	IPU	Port Power Polarity Strapping Port Power Polarity strapping determination for the active signal polarity of the [x:1]PRTPWR pins. While RESET_N is asserted, the logic state of this pin will (through the use of internal combinatorial logic) determine the active state of the PRTPWR pins in order to ensure that downstream port power is not inadvertently enabled to inactive ports during a hardware reset. When RESET_N is negated, the logic value will be latched internally, and will retain the active signal polarity for the PRTPWR[x:1] pins. ‘1’ = PRTPWR[x:1]_P/N pins have an active ‘high’ polarity ‘0’ = PRTPWR[x:1]_P/N pins have an active ‘low’ polarity **Warning:** Active low port power controllers may glitch the downstream port power when the system power is first applied. Care should be taken when designing with active low components. When PRTPWR_POL is not an available pin on the package, the hub will only support active high power controllers.
OCS_N[x:1]	IPU	Over-Current Sense Input from external current monitor indicating an over-current condition.
RBIAS	I-R	USB Transceiver Bias A 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver’s internal bias settings.

Table 5.2 USB251x Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
SERIAL PORT INTERFACES		
SDA /	I/OSD12	Serial Data signal (SDA)
SMBDATA /		Server Message Block Data signal (SMBDATA)
NON_REM[1]		Non-removable Port Strap Option If this strap is enabled by package and configuration settings (see Table 8.1), this pin will be sampled (in conjunction with LOCAL_PWR / SUSP_IND / NON_REM[0]) at RESET_N negation to determine if ports [7:1] contain permanently attached (non-removable) devices: NON_REM[1:0] = '00', All ports are removable. NON_REM[1:0] = '01', Port 1 is non-removable. NON_REM[1:0] = '10', Ports 1 & 2 are non-removable. NON_REM[1:0] = '11', When available, ports 1 2 & 3 are non-removable.
RESET_N	IS	RESET Input The system can reset the chip by driving this input low. The minimum active low pulse is 1 µs.
SCL /	I/OSD12	Serial Clock (SCL)
SMBCLK /		System Management Bus Clock (SMBCLK)
CFG_SEL[0]		Configuration Select: The logic state of this multifunction pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 8.1, "Hub Configuration Options".
HS_IND /	I/O12	Hi-Speed Upstream Port Indicator HS_IND: Hi-speed Indicator for upstream port connection speed. The active state of the LED will be determined as follows: CFG_SEL[1] = '0', HS_IND is active high, CFG_SEL[1] = '1', HS_IND is active low, 'Asserted' = the hub is connected at HS 'Negated' = the hub is connected at FS
CFG_SEL[1]		Configuration Programming Select CFG_SEL[1]: The logic state of this pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 8.1, "Hub Configuration Options".
CFG_SEL[2]	I	Configuration Programming Select The logic state of this pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 8.1, "Hub Configuration Options". When the CFG_SEL[2] pin is unavailable, then the logic is internally tied to '0'.