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USB251xB/xBi

USB 2.0 Hi-Speed Hub Controller

General Description

The Microchip USB251xB/xBi hub is a family of low-power, configurable, MTT (multi transaction translator) hub controller IC products for embedded USB solutions. The *x* in the part number indicates the number of downstream ports available, while the *B* indicates battery charging support. The Microchip hub supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

Highlights

- High performance, low-power, small footprint hub controller IC with 2, 3, or 4 downstream ports
- Fully compliant with the *USB 2.0 Specification* [1]
- Enhanced OEM configuration options available through either a single serial I^2C EEPROM, or SMBus slave port
- **MultiTRAK**™
  - High-performance multiple transaction translator which provides one transaction translator per port
- **PortMap**
  - Flexible port mapping and disable sequencing
- **PortSwap**
  - Programmable USB differential-pair pin locations ease PCB design by aligning USB signal lines directly to connectors
- **PHYBoost**
  - Programmable USB signal drive strength for recovering signal integrity using 4-level driving strength resolution

Features

- USB251xB/xBi products are fully footprint compatible with USB251x/xi/xA/xAi products as direct drop-in replacements
  - — Cost savings include using the same PCB components and application of USB-IF Compliance by Similarity
- Full power management with individual or ganged power control of each downstream port
- Fully integrated USB termination and pull-up/pull-down resistors
- Supports a single external 3.3 V supply source; internal regulators provide 1.2 V internal core voltage
- Onboard 24 MHz crystal driver or external 24 MHz clock input
- Customizable vendor ID, product ID, and device ID
- 4 kilovolts of HBM JESD22-A114F ESD protection (powered and unpowered)
- Supports self- or bus-powered operation
- Supports the USB Battery Charging specification Rev. 1.1 for Charging Downstream Ports (CDP)
- The USB251xB/xBi offers the following packages:
  - 36-pin SQFN (6x6 mm) (Preferred)
  - 36-pin QFN (6x6 mm) (Legacy)
- USB251xBi products support the industrial temperature range of -40ºC to +85ºC
- USB251xB products support the extended commercial temperature range of 0ºC to +85ºC

Applications

- LCD monitors and TVs
- Multi-function USB peripherals
- PC motherboards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems

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Table of Contents

1.0 INTRODUCTION

The Microchip USB251xB/xBi hub family is a group of low-power, configurable, MTT (multi transaction translator) hub controller ICs. The hub provides downstream ports for embedded USB solutions and is fully compliant with the *USB 2.0 Specification* [1]. Each of the hub controllers can attach to an upstream port as a full-speed or full-/hi-speed hub. The hub can support low-speed, full-speed, and hi-speed downstream devices when operating as a hi-speed hub.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors and all required pull-down and pull-up resistors on D+ and D- pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB251xB/xBi hub family includes programmable features, such as:

- **MultiTRAK™ Technology**: implements a dedicated Transaction Translator (TT) for each port. Dedicated TTs help maintain consistent full-speed data throughput regardless of the number of active downstream connections.
- **PortMap**: provides flexible port mapping and disable sequences. The downstream ports of a USB251xB/xBi hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB251xB/xBi hub controller automatically reorders the remaining ports to match the USB host controller's port numbering scheme.
- **PortSwap**: allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.
- **PHYBoost**: enables 4 programmable levels of USB signal drive strength in downstream port transceivers. PHY-Boost will also attempt to restore USB signal integrity.

1.1 Configurable Features

The USB251xB/xBi hub controller provides a default configuration that may be sufficient for most applications. Strapping option pins (see Section 3.3.1 on page 14) provide additional features to enhance the default configuration. When the hub is initialized in the default configuration, the following features may be configured using the strapping options:

- Downstream non-removable ports, where the hub will automatically report as a compound device
- Downstream disabled ports
- Enabling of battery charging option on individual ports
- The USB251xB/xBi hub controllers can alternatively be configured by an external I^2C EEPROM or a microcontroller as an SMBus slave device. When the hub is configured by an I^2C EEPROM or over SMBus, the following configurable features are provided:
- Support for compound devices on a port-by-port basis
- Selectable over-current sensing and port power control on an individual or ganged basis to match the circuit board component selection
- Customizable vendor ID, product ID, and device ID
- Configurable USB signal drive strength
- Configurable USB differential pair pin location
- Configurable delay time for filtering the over-current sense inputs
- Configurable downstream port power-on time reported to the host
- Indication of the maximum current that the hub consumes from the USB upstream port
- Indication of the maximum current required for the hub controller
- Custom string descriptors (up to 31 characters):
  - Product
  - Manufacturer
  - Serial number
- Battery charging USB251xB/xBi products are fully footprint compatible with USB251x/xi/xA/xAi products:
  - Pin-compatible
  - Direct drop-in replacement
  - Use the same PCB components
  - USB-IF Compliance by Similarity for ease of use and a complete cost reduction solution
  - Product IDs, device IDs, and other register defaults may differ. See Section 5.1 on page 19 for details.

TABLE 1-1: SUMMARY OF COMPATIBILITIES BETWEEN USB251XB/XBI AND USB251X/XI/XA/XAI PRODUCTS

Part Number	Drop-in Replacement
USB2512	USB2512B
USB2512i	USB2512Bi
USB2512A	USB2512B
USB2512Ai	USB2512Bi
USB2513	USB2513B
USB2513i	USB2513Bi
USB2514	USB2514B
USB2514i	USB2514Bi

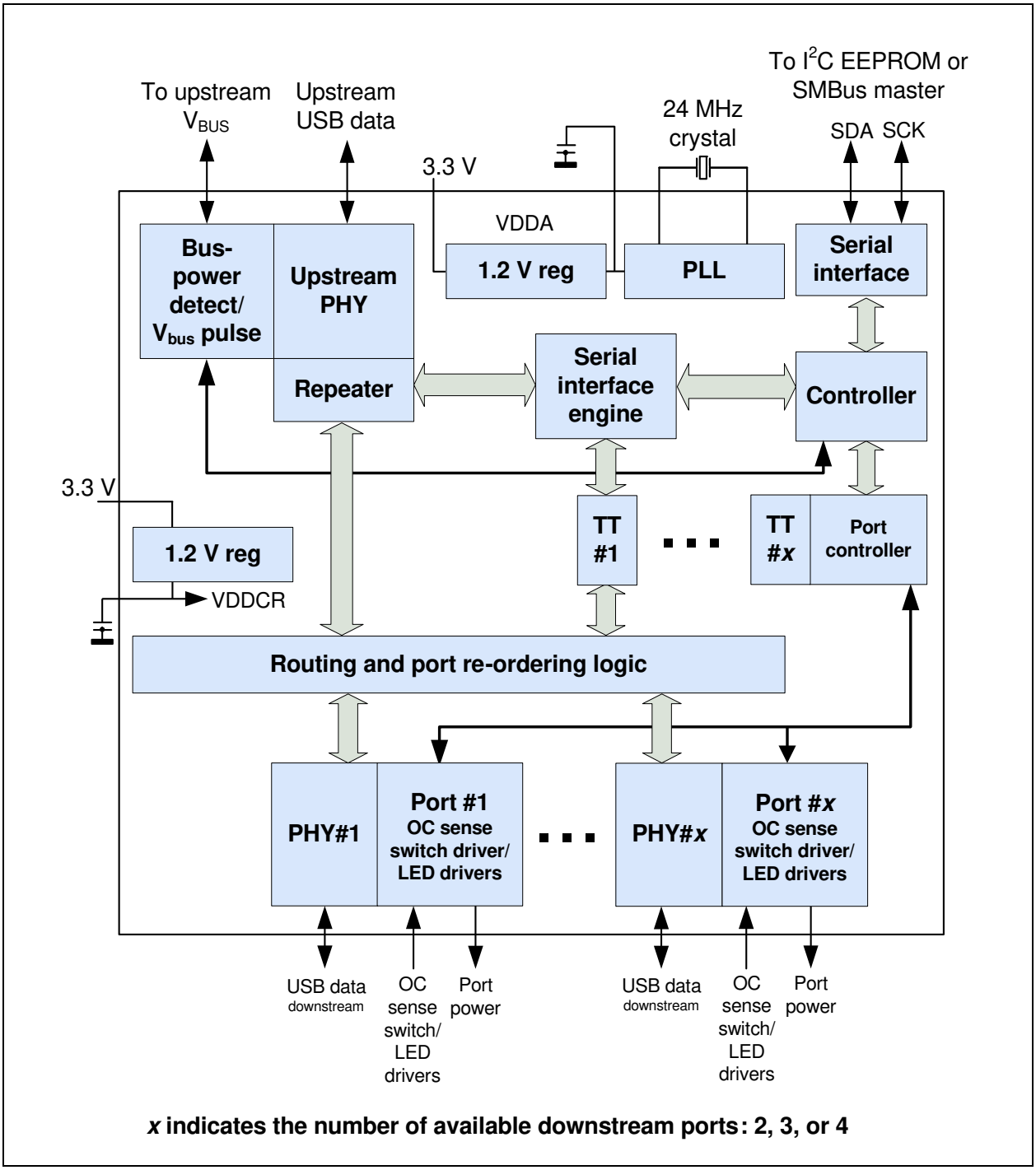
Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x…y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
`code`	Instruction code, or API function or parameter
Section Name	Section or Document name
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

2.0 BLOCK DIAGRAM

FIGURE 2-1: USB251XB/XBI HUB FAMILY BLOCK DIAGRAM



***x* indicates the number of available downstream ports: 2, 3, or 4**

3.0 PIN INFORMATION

This chapter outlines the pinning configurations for each package type available, followed by a corresponding pin list organized alphabetically. The detailed pin descriptions are listed then outlined by function in Section 3.3, "Pin Descriptions (Grouped by Function)," on page 12.

3.1 Pin Configurations

The following figures detail the pinouts of the various USB251xB/xBi versions.

FIGURE 3-1: USB2512B PIN DIAGRAM

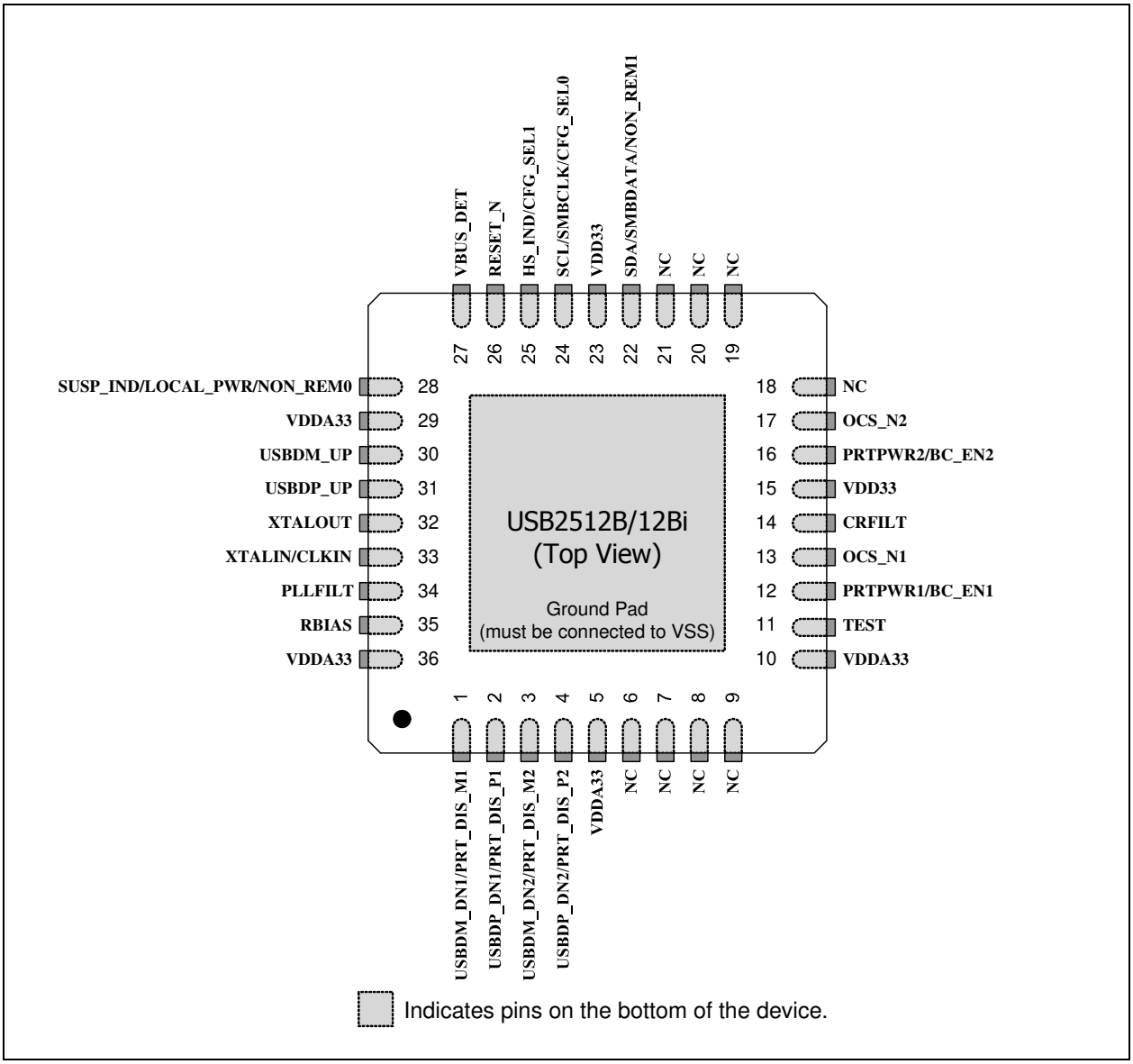


FIGURE 3-2: USB2513B PIN DIAGRAM

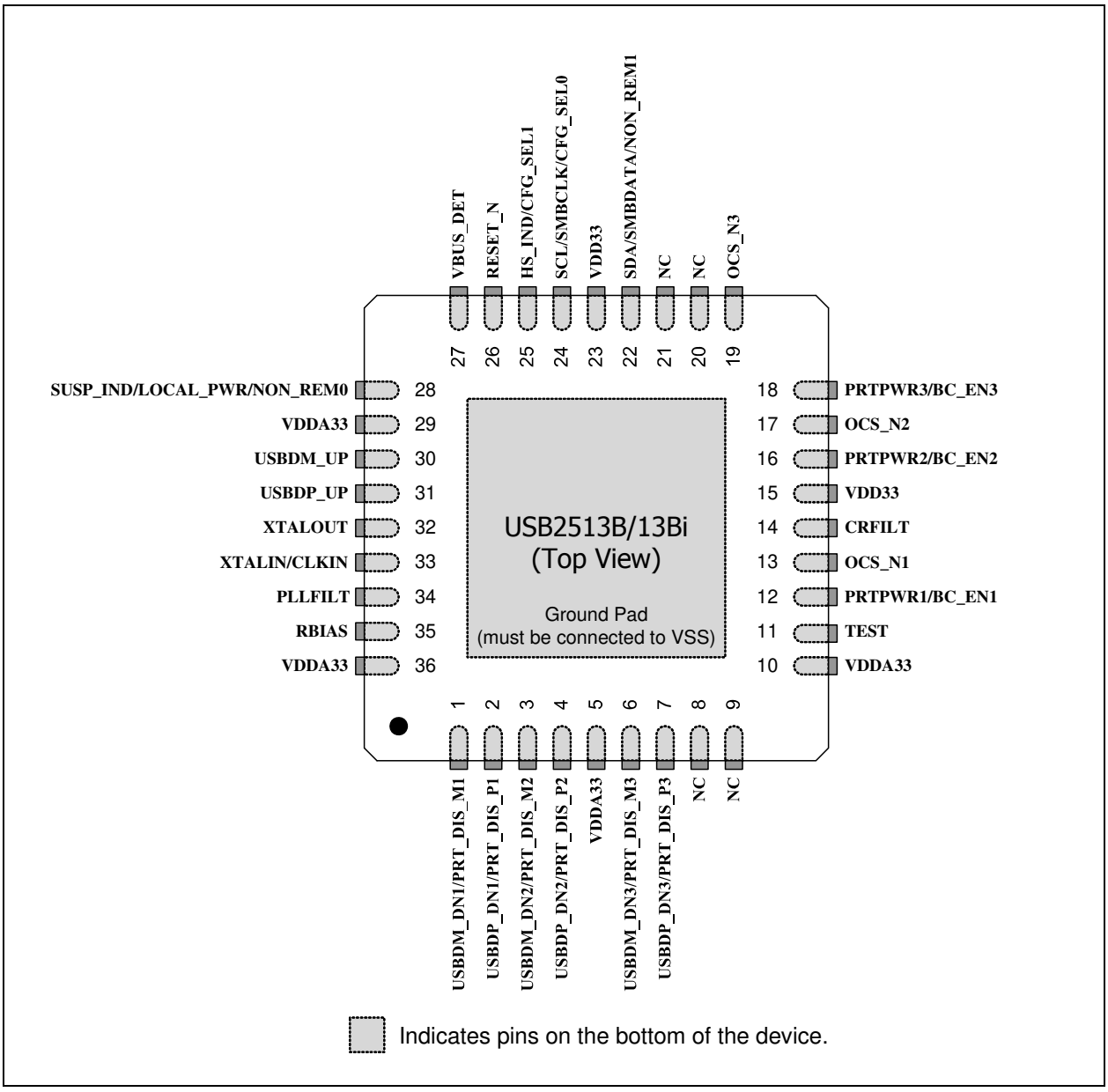
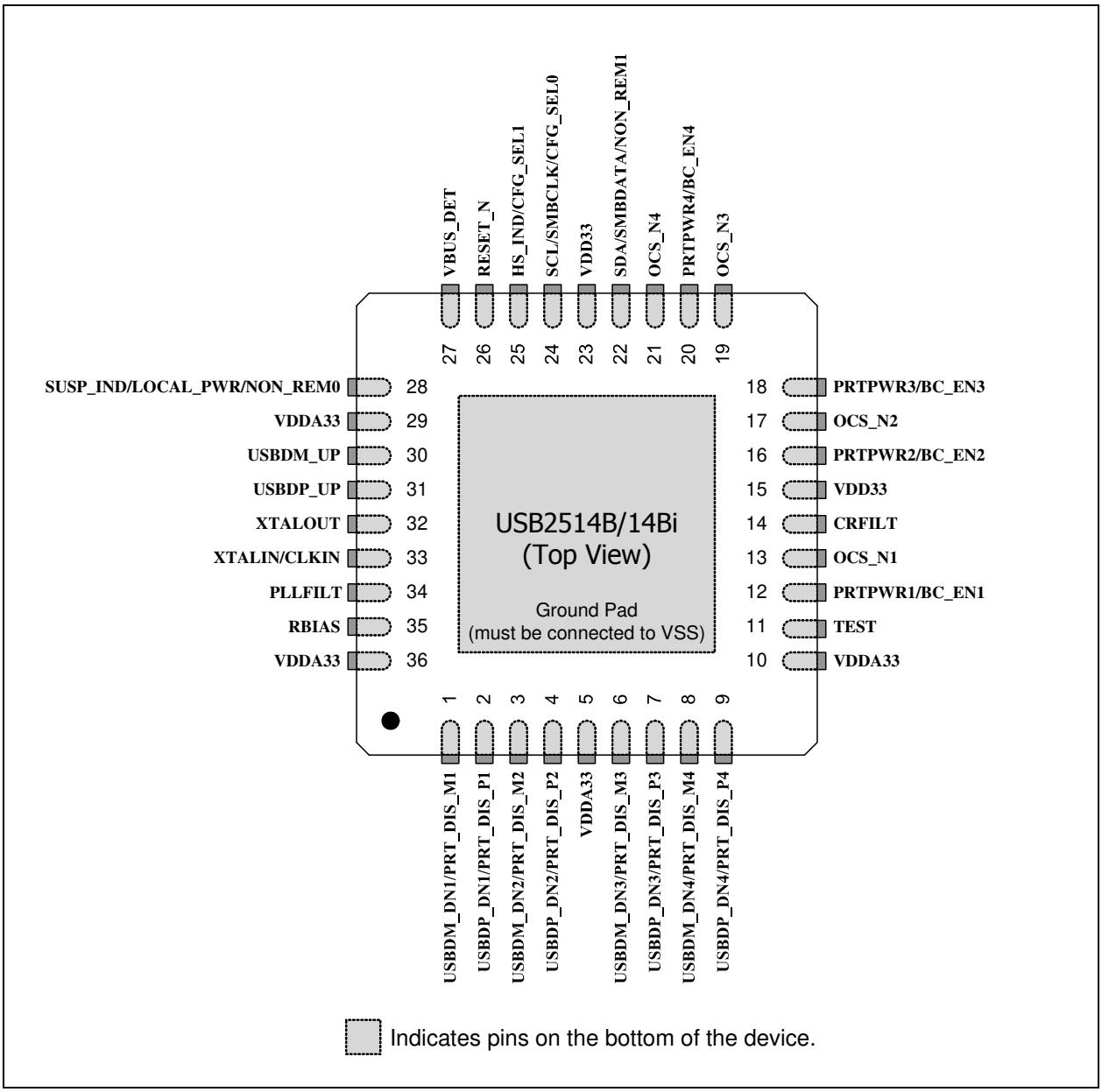


FIGURE 3-3: USB2514B PIN DIAGRAM



3.2 Pin List (Alphabetical)

TABLE 3-1: USB251XB/XBI PIN LIST (ALPHABETICAL)

Symbol	Name	Pin Numbers		
		USB2512B USB2512Bi	USB2513B USB2513Bi	USB2514B USB2514Bi
BC_EN1	Battery Charging Strap Option	12		
BC_EN2		16		
BC_EN3		-	18	
BC_EN4		-		20
CFG_SEL0	Configuration Programming Selection	24		
CFG_SEL1		25		
CLKIN	External Clock Input	33		
CRFILT	Core Regulator Filter Capacitor	14		
Ground Pad (VSS)	Exposed Pad Tied to Ground (VSS)	ePad		
HS_IND	Hi-Speed Upstream Port Indicator	25		
LOCAL_PWR	Local Power Detection	28		
NC	No Connect	6	-	
NC		7	-	
NC		18	-	
NC		19	-	
NC		8		-
NC		9		-
NC		20		-
NC		21		-
NON_REM0	Non-Removable Port Strap Option	28		
NON_REM1		22		
OCS_N1	Over-Current Sense	13		
OCS_N2		17		
OCS_N3		-	19	
OCS_N4		-		21
PLLFILT	PLL Regulator Filter Capacitor	34		
PRT_DIS_M1	Downstream Port Disable Strap Option	1		
PRT_DIS_M2		3		
PRT_DIS_M3		-	6	
PRT_DIS_M4		-		8
PRT_DIS_P1	Port Disable	2		
PRT_DIS_P2		4		
PRT_DIS_P3		-	7	
PRT_DIS_P4		-		9

TABLE 3-1: USB251XB/XBI PIN LIST (ALPHABETICAL) (CONTINUED)

Symbol	Name	Pin Numbers		
		USB2512B USB2512Bi	USB2513B USB2513Bi	USB2514B USB2514Bi
PRTPWR1	USB Port Power Enable	12		
PRTPWR2		16		
PRTPWR3		-	18	
PRTPWR4		-		20
RBIAS	USB Transceiver Bias	35		
RESET_N	Reset Input	26		
SCL	Serial Clock	24		
SDA	Serial Data Signal	22		
SMBCLK	System Management Bus Clock	24		
SMBDATA	System Management Bus Data Signal	22		
SUSP_IND	Active/Suspend Status Indicator	28		
TEST	Test Pin	11		
USBDM_UP	USB Bus Data	30		
USBDP_UP		31		
USBDM_DN1	Hi-Speed USB Data	1		
USBDM_DN2		3		
USBDM_DN3		-	6	
USBDM_DN4		-		8
USBDP_DN1		2		
USBDP_DN2		4		
USBDP_DN3		-	7	
USBDP_DN4		-		9
VBUS_DET	Upstream VBUS Power Detection	27		
VDD33	3.3 V Digital Power	15		
VDD33		23		
VDDA33	3.3 V Analog Power	5		
VDDA33		10		
VDDA33		29		
VDDA33		36		
XTALIN	Crystal Input	33		
XTALOUT	Crystal Output	32		

3.3 Pin Descriptions (Grouped by Function)

An *N* at the end of a signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *N* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

TABLE 3-2: USB251XB/XBI PIN DESCRIPTIONS

Symbol	Buffer Type	Description
UPSTREAM USB 2.0 INTERFACES		
USBDM_UP **USBDP_UP**	IO-U	USB Data: connect to the upstream USB bus data signals (host, port, or upstream hub).
VBUS_DET	I	Detect Upstream VBUS Power: detects the state of the upstream VBUS power. The hub monitors **VBUS_DET** to determine when to assert the internal D+ pull-up resistor: (signaling a connect event). When designing a detachable hub, this pin should be connected to VBUS on the upstream port via a 2:1 voltage divider. Two 100 kΩ resistors are suggested. For self-powered applications with a permanently attached host, this pin must be connected to a dedicated host control output, or connected to the 3.3 V domain that powers the host (typically **VDD33**).
DOWNSTREAM USB 2.0 INTERFACES		
USBDP_DN[x:1]/PRT_DIS_P[x:1]	IO-U	Hi-Speed USB Data: connect to the downstream USB peripheral devices attached to the hub's port. To disable, use a 10 kΩ pull-up resistor to 3.3 V.
USBDM_DN[x:1]/PRT_DIS_M[x:1]		Downstream Port Disable Strap Option: when enabled by package and configuration settings (see Table 5-1 on page 19), this pin is sampled at **RESET_N** negation to determine if the port is disabled. To disable a port, pull up both **PRT_DIS_M[x:1]** and **PRT_DIS_P[x:1]** pins for the corresponding port number(s). See Section 3.3.1, on page 14 for pull up details.
PRTPWR[x:1]/	O12	USB Power Enable: enables power to USB peripheral devices downstream.
BC_EN[x:1]	IPD	Battery Charging Strap Option: when enabled by package and configuration settings (see Table 5-1), the pin will be sampled at **RESET_N** negation to determine if ports [x:1] support the battery charging protocol. When supporting the battery charging protocol, the hub also supports external port power controllers. The battery charging protocol enables a device to draw the currents per the USB battery charging specification. See Section 3.3.1, on page 14 for strap pin details. 1 : Battery charging feature is supported for port *x* 0 : Battery charging feature is not supported for port *x*
OCS_N[x:1]	IPU	Over-Current Sense: input from external current monitor indicating an over-current condition.
RBIAS	I-R	USB Transceiver Bias: a 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.

TABLE 3-2: USB251XB/XBI PIN DESCRIPTIONS (CONTINUED)

Symbol	Buffer Type	Description
SERIAL PORT INTERFACES		
SDA/	I/OSD12	Serial Data Signal
SMBDATA/		System Management Bus Signal
NON_REM1		Non-Removable Port 1 Strap Option: when enabled by package and configuration options (see Table 5-1 on page 19), this pin will be sampled (in conjunction with **LOCAL_PWR/SUSP_IND/NON_REM0**) at **RESET_N** negation to determine if ports [x:1] contain permanently attached (non-removable) devices: **NON_REM[1:0]** = `00` : all ports are removable **NON_REM[1:0]** = `01` : port 1 is non-removable **NON_REM[1:0]** = `10` : ports 1 and 2 are non-removable **NON_REM[1:0]** = `11` : when available, ports 1, 2, and 3 are non-removable When **NON_REM[1:0]** is chosen such that there is a non-removable device, the hub will automatically report itself as a compound device (using the proper descriptors).
RESET_N	IS	RESET Input: the system can reset the chip by driving this input low. The minimum active low pulse is 1 µs.
SCL/	I/OSD12	Serial Clock (SCL)
SMBCLK/		System Management Bus Clock
CFG_SEL0		Configuration Select: the logic state of this multifunction pin is internally latched on the rising edge of **RESET_N** (**RESET_N** negation), and will determine the hub configuration method as described in Table 5-1.
HS_IND/	I/O12	Hi-Speed Upstream Port Indicator: upstream port connection speed. Asserted = the hub is connected at HS Negated = the hub is connected at FS **Note:** When implementing an external LED on this pin, the active state is indicated above and outlined in Section 3.3.1.3, on page 15.
CFG_SEL1		Configuration Programming Select 1: the logic state of this pin is internally latched on the rising edge of **RESET_N** (**RESET_N** negation), and will determine the hub configuration method as described in Table 5-1.
MISC		
XTALIN	ICLKx	Crystal Input: 24 MHz crystal. This pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.
CLKIN		External Clock Input: this pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.
XTALOUT	OCLKx	Crystal Output: this is the other terminal of the crystal circuit with 1.2 V p-p output and a weak (< 1mA) driving strength. When an external clock source is used to drive **XTALIN/CLKIN**, leave this pin unconnected, or use with appropriate caution.

TABLE 3-2: USB251XB/XBI PIN DESCRIPTIONS (CONTINUED)

Symbol	Buffer Type	Description
SUSP_IND/	I/O	Active/Suspend Status LED: indicates USB state of the hub. Negated = unconfigured; or configured and in USB suspend Asserted = hub is configured and is active (i.e., not in suspend)
LOCAL_PWR/		Local Power: detects availability of local self-power source. Low = self/local power source is NOT available (i.e., the hub gets all power from the upstream USB VBus) High = self/local power source is available
NON_REM0		Non-Removable 0 Strap Option: when enabled by package and configuration settings (see Table 5-1 on page 19), this pin will be sampled (in conjunction with **NON_REM[1]**) at **RESET_N** negation to determine if ports [x:1] contain permanently attached (non-removable) devices: **Note:** When implementing an external LED on this pin, the active state is outlined below and detailed in Section 3.3.1.3, on page 15. **NON_REM[1:0]** = `00` : all ports are removable; LED is active high **NON_REM[1:0]** = `01` : port 1 is non-removable; LED is active low **NON_REM[1:0]** = `10` : ports 1 and 2 are non-removable; LED is active high **NON_REM[1:0]** = `11` : (when available) ports 1, 2, and 3 are non-removable; LED is active low
TEST	IPD	Test Pin: treat as a no connect pin or connect to ground. No trace or signal should be routed or attached to this pin.
POWER, GROUND, and NO CONNECTS		
CRFILT		VDD Core Regulator Filter Capacitor: this pin can have up to a 0.1 µF low-ESR capacitor to VSS, or be left unconnected.
VDD33		3.3 V Power
VDDA33		3.3 V Analog Power
PLLFILT		PLL Regulator Filter Capacitor: this pin can have up to a 0.1 µF low-ESR capacitor to VSS, or be left unconnected.
VSS		Ground Pad/ePad: the package slug is the only VSS for the device and must be tied to ground with multiple vias.
NC		No Connect: no signal or trace should be routed or attached to all NC pins.

3.3.1 CONFIGURING THE STRAP PINS

If a pin's strap function is enabled thru the hub configuration selection, (Table 5-1, “Initial Interface/Configuration Options,” on page 19) the strap pins must be pulled either high or low using the values provided in Table 3-3. Each strap option is dependent on the pin’s buffer type, as outlined in the sections that follow.

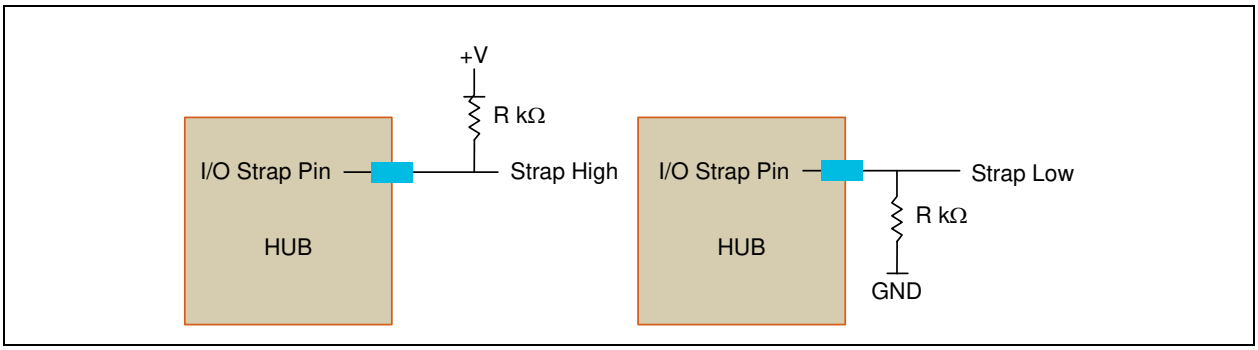
TABLE 3-3: STRAP OPTION SUMMARY

Strap Option	Resistor Value	Buffer Type	Notes
Non-Removable	47 - 100 kΩ	I/O	
Internal Pull-Down	10 kΩ	IPD	• Only applicable to port power pins • Contains a built-in resistor
LED	47 - 100 kΩ	I/O	

3.3.1.1 Non-Removable

If a strap pin's buffer type is I/O, an external pull-up or pull-down must be implemented as shown in Figure 3-4. Use Strap High to set the strap option to 1 and Stap Low to set the strap option to 0. When implementing the Strap Low option, no additional components are needed (i.e., the internal pull-down provides the resistor).

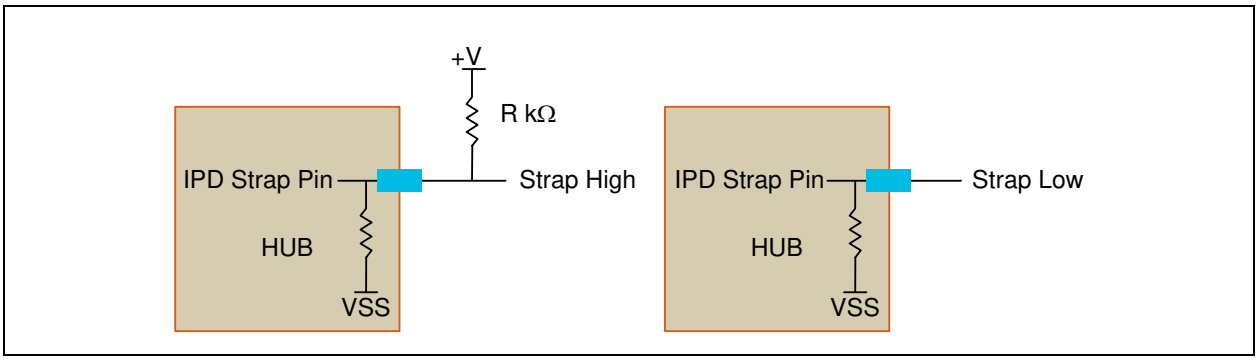
FIGURE 3-4: NON-REMOVABLE PIN STRAP EXAMPLE



3.3.1.2 Internal Pull-Down (IPD)

If a strap pin's buffer type is IPD (pins **BC_EN[x:1]**), one of the two hardware configurations outlined below must be implemented. Use the Strap High configuration to set the strap option value to 1 and Strap Low to set the strap option value to 0.

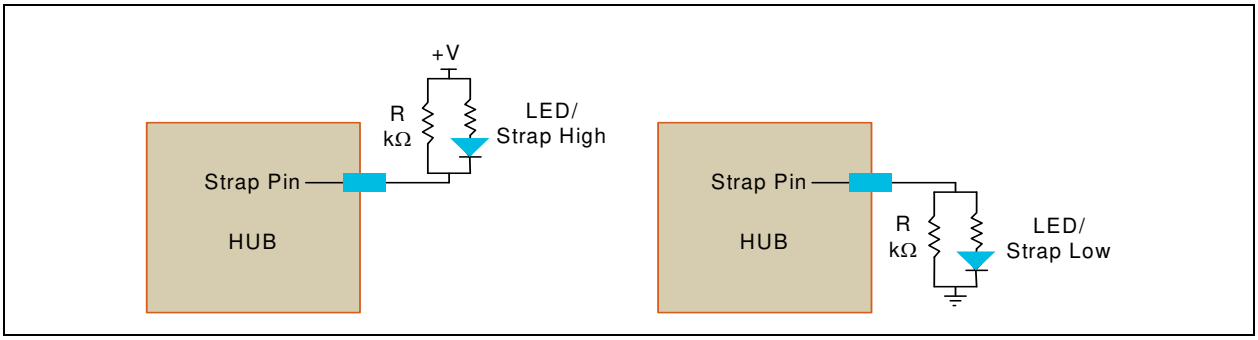
FIGURE 3-5: PIN STRAP OPTION WITH IPD PIN EXAMPLE



3.3.1.3 LED

If a strap pin's buffer type is I/O and shares functionality with an LED, the hardware configuration outlined below must be implemented. The internal logic will drive the LED appropriately (active high or low) depending on the sampled strap option. Use the Strap High configuration to set the strap option value to 1 and Strap Low to set the strap option to 0.

FIGURE 3-6: LED PIN STRAP EXAMPLE



3.4 Buffer Type Descriptions

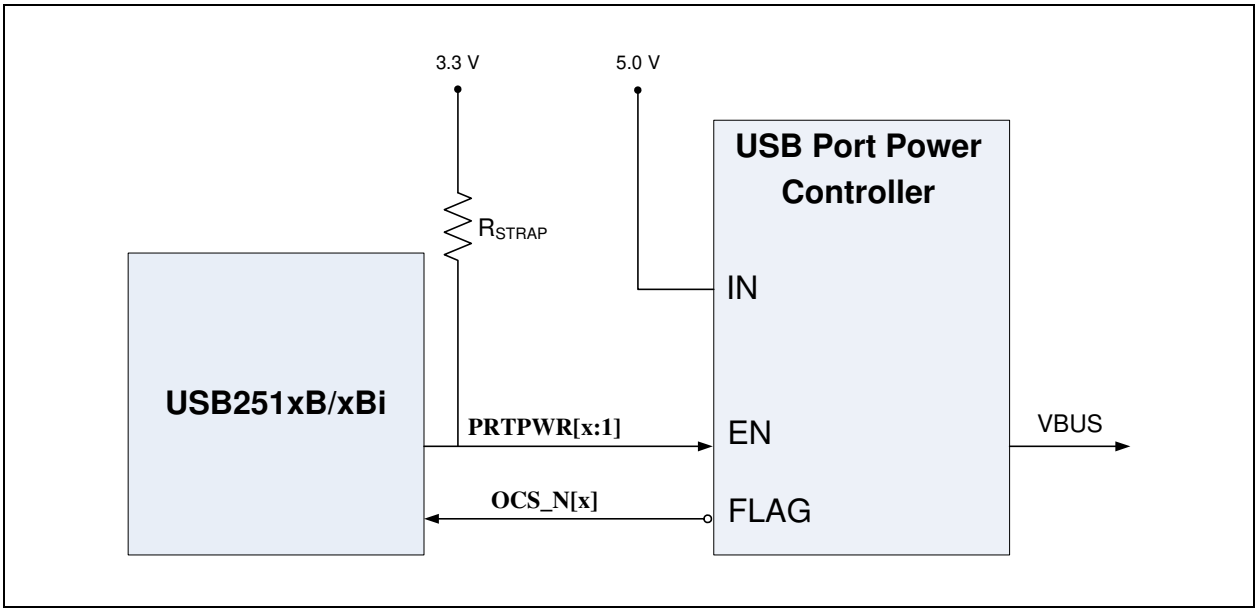
TABLE 3-4: BUFFER TYPE DESCRIPTIONS

Buffer Type	Description
I	Input
I/O	Input/output
IPD	Input with internal weak pull-down resistor
IPU	Input with internal weak pull-up resistor
IS	Input with Schmitt trigger
O12	Output 12 mA
I/O12	Input/output buffer with 12 mA sink and 12 mA source
I/OSD12	Open drain with Schmitt trigger and 12 mA sink. Meets the I^2C-Bus Specification [2] requirements.
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I-R	RBIAS
I/O-U	Analog input/output defined in USB specification

4.0 BATTERY CHARGING SUPPORT

The USB251xB/xBi hub provides support for battery charging devices on a per port basis in compliance with the *USB Battery Charging Specification, Revision 1.1*. The hub can be configured to individually enable each downstream port for battery charging support either via pin strapping as illustrated in Figure 4-1 or by setting the corresponding configuration bits via I^2C EEPROM or SMBus (Section 5.1 on page 19).

FIGURE 4-1: BATTERY CHARGING VIA EXTERNAL POWER SUPPLY



Note: R_{STRAP} enables battery charging.

4.1 USB Battery Charging

A downstream port enabled for battery charging turns on port power as soon as the power on reset and hardware configuration process has completed. The hub does not need to be enumerated nor does **VBUS_DET** need to be asserted for the port power to be enabled. These conditions allow battery charging in S3, S4, and S5 system power states as well as in the fully operational state. The *USB Battery Charging Specification* does not interfere with standard USB operation, which allows a device to perform battery charging at any time.

A port that supports battery charging must be able to support 1.5 amps of current on VBUS. Standard USB port power controllers typically only allow for 0.8 amps of current before detecting an over-current condition. Therefore, the 5 volt power supply, port power controller, or over-current protection devices must be chosen to handle the larger current demand compared to standard USB hub designs.

4.1.1 SPECIAL BEHAVIOR OF PRTPWR PINS

The USB251xB/xBi enables VBUS by asserting the port power (**PRTPWR**) as soon as the hardware configuration process has completed. If the port detects an over-current condition, **PRTPWR** will be turned off to protect the circuitry from overloading. If an over-current condition is detected when the hub is not enumerated, **PRTPWR** can only be turned on from the host or if **RESET_N** is toggled. These behaviors provide battery charging even when the hub is not enumerated and protect the hub from sustained short circuit conditions. If the short circuit condition persists when the hub is plugged into a host system the user is notified that a port has an over-current condition. Otherwise **PRTPWR** turned on by the host system and the ports operate normally.

4.2 Battery Charging Configuration

The battery charging option can be configured in one of two ways:

- When the hub is brought up in the default configuration with strapping options enabled, with the **PRTPWR[x:1]/BC_EN[x:1]** pins configured. See the following sections for details:
  - Section 3.3, "Pin Descriptions (Grouped by Function)," on page 12
  - Section 3.3.1.2, "Internal Pull-Down (IPD)," on page 15
- When the hub is initialized for configuration over I^2C EEPROM or SMBus. Either of these interfaces can be used to configure the battery charging option.

4.2.1 BATTERY CHARGING ENABLED VIA I^2C EEPROM OR SMBUS

Register memory map location 0xD0 is allocated for battery charging support. The Battery Charging register at location 0xD0 starting from bit 1 enables battery charging for each downstream port when asserted. Bit 1 represents port 1, bit 2 represents port 2, etc. Each port with battery charging enabled asserts the corresponding **PRTPWR[x:1]** pin.

5.0 INITIAL INTERFACE/CONFIGURATION OPTIONS

The hub must be configured in order to correctly function when attached to a USB host controller. The hub can be configured either internally or externally by setting the **CFG_SEL[1:0]** pins (immediately after **RESET_N** negation) as outlined in the table below.

Note:	See Chapter 11 (Hub Specification) of the USB specification for general details regarding hub operation and functionality.

To configure the hub externally, there are two principal ways to interface to the hub: over SMBus or I²C EEPROM. The hub can be configured internally, where several default configurations are available as described in the table below. When configured internally, additional configuration is available using the strap options (listed in Section 3.3.1 on page 14).

Note:	Strap options are not available when configuring the hub over I²C or SMBus.

TABLE 5-1: INITIAL INTERFACE/CONFIGURATION OPTIONS

CFG_SEL[1]	CFG_SEL[0]	Description
0	0	Default configuration: • Strap options enabled • Self-powered operation enabled • Individual power switching • Individual over-current sensing
0	1	The hub is configured externally over SMBus (as an SMBus slave device): • Strap options disabled • All registers configured over SMBus
1	0	Default configuration with the following overrides: • Bus-powered operation
1	1	The hub is configured over 2-wire I²C EEPROM: • Strap options disabled • All registers configured by I²C EEPROM

5.1 Internal Register Set (Common to I²C EEPROM and SMBus)

The register set available when configuring the hub to interface over I²C or SMBus is outlined in the table below. Each register has R/W capability, where EEPROM reset values are 0x00. Reserved registers should be written to 0 unless otherwise specified. Contents read from unavailable registers should be ignored.

Address	Register Name	Default ROM Values (Hexidecimal)		
		USB2512B/12Bi	USB2513B/13Bi	USB2514B/14Bi
00h	Vendor ID LSB	24		
01h	Vendor ID MSB	04		
02h	Product ID LSB	12	13	14
03h	Product ID MSB	25		
04h	Device ID LSB	B3		
05h	Device ID MSB	0B		

Address	Register Name	Default ROM Values (Hexidecimal)		
		USB2512B/12Bi	USB2513B/13Bi	USB2514B/14Bi
06h	Configuration Data Byte 1	9B		
07h	Configuration Data Byte 2	20		
08h	Configuration Data Byte 3	02		
09h	Non-Removable Devices	00		
0Ah	Port Disable (Self)	00		
0Bh	Port Disable (Bus)	00		
0Ch	Max Power (Self)	01		
0Dh	Max Power (Bus)	32		
0Eh	Hub Controller Max Current (Self)	01		
0Fh	Hub Controller Max Current (Bus)	32		
10h	Power-on Time	32		
11h	Language ID High	00		
12h	Language ID Low	00		
13h	Manufacturer String Length	00		
14h	Product String Length	00		
15h	Serial String Length	00		
16h-53h	Manufacturer String	00		
54h-91h	Product String	00		
92h-CFh	Serial String	00		
D0h	Battery Charging Enable	00		
E0h	rsvd	00		
F5h	rsvd	00		
F6h	Boost_Up	00		
F7h	rsvd	00		
F8h	Boost_x:0	00		
F9h	rsvd	00		
FAh	Port Swap	00		
FBh	Port Map 12	00		
FCh	Port Map 34	-	00	
FD-FEh	rsvd	00		
FFh	Status/Command Note: SMBus register only	00		

5.1.1 REGISTER 00H: VENDOR ID (LSB)

Bit Number	Bit Name	Description
7:0	VID_LSB	Least Significant Byte of the Vendor ID: a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). Set this field using either the SMBus or I2C EEPROM interface options.

5.1.2 REGISTER 01H: VENDOR ID (MSB)

Bit Number	Bit Name	Description
7:0	VID_MSB	Most Significant Byte of the Vendor ID: a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). Set this field using either the SMBus or I2C EEPROM interface options.

5.1.3 REGISTER 02H: PRODUCT ID (LSB)

Bit Number	Bit Name	Description
7:0	PID_LSB	Least Significant Byte of the Product ID: a 16-bit value that uniquely identifies the Product ID of the user device. Set this field using either the SMBus or I2C EEPROM interface options.

5.1.4 REGISTER 03H: PRODUCT ID (MSB)

Bit Number	Bit Name	Description
7:0	PID_MSB	Most Significant Byte of the Product ID: a 16-bit value that uniquely identifies the Product ID of the user device. Set this field using either the SMBus or I2C EEPROM interface options.

5.1.5 REGISTER 04H: DEVICE ID (LSB)

Bit Number	Bit Name	Description
7:0	DID_LSB	Least Significant Byte of the Device ID: a 16-bit device release number in BCD format (assigned by OEM). Set this field using either the SMBus or I2C EEPROM interface options.

5.1.6 REGISTER 05H: DEVICE ID (MSB)

Bit Number	Bit Name	Description
7:0	DID_MSB	Most Significant Byte of the Device ID: a 16-bit device release number in BCD format (assigned by OEM). Set this field using either the SMBus or I2C EEPROM interface options.

5.1.7 REGISTER 06H: CONFIG_BYTE_1

Bit Number	Bit Name	Description
7	SELF_BUS_PWR	Self or Bus Power: selects between self- and bus-powered operation. The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a bus-powered device, the hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered hub, along with all associated hub circuitry, any embedded devices (if part of a compound device), and all externally available downstream ports (max 100 mA) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent and must not violate the *USB 2.0 Specification* [1]. When configured as a self-powered device, < 1 mA of upstream VBUS current is consumed and all ports are available. Each port is capable of sourcing 500 mA of current. This field is set over either the SMBus or I^2C EEPROM interface options. 0 : bus-powered operation 1 : self-powered operation If dynamic power switching is enabled (Section 5.1.8), this bit is ignored and **LOCAL_PWR** is used to determine if the hub is operating from self or bus power.
6	rsvd	
5	HS_DISABLE	Hi-Speed Disable: disables the capability to attach as either a hi- or full-speed device, forcing full-speed attachment only (i.e., no hi-speed support). 0 : hi-/full-speed 1 : full-speed only (hi-speed disabled)
4	MTT_ENABLE	Multi-TT Enable: enables one transaction translator per port operation. Selects between a mode where only one transaction translator is available for all ports (single-TT), or each port gets a dedicated transaction translator (multi-TT). 0 : single TT for all ports 1 : multi-TT (one TT per port)
3	EOP_DISABLE	EOP Disable: disables End Of Packet (EOP) generation at End Of Frame Time #1 (EOF1) when in full-speed mode. During full-speed operation only, the hub can send EOP when no downstream traffic is detected at EOF1. See the *USB 2.0 Specification, Section 11.3.1* for details. 0 : EOP generation is normal 1 : EOP generation is disabled
2:1	CURRENT_SNS	Over-Current Sense: selects current sensing on all ports (ganged); a port-by-port basis (individual); or none (for bus-powered hubs only). The ability to support current sensing on a ganged or port-by-port basis is hardware implementation dependent. 00 : ganged sensing 01 : individual sensing 1x : over-current sensing not supported (use with bus-powered configurations)
0	PORT_PWR	Port Power Switching: enables power switching on all ports (ganged) or a port-by-port basis (individual). The ability to support power enabling on a ganged or port-by-port basis is hardware implementation dependent. 0 : ganged switching 1 : individual switching

5.1.8 REGISTER 07H: CONFIGURATION DATA BYTE 2

Bit Number	Bit Name	Description
7	DYNAMIC	Dynamic Power Enable: controls the ability of the hub to automatically change from self-powered to bus-powered operation if the local power source is removed or unavailable. It can also go from bus-powered to self-powered operation if the local power source is restored. When dynamic power switching is enabled, the hub detects the availability of a local power source by monitoring **LOCAL_PWR**. If the hub detects a change in power source availability, the hub immediately disconnects and removes power from all downstream devices. It also disconnects the upstream port. The hub will then re-attach to the upstream port as either a bus-powered hub (if local power is unavailable) or a self-powered hub (if local power is available). 0 : no dynamic auto-switching 1 : dynamic auto-switching capable
6	rsvd	
5:4	OC_TIMER	Over Current Timer Delay: 00 : 0.1 ms 01 : 4.0 ms 10 : 8.0 ms 11 : 16.0 ms
3	COMPOUND	Compound Device: indicates the hub is part of a compound device (see the *USB Specification* for definition). The applicable port(s) must also be defined as having a non-removable device. **Note:** When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. 0 : no 1 : yes, the hub is part of a compound device
2:0	rsvd	

5.1.9 REGISTER 08H: CONFIGURATION DATA BYTE 3

Bit Number	Bit Name	Description
7:4	rsvd	
3	PRTMAP_EN	Port Mapping Enable: selects the method used by the hub to assign port numbers and disable ports. 0 : standard mode 1 : port mapping mode
2:1	rsvd	
0	STRING_EN	Enables String Descriptor Support 0 : string support disabled 1 : string support enabled

5.1.10 REGISTER 09H: NON-REMOVABLE DEVICE

Bit Number	Bit Name	Description
7:0	NR_DEVICE	Non-Removable Device: indicates which port has a non-removable device. 0 : port is removable 1 : port is non-removable Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : rsvd **Note:** The device must provide its own descriptor data. When using the default configuration, the **NON_REM[1:0]** pins will designate the appropriate ports as being non-removable.

5.1.11 REGISTER 0AH: PORT DISABLE FOR SELF-POWERED OPERATION

Bit Number	Bit Name	Description
7:0	PORT_DIS_SP	Port Disable Self-Powered: disables one or more ports. 0 = port is available 1 = port is disabled Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : rsvd During self-powered operation when mapping mode is disabled (**PRTMAP_EN** = 0), this register selects the ports that will be permanently disabled. These ports are then unavailable and cannot be enabled or enumerated by a host controller. The ports can be disabled in any order, where the internal logic will automatically report the correct number of enabled ports to the USB host. The active ports will be reordered in order to ensure proper function. When using the default configuration, **PRT_DIS_P[x:1]** and **PRT_DIS_M[x:1]** pins disable the appropriate ports.

5.1.12 REGISTER 0BH: PORT DISABLE FOR BUS-POWERED OPERATION

Bit Number	Bit Name	Description
7:0	PORT_DIS_BP	Port Disable Bus-Powered: disables one or more ports. 0 = port is available 1 = port is disabled Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : rsvd During self-powered operation when mapping mode is disabled (**PRTMAP_EN** = 0), this selects the ports which will be permanently disabled.These ports are then unavailable and cannot be enabled or enumerated by a host controller. The ports can be disabled in any order, where the internal logic will automatically report the correct number of enabled ports to the USB host. The active ports will be reordered in order to ensure proper function. When using the internal default option, the **PRT_DIS_P[x:1]** and **PRT_DIS_M[x:1]** pins disable the appropriate ports.

5.1.13 REGISTER 0CH: MAX POWER FOR SELF-POWERED OPERATION

Bit Number	Bit Name	Description
7:0	MAX_PWR_SP	Max Power Self-Powered: the value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device. The embedded peripheral reports 0 mA in its descriptors. **Note:** The *USB 2.0 Specification* does not permit this value to exceed 100 mA

5.1.14 REGISTER 0DH: MAX POWER FOR BUS-POWERED OPERATION

Bit Number	Bit Name	Description
7:0	MAX_PWR_BP	Max Power Bus-Powered: the value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device. The embedded peripheral reports 0 mA in its descriptors.