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# USB2533

# USB 2.0 Hi-Speed 3-Port Hub Controller

## PRODUCT FEATURES

**Datasheet**

### Highlights

- Hub Controller IC with 3 downstream ports
- USB-IF Battery Charger revision 1.2 support on up & downstream ports (DCP, CDP, SDP)
- Battery charging support for Apple® devices
- **FlexConnect**: Downstream port 1 able to swap with upstream port, allowing master capable devices to control other devices on the hub
- USB to I²C™ bridge endpoint support
- USB Link Power Management (LPM) support
- SUSPEND pin for remote wakeup indication to host
- Vendor Specific Messaging (VSM) support
- Enhanced OEM configuration options available through a single serial I²C™ EEPROM, OTP, or SMBus Slave Port
- 36-pin (6x6mm) SQFN, RoHS compliant package
- Footprint compatible with USB2513B

### Target Applications

- LCD monitors and TVs
- Multi-function USB peripherals
- PC mother boards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems

### Additional Features

- **MultiTRAK™**
  - Dedicated Transaction Translator per port
- **PortMap**
  - Configurable port mapping and disable sequencing
- **PortSwap**
  - Configurable differential intra-pair signal swapping
- **PHYBoost™**
  - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense™**
  - Programmable USB receiver sensitivity
- Low power operation
- Full Power Management with individual or ganged power control of each downstream port
- Built-in Self-Powered or Bus-Powered internal default settings provide flexibility in the quantity of USB expansion ports utilized without redesign
- Supports “Quad Page” configuration OTP flash
  - Four consecutive 200 byte configuration pages
- Fully integrated USB termination and Pull-up/Pull-down resistors
- On-chip Power On Reset (POR)
- Internal 3.3V and 1.2V voltage regulators
- On Board 24MHz Crystal Driver, Resonator, or External 24MHz clock input
- Environmental
  - Commercial temperature range support (0ºC to 70ºC)
  - Industrial temperature range support (-40ºC to 85ºC)

**Order Number(s):**

| ORDER NUMBER | TEMPERATURE RANGE | PACKAGE TYPE |
|---|---|---|
| USB2533-1080AEN | 0°C to +70°C | 36-pin SQFN |
| USB2533-1080AEN-TR | 0°C to +70°C | 36-pin SQFN (Tape & Reel) |
| USB2533i-1080AEN | -40°C to +85°C | 36-pin SQFN |
| USB2533-1080AEN-TR | -40°C to +85°C | 36-pin SQFN (Tape & Reel) |

**This product meets the halogen maximum concentration values per IEC61249-2-21**

**The table above represents valid part numbers at the time of printing and may not represent parts that are currently available. For the latest list of valid ordering numbers for this product, please contact the nearest sales office.**

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# Chapter 1 General Description

The USB2533 is a low-power, OEM configurable, MTT (Multi-Transaction Translator) USB 2.0 hub controller with 3 downstream ports and advanced features for embedded USB applications. The USB2533 is fully compliant with the USB 2.0 Specification, USB 2.0 Link Power Management Addendum and will attach to an upstream port as a Full-Speed hub or as a Full-/Hi-Speed hub. The 3-port hub supports Low-Speed, Full-Speed, and Hi-Speed (if operating as a Hi-Speed hub) downstream devices on all of the enabled downstream ports.

The USB2533 has been specifically optimized for embedded systems where high performance, and minimal BOM costs are critical design requirements. Standby mode power has been minimized and reference clock inputs can be aligned to the customer's specific application. Additionally, all required resistors on the USB ports are integrated into the hub, including all series termination and pull-up/pull-down resistors on the D+ and D– pins.

The USB2533 supports both upstream battery charger detection and downstream battery charging. The USB2533 integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. These circuits are used to detect the attachment and type of a USB charger and provide an interrupt output to indicate charger information is available to be read from the device's status registers via the serial interface. The USB2533 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

The USB2533 provides an additional USB endpoint dedicated for use as a USB to $I^2C$ interface, allowing external circuits or devices to be monitored, controlled, or configured via the USB interface. Additionally, the USB2533 includes many powerful and unique features such as:

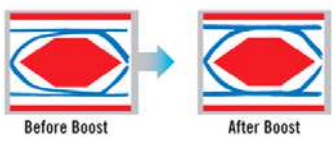
**FlexConnect**, which provides flexible connectivity options. The USB2533's downstream port 1 can be swapped with the upstream port, allowing master capable devices to control other devices on the hub.

**MultiTRAK™ Technology**, which utilizes a dedicated Transaction Translator (TT) per port to maintain consistent full-speed data throughput regardless of the number of active downstream connections. MultiTRAK™ outperforms conventional USB 2.0 hubs with a single TT in USB full-speed data transfers.

**PortMap**, which provides flexible port mapping and disable sequences. The downstream ports of a USB2533 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB2533 hub controllers automatically reorder the remaining ports to match the USB host controller's port numbering scheme.

**PortSwap**, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

**PHYBoost**, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration.




**VariSense**, which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

The USB2533 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature range versions.

## 1.1 Block Diagram

Figure 1.1 details the internal block diagram of the USB2533.

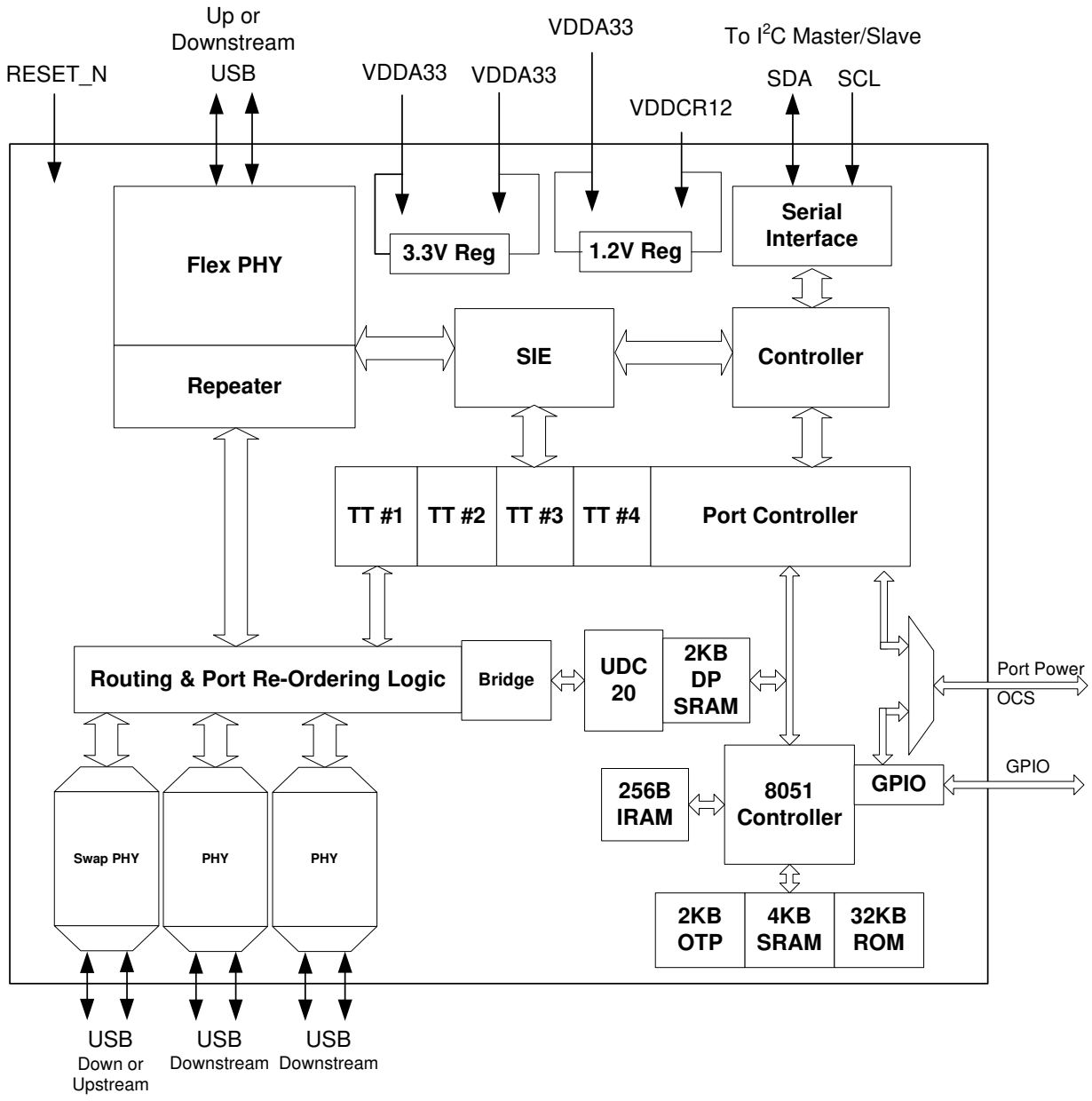



**Figure 1.1 System Block Diagram**

# Chapter 2 Acronyms and Definitions

## 2.1 Acronyms

**EOP:** End of Packet

**EP:** Endpoint

**FS:** Full-Speed

**GPIO:** General Purpose I/O (that is input/output to/from the device)

**HS:** Hi-Speed

**HSOS:** High Speed Over Sampling

**I²C®:** Inter-Integrated Circuit

**LS:** Low-Speed

**OTP:** One Time Programmable

**PCB:** Printed Circuit Board

**PCS:** Physical Coding Sublayer

**PHY:** Physical Layer

**SMBus:** System Management Bus

**UUID:** Universally Unique IDentification

## 2.2 Reference Documents

1. *UNICODE UTF-16LE For String Descriptors* USB Engineering Change Notice, December 29th, 2004, http://www.usb.org
2. *Universal Serial Bus Specification*, Revision 2.0, April 27th, 2000, http://www.usb.org
3. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
4. *I²C-Bus Specification*, Version 1.1, http://www.nxp.com
5. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

# Chapter 3 Pin Descriptions

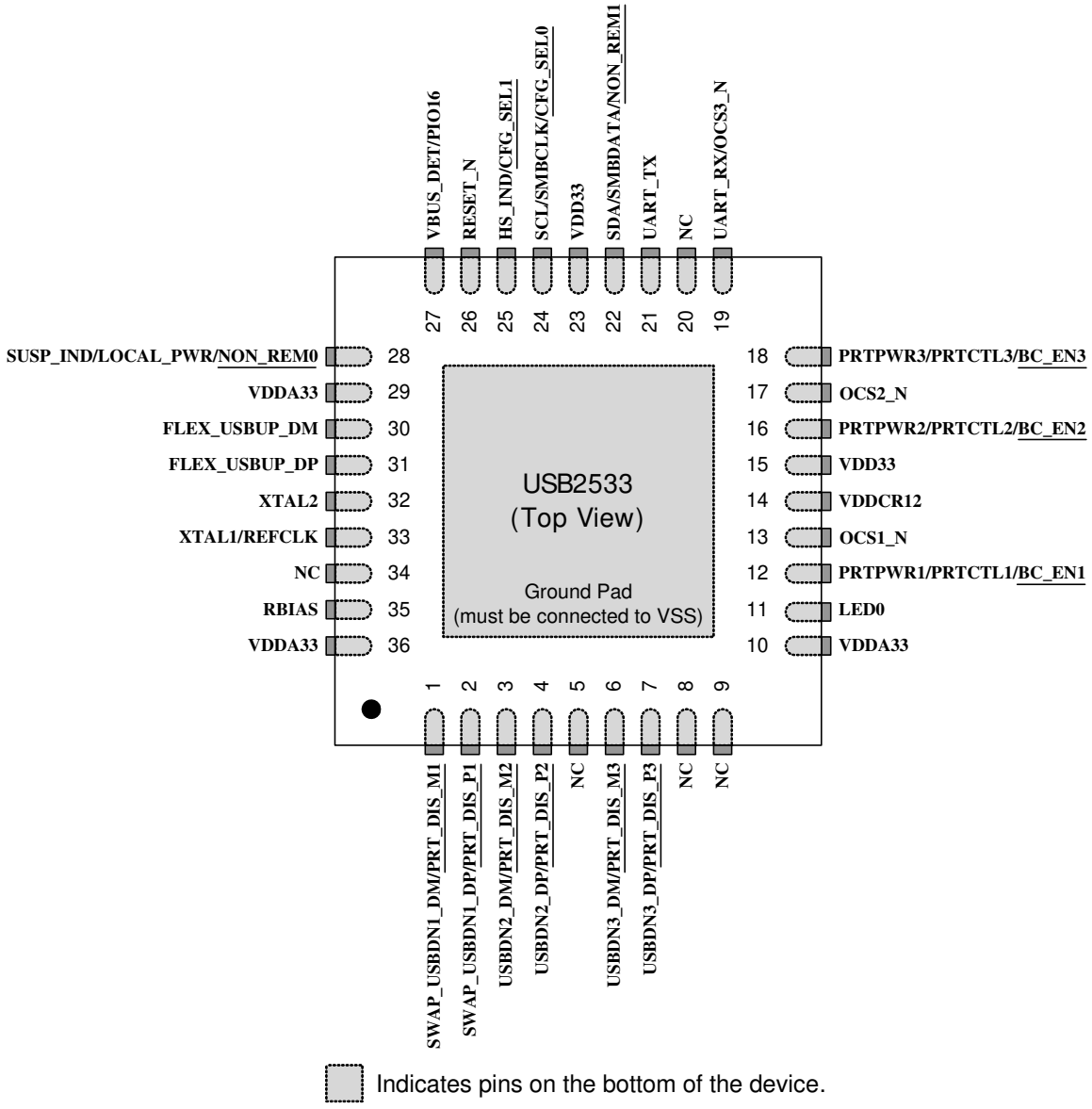



**Figure 3.1 36-SQFN Pin Assignments**

## 3.1 Pin Descriptions

This section provides a detailed description of each pin. The signals are arranged in functional groups according to their associated interface.

The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, RESET_N indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

**Note:** The buffer type for each signal is indicated in the BUFFER TYPE column of Table 3.1. A description of the buffer types is provided in Section 3.3.

**Note:** Compatibility with the UCS100x family of USB port power controllers requires the UCS100x be connected on Port 1 of the USB2533. Additionally, both PRTPWR1 and OCS1_N must be pulled high at Power-On Reset (POR).

**Table 3.1 Pin Descriptions**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| **USB/HSIC INTERFACES** | | | | |
| 1 | Upstream USB D+ (Flex Port 0) | FLEX_USBUP_DP | AIO | Upstream USB Port 0 D+ data signal.<br>**Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals. |
| 1 | Upstream USB D- (Flex Port 0) | FLEX_USBUP_DM | AIO | Upstream USB Port 0 D- data signal.<br>**Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals. |
| 1 | Downstream USB D+ (Swap Port 1) | SWAP_USBDN1_DP | AIO | Downstream USB Port 1 D+ data signal.<br>**Note:** The downstream Port 1 signals can be optionally swapped with the upstream Port 0 signals. |
| 1 | Port 1 D+ Disable Configuration Strap | PRT_DIS_P1 | IS | This strap is used in conjunction with PRT_DIS_M1 to disable USB Port 1.<br>0 = Port 1 D+ Enabled<br>1 = Port 1 D+ Disabled<br>**Note:** Both PRT_DIS_P1 and PRT_DIS_M1 must be tied to VDD33 at reset to disable the associated port.<br>See Note 3.4 for more information on configuration straps. |

**Table 3.1 Pin Descriptions (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| | Downstream USB D- (Swap Port 1) | SWAP_USBDN1_DM | AIO | Downstream USB Port 1 D- data signal.<br>**Note:** The downstream Port 1 signals can be optionally swapped with the upstream Port 0 signals. |
| 1 | Port 1 D- Disable Configuration Strap | PRT_DIS_M1 | IS | This strap is used in conjunction with PRT_DIS_P1 to disable USB Port 1.<br>0 = Port 1 D- Enabled<br>1 = Port 1 D- Disabled<br>**Note:** Both PRT_DIS_P1 and PRT_DIS_M1 must be tied to VDD33 at reset to disable the associated port.<br>See Note 3.4 for more information on configuration straps. |
| | Downstream USB D+ (Port 2) | USBDN2_DP | AIO | Downstream USB Port 2 D+ data signal. |
| 1 | Port 2 D+ Disable Configuration Strap | PRT_DIS_P2 | IS | This strap is used in conjunction with PRT_DIS_M2 to disable USB Port 2.<br>0 = Port 2 D+ Enabled<br>1 = Port 2 D+ Disabled<br>**Note:** Both PRT_DIS_P2 and PRT_DIS_M2 must be tied to VDD33 at reset to disable the associated port.<br>See Note 3.4 for more information on configuration straps. |
| | Downstream USB D- (Port 2) | USBDN2_DM | AIO | Downstream USB Port 2 D- data signal. |
| 1 | Port 2 D- Disable Configuration Strap | PRT_DIS_M2 | IS | This strap is used in conjunction with PRT_DIS_P2 to disable USB Port 2.<br>0 = Port 2 D- Enabled<br>1 = Port 2 D- Disabled<br>**Note:** Both PRT_DIS_P2 and PRT_DIS_M2 must be tied to VDD33 at reset to disable the associated port.<br>See Note 3.4 for more information on configuration straps. |

**Table 3.1 Pin Descriptions (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Downstream USB D+ (Port 3) | USBDN3_DP | AIO | Downstream USB Port 3 D+ data signal. |
| | Port 3 D+ Disable Configuration Strap | PRT_DIS_P3 | IS | This strap is used in conjunction with PRT_DIS_M3 to disable USB Port 3.<br>0 = Port 3 D+ Enabled<br>1 = Port 3 D+ Disabled<br>**Note:** Both PRT_DIS_P3 and PRT_DIS_M3 must be tied to VDD33 at reset to disable the associated port.<br>See Note 3.4 for more information on configuration straps. |
| 1 | Downstream USB D- (Port 3) | USBDN3_DM | AIO | Downstream USB Port 3 D- data signal. |
| | Port 3 D- Disable Configuration Strap | PRT_DIS_M3 | IS | This strap is used in conjunction with PRT_DIS_P3 to disable USB Port 3.<br>0 = Port 3 D- Enabled<br>1 = Port 3 D- Disabled<br>**Note:** Both PRT_DIS_P3 and PRT_DIS_M3 must be tied to VDD33 at reset to disable the associated port.<br>See Note 3.4 for more information on configuration straps. |
| **$I^2C$/SMBUS INTERFACE** | | | | |
| 1 | $I^2C$ Serial Clock Input | SCL | I_SMB | $I^2C$ serial clock input |
| | SMBus Clock | SMBCLK | I_SMB | SMBus serial clock input |
| | Configuration Select 0 Configuration Strap | CFG_SEL0 | I_SMB | This strap is used in conjunction with CFG_SEL1 to set the hub configuration method. Refer to Section 6.3.2, "Configuration Select (CFG_SEL[1:0])," on page 29 for additional information.<br>See Note 3.4 for more information on configuration straps. |

**Table 3.1 Pin Descriptions (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | $I^2C$ Serial Data | SDA | IS/OD8 | $I^2C$ bidirectional serial data |
| | SMBus Serial Data | SMBDATA | IS/OD8 | SMBus bidirectional serial data |
| | Non-Removable Device 1 Configuration Strap | NON_REM1 (Note 3.3) | IS | This strap is used in conjunction with NON_REM0 to configure the downstream ports as non-removable devices. Refer to Section 6.3.1, "Non-Removable Device (NON_REM[1:0])," on page 29 for additional information.<br>See Note 3.4 for more information on configuration straps. |
| **MISC.** | | | | |
| 1 | Port 1 Over-Current Sense Input | OCS1_N | IS (PU) | This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 1. |
| 1 | Port 2 Over-Current Sense Input | OCS2_N | IS (PU) | This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 2. |
| 1 | UART Receive Input | UART_RX | IS | Internal UART receive input<br>**Note:** This is a 3.3V signal. For RS232 operation, an external 12V translator is required. |
| | Port 3 Over-Current Sense Input | OCS3_N | IS (PU) | This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 3. |
| 1 | UART Transmit Output | UART_TX | O8 | Internal UART transmit output<br>**Note:** This is a 3.3V signal. For RS232 operation, an external 12V driver is required. |
| 1 | System Reset Input | RESET_N | I_RST | This active-low signal allows external hardware to reset the device.<br>**Note:** The active-low pulse must be at least 5us wide. Refer to Section 8.3.2, "External Chip Reset (RESET_N)," on page 36 for additional information. |
| 1 | Crystal Input | XTAL1 | ICLK | External 24 MHz crystal input |
| | Reference Clock Input | REFCLK | ICLK | Reference clock input. The device may be alternatively driven by a single-ended clock oscillator. When this method is used, XTAL2 should be left unconnected. |
| 1 | Crystal Output | XTAL2 | OCLK | External 24 MHz crystal output |

**Table 3.1 Pin Descriptions (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | External USB Transceiver Bias Resistor | RBIAS | AI | A 12.0kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings. |
| 1 | LED 0 Output | LED0 | O8 | General purpose LED 0 output that is configurable to blink or "breathe" at various rates.<br>**Note:** LED0 must be enabled via the Protouch configuration tool. |
| 1 | Detect Upstream VBUS Power | VBUS_DET | IS | Detects state of upstream bus power.<br>When designing a detachable hub, this pin must be connected to the VBUS power pin of the upstream USB port through a resistor divider (50kΩ by 100kΩ) to provide 3.3V.<br>For self-powered applications with a permanently attached host, this pin must be connected to either 3.3V or 5.0V through a resistor divider to provide 3.3V.<br>In embedded applications, VBUS_DET may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device. |

**Table 3.1 Pin Descriptions (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Remote Wakeup Indicator | SUSP_IND | OD8 | Configurable sideband signal used to indicate Suspend status (default) or Remote Wakeup events to the Host.<br><br>Suspend Indicator (default configuration):<br>0 = Unconfigured, or configured and in USB suspend mode<br>1 = Device is configured and is active (i.e., not in suspend)<br><br>For Remote Wakeup Indicator mode:<br>Refer to Section 8.5, "Remote Wakeup Indicator (SUSP_IND)," on page 37.<br><br>Refer to Section 6.3.1, "Non-Removable Device (NON_REM[1:0])," on page 29 for information on LED polarity when using this signal. |
| | Local Power Detect | LOCAL_PWR | IS | Detects the availability of a local self-power source.<br><br>0 = Self/local power source is NOT available. (i.e., device must obtain all power from upstream USB VBUS)<br>1 = Self/local power source is available<br><br>See Note 3.2 for more information on this pin. |
| | Non-Removable Device 0 Configuration Strap | NON_REM0 (Note 3.3) | IS | This strap is used in conjunction with NON_REM1 to configure the downstream ports as non-removable devices. Refer to Section 6.3.1, "Non-Removable Device (NON_REM[1:0])," on page 29 for additional information.<br><br>See Note 3.4 for more information on configuration straps. |
| 1 | High Speed Indicator | HS_IND | O8 | Indicates a high speed connection on the upstream port. The active state of the LED will be determined as follows:<br><br>If CFG_SEL1 = 0, HS_IND is active high.<br>If CFG_SEL1 = 1, HS_IND is active low.<br><br>Asserted = hub is connected at high speed<br>Negated = Hub is connected at full speed |
| | Configuration Select 1 Configuration Strap | CFG_SEL1 | IS | This strap is used in conjunction with CFG_SEL0 to set the hub configuration method. Refer to Section 6.3.2, "Configuration Select (CFG_SEL[1:0])," on page 29 for additional information.<br><br>See Note 3.4 for more information on configuration straps. |

**Table 3.1 Pin Descriptions (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Port 1 Power Output | PRTPWR1 | O8 | Enables power to a downstream USB device attached to Port 1.<br><br>0 = Power disabled on downstream Port 1<br>1 = Power enabled on downstream Port 1 |
| | Port 1 Control | PRTCTL1 | OD8/IS (PU) | When configured as PRTCTL1, this pin functions as both the Port 1 power enable output (PRTPWR1) and the Port 1 over-current sense input (OCS1_N). Refer to the PRTPWR1 and OCS1_N descriptions for additional information. |
| | Port 1 Battery Charging Configuration Strap | BC_EN1 | IS | This strap is used to indicate support of the battery charging protocol on Port 1. Enabling battery charging support allows a device on the port to draw currents per the USB battery charging specification.<br><br>0 = Battery charging is not supported on Port 1<br>1 = Battery charging is supported on Port 1<br><br>See Note 3.4 for more information on configuration straps. |
| 1 | Port 2 Power Output | PRTPWR2 | O8 | Enables power to a downstream USB device attached to Port 2.<br><br>0 = Power disabled on downstream Port 2<br>1 = Power enabled on downstream Port 2 |
| | Port 2 Control | PRTCTL2 | OD8/IS (PU) | When configured as PRTCTL2, this pin functions as both the Port 2 power enable output (PRTPWR2) and the Port 2 over-current sense input (OCS2_N). Refer to the PRTPWR2 and OCS2_N descriptions for additional information. |
| | Port 2 Battery Charging Configuration Strap | BC_EN2 | IS | This strap is used to indicate support of the battery charging protocol on Port 2. Enabling battery charging support allows a device on the port to draw currents per the USB battery charging specification.<br><br>0 = Battery charging is not supported on Port 2<br>1 = Battery charging is supported on Port 2<br><br>See Note 3.4 for more information on configuration straps. |

**Table 3.1 Pin Descriptions (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Port 3 Power Output | PRTPWR3 | O8 | Enables power to a downstream USB device attached to Port 3.<br><br>0 = Power disabled on downstream Port 3<br>1 = Power enabled on downstream Port 3 |
| | Port 3 Control | PRTCTL3 | OD8/IS (PU) | When configured as PRTCTL3, this pin functions as both the Port 3 power enable output (PRTPWR3) and the Port 3 over-current sense input (OCS3_N). Refer to the PRTPWR3 and OCS3_N descriptions for additional information. |
| | Port 3 Battery Charging Configuration Strap | BC_EN3 | IS | This strap is used to indicate support of the battery charging protocol on Port 3. Enabling battery charging support allows a device on the port to draw currents per the USB battery charging specification.<br><br>0 = Battery charging is not supported on Port 3<br>1 = Battery charging is supported on Port 3<br><br>See Note 3.4 for more information on configuration straps. |
| 5 | No Connect | NC | - | These pins must be left floating for normal device operation. |
| **POWER** | | | | |
| 3 | +3.3V Analog Power Supply | VDDA33 | P | +3.3V analog power supply. Refer to Chapter 4, "Power Connections," on page 21 for power connection information. |
| 2 | +3.3V Power Supply | VDD33 | P | +3.3V power supply. These pins must be connected to VDDA33. Refer to Chapter 4, "Power Connections," on page 21 for power connection information. |
| 1 | +1.2V Core Power Supply | VDDCR12 | P | +1.2V core power supply. A 1.0 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the device. Refer to Chapter 4, "Power Connections," on page 21 for power connection information. |
| Exposed Pad on package bottom (Figure 3.1) | Ground | VSS | P | Common ground. This exposed pad must be connected to the ground plane with a via array. |

**Note 3.2** The LOCAL_PWR pin is sampled during the configuration state, immediately after negation of reset, to determine whether the device is bus-powered or self-powered. When configuration is complete, the latched value will not change until the next reset assertion. To enable dynamic local power switching, the DYNAMIC_POWER register at location 0x4134 must be programmed with 0x41. If dynamic power switching is not required, the DYNAMIC_POWER register should be left at the default value of 0xC1. Programming may

be performed through the SMBus interface, or permanently via OTP. Refer to the Protouch MPT User Manual for additional information.

**Note 3.3** If using the local power detect function (LOCAL_PWR pin), the NON_REM[1:0] configuration straps cannot be used to configure the non-removable state of the USB ports. In this case, the non-removable state of the ports must be configured in internal device registers via the Protouch tool or SMBus.

**Note 3.4** Configuration strap values are latched on Power-On Reset (POR) and the rising edge of RESET_N (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 6.3, "Device Configuration Straps," on page 28 for additional information.

## 3.2 Pin Assignments

**Table 3.2 36-SQFN Package Pin Assignments**

| PIN NUM | PIN NAME | PIN NUM | PIN NAME |
|---|---|---|---|
| 1 | SWAP_USBDN1_DM/PRT_DIS_M1 | 19 | UART_RX/OCS3_N |
| 2 | SWAP_USBDN1_DP/PRT_DIS_P1 | 20 | NC |
| 3 | USBDN2_DM/PRT_DIS_M2 | 21 | UART_TX/ |
| 4 | USBDN2_DP/PRT_DIS_P2 | 22 | SDA/SMBDATA/NON_REM1 |
| 5 | NC | 23 | VDD33 |
| 6 | USBDN3_DM/PRT_DIS_M3 | 24 | SCL/SMBCLK/CFG_SEL0 |
| 7 | USBDN3_DP/PRT_DIS_P3 | 25 | HS_IND/CFG_SEL1 |
| 8 | NC | 26 | RESET_N |
| 9 | NC | 27 | VBUS_DET |
| 10 | VDDA33 | 28 | SUSP_IND/LOCAL_PWR/NON_REM0 |
| 11 | LED0 | 29 | VDDA33 |
| 12 | PRTPWR1/PRTCTL1/BC_EN1 | 30 | FLEX_USBUP_DM |
| 13 | OCS1_N | 31 | FLEX_USBUP_DP |
| 14 | VDDCR12 | 32 | XTAL2 |
| 15 | VDD33 | 33 | XTAL1/REFCLK |
| 16 | PRTPWR2/PRTCTL2/BC_EN2 | 34 | NC |
| 17 | OCS2_N | 35 | RBIAS |
| 18 | PRTPWR3/PRTCTL3/BC_EN3 | 36 | VDDA33 |

## 3.3 Buffer Type Descriptions

**Table 3.3 Buffer Types**

| BUFFER TYPE | DESCRIPTION |
|---|---|
| IS | Schmitt-triggered input |
| I_RST | Reset Input |
| I_SMB | $I^2C$/SMBus Clock Input |
| O8 | Output with 8 mA sink and 8 mA source |
| OD8 | Open-drain output with 8 mA sink |
| OD12 | Open-drain output with 12 mA sink |
| PU | 50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled.<br>**Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added. |
| PD | 50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled.<br>**Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added. |
| AIO | Analog bi-directional |
| ICLK | Crystal oscillator input pin |
| OCLK | Crystal oscillator output pin |
| P | Power pin |

# Chapter 4 Power Connections

## 4.1 Integrated Power Regulators

The integrated 3.3V and 1.2V power regulators allow the device to be supplied via a single 3.3V external power supply.

The regulators are controlled by RESET_N. When RESET_N is brought high, the 3.3V regulator will turn on. When RESET_N is brought low the 3.3V regulator will turn off.

## 4.2 Power Connection Diagrams

Figure 4.1 illustrates the power connections for the USB2533.

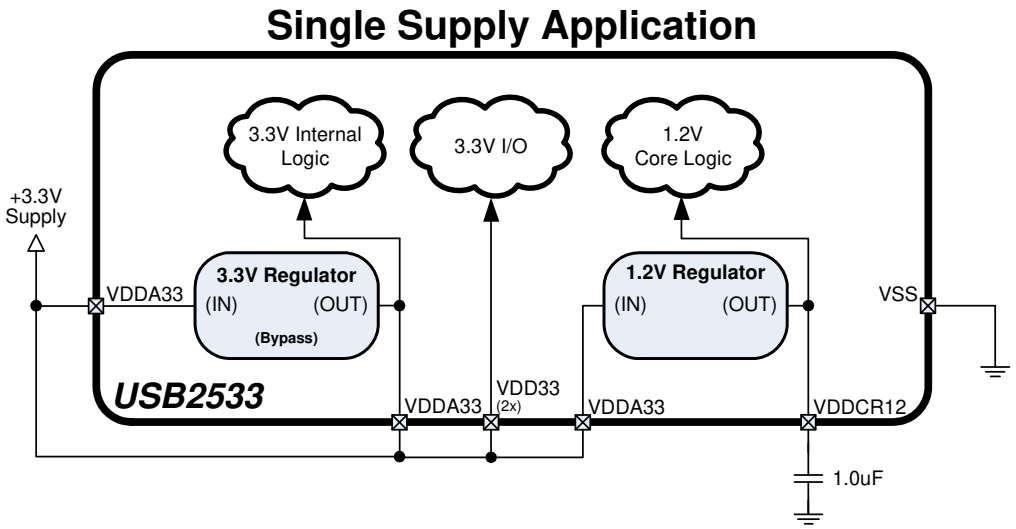



**Figure 4.1 Power Connections**

# Chapter 5 Modes of Operation

The device provides two main modes of operation: Standby Mode and Hub Mode. The operating mode of the device is selected by setting values on primary inputs according to the table below.

**Table 5.1 Controlling Modes of Operation**

| RESET_N INPUT | RESULTING MODE | SUMMARY |
|---|---|---|
| **0** | **Standby** | **Lowest Power Mode**: No functions are active other than monitoring the RESET_N input. All port interfaces are high impedance. All regulators are powered off. |
| **1** | **Hub** | **Full Feature Mode**: Device operates as a configurable USB hub with battery charger detection. Power consumption is based on the number of active ports, their speed, and amount of data transferred. |

**Note:** Refer to Section 8.3.2, "External Chip Reset (RESET_N)," on page 36 for additional information on RESET_N.

The flowchart in Figure 5.1 shows the modes of operation. It also shows how the device traverses through the Hub mode stages (shown in bold.) The flow of control is dictated by control register bits shown in italics as well as other events such as availability of a reference clock. The remaining sections in this chapter provide more detail on each stage and mode of operation.

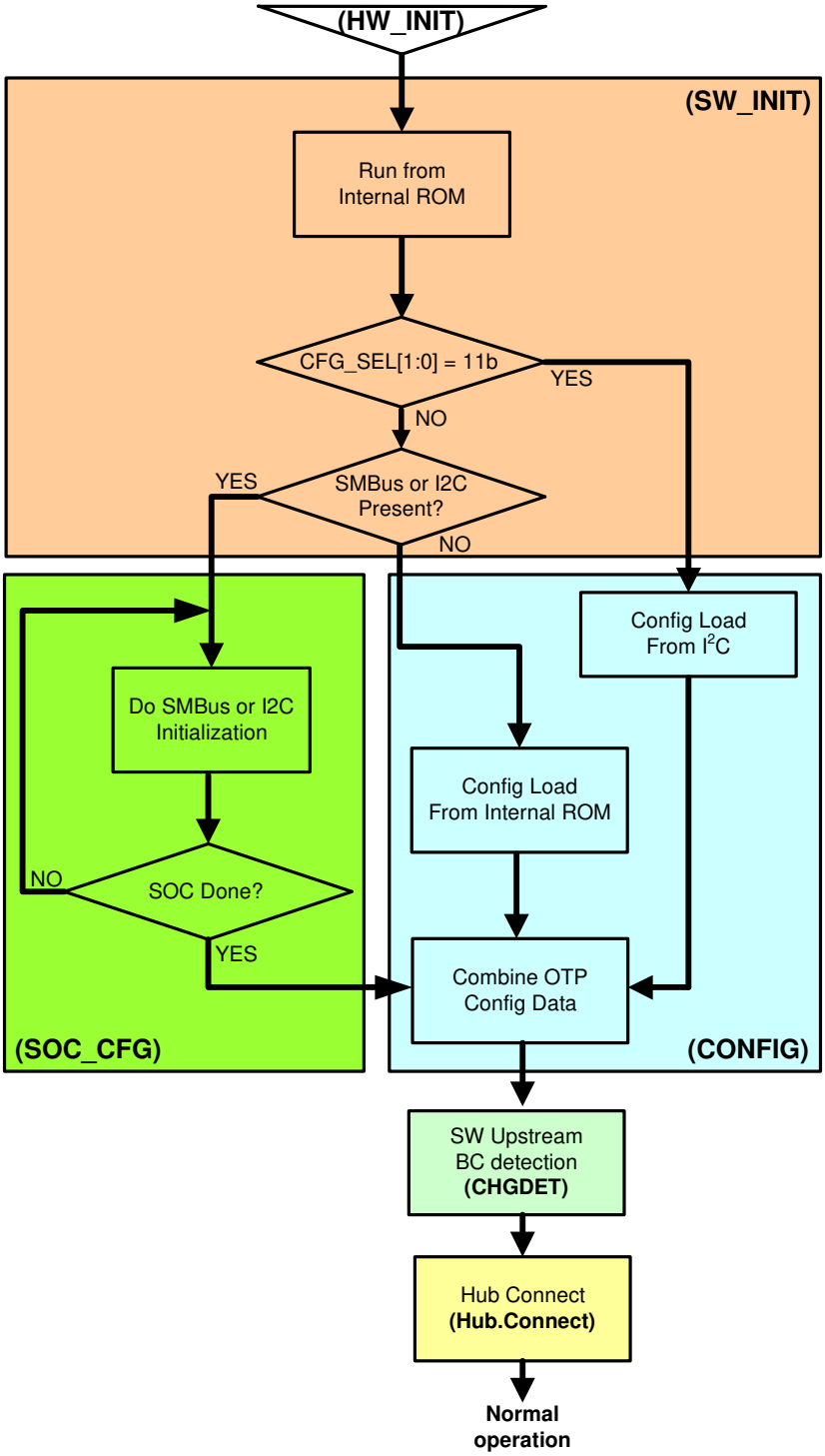



**Figure 5.1 Hub Operational Mode Flowchart**

## 5.1 Boot Sequence

### 5.1.1 Standby Mode

If the external hardware reset is asserted, the hub will be in Standby Mode. This mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all internal regulators are powered off, the PLL is not running, and core logic is powered down in order to minimize power consumption. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after RESET_N is negated high.

### 5.1.2 Hardware Initialization Stage (HW_INIT)

The first stage is the initialization stage and occurs on the negation of RESET_N. In this stage the 1.2V regulator is enabled and stabilizes, internal logic is reset, and the PLL locks if a valid REFCLK is supplied. Configuration registers are initialized to their default state and strap input values are latched. The device will complete initialization and automatically enter the next stage. Because the digital logic within the device is not yet stable, no communication with the device using the SMBus is possible. Configuration registers are initialized to their default state.

If there is a REFCLK present, the next state is SW_INIT.

### 5.1.3 Software Initialization Stage (SW_INIT)

Once the hardware is initialized, the firmware can begin to execute from the internal ROM. The firmware checks the CFG_SEL[1:0] configuration strap values to determine if it is configured for $I^2C$ Master loading. If so, the configuration is loaded from an external $I^2C$ ROM in the device's CONFIG state.

For all other configurations, the firmware checks for the presence of an external $I^2C$/SMBus. It does this by asserting two pull down resistors on the data and clock lines of the bus. The pull downs are typically 50Kohm. If there are 10Kohm pull-ups present, the device becomes aware of the presence of an external SMBus/$I^2C$ bus. If a bus is detected, the firmware transitions to the SOC_CFG state.

### 5.1.4 SOC Configuration Stage (SOC_CFG)

In this stage, the SOC may modify any of the default configuration settings specified in the integrated ROM such as USB device descriptors, or port electrical settings, and control features such as upstream battery charging detection.

There is no time limit. In this stage the firmware will wait indefinitely for the SMBus/$I^2C$ configuration. When the SOC has completed configuring the device, it must write to register 0xFF to end the configuration.

### 5.1.5 Configuration Stage (CONFIG)

Once the SOC has indicated that it is done with configuration, then all the configuration data is combined. The default data, the SOC configuration data, the OTP data are all combined in the firmware and device is programmed.

After the device is fully configured, it will go idle and then into suspend if there is no VBUS or Hub.Connect present. Once VBUS is present, and upstream battery charging is enabled, the device will transition to the Battery Charger Detection Stage (CHGDET). If VBUS is present, and upstream battery charging is not enabled, the device will transitions to the Connect (Hub.Connect) stage.

### 5.1.6 Battery Charger Detection Stage (CHGDET)

After configuration, if enabled, the device enters the Battery Charger Detection Stage. If the battery charger detection feature was disabled during the CONFIG stage, the device will immediately transition to the Hub Connect (Hub.Connect) stage. If the battery charger detection feature remains enabled, the battery charger detection sequence is started automatically.

If the charger detection remains enabled, the device will transition to the Hub.Connect stage if using the hardware detection mechanism.

### 5.1.7 Hub Connect Stage (Hub.Connect)

Once the CHGDET stage is completed, the device enters the Hub.Connect stage.

### 5.1.8 Normal Mode

Lastly the SOC enters the Normal Mode of operation. In this stage, full USB operation is supported under control of the USB Host on the upstream port. The device will remain in the normal mode until the operating mode is changed by the system.

If RESET_N is asserted low, then Standby Mode is entered. The device may then be placed into any of the designated Hub stages. Asserting the soft disconnect on the upstream port will cause the Hub to return to the Hub.Connect stage until the soft disconnect is negated.

To save power, communication over the SMBus is not supported while in USB Suspend. The system can prevent the device from going to sleep by asserting the ClkSusp control bit of the Configure Portable Hub Register anytime before entering USB Suspend. While the device is kept awake during USB Suspend, it will provide the SMBus functionality at the expense of not meeting USB requirements for average suspend current consumption.