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USB2640/USB2641

Ultra Fast USB 2.0 Multi-Format Flash Media Controller/USB Hub Combo

PRODUCT FEATURES

Datasheet

General Description

The SMSC USB2640/USB2641 is a USB 2.0 compliant, Hi-Speed hub for USB port expansion with an attached mass storage class peripheral controller. The controller allows read/write capability to popular flash media from the following families:

- Secure Digital™ (SD)
- MultiMediaCard™ (MMC)
- xD-Picture Card™ (xD)[1]
- Memory Stick®(MS)

The USB2640/USB2641 is a fully integrated, single chip solution providing USB expansion and integrated flash card media reader/writer capability of ultra high performance operation. Average sustained transfer rates exceeding 35 MB/s are possible[2].

Highlights

- Hub controller with internally connected ultra fast flash media reader/writer and 2 exposed downstream ports for external peripheral expansion
- Flash media reader/writer employs multiplexed card interfaces which are optimized for use with single card insertion combo sockets
- Hardware-controlled data flow architecture for all self-mapped media
- Optional support for external firmware access via SPI interface
- **PortMap**
  - — Flexible port mapping and port disable sequencing supports multiple platform designs
- **PortSwap**
  - — Programmable USB differential-pair pin locations eases PCB design by aligning USB signal traces directly to connectors
- **PHYBoost**
  - — Programmable USB transceiver drive strength recovers signal integrity

1.Support and capabilities for xD-Picture Card are not applicable for the USB2641. Please obtain a user license from the xD-Picture Card License Office to support this flash media format.
2.Host and media dependent.

Features

- Compliant with the following flash media card specifications: SD 2.0 / MMC 4.2 / MS 1.43 / MS-Pro 1.02 / MS-PRO-HG 1.01 / MS-Duo 1.10 / xD 1.2
- Supports a single external 3.3 V supply source; internal regulators provide 1.8 V internal core voltage for additional bill of materials and power savings
- The transaction translator (TT) in the hub supports operation of Full-Speed and Low-Speed peripherals
- 9 K RAM | 64 K on-chip ROM
- Enhanced EMI rejection and ESD protection performance
- Onboard 24 MHz crystal driver circuit
- Optional external 24 MHz clock input
- Up to 9 GPIOs for special functions
- 8051 8-bit microprocessor
- Hub and flash media reader/writer configuration from a single source: External I^2C ROM or external SPI ROM
  - — Configures internal code using an external I^2C EEPROM
  - — Supports external code using a SPI Flash EEPROM
  - — Customizable vendor ID, product ID, language ID
- EEPROM update via USB
- 48-pin QFN lead-free, RoHS compliant package (7x7 mm)

Applications

- Desktop and mobile PCs
- Personal mobile devices
- Printers
- GPS navigation systems
- Media Players/Viewers
- Consumer A/V
- Set-top boxes

ORDER NUMBERS:

USB2640/USB2641-HZH-XX for 48-PIN, QFN LEAD-FREE ROHS COMPLIANT PACKAGE

"XX" in the order number indicates the internal ROM firmware revision level.

Please contact your SMSC representative for more information.

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Table of Contents

List of Tables

List of Figures

Chapter 1 Overview

The SMSC USB2640/USB2641 is an integrated USB 2.0 compliant, Hi-Speed hub for USB port expansion with an attached bulk only mass storage class peripheral controller. This multi-format flash media controller and USB Hub Combo features three downstream ports: one port is dedicated to an internally connected ultra fast flash media reader/writer and two exposed downstream ports are available for external peripheral expansion.

The SMSC USB2640/USB2641 is an ultra fast, OEM-configurable, hub controller IC with three downstream ports for embedded USB solutions. The USB2640/USB2641 will attach to an upstream port as a Full-Speed Hub or as a Full-/Hi-Speed Hub. The hub supports Low-Speed, Full-Speed, and Hi-Speed (if operating as a Hi-Speed Hub) downstream devices on all of the enabled downstream ports.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors on D+ and D– pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB2640/USB2641 includes programmable features such as:

PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB2640/USB2641 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB2640/USB2641 automatically reorders the remaining ports to match the USB host controller's port numbering scheme.

PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors avoiding uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost which enables four programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost attempts to restore USB signal integrity that has been compromised by system level variables such as poor PCB layout, long cables, etc.

1.1 Device Features

Hardware Features

- Single chip flash media controller
- Transaction translator (TT) in the hub supports operation of FS and LS peripherals
- Full power management with individual or ganged power control of each downstream port
- Optional support for external firmware access via SPI interface
  - 30 MHz or 60 MHz operation support
  - Single bit or dual bit mode support
  - Mode 0 or mode 3 SPI support

Compliant with the following flash media card specifications:

- Secure Digital 2.0 / MultiMediaCard 4.2
  - SD 2.0, HS-SD, HC-SD
  - TransFlash™ and reduced form factor media
  - 1/4/8 bit MMC 4.2
- SDIO and MMC streaming mode support
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  - Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- xD-Picture Card 1.2 (USB2640 only)
- On board 24 MHz crystal driver circuit
- Optional external 24 MHz clock input
  - Must be used with an external resistor divider to provide a 1.8 V signal
- Up to 9 GPIOs: Configuration and polarity for special function use such as LED indicators, button inputs, and power control to memory devices
  - The number of actual GPIOs depends on the implementation configuration used
  - One GPIO available with up to 200 mA drive and protected “fold-back” short circuit current
- 8051 8-bit microprocessor
  - 60 MHz - single cycle execution
  - 64 KB ROM; 9 KB RAM
- Internal regulator for 1.8 V core operation
- Optimized pinout improves signal flow, easing implementation and allowing for improved signal integrity treatment

Software Features

- Optimized for low latency interrupt handling
- Hub and flash media reader/writer configuration from a single source: External I^2C ROM or external SPI ROM
- EEPROM update via USB
- Please see the USB2640/USB2641 Software Release Notes for additional software features

1.2 OEM Selectable Features

Hub

A default configuration is available in USB2640/USB2641 following a reset. The USB2640/USB2641 may also be configured by an external I^2C EEPROM or via external SPI ROM flash.

The USB2640/USB2641 supports several OEM selectable features:

- Compound Device support (port is permanently hardwired to a downstream USB peripheral device), on a port-by-port basis.
- Select over-current sensing and port power control on an individual (port-by-port) or ganged (all ports together) basis to match the OEM's choice of circuit board component selection.
- Port power control and over-current detection/delay features
- Configure the delay time for filtering the over-current sense inputs.
- Configure the delay time for turning on downstream port power.
- Bus- or self-powered selection
- Hub port disable or non-removable configurations
- Flexible port mapping and disable sequence. Ports can be disabled/reordered in any sequence to support multiple platforms with a single design. The hub will automatically reorder the remaining ports to match the host controller's numbering scheme.
- Programmable USB differential-pair pin location.
  - Eases PCB layout by aligning USB signal lines directly to connectors
- Programmable USB signal drive strength. Recover USB signal integrity due to compromised system environments using four levels of signal drive strength.
- Indicate the maximum current that the 2-port hub consumes from the USB upstream port.
- Indicate the maximum current required for the hub controller.

Flash Media Controller

- Customize vendor ID, product ID, and device ID.
- 12-hex digit (max) serial number string
- Customizable vendor specific data by optional use of external serial EEPROM
- 28-character manufacturer ID and product string for flash media reader/writer
- LED blink interval or duration

Chapter 2 Acronyms

FM: Flash Media

FMC: Flash Media Controller

FS: Full-speed Device

LS: Low-speed Device

HS: Hi-speed Device

I²C®: Inter-Integrated Circuit[1]

MMC: MultiMediaCard

MS: Memory Stick

MSC: Memory Stick Controller

OCS: Over-current Sense

RXD: Received eXchange Data

SD: Secure Digital

SDC: Secure Digital Controller

TXD: Transmit eXchange Data

UART: Universal Asynchronous Receiver-Transmitter

UCHAR: Unsigned Character

UINT: Unsigned Integer

xD: xD-Picture Card

1. I²C is a registered trademark of Philips Corporation.

Chapter 3 Pin Configurations

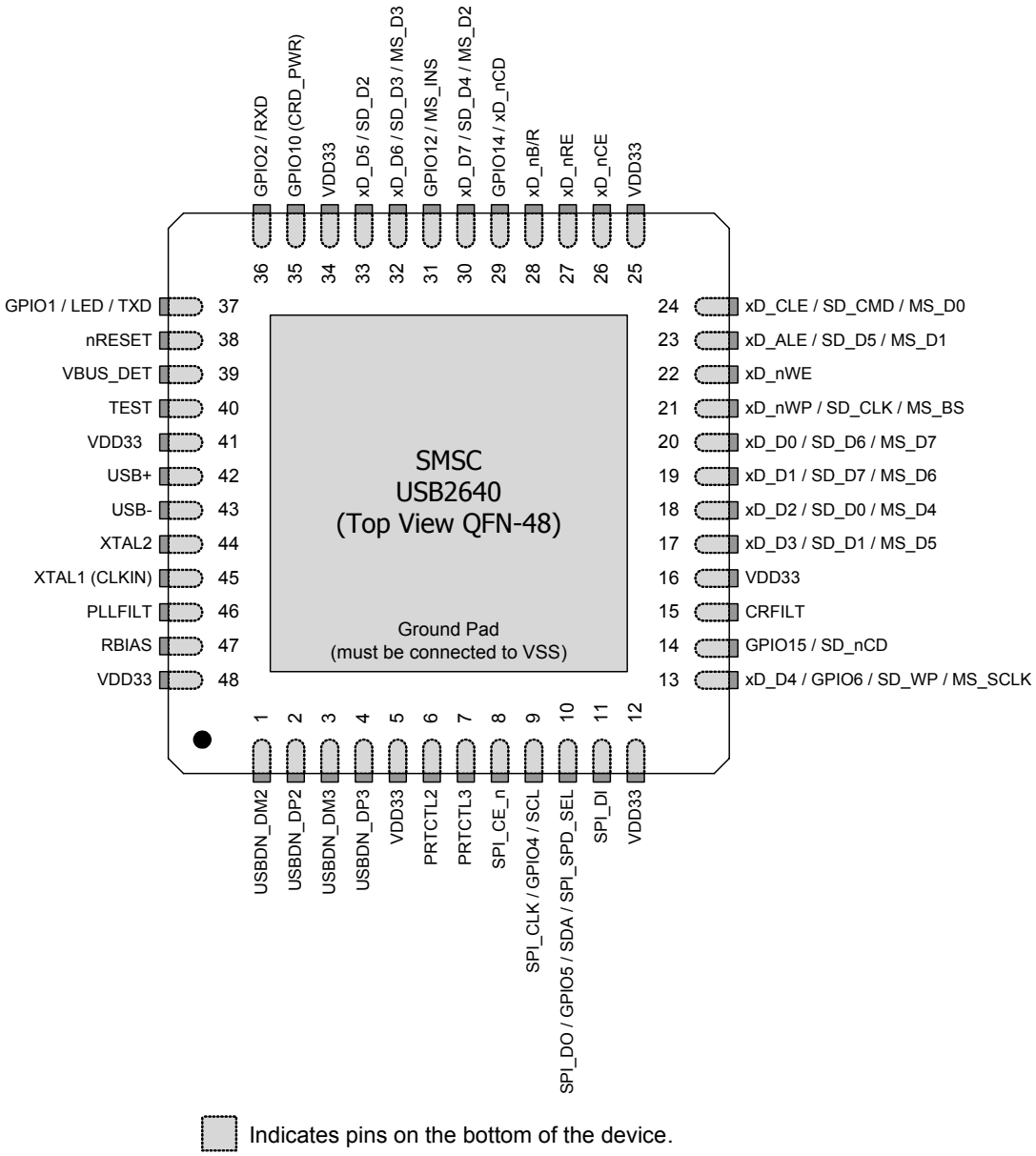

Figure 3.1 USB2640 48-Pin QFN

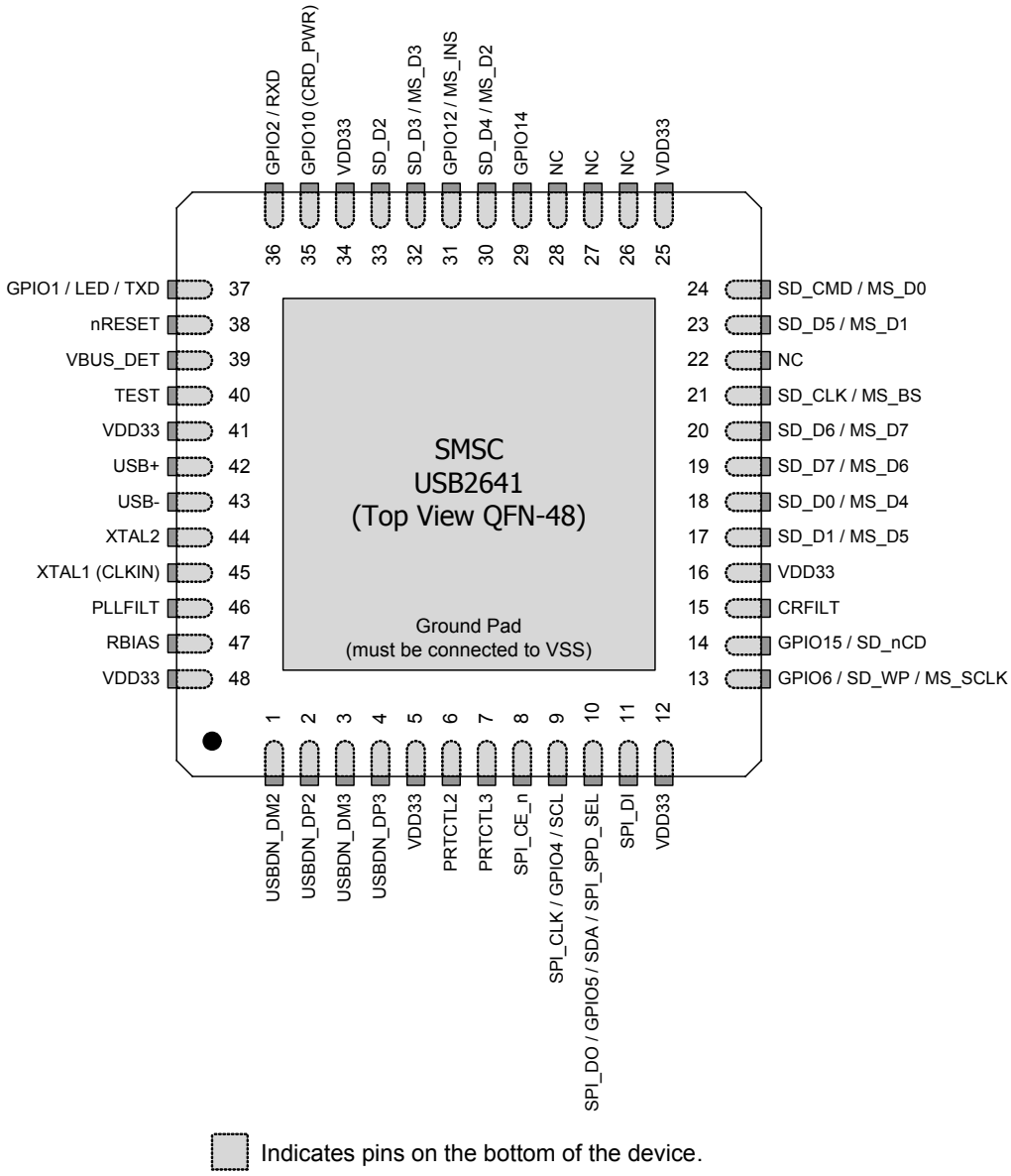

Figure 3.2 USB2641 48-Pin QFN

Chapter 4 Block Diagrams

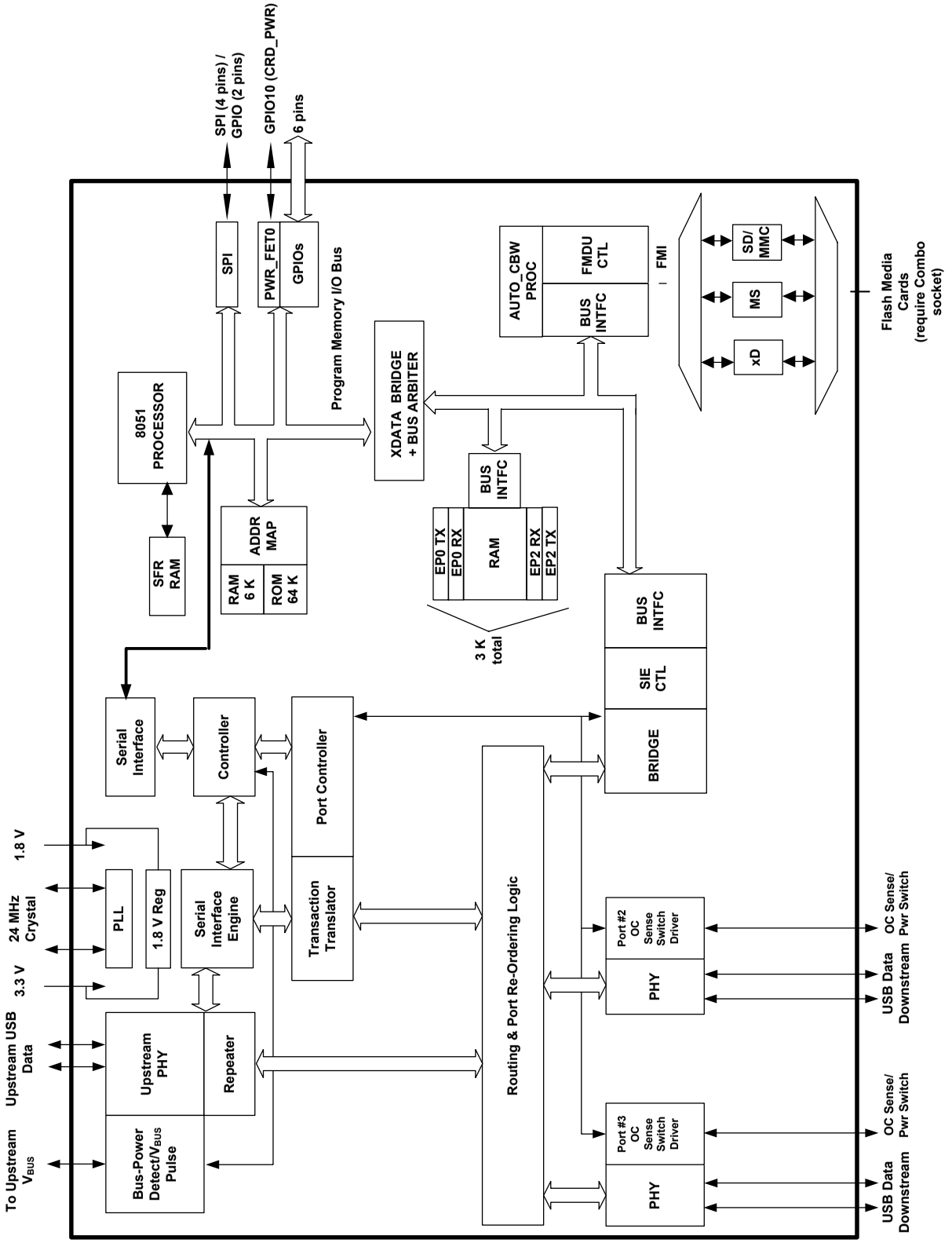

Figure 4.1 USB2640 Block Diagram

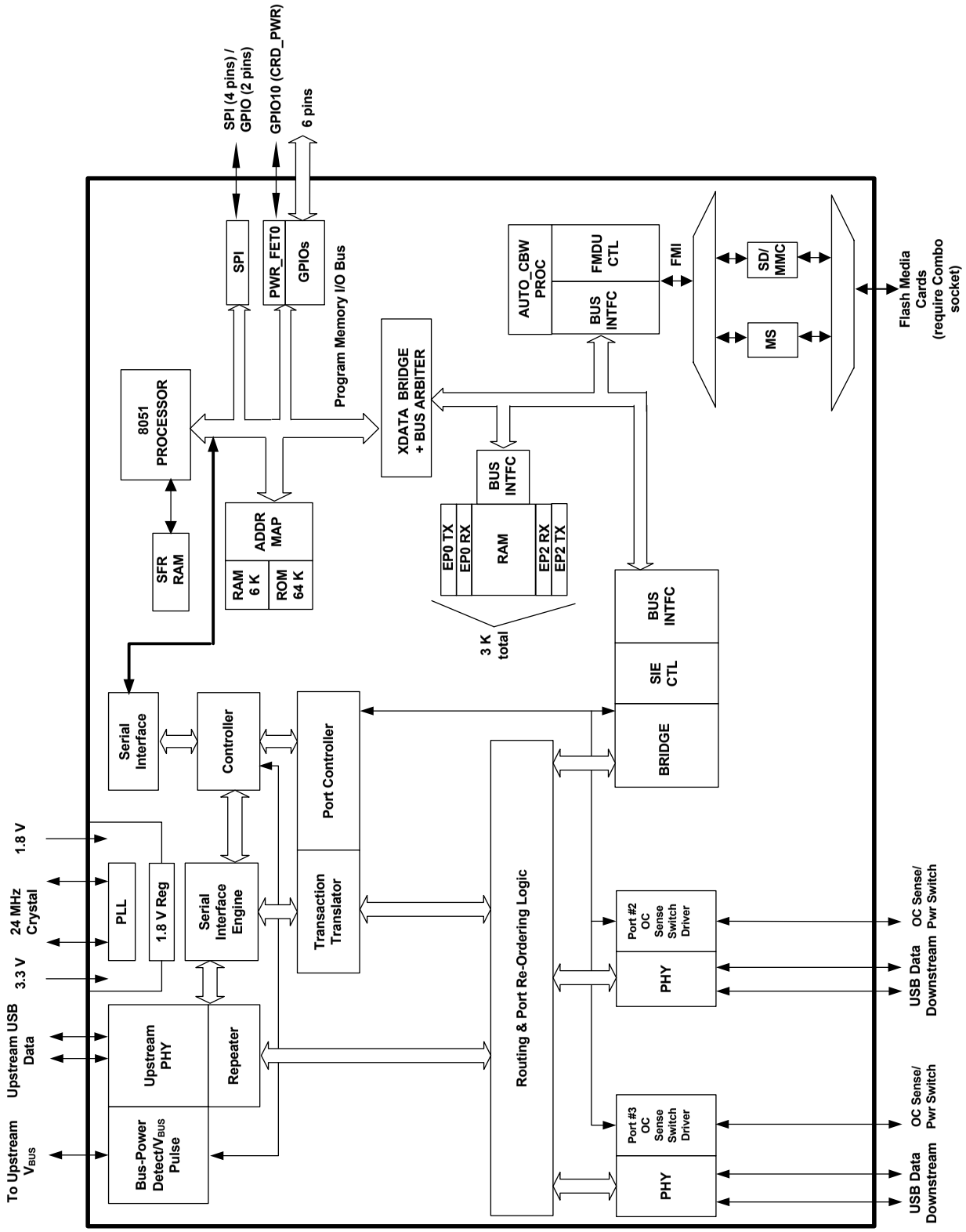

Figure 4.2 USB2641 Block Diagram

Chapter 5 Pin Tables

5.1 48-Pin Tables

Table 5.1 USB2640 48-Pin Table

xD-PICTURE CARD (Only in USB2640) / SECURE DIGITAL / MEMORY STICK INTERFACE (18 PINS)			
xD_D3 / SD_D1 / MS_D5	xD_D2 / SD_D0 / MS_D4	xD_D1 / SD_D7 / MS_D6	xD_D0 / SD_D6 / MS_D7
xD_nWP / SD_CLK / MS_BS	xD_ALE / SD_D5 / MS_D1	xD_CLE / SD_CMD / MS_D0	xD_D7 / SD_D4 / MS_D2
xD_D6 / SD_D3 / MS_D3	xD_D5 / SD_D2	xD_nRE	xD_nWE
xD_D4 / GPIO6 / SD_WP / MS_SCLK	xD_nB/R	xD_nCE	GPIO12 / MS_INS
GPIO14 / xD_nCD	GPIO15 / SD_nCD		
USB INTERFACE (5 PINS)			
USB+	USB-	XTAL1 (CLKIN)	XTAL2
RBIAS			
2-PORT USB INTERFACE (7 PINS)			
USBDN_DP2	USBDN_DM2	PRTCTL2	PRTCTL3
USBDN_DP3	USBDN_DM3	VBUS_DET	

Table 5.1 USB2640 48-Pin Table (continued)

SPI INTERFACE (4 PINS)			
SPI_CE_n	SPI_CLK / GPIO4 / SCL	SPI_DO / GPIO5 / SDA / SPI_SPD_SEL	SPI_DI
MISC (5 PINS)			
nRESET	TEST	GPIO1 / LED / TXD	GPIO2 / RXD
GPIO10 (CRD_PWR)			
POWER AND GROUND (9 PINS)			
(7) VDD33	CRFILT	PLLFILT	
TOTAL 48			

Table 5.2 USB2641 48-Pin Table

SECURE DIGITAL / MEMORY STICK INTERFACE (14 PINS)			
SD_D1 / MS_D5	SD_D0 / MS_D4	SD_D7 / MS_D6	SD_D6 / MS_D7
SD_CLK / MS_BS	SD_D5 / MS_D1	SD_CMD / MS_D0	SD_D4 / MS_D2
SD_D3 / MS_D3	SD_D2	GPIO12 / MS_INS	GPIO14
GPIO6 / SD_WP / MS_SCLK	GPIO15 / SD_nCD		
USB INTERFACE (5 PINS)			
USB+	USB-	XTAL1 (CLKIN)	XTAL2

Table 5.2 USB2641 48-Pin Table (continued)

RBIAS			
2-PORT USB INTERFACE (7 PINS)			
USBDN_DP2	USBDN_DM2	PRTCTL2	PRTCTL3
USBDN_DP3	USBDN_DM3	VBUS_DET	
SPI INTERFACE (4 PINS)			
SPI_CE_n	SPI_CLK / GPIO4 / SCL	SPI_DO / GPIO5 / SDA / SPI_SPD_SEL	SPI_DI
MISC (5 PINS)			
nRESET	TEST	GPIO1 / LED / TXD	GPIO2 / RXD
GPIO10 (CRD_PWR)			
POWER AND GROUND (13 PINS)			
(7) VDD33	CRFILT	PLLFILT	PLLFILT
(4) NC			
TOTAL 48			

Chapter 6 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The pin descriptions below are applied when using the internal default firmware and can be referenced in Chapter 7, "Configuration Options," on page 28. Please reference Chapter 2, Acronyms for a list of the acronyms used.

The “n” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “n” is not present in the signal name, the signal is asserted at a high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

6.1 USB2640/USB2641 Pin Descriptions

Table 6.1 USB2640/USB2641 Pin Descriptions

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
xD-PICTURE CARD INTERFACE (APPLIES ONLY TO USB2640)			
xD_D[7:0]	30 32 33 13 17 18 19 20	I/O12PU	xD-Picture Card Data 7-0 These pins are the bi-directional data signal xD_D7 - xD_D0 and have weak internal pull-up resistors.
xD_ALE	23	O12PD	xD-Picture Card Address Strobe This pin is an active high Address Latch Enable signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled.
xD_nB/R	28	IPU	xD-Picture Card Busy or Data Ready This pin is connected to the BSY/RDY pin of the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (the internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).

Table 6.1 USB2640/USB2641 Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
xD_nCE	26	O12PU	xD-Picture Card Chip Enable This pin is an active low chip enable signal for the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (the internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_CLE	24	O12PD	xD-Picture Card Command Strobe This pin is an active high Command Latch Enable signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled.
GPIO14 /	29	I/O12	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
xD_nCD			xD-Picture Card Detection GPIO This is a GPIO designated by the default firmware as the xD-Picture Card detection pin.
xD_nRE	27	O12PU	xD-Picture Read Enable This pin is an active low read strobe signal for the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (the internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_nWE	22	O12PU	xD-Picture Card Write Enable This pin is an active low write strobe signal for the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (the internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_nWP	21	O12PD	xD-Picture Card Write Protect This pin is an active low write protect signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled.
MEMORY STICK INTERFACE			
MS_BS	21	O12	Memory Stick Bus State This pin is connected to the bus state pin of the MS device. It is used to control the Bus States 0, 1, 2, and 3 (BS0, BS1, and BS3) of the MS device.

Table 6.1 USB2640/USB2641 Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
GPIO12 /	31	I/O12	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
MS_INS		IPU	Memory Stick Card Insertion GPIO This is a GPIO designated by the default firmware as the Memory Stick card detection pin and has an internal weak pull-up resistor.
MS_SCLK	13	O12	Memory Stick System Clock This pin is an output clock signal to the MS device.
MS_D[7:0]	20 19 17 18 32 30 23 24	I/O12PD	Memory Stick System Data In/Out These pins are the bi-directional data signals for the MS device. In serial mode, the most significant bit (MSB) of each byte is transmitted first by either MSC or MS device on MS_D0. MS_D0, MS_D2, and MS_D3 have weak pull-down resistors. MS_D1 has a pull down resistor if in parallel mode, otherwise it is disabled. In 4- or 8-bit parallel modes, all MS_D7 - MS_D0 signals have weak pull-down resistors.
SECURE DIGITAL / MULTIMEDIACARD INTERFACE			
SD_D[7:0]	19 20 23 30 32 33 17 18	I/O12PU	Secure Digital Data 7-0 These are the bi-directional data signals SD_D0-SD_D7 and have weak pull-up resistors.
SD_CLK	21	O12	Secure Digital Clock This is an output clock signal to the SD/MMC device.
SD_CMD	24	I/O12PU	Secure Digital Command This is a bi-directional signal that connects to the CMD signal of the SD/MMC device and has an internal weak pull-up resistor.
GPIO6 /	13	I/O12	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SD_WP			Secure Digital Write Protected GPIO This is a GPIO designated by the default firmware as the Secure Digital card mechanical write protect detect pin.
GPIO15 /	14	I/O12	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SD_nCD			Secure Digital Card Detect GPIO This is a GPIO designated by the default firmware as the Secure Digital card detection pin.

Table 6.1 USB2640/USB2641 Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
USB INTERFACE			
USB- USB+	43 42	I/O-U	USB Bus Data These pins connect to the upstream USB bus data signals. USB+ and USB- can be swapped using the PortSwap feature (See Section 7.3.5.20, "F1h: Port Swap," on page 46).
USBDN_DM [3:2] USBDN_DP [3:2]	3 1 4 2	I/O-U	USB Bus Data These pins connect to the downstream USB bus data signals and can be swapped using the PortSwap feature (See Section 7.3.5.20, "F1h: Port Swap," on page 46).
PRTCTL[3:2]	7 6	I/OD12PU	USB Power Enable As an output, these pins enable power to downstream USB peripheral devices and have weak internal pull-up resistors. See Section 6.3, "Port Power Control" for diagram and usage instructions. As an input, when the power is enabled, these pins monitor the over-current condition. When an over-current condition is detected, the pins turn the power off.
VBUS_DET	39	I	Detect Upstream VBUS Power Detects the state of upstream VBUS power. The Hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor (signaling a connect event). When designing a detachable hub, connect this pin to the VBUS power pin of the USB port that is upstream of the Hub. For self-powered applications with a permanently attached host, this pin should be pulled up, typically to VDD33. VBUS is a 3.3 volt input. A resistor divider must be used if connecting to 5 volts of USB power.
RBIAS	47	I-R	USB Transceiver Bias A 12.0 kΩ ±1.0% resistor is attached from VSS to this pin in order to set the transceiver's internal bias currents.
XTAL1 (CLKIN)	45	ICLKx	24 MHz Crystal Input or External clock Input This pin can be connected to one terminal of the crystal or it can be connected to an external 24 MHz 1.8 V clock when a crystal is not used.
XTAL2	44	OCLKx	24 MHz Crystal Output This is the other terminal of the crystal, or it is left open when an external clock source is used to drive XTAL1(CLKIN).

Table 6.1 USB2640/USB2641 Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
SPI INTERFACE			
SPI_CE_n	8	O12	SPI Chip Enable This is the active low chip enable output. When the SPI interface is enabled, drive this pin high in power down states.
SPI_CLK /	9	I/O12	SPI Clock This is the SPI clock out to the serial ROM. See Section 6.4, "ROM BOOT Sequence" for diagram and usage instructions. During reset, drive this pin low.
GPIO4 /			This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SCL			When configured, this is the I^2C EEPROM clock pin.
SPI_DO /	10	I/O12	SPI Data Out This is the data out for the SPI port. See Section 6.4, "ROM BOOT Sequence" for diagram and usage instructions.
GPIO5 /			This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SDA /			This pin is the data pin when the device is connected to the optional I^2C EEPROM.
SPI_SPD_SEL			This pin is used to select the speed of the SPI interface. During nRESET assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When nRESET is negated, the value on the pin will be internally latched, and the pin will revert to SPI_DO functionality, the internal pull-down will be disabled. ‘0’ = 30 MHz (No external resistor should be applied) ‘1’ = 60 MHz (A 10 K external pull-up resistor must be applied) If the latched value is '1', then the pin is tri-stated when the chip is in the suspend state. If the latched value is '0', then the pin is driven low during a suspend state.
SPI_DI	11	I/O12PD	SPI Data In This is the data in to the controller from the ROM. This pin has a weak internal pull-down applied at all times to prevent floating.
MISC			
GPIO1 /	37	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
LED /			GPIO1 can be used as an LED output.
TXD			The signal can be used as input to the TxD of UART in the device. Custom firmware is required to activate this function.

Table 6.1 USB2640/USB2641 Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
GPIO2 /	36	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
RXD			This signal can used as input to the RXD of the internal UART. Custom firmware is required to activate this function.
GPIO10 (CRD_PWR)	35	I/O200	Card power drive: 3.3 V (100 mA or 200 mA) This pin powers the multiplexed flash media interface (slot) for xD, MS, and SD/MMC. If card power is not being used to power the multiplexed flash media interface, this pin may be used as a GPIO. It is a requirement for this to be the only FET used to power xD-Picture Card devices. Failure to do this will violate xD voltage specification on xD-Picture Card device pins. Bits 0, 1, 2, and 3 control FET 2 of Register A5h. Please reference Section 7.3.4.5, "A8h: LED Blink Interval (1 byte)," on page 38.
nRESET	38	IS	RESET Input The system uses this active low signal to reset the chip. The active low pulse should be at least 1 µs wide.
TEST	40	I	TEST Input Tie this pin to ground for normal operation.
NC	22 26 27 28		No Connects No connect pins only apply to the USB2641. No trace or signal should be routed or attached to these pins.
DIGITAL / POWER / GROUND			
CRFILT	15		VDD Core Regulator Filter Capacitor This pin must have a 1.0 µF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS.
VDD33	5 12 16 25 34 41 48		3.3 V Power and Voltage Regulator Inputs Please refer to Chapter 10, "DC Parameters," on page 58 for more information. Pins 16 and 48 each require an external bypass capacitor of 4.7 µF minimum.
PLLFILT	46		PLL Regulator Filter Capacitor This pin must have a 1.0 µF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS.
VSS	ePad		The ground pad / ePad is the only VSS for the device and must be tied to ground with multiple vias.

6.2 Buffer Type Descriptions

Table 6.2 USB2640/USB2641 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input.
IPU	Input, weak internal pull-up.
IS	Input with Schmitt trigger.
I/O12	Input/output buffer with 12 mA sink and 12 mA source.
I/O200	Input/output buffer 12 mA with FET disabled, 100/200 mA source only when the FET is enabled.
I/O12PD	Input/output buffer with 12 mA sink and 12 mA source, with an internal weak pull-down resistor.
I/O12PU	Open drain, 12 mA sink with pull-up. Input with Schmitt trigger.
I/OD12PU	Input/open drain output buffer with a 12 mA sink.
O12	Output buffer with a 12 mA sink and a 12 mA source.
O12PD	Output buffer with 12 mA sink and 12 mA source, with a pull-down resistor.
O12PU	Output buffer with 12 mA sink and 12 mA source, with a pull-up resistor.
ICLKx	XTAL clock input.
OCLKx	XTAL clock output.
I/O-U	Analog input/output as defined in the USB 2.0 Specification.
I-R	RBIAS.

6.3 Port Power Control

Port Power Control Using USB Power Switch

The USB2640/USB2641 has a single port power control and over-current sense signal for each downstream port. When disabling port power, the driver will actively drive a '0'. To avoid unnecessary power dissipation, the internal pull-up resistor will be disabled at that time. When port power is enabled, the output driver is disabled, and the pull-up resistor is enabled creating an open drain output. If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmitt trigger input will detect this event as a low. The open drain output does not interfere. The internal over-current sense filter handles the transient conditions, such as low voltage, while the device is powering up.

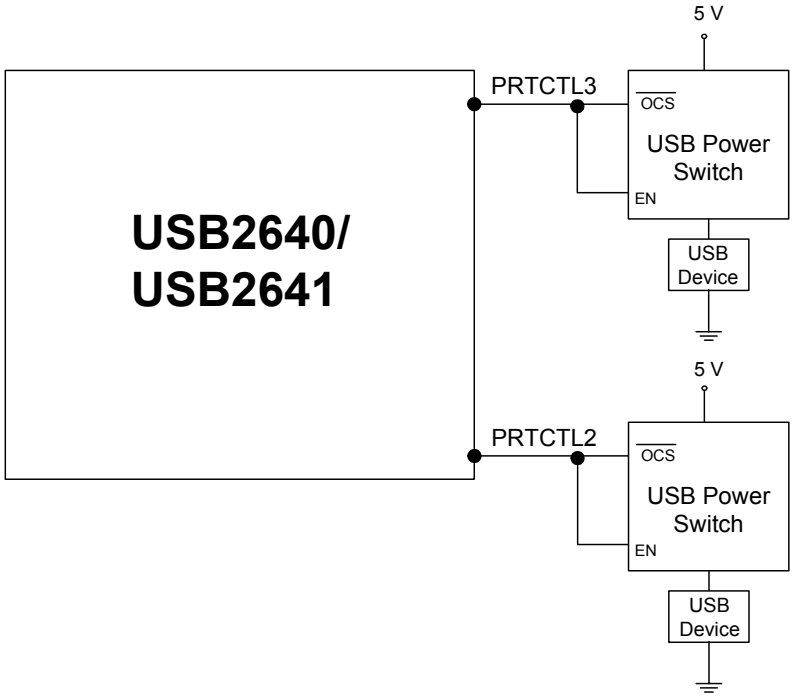

Figure 6.1 Port Power Control with USB Power Switch