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USB2660/USB2660i

Ultra Fast USB 2.0 Hub and Multi-Format Flash Media Controller with Dual SD Interfaces

PRODUCT FEATURES

Datasheet

General Description

The SMSC USB2660/USB2660i is a USB 2.0 compliant, Hi-Speed hub, card reader, and protocol converter combo solution. This fully integrated single chip solution provides USB expansion and flash card media reader/writer integration. SDIO bridging is possible with custom firmware. The SMSC USB2660/USB2660i provides an ultra fast interface between a USB host and today's popular flash media formats. The controller allows read/write capability to flash media from the following families:

- Secure Digital™ (SD)
- MultiMediaCard™ (MMC)
- Memory Stick® (MS)
- xD-Picture Card™ (xD)[1]

The USB2660/USB2660i offers a versatile, cost-effective, and energy-efficient hub controller with 2 downstream USB 2.0 ports. This combo solution leverages SMSC's innovative technology that delivers industry-leading data throughput in mixed-speed USB environments. Average sustained transfer rates exceeding 35 MB/s are possible[2].

Highlights

- 2 exposed Hi-Speed USB 2.0 downstream ports for external peripheral expansion
- The dedicated flash media reader is internally attached to a 3rd downstream port of the hub as a USB Compound Device
  - a single or multiplexed flash media reader interface
  - a non-multiplexed SD/SDIO interface (slot) for SD card reader or SDIO bridging applications
- **PortMap**
  - Flexible port mapping and port disable sequencing supports multiple platform designs
- **PortSwap**
  - Programmable USB differential-pair pin locations eases PCB design by aligning USB signal traces directly to connectors
- **PHYBoost**
  - Programmable USB transceiver drive strength recovers signal integrity

Features

- Compliance with the following flash media card specifications SD 2.0 / MMC 4.2 / MS 1.43 / MS-Pro 1.02 / MS-Pro-HG 1.01 / MS-Duo 1.10 / xD 1.2
- Supports a single external 3.3 V supply source; internal regulators provide 1.8 V internal core voltage for additional bill of materials and power savings
- The transaction translator (TT) in the hub supports operation of Full-Speed and Low-Speed peripherals
- 9 K RAM | 64 K on-chip ROM
- Enhanced EMI rejection and ESD protection performance
- Hub and flash media reader/writer configuration from a single source: External I²C® ROM or external SPI ROM
  - Configures internal code using an external I²C EEPROM
  - Supports external code using an SPI Flash EEPROM
  - Customizable vendor ID, product ID, and language ID if using an external EEPROM
- Additional SD/SDIO port for card reader or to host wireless applications such as WiFi™, Bluetooth®, and GPS
- Up to 20 configurable GPIOs for special functions
- The USB2660 supports the commercial temperature range of 0°C to +70°C
- The USB2660i supports the industrial temperature range of -40°C to +85°C
- 64-pin QFN lead-free, RoHS compliant package (9 x 9 mm)

Applications

- Desktop and mobile PCs
- Printers
- GPS navigation systems
- Media players/viewers
- Consumer A/V
- Set-top boxes
- Industrial products

1.For xD-Picture Card™ support, please obtain a user license from the xD-Picture Card License Office.
2.Host and media dependent.

ORDER NUMBERS:

USB2660/USB2660i-JZX for 64-PIN, QFN LEAD-FREE RoHS COMPLIANT PACKAGE

THIS PRODUCT MEETS THE HALOGEN MAXIMUM CONCENTRATION VALUES PER IEC61249-2-21.

FOR ROHS COMPLIANCE AND ENVIRONMENTAL INFORMATION, PLEASE VISIT WWW.SMSC.COM/ROHS.

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Table of Contents

List of Tables

List of Figures

Chapter 1 Overview

The SMSC USB2660/USB2660i is an integrated USB 2.0 compliant, Hi-Speed hub, card reader, and protocol converter combo solution. This combo solution supports today's popular multi-format flash media cards. This multi-format flash media controller and USB hub combo features two exposed downstream USB ports available for external peripheral expansion. The dedicated flash media reader/writer is internally attached to a third downstream port of the hub as a USB Compound Device which supports the following two interfaces: One interface is multiplexed for xD-Picture Card, Memory Stick, Secure Digital/MultiMediaCard, and SD/Secure Digital Input/Output. The other interface is dedicated to a second SD card slot for SDIO bridging applications. SDIO bridging is possible with custom firmware.

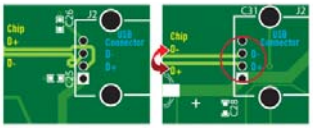
The USB2660/USB2660i will attach to an upstream port as a Full-Speed hub or as a Full-/Hi-Speed hub. The hub supports Low-Speed, Full-Speed, and Hi-Speed (if operating as a Hi-Speed hub) downstream devices on all of the enabled downstream ports.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

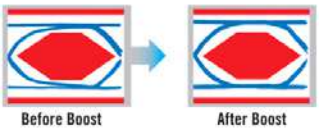
The USB2660/USB2660i includes programmable features such as:

PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB2660/USB2660i hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB2660/USB2660i automatically reorders the remaining ports to match the USB host controller's port numbering scheme.

PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors avoiding uneven trace length or crossing of the USB differential signals on the PCB.



PHYBoost which enables four programmable levels of USB signal drive strengths in downstream port transceivers. PHYBoost attempts to restore USB signal integrity. The diagram on the right shows an example of Hi-Speed USB eye diagrams before (PHYBoost at 0%) and after (PHYBoost at 12%) signal integrity restoration in a compromised system environment.



Hardware Features

- Single chip hub and flash media controller combo
- USB2660 supports the commercial temperature range of 0°C to +70°C
- USB2660i supports the industrial temperature range of -40°C to +85°C
- Transaction translator (TT) in the hub supports operation of FS and LS peripherals
- Full power management with individual or ganged power control of each downstream port
- Optional support for external firmware access via SPI interface
- Onboard 24 MHz crystal driver circuit
- Optional external 24 MHz clock input which must be a 1.8 V signal
- Code execution via SPI ROM which must meet
  - 30 MHz or 60 MHz operation support
  - Single bit or dual bit mode support
  - Mode 0 or mode 3 SPI support

  Compliance with the following flash media card specifications:
- Secure Digital 2.0 / MultiMediaCard 4.2
  - SD 2.0, SD-HS, SD-HC
  - TransFlash™ and reduced form factor media
  - 1/4/8 bit MMC 4.2
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  - Memory Stick, MS Duo, MS-HS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- xD-Picture Card 1.2
- Up to 20 GPIOs: Configuration and polarity for special function use
  - The number of actual GPIOs depends on the implementation configuration used
  - Two GPIOs available with up to 200 mA drive and protected “fold-back” short circuit current
- 8051 8-bit microprocessor
  - 60 MHz - single cycle execution
  - 64 KB ROM | 9 KB RAM
- Integrated regulator for 1.8 V core operation

Software Features

- Hub and flash media reader/writer configuration from a single source:
  External I^2C ROM or external SPI ROM
- If the OEM is using an external EEPROM or an external SPI ROM, the following features are available:
  - Customizable vendor ID, product ID, and device ID
  - 12-hex digits maximum for the serial number string
  - 28-character manufacturer ID and product strings for the flash media reader/writer

OEM Selectable Hub Features

A default configuration is available in the USB2660/USB2660i following a reset. The USB2660/USB2660i may also be configured by an external I^2C EEPROM or via external SPI ROM flash.

- Compound Device support on a port-by-port basis
  - a port is permanently hardwired to a downstream USB peripheral device
- Select over-current sensing and port power control on an individual or ganged (all ports together) basis to match the OEM's choice of circuit board component selection
- Port power control and over-current detection/delay features
- Configure the delay time for filtering the over-current sense inputs
- Configure the delay time for turning on downstream port power
- Bus- or self-powered selection
- Hub port disable or non-removable configurations
- Flexible port mapping and disable sequencing supports multiple platform designs
- Programmable USB differential-pair pin location eases PCB layout by aligning USB signal lines directly to connectors
- Programmable USB signal drive strength recovers USB signal integrity using 4 levels of signal drive strength
- Indicate the maximum current that the 2-port hub consumes from the USB upstream port
- Indicate the maximum current required for the hub controller

Chapter 2 Acronyms

ACK: Handshake packet (positive acknowledgement)

EOP: End of Packet

EOF: End of (micro) Frame

FM: Flash Media

FMC: Flash Media Controller

FS: Full-Speed Device

LS: Low-Speed Device

HS: Hi-Speed Device

I^2C®: Inter-Integrated Circuit[1]

MMC: MultiMediaCard

MS: Memory Stick

MSC: Memory Stick Controller

OCS: Over-current Sense

PHY: Physical Layer

PLL: Phase-Locked Loop

RXD: Received eXchange Data

SD: Secure Digital

SDC: Secure Digital Controller

TXD: Transmit eXchange Data

UART: Universal Asynchronous Receiver-Transmitter

UCHAR: Unsigned Character

UINT: Unsigned Integer

1. I^2C is a registered trademark of Philips Corporation.

Chapter 3 Pin Configuration

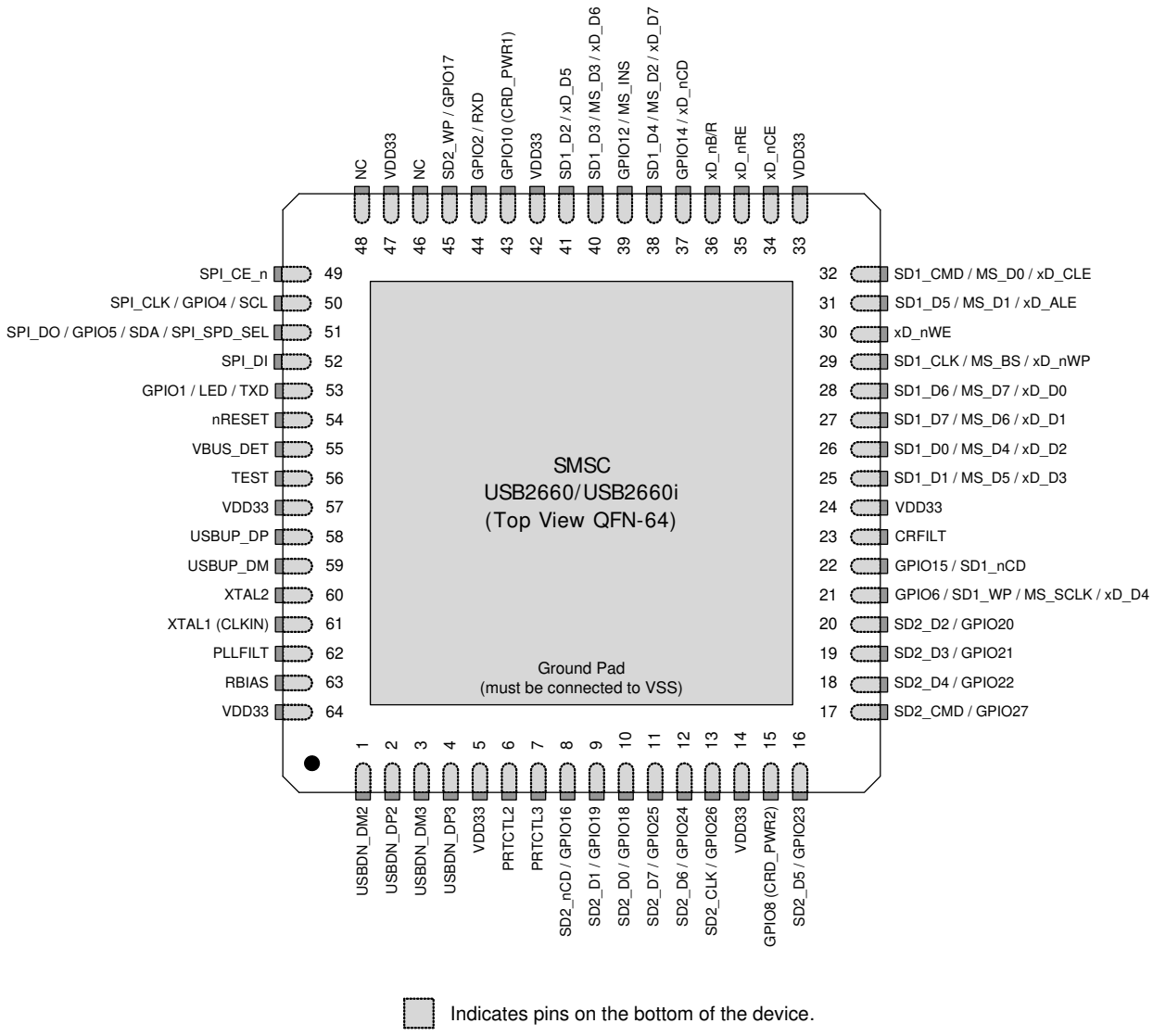


Figure 3.1 USB2660/USB2660i 64-Pin QFN

Chapter 4 Block Diagram

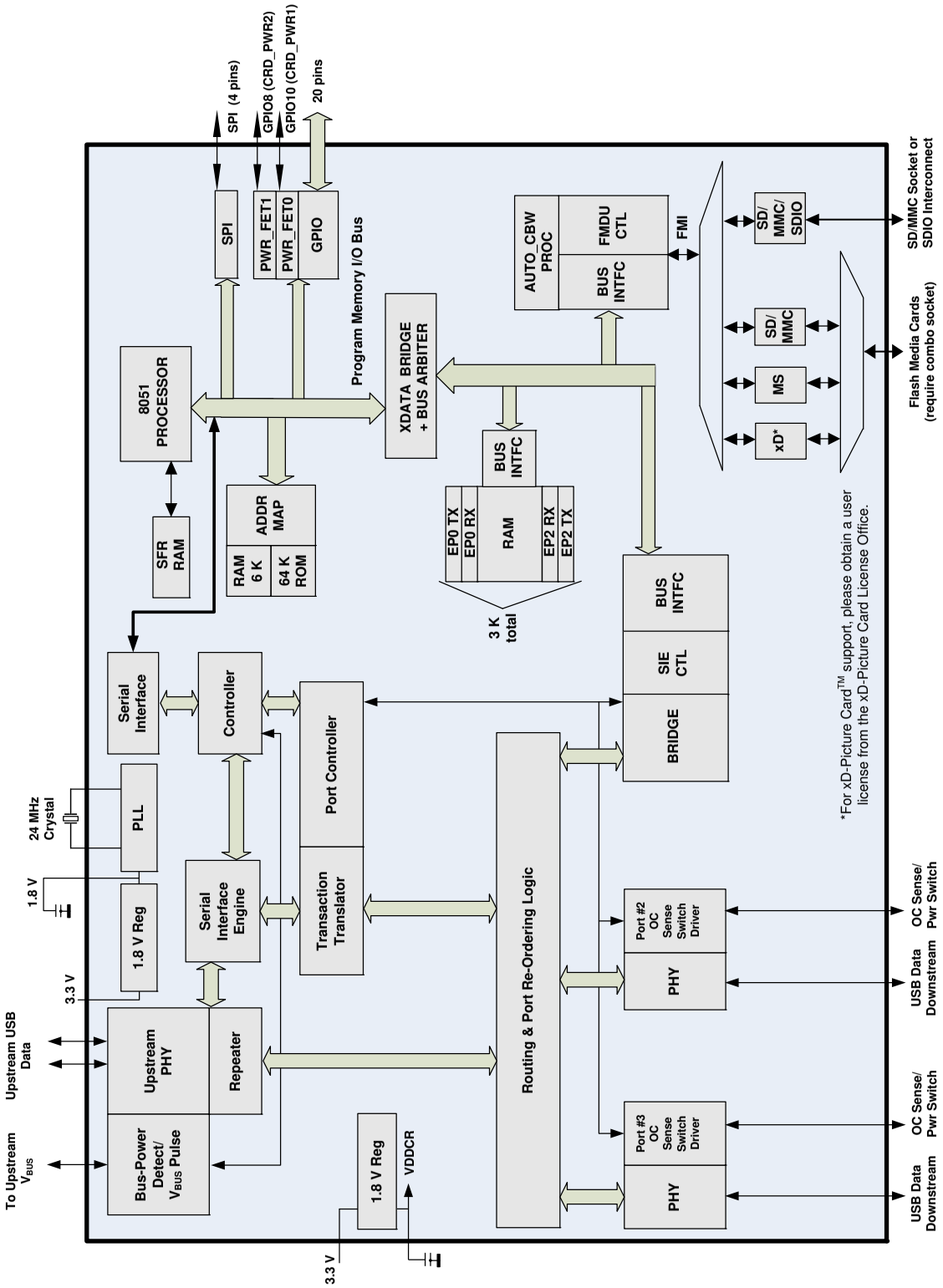


Figure 4.1 USB2660/USB2660i Block Diagram

Chapter 5 Pin Table

5.1 64-Pin Table

Table 5.1 USB2660/USB2660i 64-Pin Table

SECURE DIGITAL / MEMORY STICK / xD INTERFACE (18 PINS)			
SD1_D7 / MS_D6 / xD_D1	SD1_D6 / MS_D7 / xD_D0	SD1_D5 / MS_D1 / xD_ALE	SD1_D4 / MS_D2 / xD_D7
SD1_D3 / MS_D3 / xD_D6	SD1_D2 / xD_D5	SD1_D1 / MS_D5 / xD_D3	SD1_D0 / MS_D4 / xD_D2
SD1_CLK / MS_BS / xD_ nWP	SD1_CMD / MS_D0 / xD_CLE	GPIO15 / SD1_nCD	GPIO12 / MS_INS
GPIO6 / SD1_WP / MS_SCLK / xD_D4	GPIO14 / xD_nCD	xD_nB/R	xD_nRE
xD_nCE	xD_nWE		
SECOND SECURE DIGITAL INTERFACE (12 PINS)			
SD2_D7 / GPIO25	SD2_D6 / GPIO24	SD2_D5 / GPIO23	SD2_D4 / GPIO22
SD2_D3 / GPIO21	SD2_D2 / GPIO20	SD2_D1 / GPIO19	SD2_D0 / GPIO18
SD2_nCD / GPIO16	SD2_CLK / GPIO26	SD2_CMD / GPIO27	SD2_WP / GPIO17
USB INTERFACE (5 PINS)			
USBUP_DP	USBUP_DM	XTAL1 (CLKIN)	XTAL2
RBIAS			
2-PORT USB INTERFACE (7 PINS)			
USBDN_DP2	USBDN_DM2	PRTCTL2	PRTCTL3
USBDN_DP3	USBDN_DM3	VBUS_DET	

Table 5.1 USB2660/USB2660i 64-Pin Table (continued)

SPI INTERFACE (4 PINS)			
SPI_CE_n	SPI_CLK / GPIO4 / SCL	SPI_DO / GPIO5 / SDA / SPI_SPD_SEL	SPI_DI
MISC (8 PINS)			
nRESET	TEST	GPIO1 / LED / TXD	GPIO2 / RXD
GPIO8 (CRD_PWR2)	GPIO10 (CRD_PWR1)	(2) NC	
POWER (10 PINS)			
(8) VDD33	CRFILT	PLLFILT	
TOTAL 64			

Chapter 6 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The pin descriptions below are applied when using the internal default firmware and can be referenced in Chapter 8, "Configuration Options," on page 29. Please reference Chapter 2, "Acronyms," on page 10 for a list of the acronyms used.

The “n” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “n” is not present in the signal name, the signal is asserted at a high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

6.1 USB2660/USB2660i Pin Descriptions

Table 6.1 USB2660/USB2660i Pin Descriptions

SYMBOL	64-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
SECURE DIGITAL INTERFACE			
SD1_D[7:0]	27 28 31 38 40 41 25 26	I/O8PU	Secure Digital Data 7-0 These are the bi-directional data signals SD_D0 - SD_D7 with weak pull-up resistors.
SD1_CLK	29	O8	Secure Digital Clock This is an output clock signal to the SD/MMC device.
SD1_CMD	32	I/O8PU	Secure Digital Command This is a bi-directional signal that connects to the CMD signal of the SD/MMC device. The bi-directional signal has a weak internal pull-up resistor.
GPIO15 /	22	I/O6	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SD1_nCD		I/O8PU	Secure Digital Card Detect GPIO This is a GPIO designated by the default firmware as the Secure Digital card detection pin and has an internal pull-up.

Table 6.1 USB2660/USB2660i Pin Descriptions (continued)

SYMBOL	64-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
GPIO6 /	21	I/O6	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SD1_WP		I/O8	Secure Digital Write Protected GPIO This is a GPIO designated by the default firmware as the Secure Digital card mechanical write protect detect pin.
SECOND SECURE DIGITAL INTERFACE			
SD2_D[7:0] /	11 12 16 18 19 20 9 10	I/O8PU	SD2 Data 7-0 These are the bi-directional data signals SD2_D0 - SD2_D7 and have weak pull-up resistors.
GPIO[25:18]		I/O6	These general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SD2_CLK /	13	O8	SD2 Clock GPIO This is an output clock signal designated by the default firmware to the SD2/MMC device.
GPIO26		I/O6	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SD2_CMD /	17	I/O8PU	SD2 Command GPIO This is a bi-directional signal designated by the default firmware that connects to the CMD signal of the SD2/MMC device. The bi-directional signal has a weak internal pull-up resistor.
GPIO27		I/O6	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SD2_nCD /	8	I/O8	SD2 Card Detect GPIO This is a GPIO designated by the default firmware as the second Secure Digital card detection pin and has an internal pull-up.
GPIO16		I/O6	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SD2_WP /	45	I/O8	SD2 Write Protected GPIO This is a GPIO designated by the default firmware as the second Secure Digital card interface mechanical write detect pin.
GPIO17		I/O6	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.

Table 6.1 USB2660/USB2660i Pin Descriptions (continued)

SYMBOL	64-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
MEMORY STICK INTERFACE			
MS_BS	29	O8	Memory Stick Bus State This pin is connected to the bus state pin of the MS device. It is used to control the Bus States 0, 1, 2, and 3 (BS0, BS1, and BS3) of the MS device.
GPIO12 /	39	I/O6	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
MS_INS		IPU	Memory Stick Card Insertion GPIO This is a GPIO designated by the default firmware as the Memory Stick card detection pin and has a weak internal pull-up resistor.
MS_SCLK	21	O8	Memory Stick System Clock This pin is an output clock signal to the MS device.
MS_D[7:0]	28 27 25 26 40 38 31 32	I/O8PD	Memory Stick System Data In/Out These pins are the bi-directional data signals for the MS device. In serial mode, the most significant bit (MSB) of each byte is transmitted first by either MSC or MS device on MS_D0. MS_D0, MS_D2, and MS_D3 have weak pull-down resistors. MS_D1 has a pull-down resistor if in parallel mode, otherwise it is disabled. In 4- or 8-bit parallel modes, all MS_D7 - MS_D0 signals have weak pull-down resistors.
xD-PICTURE CARD INTERFACE			
xD_D[7:0]	38 40 41 21 25 26 27 28	I/O8PD	xD-Picture Card Data 7-0 These pins are the bi-directional data signals xD_D7 - xD_D0 and have weak internal pull-down resistors.
xD_ALE	31	O8PD	xD-Picture Card Address Strobe This pin is an active high Address Latch Enable (ALE) signal for the xD device. This pin has a weak pull-down resistor that is permanently enabled.
xD_nB/R	36	IPU	xD-Picture Card Busy or Data Ready This pin is connected to the BSY/RDY pin of the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (the internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).

Table 6.1 USB2660/USB2660i Pin Descriptions (continued)

SYMBOL	64-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
xD_nCE	34	O8PU	xD-Picture Card Chip Enable This pin is an active low chip enable signal for the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_CLE	32	O8PD	xD-Picture Card Command Strobe This pin is an active high Command Latch Enable signal for the xD device. This pin has a weak pull-down resistor that is permanently enabled.
GPIO14 /	37	I/O6	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
xD_nCD		I/O8	xD-Picture Card Detection GPIO This is a GPIO designated by the default firmware as the xD-Picture Card detection pin.
xD_nRE	35	O8PU	xD-Picture Card Read Enable This pin is an active low read strobe signal for the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_nWE	30	O8PU	xD-Picture Card Write Enable This pin is an active low write strobe signal for the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_nWP	29	O8PD	xD-Picture Card Write Protect This pin is an active low write protect signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled.

Table 6.1 USB2660/USB2660i Pin Descriptions (continued)

SYMBOL	64-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
USB INTERFACE			
USBUP_DM USBUP_DP	59 58	I/O-U	USB Bus Data These pins connect to the upstream USB bus data signals (host port or upstream hub). USBUP_DM and USBUP_DP can be swapped using the PortSwap feature (See Section 8.4.4.20, "F1h: Port Swap," on page 48).
USBDN_DM [3:2] USBDN_DP [3:2]	3 1 4 2	I/O-U	USB Bus Data These pins connect to the downstream USB bus data signals and can be swapped using the PortSwap feature (See Section 8.4.4.20, "F1h: Port Swap," on page 48).
PRTCTL[3:2]	7 6	I/OD6 PU	USB Power Enable As an output, these pins enable power to downstream USB peripheral devices and have weak internal pull-up resistors. See Section 6.3, "Port Power Control" for diagram and usage instructions. As an input, when the power is enabled, these pins monitor the over-current condition. When an over-current condition is detected, the pins turn the power off.
VBUS_DET	55	I	Detect Upstream VBUS Power Detects the state of upstream VBUS power. The hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor (signaling a connect event). When designing a detachable hub, connect this pin to the VBUS power pin of the USB port that is upstream of the hub. For self-powered applications with a permanently attached host, this pin should be pulled up, typically to VDD33. VBUS is a 3.3 volt input. A resistor divider must be used if connecting to 5 volts of USB power.
RBIAS	63	I-R	USB Transceiver Bias A 12.0 kΩ, ±1.0% resistor is attached from VSS to this pin in order to set the transceiver's internal bias currents.
XTAL1 (CLKIN)	61	ICLKx	24 MHz Crystal Input or External Clock Input This pin can be connected to one terminal of the crystal or it can be connected to an external 24 MHz clock when a crystal is not used.
XTAL2	60	OCLKx	24 MHz Crystal Output This is the other terminal of the crystal, or it is left open when an external clock source is used to drive XTAL1(CLKIN).
SPI INTERFACE			
SPI_CE_n	49	O12	SPI Chip Enable This is the active low chip enable output. If the SPI interface is enabled, this pin must be driven high in power down states.

Table 6.1 USB2660/USB2660i Pin Descriptions (continued)

SYMBOL	64-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
SPI_CLK /	50	I/O12	This is the SPI clock out to the serial ROM. See Section 6.4, "ROM BOOT Sequence" for diagram and usage instructions. During reset, drive this pin low.
GPIO4 /		I/O6	This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SCL			When configured, this is the I^2C EEPROM clock pin.
SPI_DO /	51	I/O12	This is the data out for the SPI port. See Section 6.4, "ROM BOOT Sequence" for diagram and usage instructions.
GPIO5 /		I/O6	This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SDA /			This pin is the data pin when the device is connected to the optional I^2C EEPROM.
SPI_SPD_SEL		I/O12	This pin is used to select the speed of the SPI interface. During nRESET assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When nRESET is negated, the value on the pin will be internally latched, and the pin will revert to SPI_DO functionality, the internal pull-down will be disabled. '0' = 30 MHz (No external resistor should be applied.) '1' = 60 MHz (A 10 K external pull-up resistor must be applied.) If the latched value is '1', then the pin is tri-stated when the chip is in the suspend state. If the latched value is '0', then the pin is driven low during a suspend state.
SPI_DI	52	I/O12PD	This is the data in to the controller from the ROM. This pin has a weak internal pull-down applied at all times to prevent floating.
MISC			
GPIO1 /	53	I/O6	General Purpose I/O This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
LED /			GPIO1 can be used as an LED output.
TXD			This signal can be configured as the TXD output of the internal UART. Custom firmware is required to activate this function.
GPIO2 /	44	I/O6	This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
RXD			This signal can be configured as input to the RXD of the internal UART. Custom firmware is required to activate this function.

Table 6.1 USB2660/USB2660i Pin Descriptions (continued)

SYMBOL	64-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
GPIO8 (CRD_PWR2)	15	I/O200	Card power drive: 3.3 V (100 mA or 200 mA) This pin specifically powers the second Secure Digital interface (slot). If card power is not being used to power the second SD interface, this pin may be used as a GPIO. Please reference Section 8.4.5.9, "147h-14Bh: Device to LUN Mapping," on page 52.
GPIO10 (CRD_PWR1)	43	I/O200	Card power drive: 3.3 V (100 mA or 200 mA) This pin powers the multiplexed flash media interface (slot) for xD, MS, and SD/MMC. If card power is not being used to power the multiplexed flash media interface, this pin may be used as a GPIO. Please reference Section 8.4.2.3, "A4h-A5h: Smart Media Device Power Configuration," on page 39.
nRESET	54	IS	RESET Input The system uses this active low signal reset the chip. The active low pulse should be at least 1 µs wide.
TEST	56	I	TEST Input Tie this pin to ground for normal operation.
DIGITAL / POWER / GROUND			
CRFILT	23		VDD Core Regulator Filter Capacitor This pin requires a 1.0 µF (or greater) ± 20% (ESR <0.1Ω) capacitor to VSS.
PLLFILT	62		Phase-locked Loop Regulator Filter Capacitor This pin requires 1.0 µF (or greater) ± 20% (ESR <0.1Ω) capacitor to VSS.
VDD33	5 14 24 33 42 47 57 64		3.3 V Power and Regulator Input Please refer to Chapter 10, "DC Parameters," on page 58 for more information. Pins 24 and 64 require external bypass capacitors of 4.7 µF minimum.
VSS	ePad		The ground pad is the only VSS for the device and must be tied to ground with multiple vias.
NC	46 48		No Connect pins No trace or signal should be routed/attached to these pins.

6.2 Buffer Type Descriptions

Table 6.2 USB2660/USB2660i Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input.
IPU	Input with weak internal pull-up.
IS	Input with Schmitt trigger.
I/O6	Input/output buffer with 6 mA sink and 6 mA source.
I/OD6PU	Input/open drain output buffer with a 6 mA sink.
O8	Output buffer with an 8 mA sink and an 8 mA source.
O8PD	Output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-down resistor.
O8PU	Output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-up resistor.
I/O8	Input/output buffer with an 8 mA sink and an 8 mA source.
I/O8PD	Input/output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-down resistor.
I/O8PU	Input/output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-up resistor.
O12	Output buffer with a 12 mA sink and a 12 mA source.
I/O12	Input/output buffer with 12 mA sink and 12 mA source.
I/O12PD	Input/output buffer with 12 mA sink and 12 mA source with a weak internal pull-down resistor.
I/O200	Input/output buffer 12 mA with FET disabled, 100/200 mA source only when the FET is enabled.
ICLKx	XTAL clock input.
OCLKx	XTAL clock output.
I/O-U	Analog input/output as defined in the USB 2.0 Specification.
I-R	RBIAS.

6.3 Port Power Control

Port Power control using a USB Power Switch

The USB2660/USB2660i has a single port power control and over-current sense signal for each downstream port. When disabling port power, the driver will actively drive a '0'. To avoid unnecessary power dissipation, the internal pull-up resistor will be disabled at that time. When port power is enabled, the output driver is disabled, and the pull-up resistor is enabled creating an open drain output.

If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmitt trigger input will detect this event as a low. The open drain output does not interfere. The internal over-current sense filter handles the transient conditions, such as low voltage, while the device is powering up.

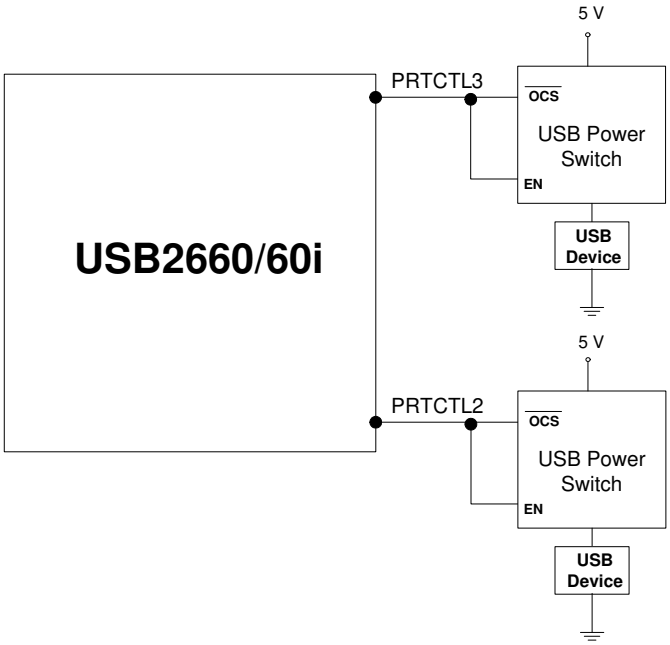


Figure 6.1 Port Power Control with USB Power Switch

Port Power control using a Poly Fuse

When using the USB2660/USB2660i with a poly fuse, an external diode must be used (See Figure 6.2). When disabling port power, the USB2660/USB2660i will drive a '0'. This procedure will have no effect since the external diode will isolate the pin from the load. When port power is enabled, the USB2660/USB2660i output driver is disabled, and the pull-up resistor is enabled which creates an open drain output. This open drain output condition means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open. This will cause the cathode of the diode to go to zero volts. The anode of the diode will be at 0.7 volts, and the Schmitt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

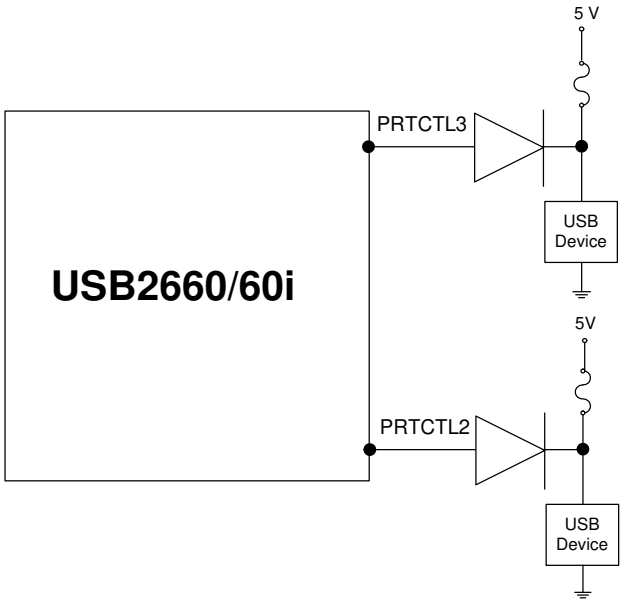


Figure 6.2 Port Power Control with a Single Poly Fuse and Multiple Loads

When using a single poly fuse to power all devices, note that for the ganged situation, all power control pins must be tied together.

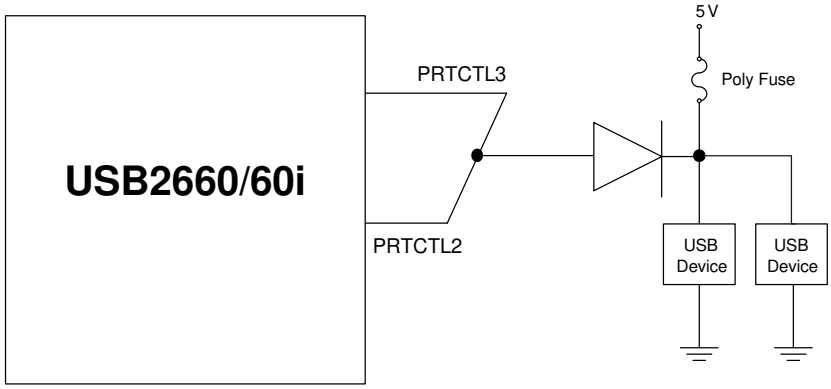


Figure 6.3 Port Power with Ganged Control with Poly Fuse

6.4 ROM BOOT Sequence

After power-on reset, the internal firmware checks for an external SPI flash device that contains a valid signature of "2DFU" (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and code execution begins at address 0x0000 in the external SPI device. Otherwise, code execution continues from the internal ROM.

If there is no SPI ROM detected, the internal firmware then checks for the presence of an I^2C ROM. The firmware looks for the signature 'ATA2' at the offset of FCh-FFh and 'ecf1' at the offset of 17Ch-17Fh in the I^2C ROM. The firmware reads in the I^2C ROM to configure the hardware and software internally. Please refer to Section 8.3.2, "EEPROM Data Descriptor," on page 30 for the details of the configuration options.

The SPI ROM required for the USB2660/USB2660i is a recommended minimum of 1 Mbit and support either 30 MHz or 60 MHz. The frequency used is set using the SPI_SPD_SEL. For 30 MHz operation, this pin must be pulled to ground through a 100 kΩ resistor. For 60 MHz operation, this pin must pulled up through a 100 kΩ resistor.

The SPI_SPD_SEL pin is used to choose the speed of the SPI interface. During nRESET assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When nRESET is negated, the value on the pin will be internally latched, and the pin will revert to SPI_DO functionality. The internal pull-down will be disabled.

The firmware can determine the speed of operation on the SPI port by checking the SPI_SPEED in the SPI_CTL register (0x2400 - RESET = 0x02). Both 1- and 2-bit SPI operation is supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMS are also supported.

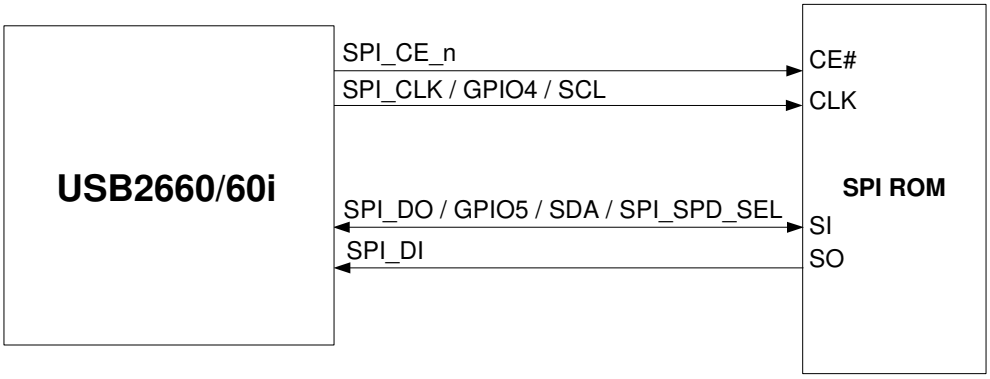


Figure 6.4 SPI ROM Connection

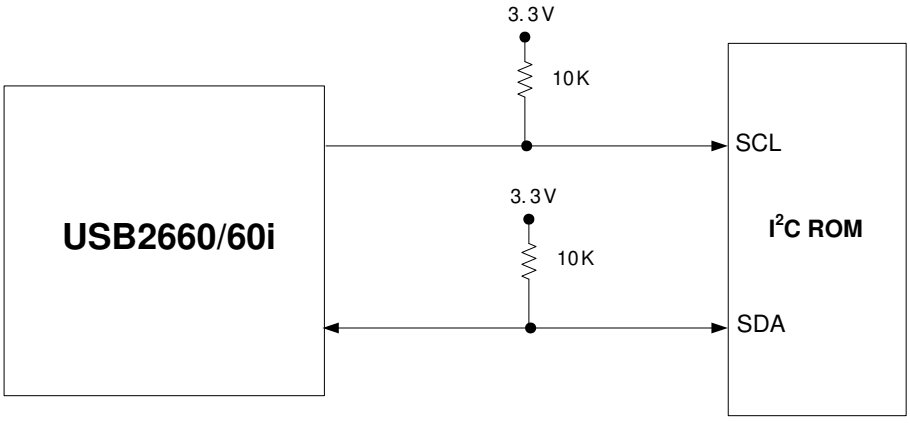


Figure 6.5 I^2C Connection