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USB3250

Hi-Speed USB Device Transceiver with UTMI Interface

Highlights

- USB-IF "Hi-Speed" certified to USB 2.0 electrical specification
- Interface compliant with the UTMI specification (60MHz 8-bit unidirectional interface or 30MHz 16-bit bidirectional interface)
- Supports 480Mbps High Speed (HS) and 12Mbps Full Speed (FS) serial data transmission rates
- Integrated 45Ω and 1.5kΩ termination resistors reduce external component count
- Internal short circuit protection of DP and DM lines
- On-chip oscillator operates with low cost 12MHz crystal
- Robust and low power digital clock and data recovery circuit
- SYNC and EOP generation on transmit packets and detection on receive packets
- NRZI encoding and decoding
- Bit stuffing and unstuffing with error detection
- Supports the USB suspend state, HS detection, HS Chirp, Reset and Resume
- Support for all test modes defined in the USB 2.0 specification
- Draws 72mA (185mW) maximum current consumption in HS mode - ideal for bus powered functions
- On-die decoupling capacitance and isolation for immunity to digital switching noise
- Available in a 56-pin VQFN package
- Full industrial operating temperature range from -40°C to +85°C (ambient)

Applications

The Universal Serial Bus (USB) is the preferred interface to connect Hi-Speed PC peripherals.

- Digital Still and Video Cameras
- MP3 Players
- External Hard Drives
- Scanners
- Entertainment Devices
- Printers
- Test and Measurement Systems
- POS Terminals
- Set Top Boxes

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Table of Contents

1.0 GENERAL DESCRIPTION

The USB3250 provides the Physical Layer (PHY) interface to a USB 2.0 Device Controller. The IC is available in a 56-pin VQFN.

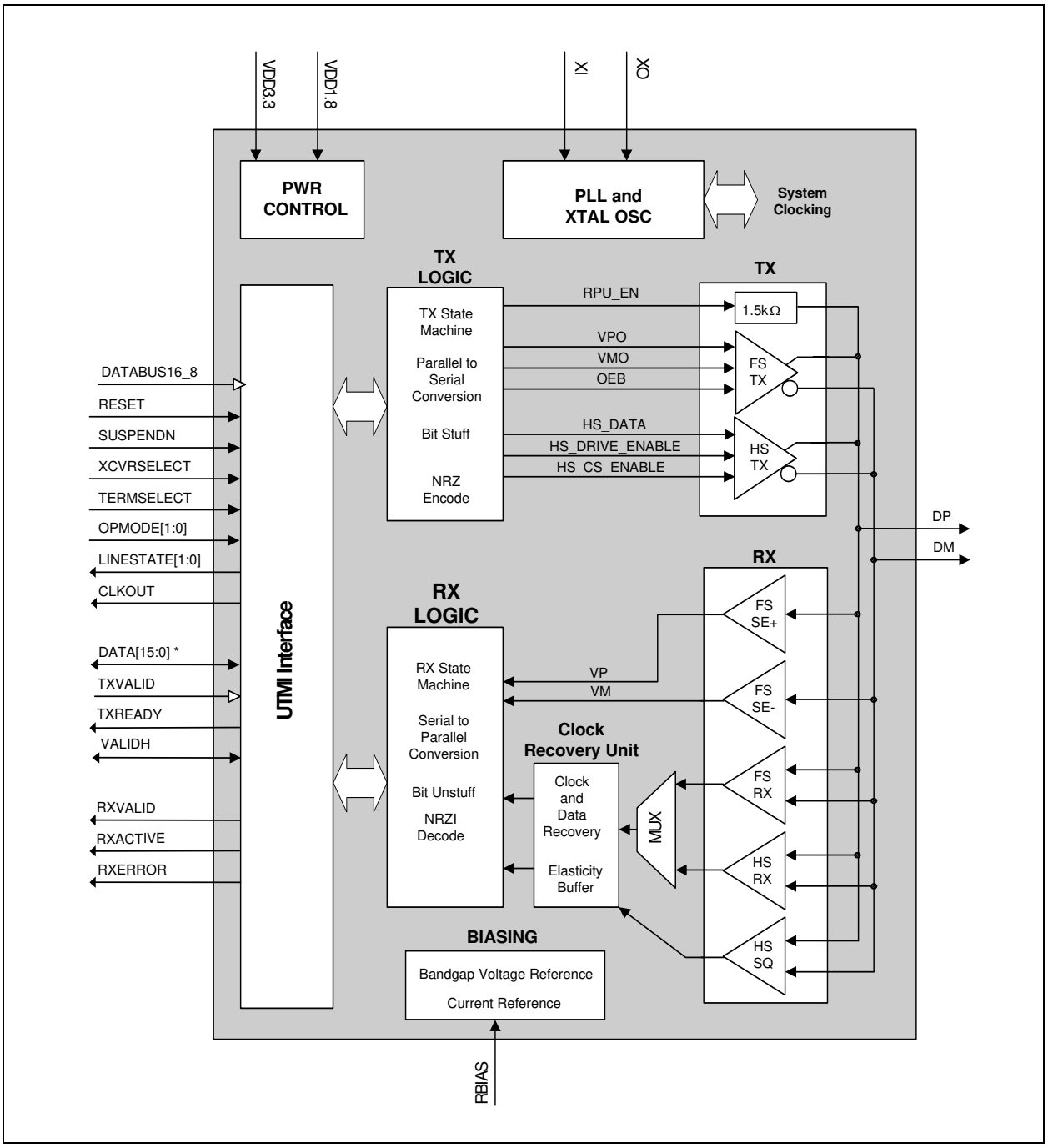
The USB3250 is a USB 2.0 physical layer transceiver (PHY) integrated circuit. Microchip's proprietary technology results in low power dissipation, which is ideal for building a bus powered USB 2.0 peripheral. The PHY can be configured for either an 8-bit unidirectional or a 16-bit bidirectional parallel interface, which complies with the USB Transceiver Macrocell Interface (UTMI) specification. It supports 480Mbps transfer rate, while remaining backward compatible with USB 1.1 legacy protocol at 12Mbps.

All required termination for the USB 2.0 Transceiver is internal. Internal 5.25V short circuit protection of DP and DM lines is provided for USB compliance.

While transmitting data, the PHY serializes data and generates SYNC and EOP fields. It also performs needed bit stuffing and NRZI encoding. Likewise, while receiving data, the PHY de-serializes incoming data, stripping SYNC and EOP fields and performs bit un-stuffing and NRZI decoding.

2.0 FUNCTIONAL BLOCK DIAGRAM

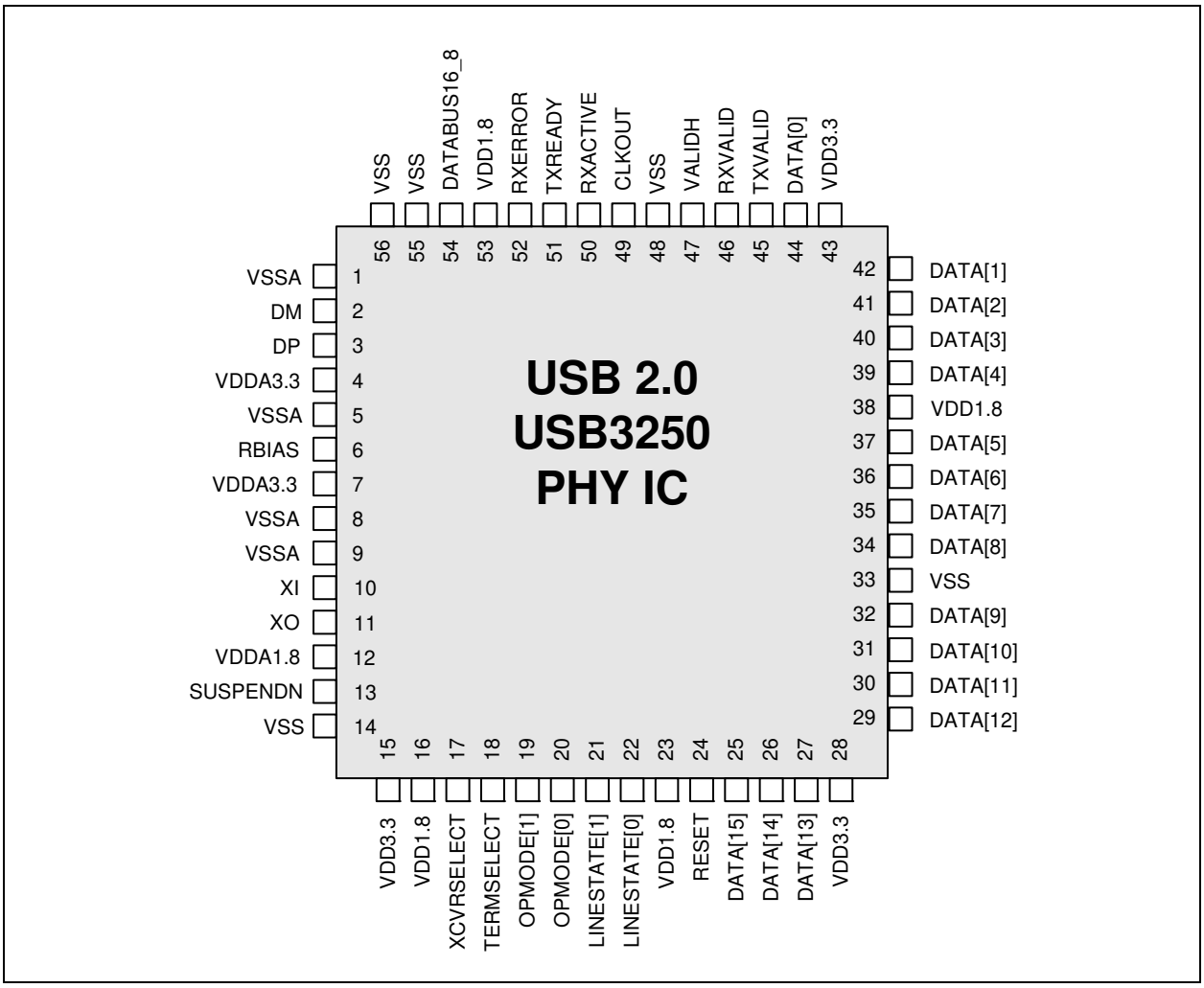
FIGURE 2-1: BLOCK DIAGRAM



Note: See Section 7.1, "Modes of Operation," on page 19 for a description of the digital interface.

3.0 PIN CONFIGURATION

FIGURE 3-1: 56-PIN USB3250 PIN CONFIGURATION (TOP VIEW)



4.0 INTERFACE SIGNAL DEFINITION

TABLE 4-1: SYSTEM INTERFACE SIGNALS

Name	Direction	Active Level	Description
RESET	Input	High	**Reset.** Reset all state machines. After coming out of reset, must wait 5 rising edges of clock before asserting TXValid for transmit. Assertion of Reset: May be asynchronous to CLKOUT. De-assertion of Reset: Must be synchronous to CLKOUT unless RESET is asserted longer than two periods of CLKOUT.
XCVRSELECT	Input	N/A	**Transceiver Select.** This signal selects between the FS and HS transceivers: 0: HS transceiver enabled 1: FS transceiver enabled.
TERMSELECT	Input	N/A	**Termination Select.** This signal selects between the FS and HS terminations: 0: HS termination enabled 1: FS termination enabled
SUSPENDN	Input	Low	**Suspend.** Places the transceiver in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for Suspend/Resume operation. While suspended, TERMSELECT must always be in FS mode to ensure that the 1.5k Ω pull-up on DP remains powered. 0: Transceiver circuitry drawing suspend current 1: Transceiver circuitry drawing normal current
CLKOUT	Output	Rising Edge	**System Clock.** This output is used for clocking receive and transmit parallel data at 60MHz (8-bit mode) or 30MHz (16-bit mode). When in 8-bit mode, this specification refers to CLKOUT as CLK60. When in 16-bit mode, CLKOUT is referred to as CLK30.
OPMODE[1:0]	Input	N/A	**Operational Mode.** These signals select between the various operational modes: [1] [0] Description 0 0 0: Normal Operation 0 1 1: Non-driving (all terminations removed) 1 0 2: Disable bit stuffing and NRZI encoding 1 1 3: Reserved
LINESTATE[1:0]	Output	N/A	**Line State.** These signals reflect the current state of the USB data bus in FS mode, with [0] reflecting the state of DP and [1] reflecting the state of DM. When the device is suspended or resuming from a suspended state, the signals are combinatoria. Otherwise, the signals are synchronized to CLKOUT. [1] [0] Description 0 0 0: SE0 0 1 1: J State 1 0 2: K State 1 1 3: SE1
DATABUS16_8	Input	N/A	**Databus Select.** Selects between 8-bit and 16-bit data transfers. 0 8-bit data path enabled. VALIDH is undefined. CLKOUT = 60MHz. 1: 16-bit data path enabled. CLKOUT = 30MHz.

TABLE 4-2: DATA INTERFACE SIGNALS

<table>
<tr><th>Name</th><th>Direction</th><th>Active Level</th><th>Description</th></tr>
<tr><td rowspan="13">DATA[15:0]</td><td rowspan="13">Bidir</td><td rowspan="13">N/A</td><td>DATA BUS. 16-BIT BIDIRECTIONAL MODE.</td></tr>
<tr><td>TXVALID | RXVALID | VALIDH | DATA[15:0]</td></tr>
<tr><td>0 | 0 | X | Not used</td></tr>
<tr><td>0 | 1 | 0 | DATA[7:0] output is valid for receive
VALIDH is an output</td></tr>
<tr><td>0 | 1 | 1 | DATA[15:0] output is valid for receive
VALIDH is an output</td></tr>
<tr><td>1 | X | 0 | DATA[7:0] input is valid for transmit
VALIDH is an input</td></tr>
<tr><td>1 | X | 1 | DATA[15:0] input is valid for transmit
VALIDH is an input</td></tr>
<tr><td>DATA BUS. 8-BIT UNIDIRECTIONAL MODE.</td></tr>
<tr><td>TXVALID | RXVALID | DATA[15:0]</td></tr>
<tr><td>0 | 0 | Not used</td></tr>
<tr><td>0 | 1 | DATA[15:8] output is valid for receive</td></tr>
<tr><td>1 | X | DATA[7:0] input is valid for transmit</td></tr>
<tr><td>TXVALID</td><td>Input</td><td>High</td><td>Transmit Valid. Indicates that the TXDATA bus is valid for transmit. The assertion of TXVALID initiates the transmission of SYNC on the USB bus. The negation of TXVALID initiates EOP on the USB.

Control inputs (OPMODE[1:0], TERMSELECT,XCVRSELECT) must not be changed on the de-assertion or assertion of TXVALID. The PHY must be in a quiescent state when these inputs are changed.</td></tr>
<tr><td>TXREADY</td><td>Output</td><td>High</td><td>Transmit Data Ready. If TXVALID is asserted, the SIE must always have data available for clocking into the TX Holding Register on the rising edge of CLKOUT. TXREADY is an acknowledgment to the SIE that the transceiver has clocked the data from the bus and is ready for the next transfer on the bus. If TXVALID is negated, TXREADY can be ignored by the SIE.</td></tr>
<tr><td>VALIDH</td><td>Bidir</td><td>N/A</td><td>Transmit/Receive High Data Bit Valid (used in 16-bit mode only). When TXVALID = 1, the 16-bit data bus direction is changed to inputs, and VALIDH is an input. If VALIDH is asserted, DATA[15:0] is valid for transmission. If deasserted, only DATA[7:0] is valid for transmission. The DATA bus is driven by the SIE.

When TXVALID = 0 and RXVALID = 1, the 16-bit data bus direction is changed to outputs, and VALIDH is an output. If VALIDH is asserted, the DATA[15:0] outputs are valid for receive. If deasserted, only DATA[7:0] is valid for receive. The DATA bus is read by the SIE.</td></tr>
<tr><td>RXVALID</td><td>Output</td><td>High</td><td>Receive Data Valid. Indicates that the RXDATA bus has received valid data. The Receive Data Holding Register is full and ready to be unloaded. The SIE is expected to latch the RXDATA bus on the rising edge of CLKOUT.</td></tr>
<tr><td>RXACTIVE</td><td>Output</td><td>High</td><td>Receive Active. Indicates that the receive state machine has detected Start of Packet and is active.</td></tr>
<tr><td>RXERROR</td><td>Output</td><td>High</td><td>Receive Error. 0: Indicates no error. 1: Indicates a receive error has been detected. This output is clocked with the same timing as the RXDATA lines and can occur at anytime during a transfer.</td></tr>
</table>

TABLE 4-3: USB I/O SIGNALS

Name	Direction	Active Level	Description
DP	I/O	N/A	**USB Positive Data Pin**.
DM	I/O	N/A	**USB Negative Data Pin**.

TABLE 4-4: BIASING AND CLOCK OSCILLATOR SIGNALS

Name	Direction	Active Level	Description
RBIAS	Input	N/A	**External 1% bias resistor**. Requires a 12KΩ resistor to ground. Used for setting HS transmit current level and on-chip termination impedance.
XI/XO	Input	N/A	**External crystal**. 12MHz crystal connected from XI to XO.

TABLE 4-5: POWER AND GROUND SIGNALS

Name	Direction	Active Level	Description
VDD3.3	N/A	N/A	**3.3V Digital Supply**. Powers digital pads. See Note 4-1
VDD1.8	N/A	N/A	**1.8V Digital Supply**. Powers digital core.
VSS	N/A	N/A	**Digital Ground**. See Note 4-2
VDDA3.3	N/A	N/A	**3.3V Analog Supply**. Powers analog I/O and 3.3V analog circuitry.
VDDA1.8	N/A	N/A	**1.8V Analog Supply**. Powers 1.8V analog circuitry. See Note 4-1
VSSA	N/A	N/A	**Analog Ground**. See Note 4-2

Note 4-1 A Ferrite Bead (with DC resistance <.5 Ohms) is recommended for filtering between both the VDD3.3 and VDDA3.3 supplies and the VDD1.8 and VDDA1.8 Supplies. See FIGURE 8-9: Application Diagram for 56-pin VQFN Package on page 39.

Note 4-2 All VSS and VSSA are bonded to the exposed pad under the IC in the package. The exposed pad must be connected to solid GND plane on printed circuit board.

5.0 LIMITING VALUES

FIGURE 5-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
1.8V Supply Voltage (VDD1.8 and VDDA1.8)	$V_{DD1.8}$		-0.5		TBD	V
3.3V Supply Voltage (VDD3.3 and VDDA3.3)	$V_{DD3.3}$		-0.5		4.6	V
Input Voltage	V_I		-0.5		4.6	V
Storage Temperature	T_{STG}		-40		+125	°C
[1] Equivalent to discharging a 100pF capacitor via a 1.5kΩ resistor (HBM).						

Note: In accordance with the Absolute Maximum Rating System (IEC 60134).

FIGURE 5-2: RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
1.8V Supply Voltage (VDD1.8 and VDDA1.8)	$V_{DD1.8}$		1.6	1.8	2.0	V
3.3V Supply Voltage (VDD3.3 and VDDA3.3)	$V_{DD3.3}$		3.0	3.3	3.6	V
Input Voltage on Digital Pins	V_I		0.0		$V_{DD3.3}$	V
Input Voltage on Analog I/O Pins (DP, DM)	$V_{I(I/O)}$		0.0		$V_{DD3.3}$	V
Ambient Temperature	T_A		-40		+85	°C

FIGURE 5-3: RECOMMENDED EXTERNAL CLOCK CONDITIONS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
System Clock Frequency		XO driven by the external clock; and no connection at XI		12 (+/- 100ppm) Note 5-1		MHz
System Clock Duty Cycle		XO driven by the external clock; and no connection at XI	45	50	55	%

Note 5-1 The USB 2.0 Specification requires a frequency accuracy of +/-500ppm. For applications using a quartz crystal, Microchip recommends that it be specified with an accuracy of +/-100ppm. Resonators that are specified to meet the +/-500ppm accuracy have also been used successfully with the USB3250.

6.0 ELECTRICAL CHARACTERISTICS

TABLE 6-1: ELECTRICAL CHARACTERISTICS: SUPPLY PINS

Parameter		Symbol	Conditions	MIN	TYP	MAX	Units
FS TRANSMIT	Total Power	$P_{TOT(FSTX)}$	FS transmitting at 12Mb/s; 50pF load on DP and DM		86	115	mW
	VDD3.3 Power	$P_{3.3V(FSTX)}$			57	76	mW
	VDD1.8 Power	$P_{1.8V(FSTX)}$			29	39	mW
FS RECEIVE	Total Power	$P_{TOT(FSRX)}$	FS receiving at 12Mb/s		75	115	mW
	VDD3.3 Power	$P_{3.3V(FSRX)}$			46	76	mW
	VDD1.8 Power	$P_{1.8V(FSRX)}$			29	39	mW
HS TRANSMIT	Total Power	$P_{TOT(HSTX)}$	HS transmitting into a 45Ω load		158	185	mW
	VDD3.3 Power	$P_{3.3V\ (HSTX)}$			110	130	mW
	VDD1.8 Power	$P_{1.8V\ (HSTX)}$			48	55	mW
HS RECEIVE	Total Power	$P_{TOT(HSRX)}$	HS receiving at 480Mb/s		155	185	mW
	VDD3.3 Power	$P_{3.3V\ (HSRX)}$			107	130	mW
	VDD1.8 Power	$P_{1.8V\ (HSRX)}$			48	55	mW
SUSPEND MODE 1	Total Current	$I_{DD(SUSP1)}$	15kΩ pull-down and 1.5kΩ pull-up resistor on pin DP not connected.		123	240	uA
	VDD3.3 Current	$I_{3.3V\ (SUSP1)}$			68	120	uA
	VDD1.8 Current	$I_{1.8V\ (SUSP1)}$			55	120	uA
SUSPEND MODE 2	Total Current	$I_{DD(SUSP2)}$	15kΩ pull-down and 1.5kΩ pull-up resistor on pin DP connected.		323	460	uA
	VDD3.3 Current	$I_{3.3V\ (SUSP2)}$			268	340	uA
	VDD1.8 Current	$I_{1.8V\ (SUSP2)}$			55	120	uA
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified.)							

TABLE 6-2: DC ELECTRICAL CHARACTERISTICS: LOGIC PINS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Low-Level Input Voltage	V_{IL}		V_{SS}		0.8	V
High-Level Input Voltage	V_{IH}		2.0		$V_{DD3.3}$	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	$V_{DD3.3}$ - 0.5			V
Input Leakage Current	I_{LI}				± 1	uA
Pin Capacitance	C_{pin}				4	pF
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified. Pins Data[15:0] and VALIDH have passive pull-down elements.)						

TABLE 6-3: DC ELECTRICAL CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
FS FUNCTIONALITY						
INPUT LEVELS						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}				0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}		2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
OUTPUT LEVELS						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to $V_{DD3.3}$			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; R_L = 15kΩ to GND	2.8		3.6	V
TERMINATION						
Driver Output Impedance for HS and FS	Z_{HSDRV}	Steady state drive (See Figure 6-1)	40.5	45	49.5	Ω
Input Impedance	Z_{INP}	TX, RPU disabled	10			MΩ
Pull-up Resistor Impedance	Z_{PU}		1.425		1.575	KΩ
Termination Voltage For Pull-up Resistor On Pin DP	V_{TERM}		3.0		3.6	V
HS FUNCTIONALITY						
INPUT LEVELS						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
HS Squelch Detection Threshold (Differential)	V_{HSSQ}	Squelch Threshold			100	mV
		Unsquelch Threshold	150			mV
OUTPUT LEVELS						
High Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV
High Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
High Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified.)						

TABLE 6-3: DC ELECTRICAL CHARACTERISTICS: ANALOG I/O PINS (DP/DM) (CONTINUED)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
LEAKAGE CURRENT						
OFF-State Leakage Current	I_{LZ}				± 1	uA
PORT CAPACITANCE						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified.)						

TABLE 6-4: DYNAMIC CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
FS OUTPUT DRIVER TIMING						
Rise Time	T_{FSR}	CL = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Fall Time	T_{FFF}	CL = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	F_{RFM}	Excluding the first transition from IDLE state	90		111.1	%
HS OUTPUT DRIVER TIMING						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification			See Figure 6 -2	
HIGH SPEED MODE TIMING						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification			See Figure 6 -2	
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification			See Figure 6 -2	
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified.)						

TABLE 6-5: DYNAMIC CHARACTERISTICS: DIGITAL UTMI PINS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
UTMI TIMING						
RXDATA[7:0]	T_{PD}	Propagation delay from CLKOUT to signal CL = 10pF		2	4	ns
RXVALID				2	4	
RXACTIVE				2	4	
RXERROR				2	4	
LINESTATE[1:0]				2	4	
TXREADY				2	4	
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified.)						

TABLE 6-5: DYNAMIC CHARACTERISTICS: DIGITAL UTMI PINS (CONTINUED)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
TXDATA[7:0]	T_{SU}	Setup time from signal to CLKOUT	4			ns
TXVALID			4			
OPMODE[1:0]			4			
XCVRSELECT			4			
TERMSELECT			4			
SUSPENDN			4			
TXDATA[7:0]	T_H	Hold time from CLKOUT to signal	0			ns
TXVALID			0			
OPMODE[1:0]			0			
XCVRSELECT			0			
TERMSELECT			0			
SUSPENDN			0			
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified.)						

6.1 Driver Characteristics of Full-Speed Drivers in Hi-Speed Capable Transceivers

The USB transceiver uses a differential output driver to drive the USB data signal onto the USB cable. Figure 6-1 shows the V/I characteristics for a full-speed driver which is part of a Hi-Speed capable transceiver. The normalized V/I curve for the driver must fall entirely inside the shaded region. The V/I region is bounded by the minimum driver impedance above (40.5 Ohm) and the maximum driver impedance below (49.5 Ohm). The output voltage must be within 10mV of ground when no current is flowing in or out of the pin.

FIGURE 6-1: FULL-SPEED DRIVER VOH/IOH CHARACTERISTICS FOR HI-SPEED CAPABLE TRANSCEIVER

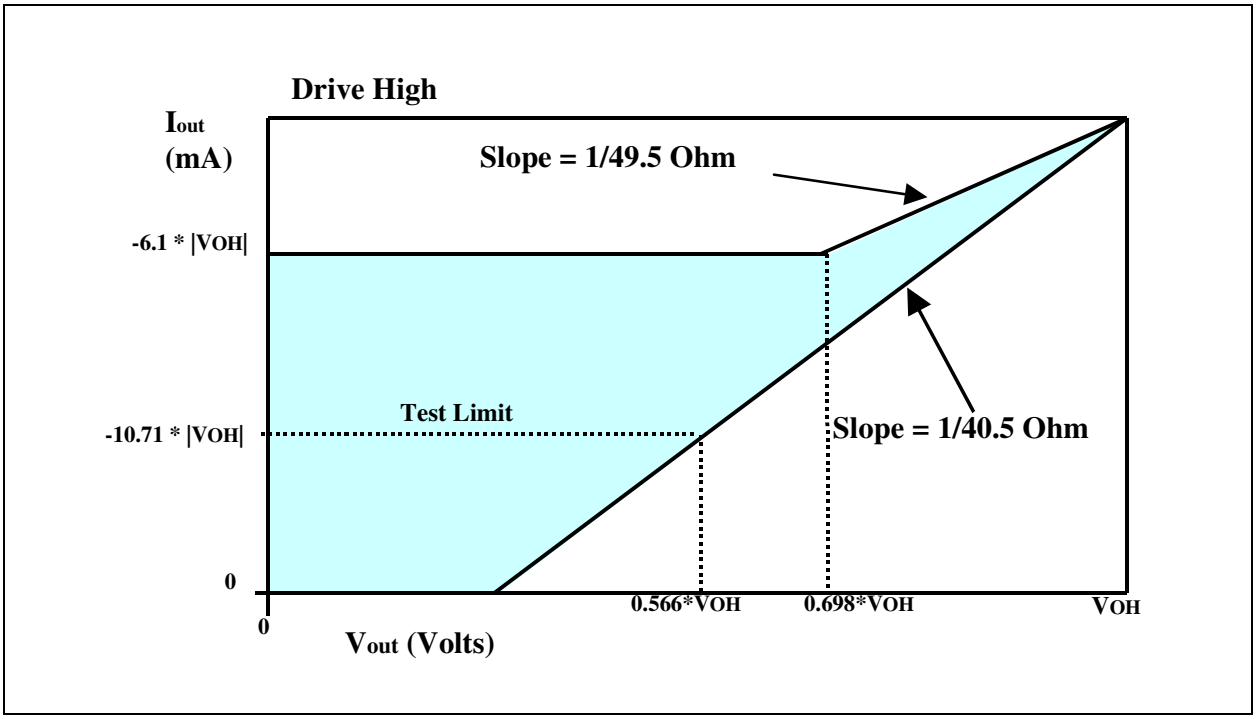
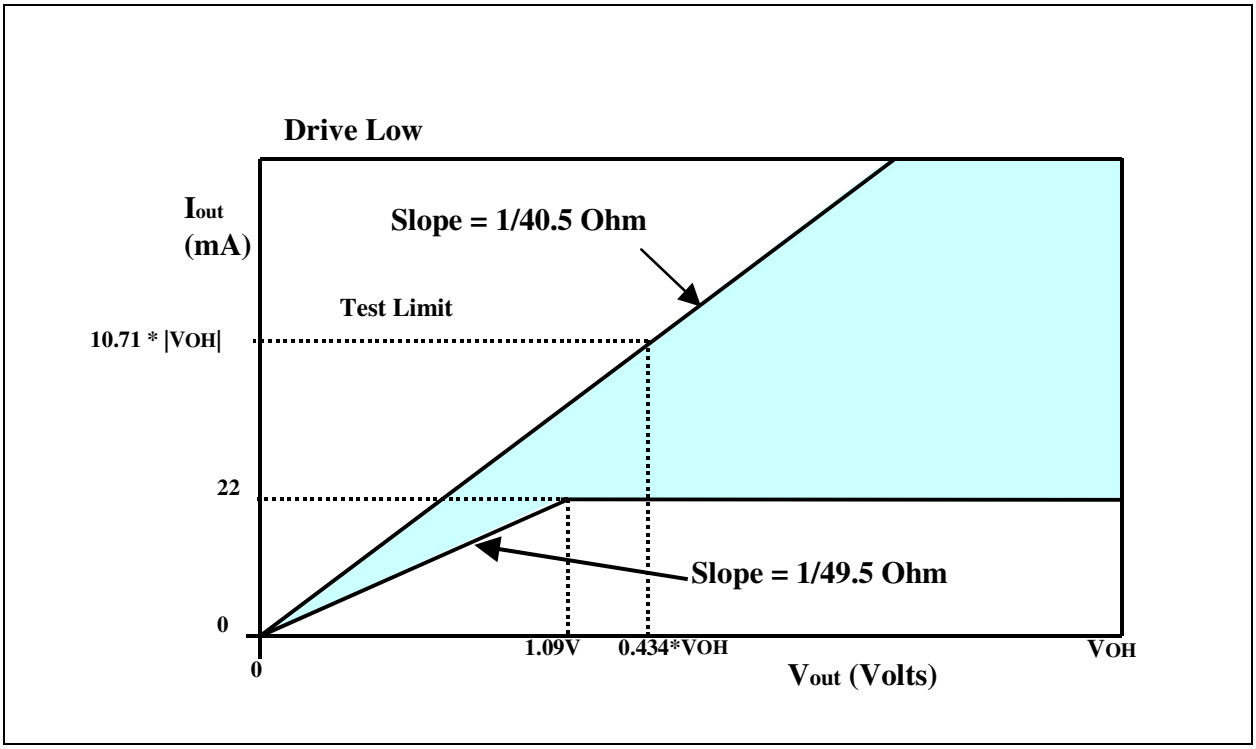


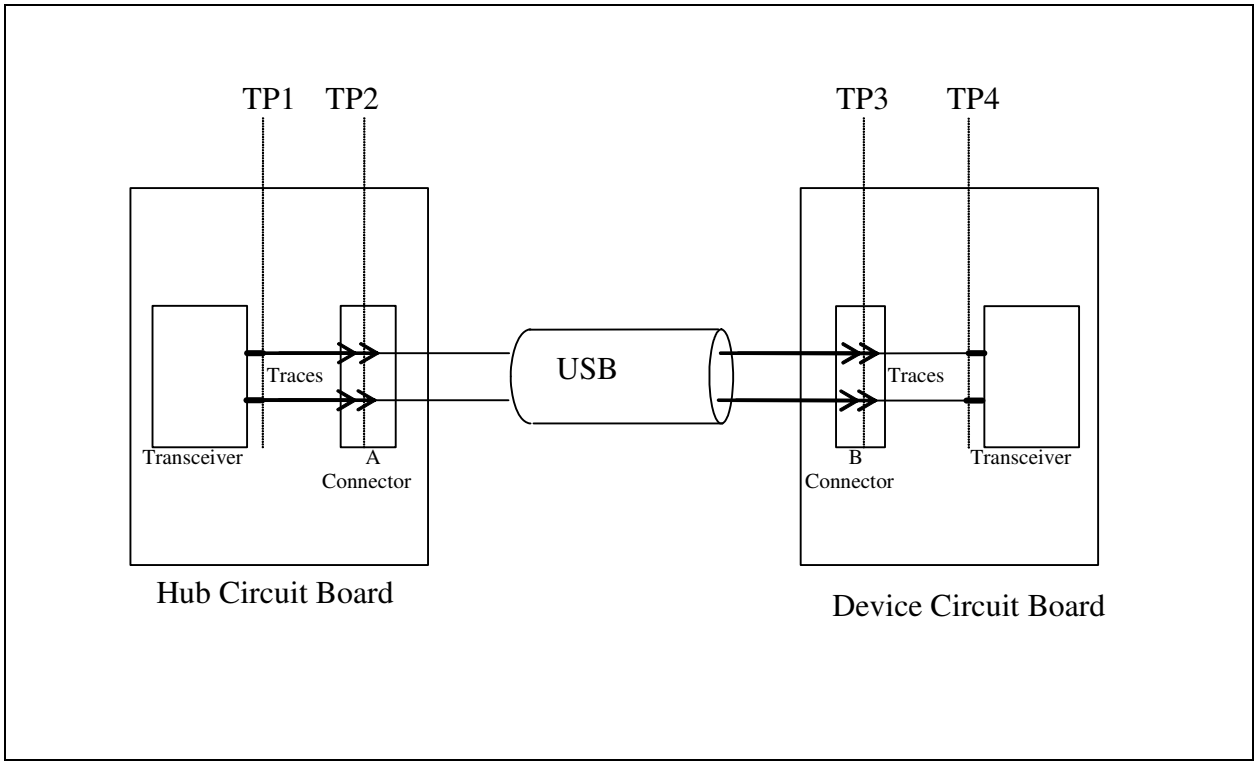
FIGURE 6-2: FULL-SPEED DRIVER VOL/IOL CHARACTERISTICS FOR HI-SPEED CAPABLE TRANSCEIVER



6.2 Hi-Speed Signaling Eye Patterns

Hi-Speed USB signals are characterized using eye patterns. For measuring the eye patterns 4 points have been defined (see Figure 6-3). The Universal Serial Bus Specification Rev.2.0 defines the eye patterns in several 'templates'. The two templates that are relevant to the PHY are shown below.

FIGURE 6-3: EYE PATTERN MEASUREMENT PLANES



The eye pattern in Figure 6-4 defines the transmit waveform requirements for a hub (measured at TP2 of Figure 6-3) or a device without a captive cable (measured at TP3 of Figure 6-3). The corresponding signal levels and timings are given in Table 6-6. Time is specified as a percentage of the unit interval (UI), which represents the nominal bit duration for a 480 Mbit/s transmission rate.

FIGURE 6-4: EYE PATTERN FOR TRANSMIT WAVEFORM AND EYE PATTERN DEFINITION

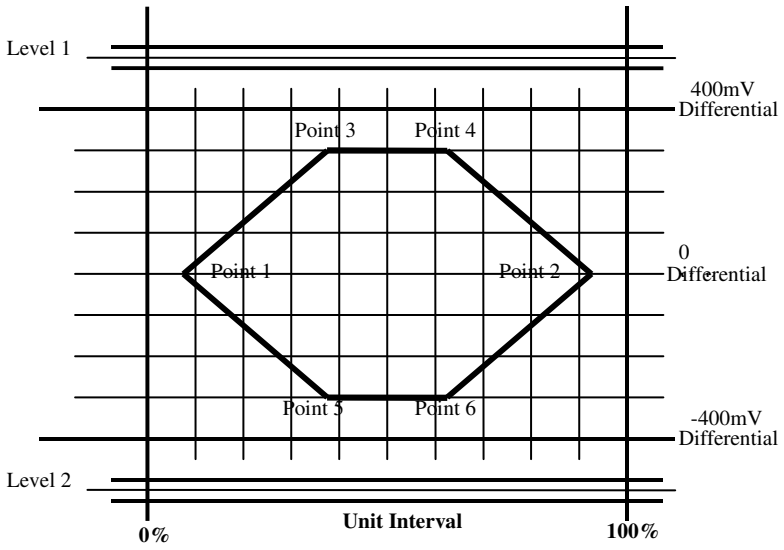


TABLE 6-6: EYE PATTERN FOR TRANSMIT WAVEFORM AND EYE PATTERN DEFINITION

	Voltage Level (D+, D-)	Time (% Of Unit Interval)
Level 1	525mV in UI following a transition, 475mV in all others	N/A
Level 2	-525mV in UI following a transition, -475mV in all others	N/A
Point 1	0V	7.5% UI
Point 2	0V	92.5% UI
Point 3	300mV	37.5% UI
Point 4	300mV	62.5% UI
Point 5	-300mV	37.5% UI
Point 6	-300mV	62.5% UI

The eye pattern in Figure 6-5 defines the receiver sensitivity requirements for a hub (signal applied at test point TP2 of Figure 6-3) or a device without a captive cable (signal applied at test point TP3 of Figure 6-3). The corresponding signal levels and timings are given in Table 6-7. Timings are given as a percentage of the unit interval (UI), which represents the nominal bit duration for a 480 Mbit/s transmission rate.

FIGURE 6-5: EYE PATTERN FOR RECEIVE WAVEFORM AND EYE PATTERN DEFINITION

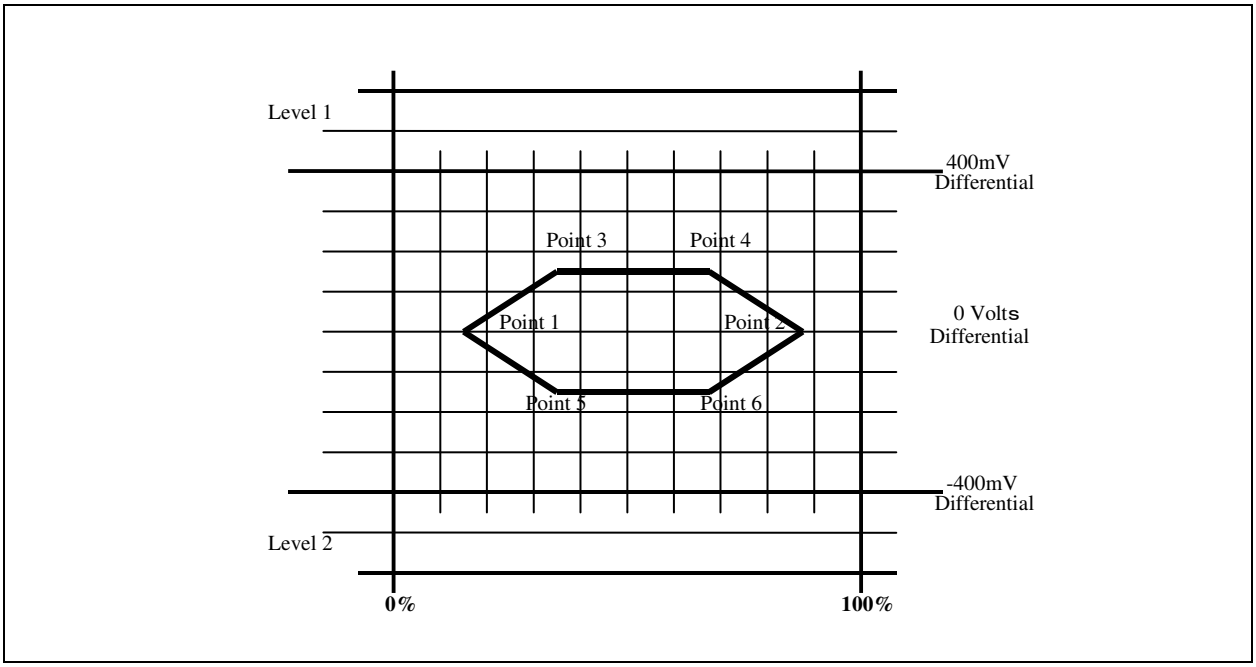


TABLE 6-7: EYE PATTERN FOR RECEIVE WAVEFORM AND EYE PATTERN DEFINITION

	Voltage Level (D+, D-)	Time (% Of Unit Interval)
Level 1	575mV	N/A
Level 2	-575mV	N/A
Point 1	0V	15% UI
Point 2	0V	85% UI
Point 3	150mV	35% UI
Point 4	150mV	65% UI
Point 5	-150mV	35% UI
Point 6	-150mV	65% UI

7.0 FUNCTIONAL OVERVIEW

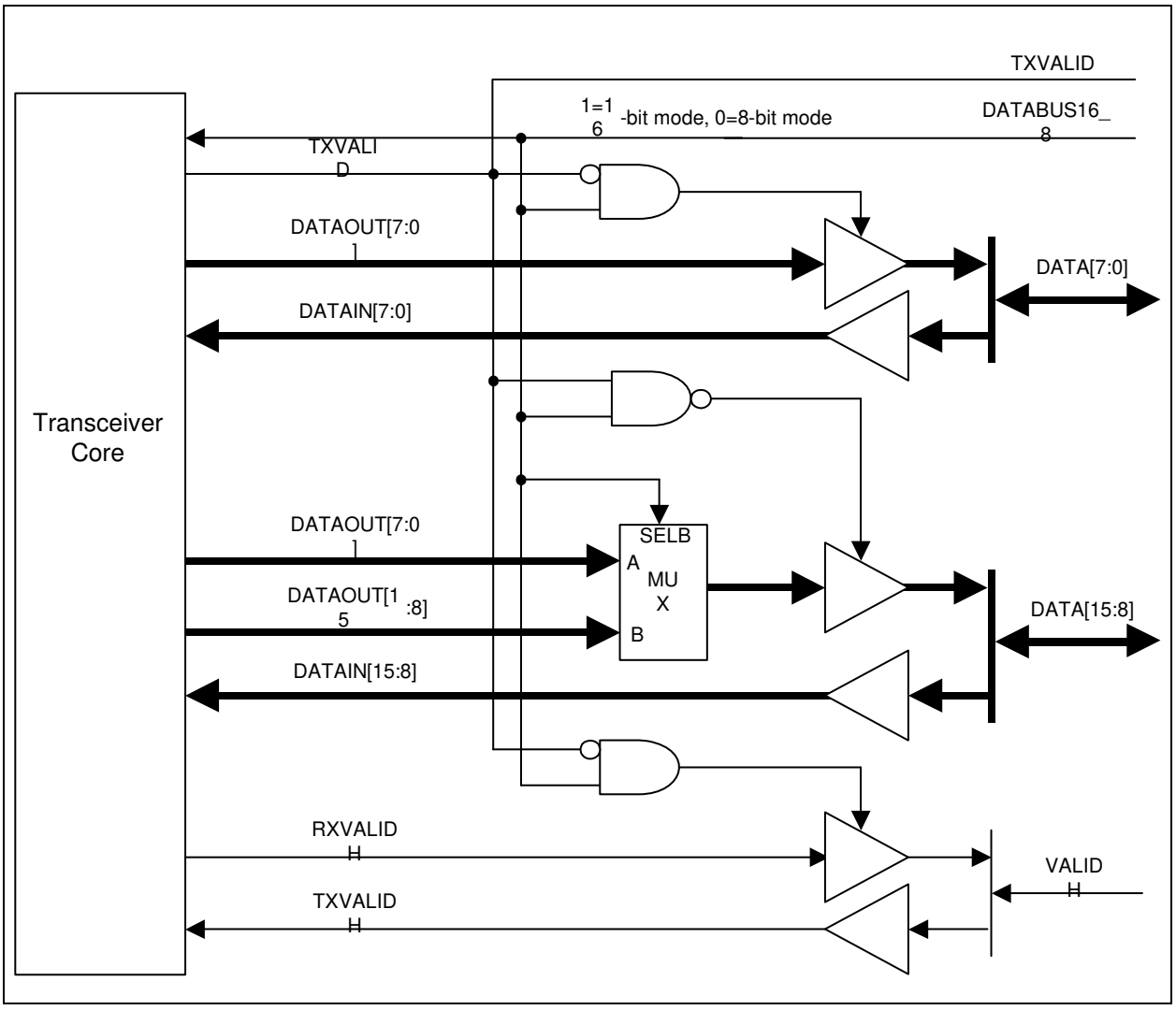
FIGURE 2-1: Block Diagram on page 5 shows the functional block diagram of the USB3250. Each of the functions is described in detail below.

7.1 Modes of Operation

The USB3250 supports two modes of operation. See Figure 7-1 for a block diagram of the digital interface.

- 8-bit unidirectional mode. Selected when DATABUS16_8 = 0. CLKOUT runs at 60MHz. The 8-bit transmit data bus uses the lower 8 bits of the DATA bus (ie, TXDATA[7:0] = DATA[7:0]). The 8-bit receive data bus uses the upper 8 bits of the DATA bus (ie, RXDATA[7:0] = DATA[15:8]).
- 16-bit bidirectional mode. Selected when DATABUS16_8 = 1. CLKOUT runs at 30MHz. An additional signal (VALIDH) is used to identify whether the high byte of the respective 16-bit data word is valid. The full 16-bit DATA bus is used for transmit and receive operations. If TXVALID is asserted, then the DATA[15:0] bus accepts transmit data from the SIE. If TXVALID is deasserted, then the DATA[15:0] bus presents received data to the SIE. VALIDH is undefined when DATABUS16_8 = 0 (8-bit mode).

FIGURE 7-1: BIDIRECTIONAL 16-BIT INTERFACE



7.2 System Clocking

This block connects to either an external 12MHz crystal or an external clock source and generates a 480MHz multi-phase clock. The clock is used in the CRC block to over-sample the incoming received data, resynchronize the transmit data, and is divided down to a 30MHz or 60MHz version (CLKOUT) which acts as the system byte clock. The PLL block also outputs a clock valid signal to the other parts of the transceiver when the clock signal is stable. All UTMI signals are synchronized to the CLKOUT output. The behavior of the CLKOUT is as follows:

- Produce the first CLKOUT transition no later than 5.6ms after negation of SUSPENDN. The CLKOUT signal frequency error is less than 10% at this time.
- The CLKOUT signal will fully meet the required accuracy of ±500ppm no later than 1.4ms after the first transition of CLKOUT.

In HS mode there is one CLKOUT cycle per byte time. The frequency of CLKOUT does not change when the Macrocell is switched between HS to FS modes. In FS mode (8-bit mode) there are 5 CLK60 cycles per FS bit time, typically 40 CLK60 cycles per FS byte time. If a received byte contains a stuffed bit then the byte boundary can be stretched to 45 CLK60 cycles, and two stuffed bits would result in a 50 CLK60 cycles.

Figure 7-2 shows the relationship between CLK60 and the transmit data transfer signals in FS mode. TXREADY is only asserted for one CLK60 per byte time to signal the SIE that the data on the TXDATA lines has been read by the Macrocell. The SIE may hold the data on the TXDATA lines for the duration of the byte time. Transitions of TXVALID must meet the defined setup and hold times relative to CLK60.

FIGURE 7-2: FS CLK RELATIONSHIP TO TRANSMIT DATA AND CONTROL SIGNALS (8-BIT MODE)

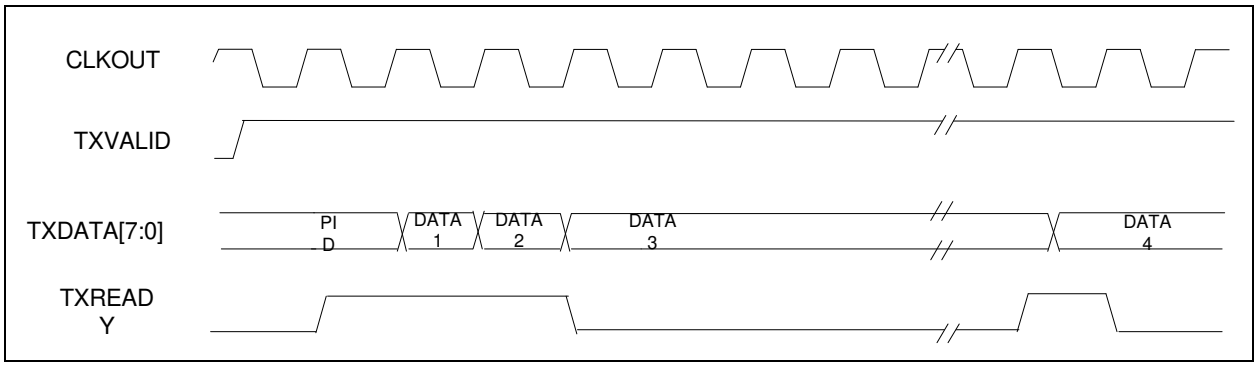
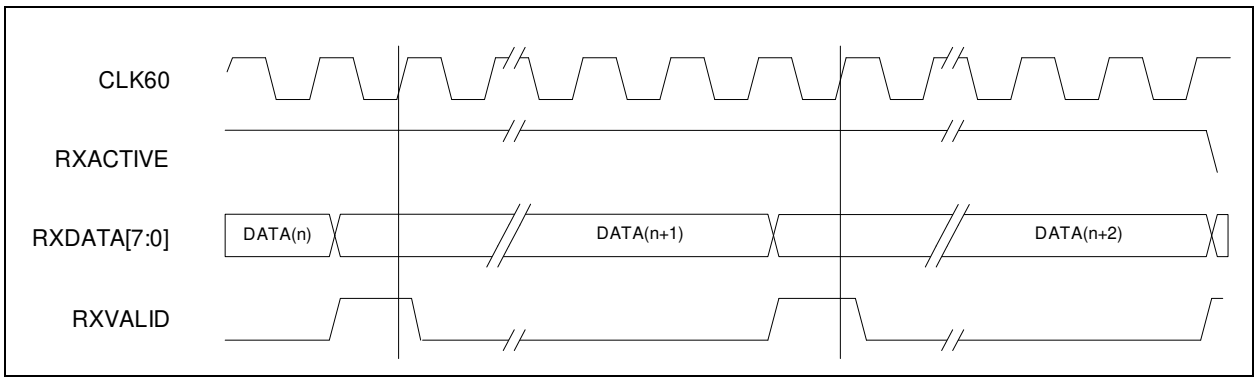


Figure 7-3 shows the relationship between CLK60 and the receive data control signals in FS mode. RXACTIVE "frames" a packet, transitioning only at the beginning and end of a packet. However transitions of RXVALID may take place any time 8 bits of data are available. Figure 7-3 also shows how RXVALID is only asserted for one CLKOUT cycle per byte time even though the data may be presented for the full byte time. The XCVRSELECT signal determines whether the HS or FS timing relationship is applied to the data and control signals.

FIGURE 7-3: FS CLK RELATIONSHIP TO RECEIVE DATA AND CONTROL SIGNALS (8-BIT MODE)



7.3 Clock and Data Recovery Circuit

This block consists of the Clock and Data Recovery Circuit and the Elasticity Buffer. The Elasticity Buffer is used to compensate for differences between the transmitting and receiving clock domains. The USB 2.0 specification defines a maximum clock error of ±1000ppm of drift.

7.4 TX Logic

This block receives parallel data bytes placed on the DATA bus and performs the necessary transmit operations. These operations include parallel to serial conversion, bit stuffing and NRZI encoding. Upon valid assertion of the proper TX control lines by the SIE and TX State Machine, the TX LOGIC block will synchronously shift, at either the FS or HS rate, the data to the FS/HS TX block to be transmitted on the USB cable. Data transmit timing is shown in Figure 7-4.

FIGURE 7-4: TRANSMIT TIMING FOR A DATA PACKET (8-BIT MODE)

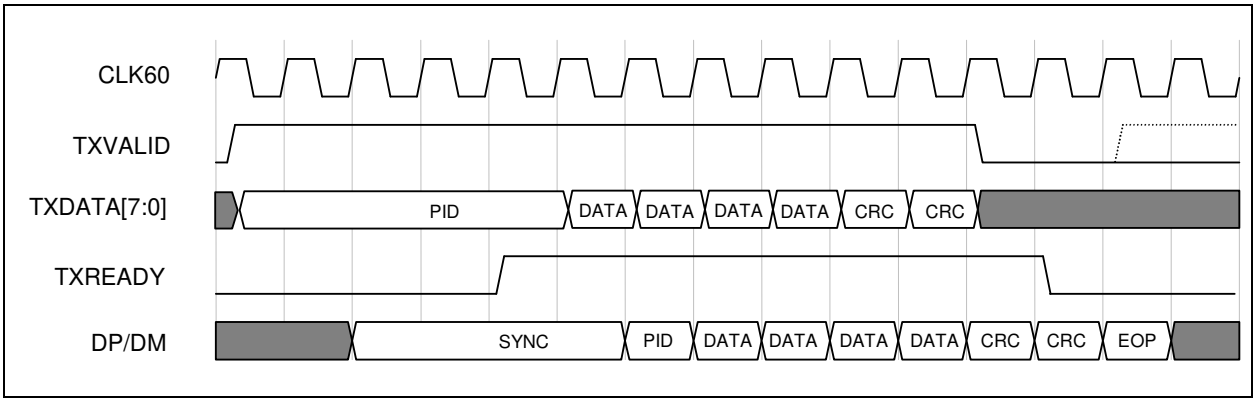


FIGURE 7-5: TRANSMIT TIMING FOR 16-BIT DATA, EVEN BYTE COUNT

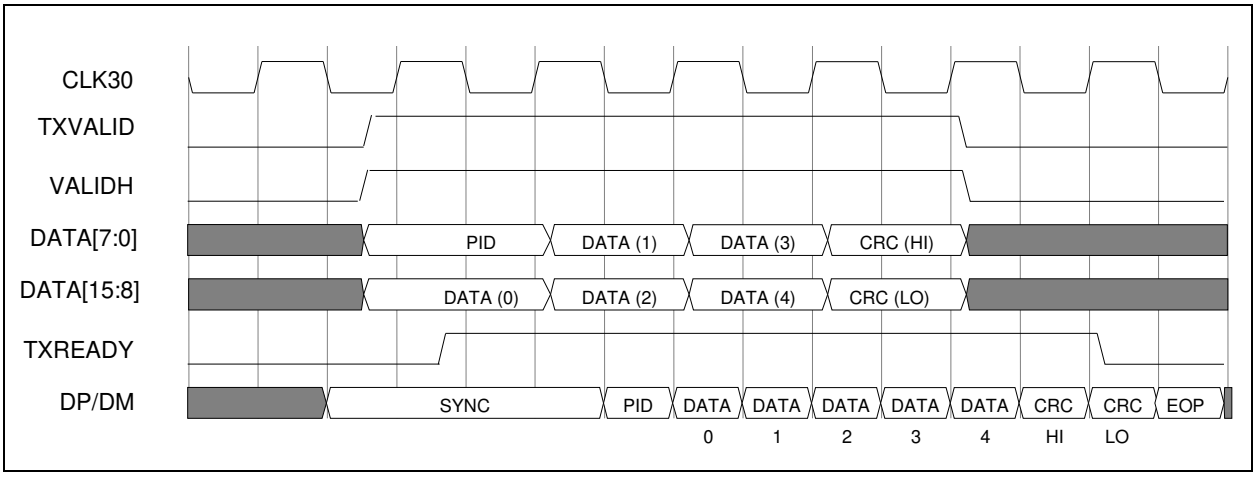
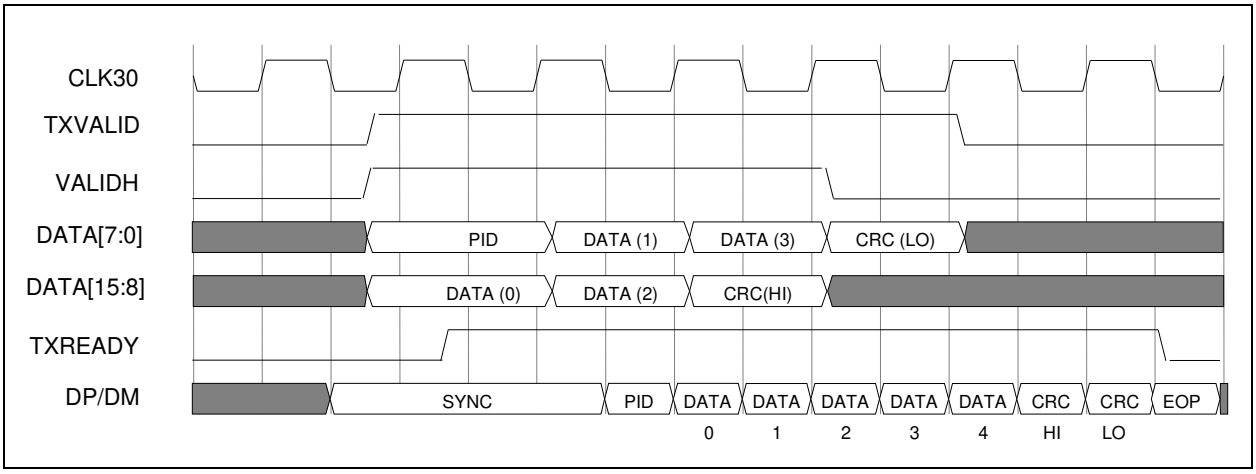


FIGURE 7-6: TRANSMIT TIMING FOR 16-BIT DATA, ODD BYTE COUNT



The behavior of the Transmit State Machine is described below.

- Asserting a RESET forces the transmit state machine into the Reset state which negates TXREADY. When RESET is negated the transmit state machine will enter a wait state.
- The SIE asserts TXVALID to begin a transmission.
- After the SIE asserts TXVALID it can assume that the transmission has started when it detects TXREADY has been asserted.
- The SIE must assume that the PHY has consumed a data byte if TXREADY and TXVALID are asserted on the rising edge of CLKOUT.
- The SIE must have valid packet information (PID) asserted on the TXDATA bus coincident with the assertion of TXVALID.
- TXREADY is sampled by the SIE on the rising edge of CLKOUT.
- The SIE negates TXVALID to complete a packet. Once negated, the transmit logic will never reassert TXREADY until after the EOP has been generated. (TXREADY will not re-assert until TXVALID asserts again).
- The PHY is ready to transmit another packet immediately, however the SIE must conform to the minimum inter-packet delays identified in the USB 2.0 specification.

7.5 RX Logic

This block receives serial data from the CRC block and processes it to be transferred to the SIE on the RXDATA bus. The processing involved includes NRZI decoding, bit unstuffing, and serial to parallel conversion. Upon valid assertion of the proper RX control lines by the RX State Machine, the RX Logic block will provide bytes to the RXDATA bus as shown in the figures below. The behavior of the Receive State Machine is described below.

FIGURE 7-7: RECEIVE TIMING FOR DATA WITH UNSTUFFED BITS (8-BIT MODE)

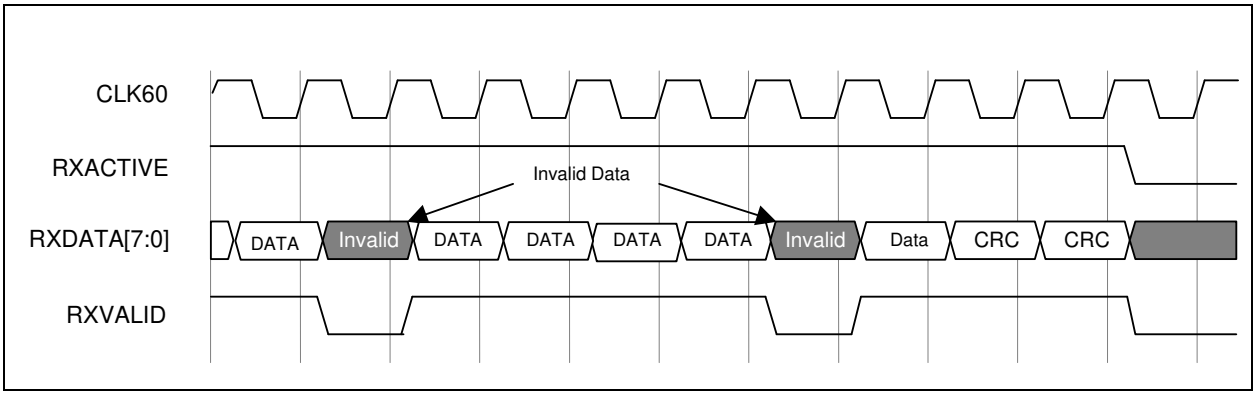


FIGURE 7-8: RECEIVE TIMING FOR 16-BIT DATA, EVEN BYTE COUNT

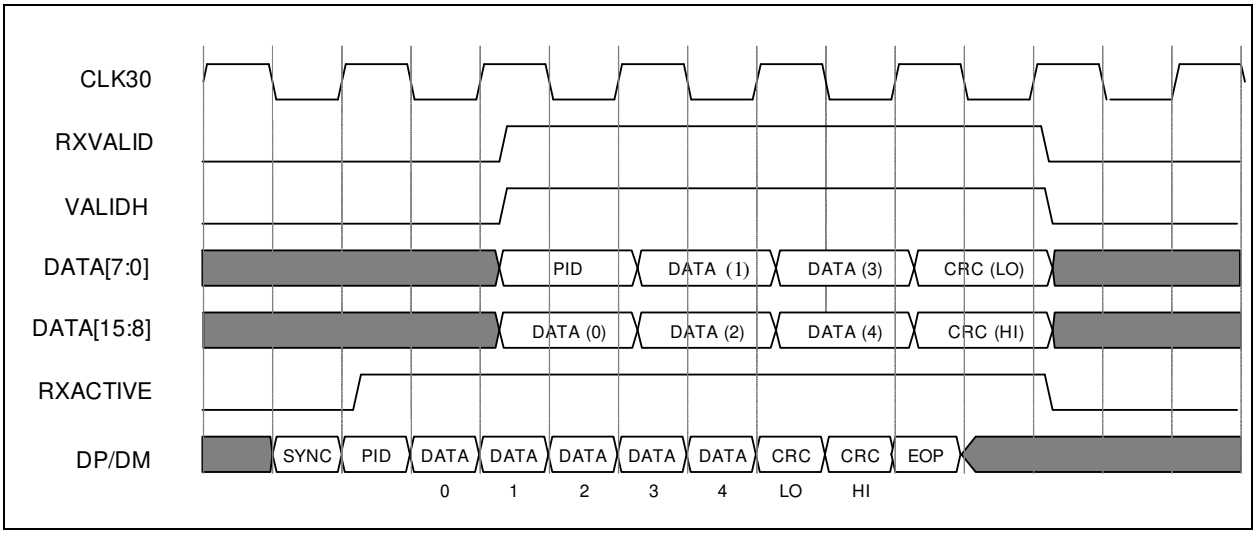
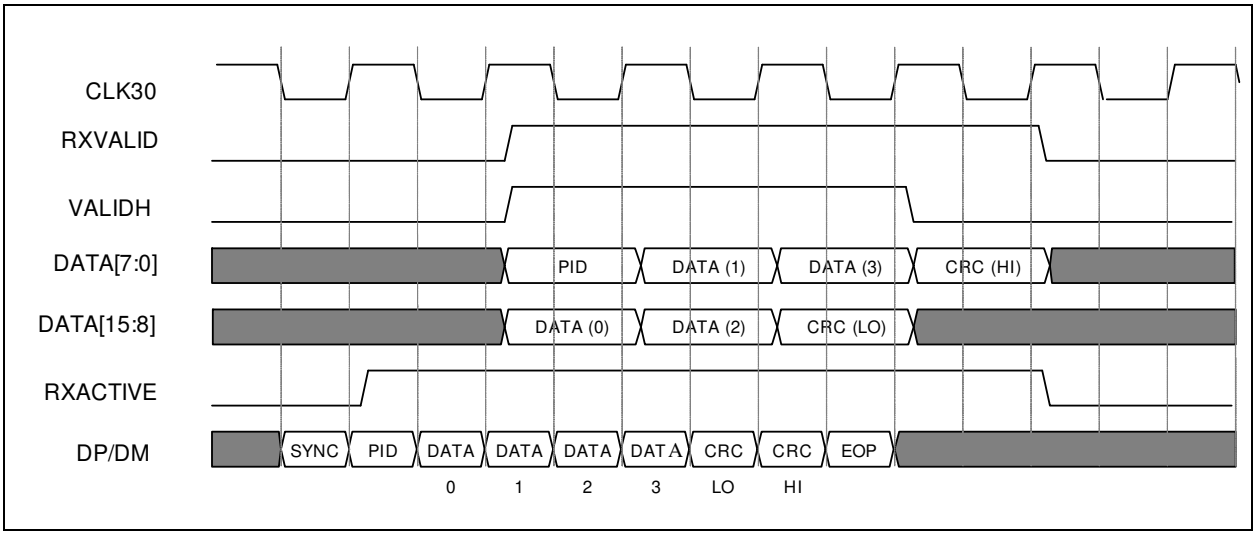


FIGURE 7-9: RECEIVE TIMING FOR 16-BIT DATA, ODD BYTE COUNT



The assertion of RESET will force the Receive State Machine into the Reset state. The Reset state deasserts RXACTIVE and RXVALID. When the RESET signal is deasserted the Receive State Machine enters the RX Wait state and starts looking for a SYNC pattern on the USB. When a SYNC pattern is detected the state machine will enter the Strip SYNC state and assert RXACTIVE. The length of the received Hi-Speed SYNC pattern varies and can be up to 32 bits long or as short as 12 bits long when at the end of five hubs. As a result, the state machine may remain in the Strip SYNC state for several byte times before capturing the first byte of data and entering the RX Data state.

After valid serial data is received, the state machine enters the RX Data state, where the data is loaded into the RX Holding Register on the rising edge of CLKOUT and RXVALID is asserted. The SIE must clock the data off the RXDATA bus on the next rising edge of CLKOUT. If OPMODE = Normal, then stuffed bits are stripped from the data stream. Each time 8 stuffed bits are accumulated the state machine will enter the RX Data Wait state, negating RXVALID thus skipping a byte time.

When the EOP is detected the state machine will enter the Strip EOP state and negate RXACTIVE and RXVALID. After the EOP has been stripped the Receive State Machine will reenter the RX Wait state and begin looking for the next packet.

The behavior of the Receive State Machine is described below:

- RXACTIVE and RXREADY are sampled on the rising edge of CLKOUT.
- In the RX Wait state the receiver is always looking for SYNC.
- The USB3250asserts RXACTIVE when SYNC is detected (Strip SYNC state).
- The USB3250 negates RXACTIVE when an EOP is detected and the elasticity buffer is empty (Strip EOP state).
- When RXACTIVE is asserted, RXVALID will be asserted if the RX Holding Register is full.
- RXVALID will be negated if the RX Holding Register was not loaded during the previous byte time. This will occur if 8 stuffed bits have been accumulated.
- The SIE must be ready to consume a data byte if RXACTIVE and RXVALID are asserted (RX Data state).
- Figure 7-10 shows the timing relationship between the received data (DP/DM), RXVALID, RXACTIVE, RXERROR and RXDATA signals.

Note 7-1 The USB 2.0 Transceiver does NOT decode Packet ID's (PIDs). They are passed to the SIE for decoding.

Note 7-2 Figure 7-10, Figure 7-11 and Figure 7-12 are timing examples of a HS/FS Macrocell when it is in HS mode. When a HS/FS Macrocell is in FS Mode (8-bit mode) there are approximately 40 CLK60 cycles every byte time. The Receive State Machine assumes that the SIE captures the data on the RXDATA bus if RXACTIVE and RXVALID are asserted. In FS mode, RXVALID will only be asserted for one CLK60 per byte time.

Note 7-3 Figure 7-10, Figure 7-11 and Figure 7-12 the SYNC pattern on DP/DM is shown as one byte long. The SYNC pattern received by a device can vary in length. These figures assume that all but the last 12 bits have been consumed by the hubs between the device and the host controller.

FIGURE 7-10: RECEIVE TIMING FOR DATA (WITH CRC-16 IN 8-BIT MODE)

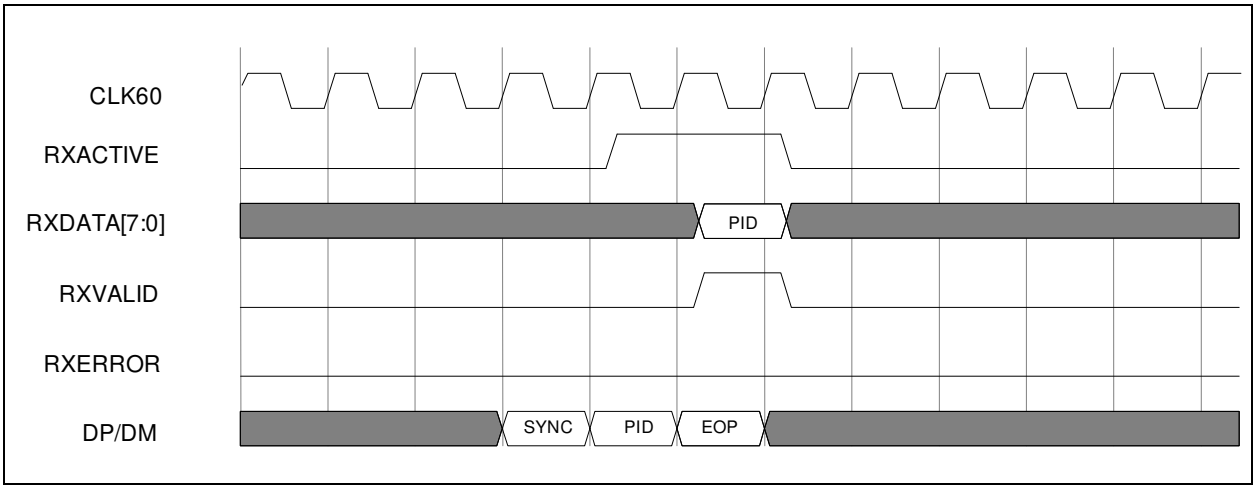


FIGURE 7-11: RECEIVE TIMING FOR SETUP PACKET (8-BIT MODE)