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USB3280

Hi-Speed USB Device PHY with UTMI Interface

PRODUCT FEATURES

Datasheet

- Available in a 36-pin lead-free RoHS compliant (6 x 6 x 0.90mm) QFN package
- Interface compliant with the UTMI specification (60MHz, 8-bit bidirectional interface)
- Only one required power supply (+3.3V)
- USB-IF “Hi-Speed” certified to USB 2.0 electrical specification
- Supports 480Mbps Hi-Speed (HS) and 12Mbps Full Speed (FS) serial data transmission rates
- Integrated 45Ω and 1.5kΩ termination resistors reduce external component count
- Internal short circuit protection of DP and DM lines
- On-chip oscillator operates with low cost 24MHz crystal
- Latch-up performance exceeds 150mA per EIA/JESD 78, Class II
- ESD protection levels of 5kV HBM without external protection devices
- SYNC and EOP generation on transmit packets and detection on receive packets
- NRZI encoding and decoding
- Bit stuffing and unstuffing with error detection
- Supports the USB suspend state, HS detection, HS Chirp, Reset and Resume
- Support for all test modes defined in the USB 2.0 specification
- 55mA Unconfigured Current (typical) - ideal for bus powered applications.
- 83uA suspend current (typical) - ideal for battery powered applications.
- Industrial Operating Temperature -40°C to +85°C

Applications

The USB3280 is the ideal companion to any ASIC, SoC or FPGA solution designed with a UTMI Hi-Speed USB device (peripheral) core.

The USB3280 is well suited for:

- Cell Phones
- MP3 Players
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Entertainment Devices
- Printers

ORDER NUMBER(S):

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Table of Contents

List of Figures

List of Tables

Chapter 1 General Description

The USB3280 provides the Physical Layer (PHY) interface to a USB 2.0 Device Controller. The IC is available in a 36-pin lead-free RoHS compliant QFN package.

1.1 Product Description

The USB3280 is an industrial temperature USB 2.0 physical layer transceiver (PHY) integrated circuit. SMSC's proprietary technology results in low power dissipation, which is ideal for building a bus powered USB 2.0 peripheral. The PHY uses an 8-bit bidirectional parallel interface, which complies with the USB Transceiver Macrocell Interface (UTMI) specification. It supports 480Mbps transfer rate, while remaining backward compatible with USB 1.1 legacy protocol at 12Mbps.

All required termination and 5.25V short circuit protection of the DP/DM lines are internal to the chip. The USB3280 also has an integrated 1.8V regulator so that only a 3.3V supply is required.

While transmitting data, the PHY serializes data and generates SYNC and EOP fields. It also performs needed bit stuffing and NRZI encoding. Likewise, while receiving data, the PHY de-serializes incoming data, stripping SYNC and EOP fields and performs bit un-stuffing and NRZI decoding.

Chapter 2 Functional Block Diagram

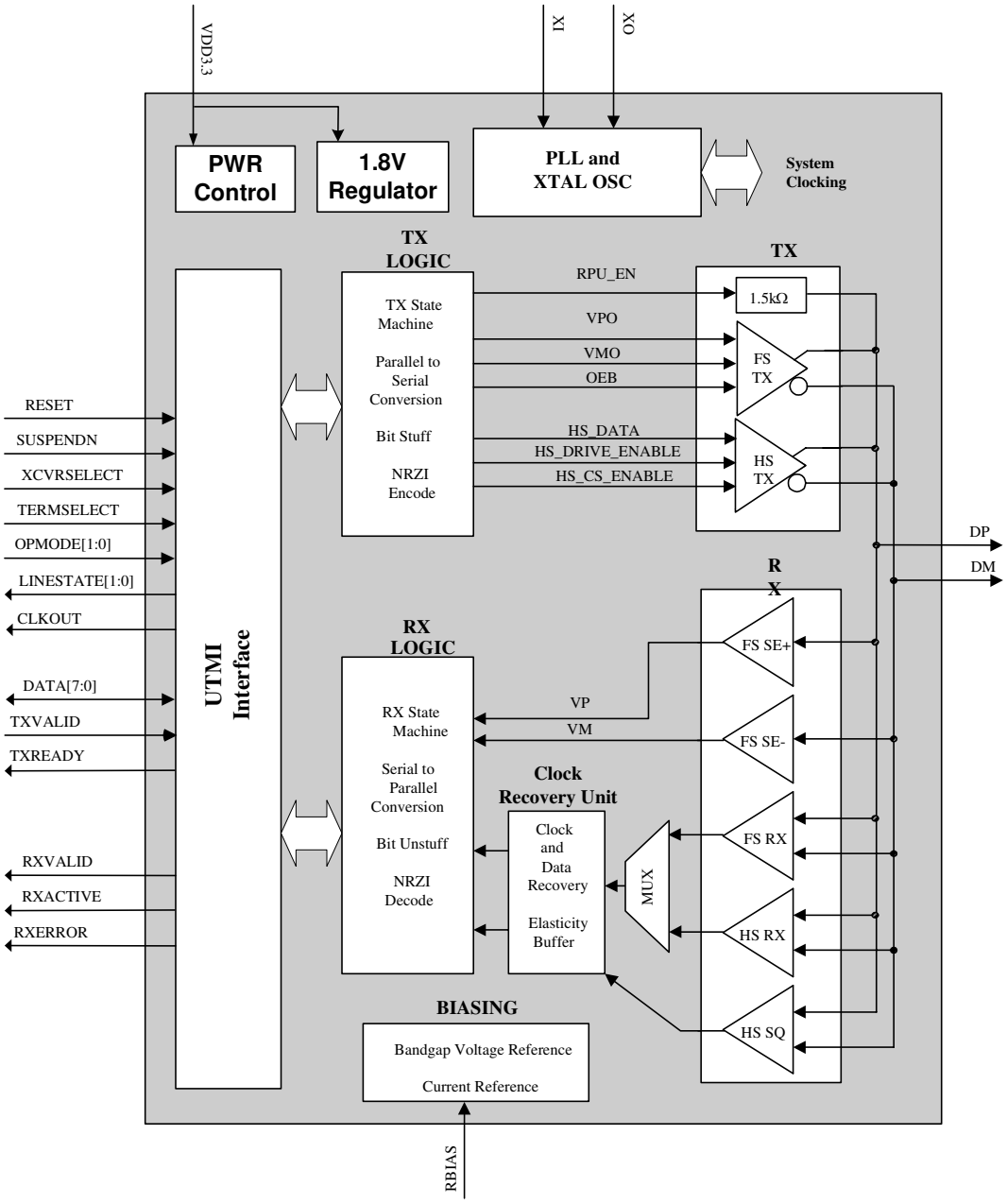

Figure 2.1 USB3280 Block Diagram

Chapter 3 Pinout

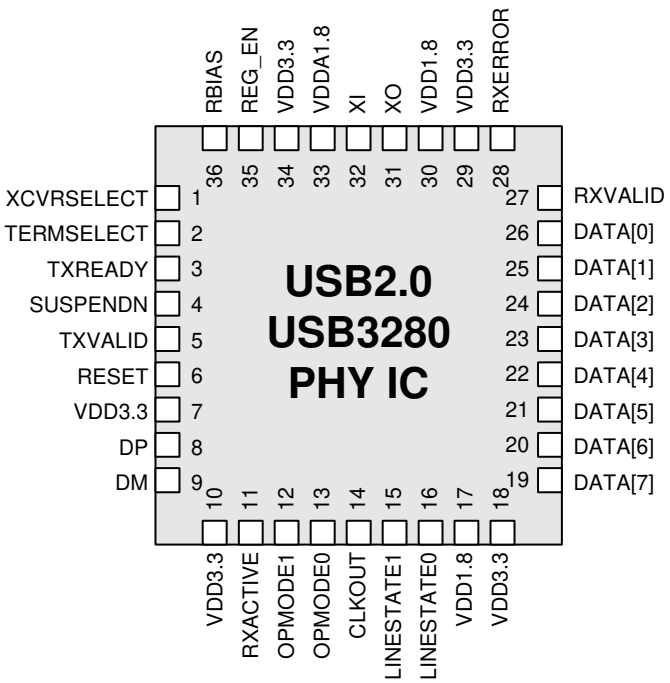

Figure 3.1 USB3280 Pinout - Top View

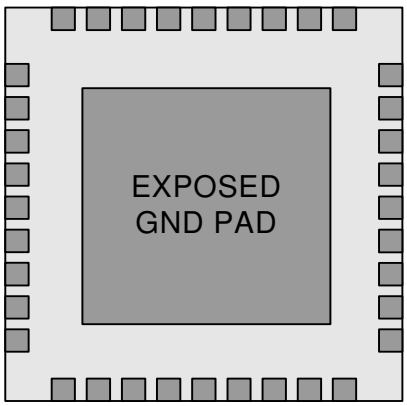

Figure 3.2 USB3280 Pinout - Bottom View

The flag of the QFN package must be connected to ground.

Chapter 4 Interface Signal Definition

Table 4.1 System Interface Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
RESET (RST)	Input	High	**Reset.** Reset all state machines. After coming out of reset, must wait 5 rising edges of clock before asserting TXValid for transmit. See Section 7.8.3
XCVRSELECT (XSEL)	Input	N/A	**Transceiver Select.** This signal selects between the FS and HS transceivers: 0: HS transceiver enabled 1: FS transceiver enabled.
TERMSELECT (TSEL)	Input	N/A	**Termination Select.** This signal selects between the FS and HS terminations: 0: HS termination enabled 1: FS termination enabled
SUSPENDN (SPDN)	Input	Low	**Suspend.** Places the transceiver in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for Suspend/Resume operation. While suspended, TERMSELECT must always be in FS mode to ensure that the 1.5kΩ pull-up on DP remains powered. 0: Transceiver circuitry drawing suspend current 1: Transceiver circuitry drawing normal current
CLKOUT (CLK)	Output	Rising Edge	**System Clock**. This output is used for clocking receive and transmit parallel data at 60MHz.
OPMODE[1:0] (OM1) (OM0)	Input	N/A	**Operational Mode.** These signals select between the various operational modes: [1] [0] Description 0 0 0: Normal Operation 0 1 1: Non-driving (all terminations removed) 1 0 2: Disable bit stuffing and NRZI encoding 1 1 3: Reserved
LINESTATE[1:0] (LS1) (LS0)	Output	N/A	**Line State**. These signals reflect the current state of the USB data bus in FS mode, with [0] reflecting the state of DP and [1] reflecting the state of DM. When the device is suspended or resuming from a suspended state, the signals are combinatorial. Otherwise, the signals are synchronized to CLKOUT. [1] [0] Description 0 0 0: SE0 0 1 1: J State 1 0 2: K State 1 1 3: SE1

Table 4.2 Data Interface Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION	
DATA[7:0] (D7) . . . (D0)	Bidirectional	High	**Data bus. 8-bit Bidirectional mode.**	
			TXVALID	**DATA[7:0]**
			0	output
			1	input
TXVALID (TXV)	Input	High	**Transmit Valid.** Indicates that the DATA bus is valid for transmit. The assertion of TXVALID initiates the transmission of SYNC on the USB bus. The negation of TXVALID initiates EOP on the USB. Control inputs (OPMODE[1:0], TERMSELECT,XCVRSELECT) must not be changed on the de-assertion or assertion of TXVALID. The PHY must be in a quiescent state when these inputs are changed.	
TXREADY (TXR)	Output	High	**Transmit Data Ready.** If TXVALID is asserted, the SIE must always have data available for clocking into the TX Holding Register on the rising edge of CLKOUT. TXREADY is an acknowledgement to the SIE that the transceiver has clocked the data from the bus and is ready for the next transfer on the bus. If TXVALID is negated, TXREADY can be ignored by the SIE.	
RXVALID (RXV)	Output	High	**Receive Data Valid.** Indicates that the DATA bus has received valid data. The Receive Data Holding Register is full and ready to be unloaded. The SIE is expected to latch the DATA bus on the rising edge of CLKOUT.	
RXACTIVE (RXA)	Output	High	**Receive Active.** Indicates that the receive state machine has detected Start of Packet and is active.	
RXERROR (RXE)	Output	High	**Receive Error**. 0: Indicates no error. 1: Indicates a receive error has been detected. This output is clocked with the same timing as the receive DATA lines and can occur at anytime during a transfer.	

Table 4.3 USB I/O Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
DP	I/O	N/A	**USB Positive Data Pin.**
DM	I/O	N/A	**USB Negative Data Pin.**

Table 4.4 Biasing and Clock Oscillator Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
RBIAS (RB)	Input	N/A	**External 1% bias resistor.** Requires a 12kΩ resistor to ground. Used for setting HS transmit current level and on-chip termination impedance.
XI/XO	Input	N/A	**External crystal.** 24MHz crystal connected from XI to XO.

Table 4.5 Power and Ground Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
VDD3.3 (V33)	N/A	N/A	**3.3V Supply.** Provides power for USB 2.0 Transceiver, UTMI+ Digital, Digital I/O, and Regulators.
REG_EN (REN)	Input	High	**On-Chip 1.8V regulator enable.** Connect to ground to disable both of the on chip (VDDA1.8 and VDD1.8) regulators. When regulators are disabled: ▪ External 1.8V must be supplied to VDDA1.8 and VDD1.8 pins. When the regulators are disabled, VDDA1.8 may be connected to VDD1.8 and a bypass capacitor (0.1μF recommended) should be connected to each pin. ▪ The voltage at VDD3.3 must be at least 2.64V (0.8 * 3.3V) before voltage is applied to VDDA1.8 and VDD1.8.
VDD1.8 (V18)	N/A	N/A	**1.8V Digital Supply.** Supplied by On-Chip Regulator when REG_EN is active. Low ESR 4.7uF minimum capacitor requirement when using internal regulators. Do not connect VDD1.8 to VDDA1.8 when using internal regulators. When the regulators are disabled, VDD1.8 may be connected to VDD1.8A.
VSS (GND)	N/A	N/A	**Common Ground.**
VDDA1.8 (V18A)	N/A	N/A	**1.8V Analog Supply.** Supplied by On-Chip Regulator when REG_EN is active. Low ESR 4.7uF minimum capacitor requirement when using internal regulators. Do not connect VDD1.8A to VDD1.8 when using internal regulators. When the regulators are disabled, VDD1.8A may be connected to VDD1.8.

Chapter 5 Limiting Values

Table 5.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum DP and DM voltage to Ground	V_{MAX_5V}		-0.3		5.5	V
Maximum VDD1.8 and VDDA1.8 voltage to Ground	$V_{MAX\_1.8V}$		-0.3		2.5	V
Maximum 3.3V Supply Voltage to Ground	$V_{MAX\_3.3V}$		-0.3		4.0	V
Maximum I/O Voltage to Ground	V_I		-0.3		4.0	V
Storage Temperature	T_{STG}		-55		150	°C
ESD PERFORMANCE						
All Pins	V_{HBM}	Human Body Model	±5			kV
LATCH-UP PERFORMANCE						
All Pins	I_{LTCH_UP}	EIA/JESD 78, Class II	150			mA

Note: In accordance with the Absolute Maximum Rating system (IEC 60134)

Table 5.2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage (VDD3.3 and VDDA3.3)	$V_{DD3.3}$		3.0	3.3	3.6	V
Input Voltage on Digital Pins	V_I		0.0		$V_{DD3.3}$	V
Input Voltage on Analog I/O Pins (DP, DM)	$V_{I(I/O)}$		0.0		$V_{DD3.3}$	V
Ambient Temperature	T_A		-40		85	°C

Table 5.3 Recommended External Clock Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Clock Frequency		XO driven by the external clock; and no connection at XI		24 (±100ppm)		MHz
System Clock Duty Cycle		XO driven by the external clock; and no connection at XI	45	50	55	%

Chapter 6 Electrical Characteristics

Table 6.1 Electrical Characteristics: Supply Pins (Note 6.1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Unconfigured Current	$I_{AVG(UCFG)}$	Device Unconfigured		55		mA
FS Idle Current	$I_{AVG(FS)}$	FS idle not data transfer		55		mA
FS Transmit Current	$I_{AVG(FSTX)}$	FS current during data transmit		60.5		mA
FS Receive Current	$I_{AVG(FSRX)}$	FS current during data receive		57.5		mA
HS Idle Current	$I_{AVG(HS)}$	HS idle not data transfer		60.6		mA
HS Transmit Current	$I_{AVG(HSTX)}$	HS current during data transmit		62.4		mA
HS Receive Current	$I_{AVG(HSRX)}$	HS current during data receive		61.5		mA
Low Power Mode	$I_{DD(LPM)}$	VBUS 15kΩ pull-down and 1.5kΩ pull-up resistor currents not included.		83		uA

Note 6.1 $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = -40°C to 85°C; unless otherwise specified.

Table 6.2 DC Electrical Characteristics: Logic Pins (Note 6.2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}		V_{SS}		0.8	V
High-Level Input Voltage	V_{IH}		2.0		$V_{DD3.3}$	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	$V_{DD3.3}$ - 0.5			V
Input Leakage Current	I_{LI}				± 1	uA
Pin Capacitance	Cpin				4	pF

Note 6.2 $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = -40°C to 85°C; unless otherwise specified.

Table 6.3 DC Electrical Characteristics: Analog I/O Pins (DP/DM) (Note 6.3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}				0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}		2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to $V_{DD3.3}$			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS and FS	Z_{HSDRV}	Steady state drive (See Figure 6.1)	40.5	45	49.5	Ω
Input Impedance	Z_{INP}	TX, RPU disabled	10			MΩ
Pull-up Resistor Impedance	Z_{PU}	Bus Idle	0.900	1.24	1.575	kΩ
Pull-up Resistor Impedance	Z_{PURX}	Device Receiving	1.425	2.26	3.09	kΩ
Termination Voltage For Pull-up Resistor On Pin DP	V_{TERM}		3.0		3.6	V
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
HS Squelch Detection Threshold (Differential)	V_{HSSQ}	Squelch Threshold			100	mV
		Unsquelch Threshold	150			mV
Output Levels						
High Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV

Table 6.3 DC Electrical Characteristics: Analog I/O Pins (DP/DM) (Note 6.3) (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
High Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV
Leakage Current						
OFF-State Leakage Current	I_{LZ}				± 1	uA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

Note 6.3 $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = -40°C to 85°C; unless otherwise specified.

Table 6.4 Dynamic Characteristics: Analog I/O Pins (DP/DM) (Note 6.4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS Output Driver Timing						
Rise Time	T_{FSR}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Fall Time	T_{FFF}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	FRFM	Excluding the first transition from IDLE state	90		111.1	%
HS Output Driver Timing						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification			See Figure 6.2	
High Speed Mode Timing						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification			See Figure 6.2	
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification			See Figure 6.2	

Note 6.4 $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = -40°C to 85°C; unless otherwise specified.

Table 6.5 Dynamic Characteristics: Digital UTMI Pins (Note 6.5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UTMI Timing						
DATA[7:0]	T_{PD}	Output Delay. Measured from PHY output to the rising edge of CLKOUT	2		5	ns
RXVALID						
RXACTIVE						
RXERROR						
LINESTATE[1:0]						
TXREADY						
DATA[7:0]	T_{SU}	Setup Time. Measured from PHY input to the rising edge of CLKOUT.	5			ns
TXVALID						
OPMODE[1:0]						
XCVRSELECT						
TERMSELECT						
DATA[7:0]	T_H	Hold time. Measured from the rising egde of CLKOUT to the PHY input signal edge.	0			ns
TXVALID						
OPMODE[1:0]						
XCVRSELECT						
TERMSELECT						

Note 6.5 $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = -40°C to 85°C; unless otherwise specified.

6.1 Driver Characteristics of Full-Speed Drivers in High-Speed Capable Transceivers

The USB3280 uses a differential output driver to drive the USB data signal onto the USB cable. Figure 6.1 Full-Speed Driver VOH/IOH Characteristics for High-speed Capable Transceiveron page 17 shows the V/I characteristics for a full-speed driver which is part of a high-speed capable transceiver. The normalized V/I curve for the driver must fall entirely inside the shaded region. The V/I region is bounded by the minimum driver impedance above (40.5 Ohm) and the maximum driver impedance below (49.5 Ohm). The output voltage must be within 10mV of ground when no current is flowing in or out of the pin.

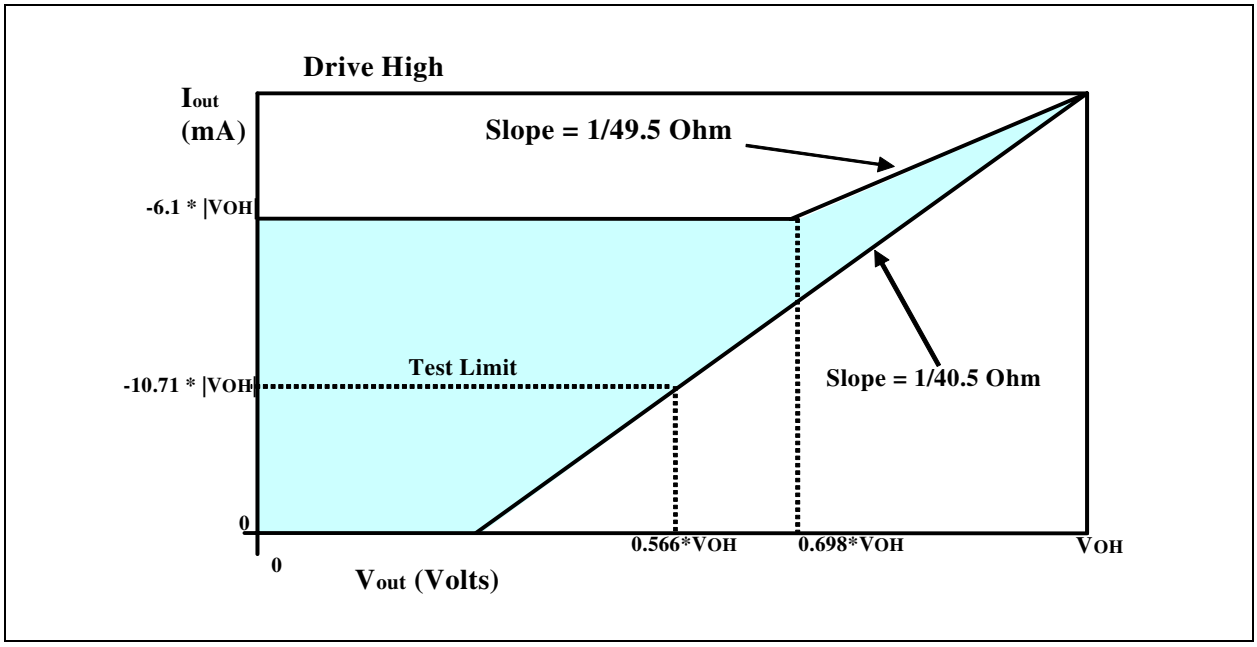

Figure 6.1 Full-Speed Driver VOH/IOH Characteristics for High-speed Capable Transceiver

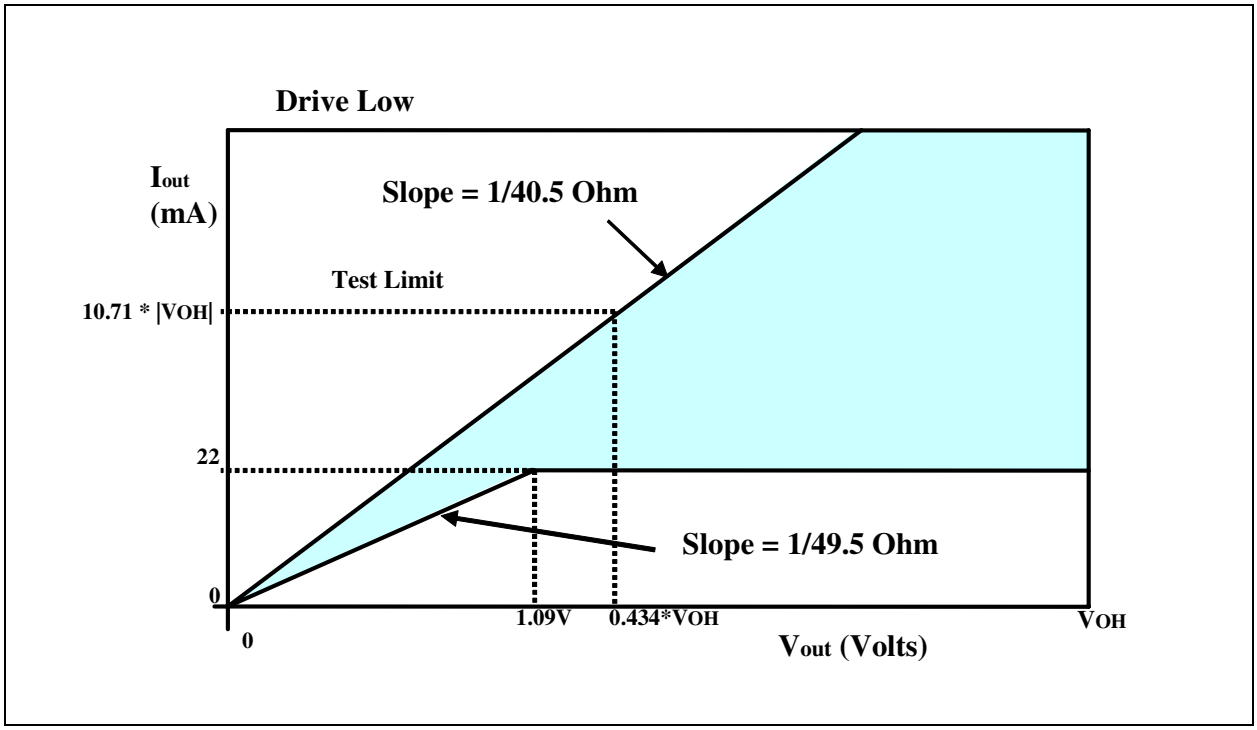

Figure 6.2 Full-Speed Driver VOL/IOL Characteristics for High-speed Capable Transceiver

6.2 High-speed Signaling Eye Patterns

High-speed USB signals are characterized using eye patterns. For measuring the eye patterns 4 points have been defined (see Figure 6.3). The Universal Serial Bus Specification Rev.2.0 defines the eye patterns in several 'templates'. The two templates that are relevant to the PHY are shown below.

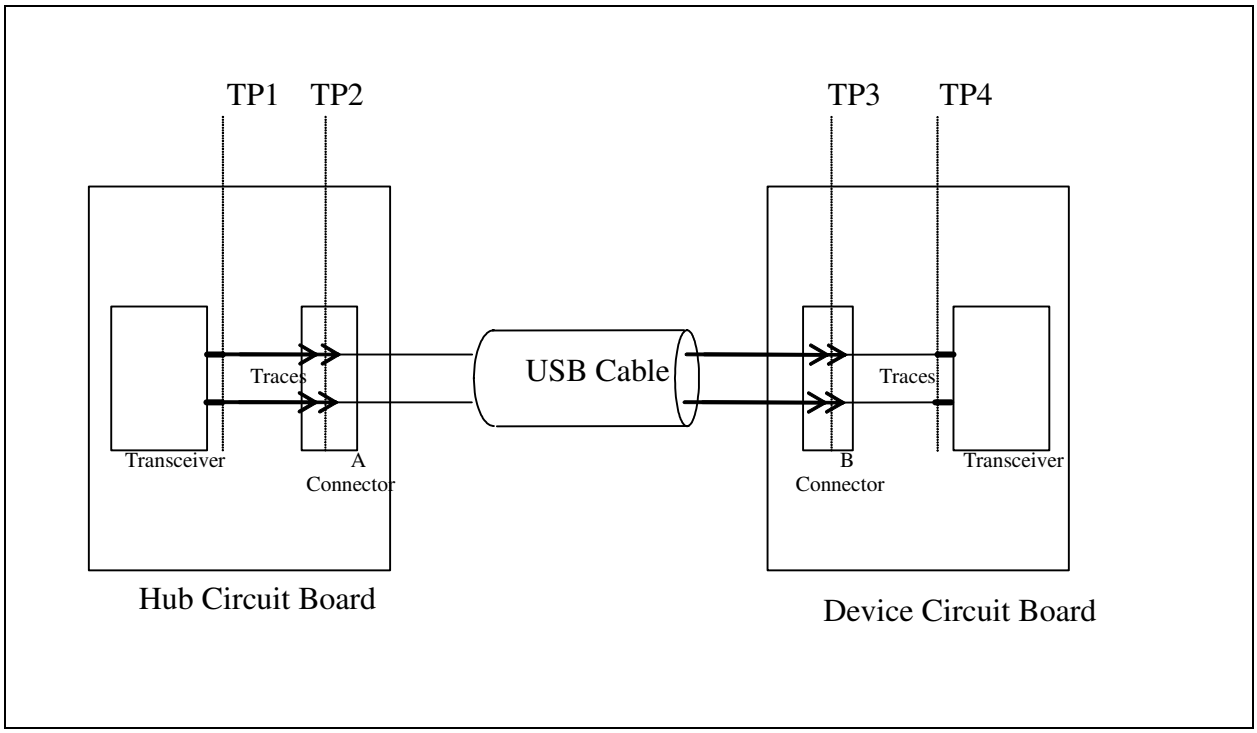

Figure 6.3 Eye Pattern Measurement Planes

The eye pattern in Figure 6.4 defines the transmit waveform requirements for a hub (measured at TP2 of Figure 6.3) or a device without a captive cable (measured at TP3 of Figure 6.3). The corresponding signal levels and timings are given in table below. Time is specified as a percentage of the unit interval (UI), which represents the nominal bit duration for a 480 Mbit/s transmission rate.

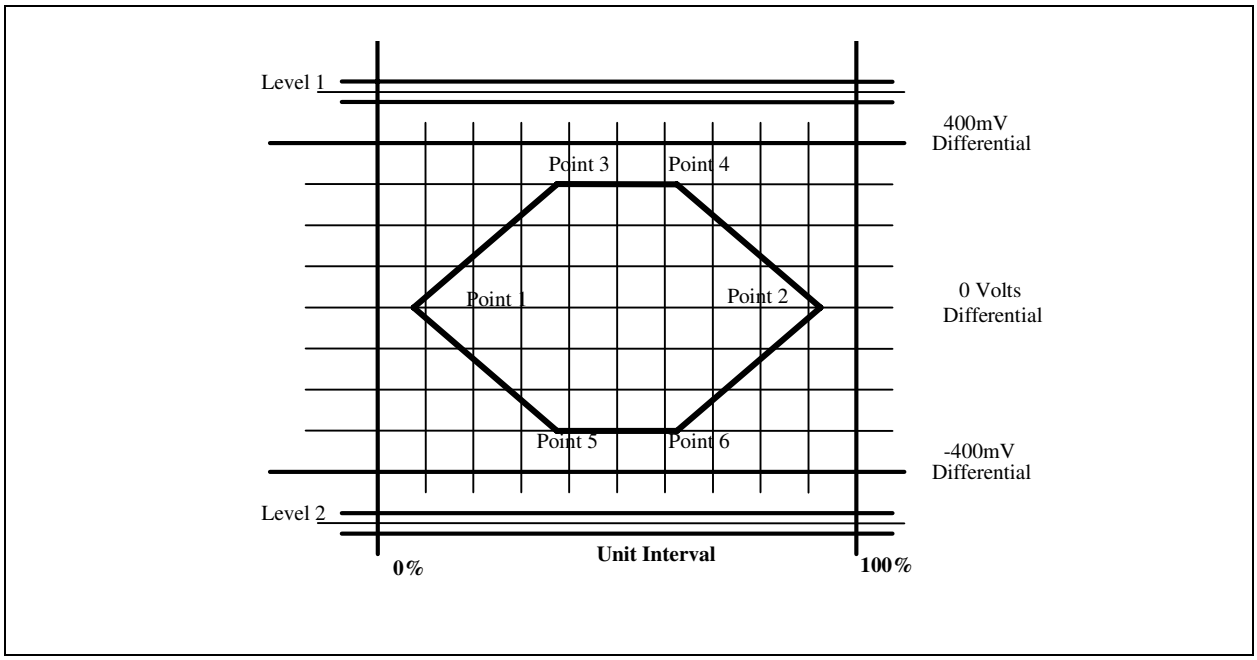

Figure 6.4 Eye Pattern for Transmit Waveform and Eye Pattern Definition

	VOLTAGE LEVEL (D+, D-)	TIME (% OF UNIT INTERVAL)
Level 1	525mV in UI following a transition, 475mV in all others	N/A
Level 2	-525mV in UI following a transition, -475mV in all others	N/A
Point 1	0V	7.5% UI
Point 2	0V	92.5% UI
Point 3	300mV	37.5% UI
Point 4	300mV	62.5% UI
Point 5	-300mV	37.5% UI
Point 6	-300mV	62.5% UI

The eye pattern in Figure 6.5 defines the receiver sensitivity requirements for a hub (signal applied at test point TP2 of Figure 6.3) or a device without a captive cable (signal applied at test point TP3 of Figure 6.3). The corresponding signal levels and timings are given in the table below. Timings are given as a percentage of the unit interval (UI), which represents the nominal bit duration for a 480 Mbit/s transmission rate.

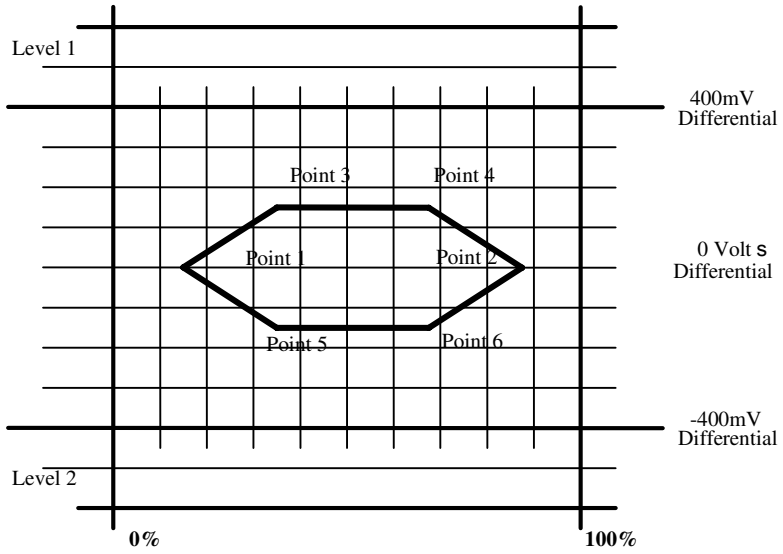

Figure 6.5 Eye Pattern for Receive Waveform and Eye Pattern Definition

	VOLTAGE LEVEL (D+, D-)	TIME (% OF UNIT INTERVAL)
Level 1	575mV	N/A
Level 2	-575mV	N/A
Point 1	0V	15% UI
Point 2	0V	85% UI
Point 3	150mV	35% UI
Point 4	150mV	65% UI
Point 5	-150mV	35% UI
Point 6	-150mV	65% UI

Chapter 7 Functional Overview

Figure 2.1 on page 7 shows the functional block diagram of the USB3280. Each of the functions is described in detail below.

7.1 Modes of Operation

The USB3280 supports an 8-bit bi-directional parallel interface.

- CLKOUT runs at 60MHz
- The 8-bit data bus (DATA[7:0]) is used for transmit when TXVALID = 1
- The 8-bit data bus (DATA[7:0]) is used for receive when TXVALID = 0

7.2 System Clocking

This block connects to either an external 24MHz crystal or an external clock source and generates a 480MHz multi-phase clock. The clock is used in the CRC block to over-sample the incoming received data, resynchronize the transmit data, and is divided down to 60MHz (CLKOUT) which acts as the system byte clock. The PLL block also outputs a clock valid signal to the other parts of the transceiver when the clock signal is stable. All UTMI signals are synchronized to the CLKOUT output. The behavior of the CLKOUT is as follows:

- Produce the first CLKOUT transition no later than 5.6ms after negation of SUSPENDN. The CLKOUT signal frequency error is less than 10% at this time.
- The CLKOUT signal will fully meet the required accuracy of ±500ppm no later than 1.4ms after the first transition of CLKOUT.

In HS mode there is one CLKOUT cycle per byte time. The frequency of CLKOUT does not change when the PHY is switched between HS to FS modes. In FS mode there are 5 CLKOUT cycles per FS bit time, typically 40 CLKOUT cycles per FS byte time. If a received byte contains a stuffed bit then the byte boundary can be stretched to 45 CLKOUT cycles, and two stuffed bits would result in a 50 CLKOUT cycles.

Figure 7.1 shows the relationship between CLKOUT and the transmit data transfer signals in FS mode. TXREADY is only asserted for one CLKOUT per byte time to signal the SIE that the data on the DATA lines has been read by the PHY. The SIE may hold the data on the DATA lines for the duration of the byte time. Transitions of TXVALID must meet the defined setup and hold times relative to CLKOUT.

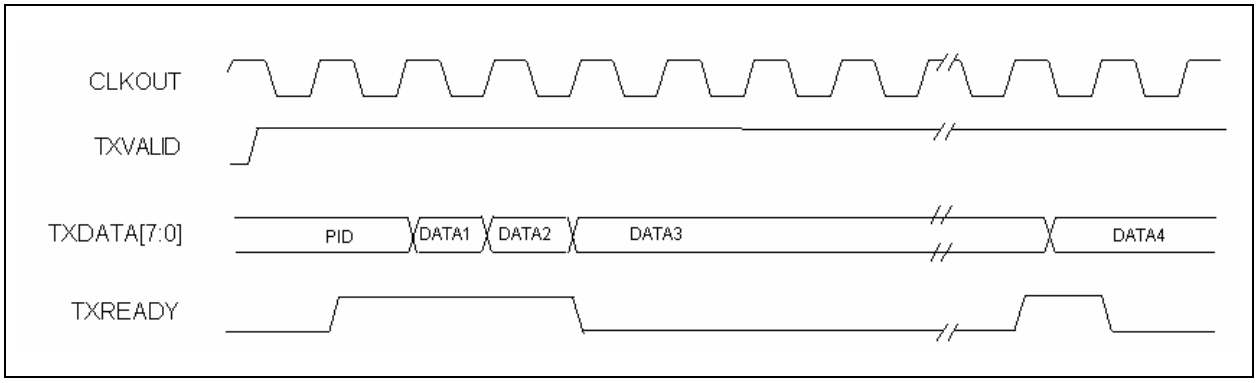

Figure 7.1 FS CLK Relationship to Transmit Data and Control Signals

Figure 7.2 shows the relationship between CLKOUT and the receive data control signals in FS mode. RXACTIVE "frames" a packet, transitioning only at the beginning and end of a packet. However transitions of RXVALID may take place any time 8 bits of data are available. Figure 7.1 also shows how RXVALID is only asserted for one CLKOUT cycle per byte time even though the data may be presented for the full byte time. The XCVRSELECT signal determines whether the HS or FS timing relationship is applied to the data and control signals.

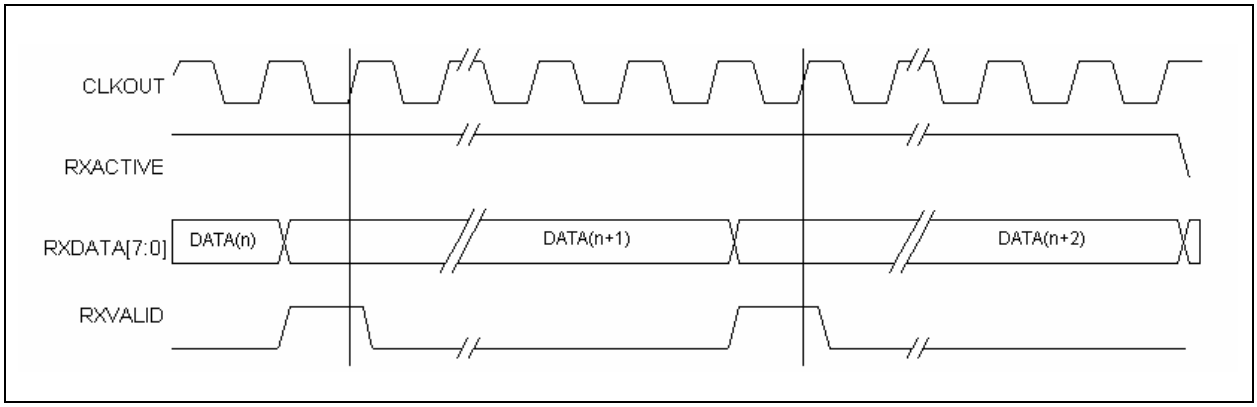

Figure 7.2 FS CLK Relationship to Receive Data and Control Signals

7.3 Clock and Data Recovery Circuit

This block consists of the Clock and Data Recovery Circuit and the Elasticity Buffer. The Elasticity Buffer is used to compensate for differences between the transmitting and receiving clock domains. The USB 2.0 specification defines a maximum clock error of ±1000ppm of drift.

7.4 TX Logic

This block receives parallel data bytes placed on the DATA bus and performs the necessary transmit operations. These operations include parallel to serial conversion, bit stuffing and NRZI encoding. Upon valid assertion of the proper TX control lines by the SIE and TX State Machine, the TX LOGIC block will synchronously shift, at either the FS or HS rate, the data to the FS/HS TX block to be transmitted on the USB cable. Data transmit timing is shown in Figure 7.3.

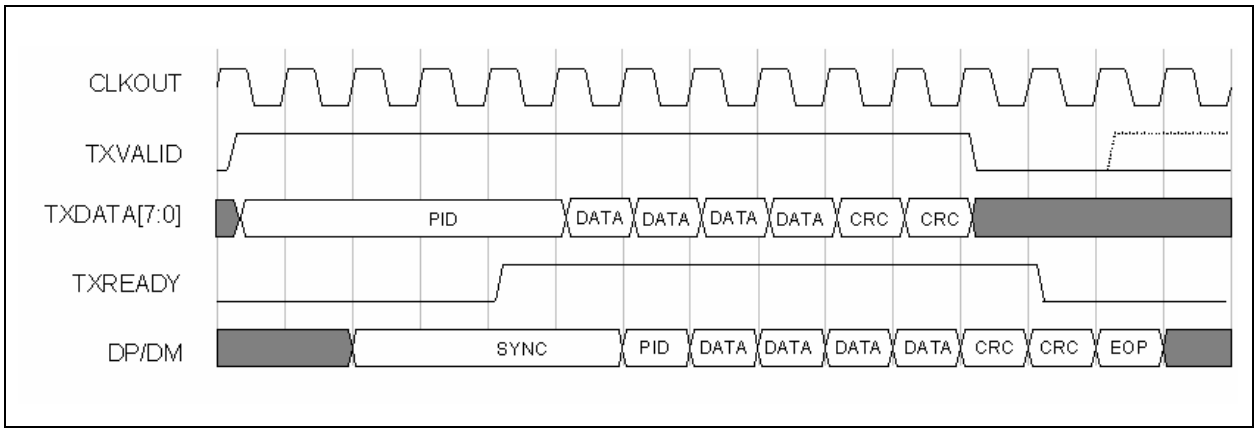

Figure 7.3 Transmit Timing for a Data Packet

The behavior of the Transmit State Machine is described below.

- Asserting a RESET forces the transmit state machine into the Reset state which negates TXREADY. When RESET is negated the transmit state machine will enter a wait state.
- The SIE asserts TXVALID to begin a transmission.
- After the SIE asserts TXVALID it can assume that the transmission has started when it detects TXREADY has been asserted.
- The SIE must assume that the USB3280 has consumed a data byte if TXREADY and TXVALID are asserted on the rising edge of CLKOUT.
- The SIE must have valid packet information (PID) asserted on the DATA bus coincident with the assertion of TXVALID.
- TXREADY is sampled by the SIE on the rising edge of CLKOUT.
- The SIE negates TXVALID to complete a packet. Once negated, the transmit logic will never reassert TXREADY until after the EOP has been generated. (TXREADY will not re-assert until TXVALD asserts again.
- The USB3280 is ready to transmit another packet immediately, however the SIE must conform to the minimum inter-packet delays identified in the USB 2.0 specification.

7.5 RX Logic

This block receives serial data from the CRC block and processes it to be transferred to the SIE on the DATA bus. The processing involved includes NRZI decoding, bit unstuffing, and serial to parallel conversion. Upon valid assertion of the proper RX control lines by the RX State Machine, the RX Logic block will provide bytes to the DATA bus as shown in the figures below. The behavior of the Receive State Machine is described below.

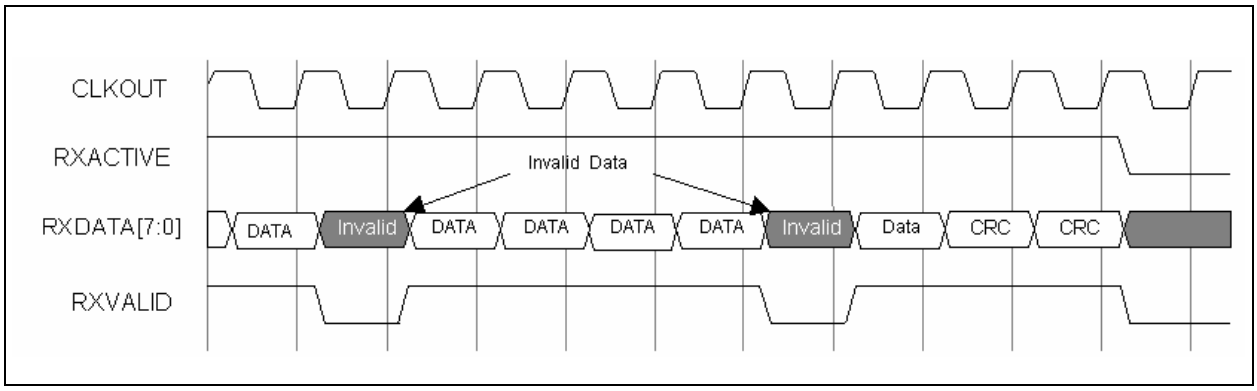

Figure 7.4 Receive Timing for Data with Unstuffed Bits

The assertion of RESET will force the Receive State Machine into the *Reset* state. The *Reset* state deasserts RXACTIVE and RXVALID. When the RESET signal is deasserted the Receive State Machine enters the *RX Wait* state and starts looking for a SYNC pattern on the USB. When a SYNC pattern is detected the state machine will enter the *Strip SYNC* state and assert RXACTIVE. The length of the received Hi-Speed SYNC pattern varies and can be up to 32 bits long or as short as 12 bits long when at the end of five hubs. As a result, the state machine may remain in the *Strip SYNC* state for several byte times before capturing the first byte of data and entering the *RX Data* state.

After valid serial data is received, the state machine enters the *RX Data* state, where the data is loaded into the RX Holding Register on the rising edge of CLKOUT and RXVALID is asserted. The SIE must clock the data off the DATA bus on the next rising edge of CLKOUT. If OPMODE = Normal, then stuffed bits are stripped from the data stream. Each time 8 stuffed bits are accumulated the state machine will enter the *RX Data Wait* state, negating RXVALID thus skipping a byte time.

When the EOP is detected the state machine will enter the *Strip EOP* state and negate RXACTIVE and RXVALID. After the EOP has been stripped the Receive State Machine will reenter the *RX Wait* state and begin looking for the next packet.

The behavior of the Receive State Machine is described below:

- RXACTIVE and RXREADY are sampled on the rising edge of CLKOUT.
- In the RX Wait state the receiver is always looking for SYNC.
- The USB3280 asserts RXACTIVE when SYNC is detected (Strip SYNC state).
- The USB3280 negates RXACTIVE when an EOP is detected and the elasticity buffer is empty (Strip EOP state).
- When RXACTIVE is asserted, RXVALID will be asserted if the RX Holding Register is full.
- RXVALID will be negated if the RX Holding Register was not loaded during the previous byte time. This will occur if 8 stuffed bits have been accumulated.
- The SIE must be ready to consume a data byte if RXACTIVE and RXVALID are asserted (RX Data state).
- Figure 7.5 shows the timing relationship between the received data (DP/DM), RXVALID, RXACTIVE, RXERROR and DATA signals.

Notes:

- The USB 2.0 Transceiver does NOT decode Packet ID's (PIDs). They are passed to the SIE for decoding.
- Figure 7.5, Figure 7.6 and Figure 7.7 are timing examples of a HS/FS PHY when it is in HS mode. When a HS/FS PHY is in FS Mode there are approximately 40 CLKOUT cycles every byte time. The Receive State Machine assumes that the SIE captures the data on the DATA bus if RXACTIVE and RXVALID are asserted. In FS mode, RXVALID will only be asserted for one CLKOUT per byte time.
- In Figure 7.5, Figure 7.6 and Figure 7.7 the SYNC pattern on DP/DM is shown as one byte long. The SYNC pattern received by a device can vary in length. These figures assume that all but the last 12 bits have been consumed by the hubs between the device and the host controller.

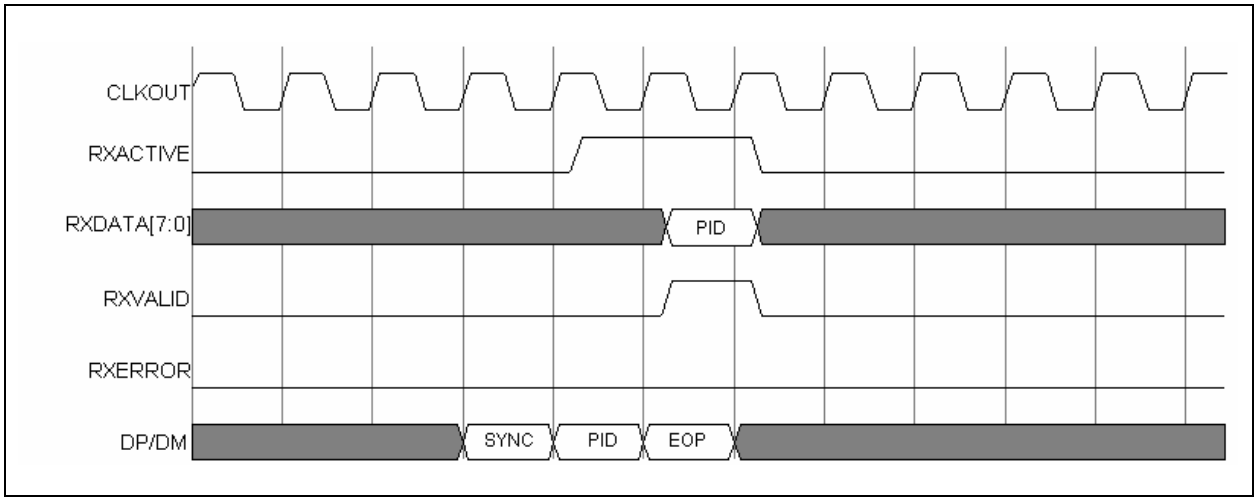

Figure 7.5 Receive Timing for a Handshake Packet (no CRC)

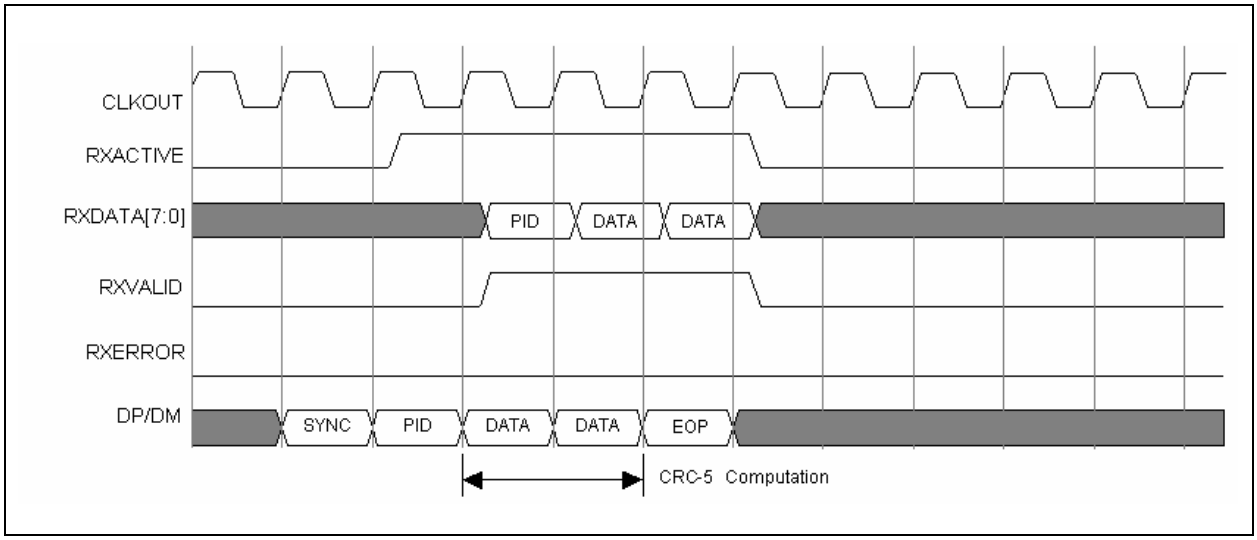

Figure 7.6 Receive Timing for Setup Packet

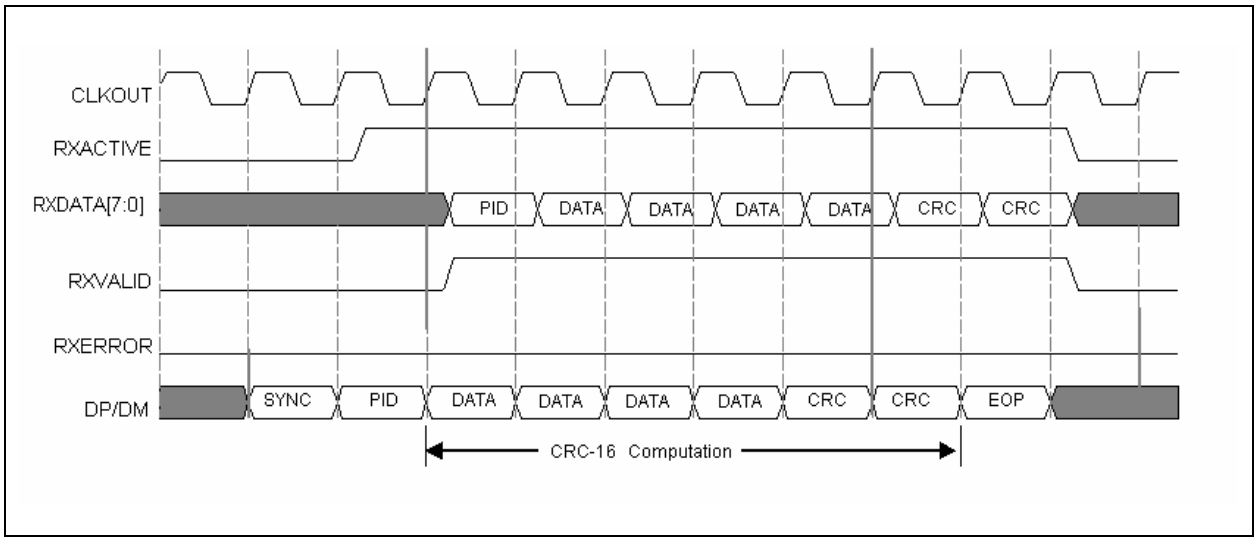

Figure 7.7 Receive Timing for Data Packet (with CRC-16)

The receivers connect directly to the USB cable. The block contains a separate differential receiver for HS and FS mode. Depending on the mode, the selected receiver provides the serial data stream through the mulitplexer to the RX Logic block. The FS mode section of the FS/HS RX block also consists of a single-ended receiver on each of the data lines to determine the correct FS LINESTATE. For HS mode support, the FS/HS RX block contains a squelch circuit to insure that noise is never interpreted as data.