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# USB3300

## Hi-Speed USB Host, Device or OTG PHY with ULPI Low Pin Interface

### Product Features

- USB-IF Hi-Speed certified to the Universal Serial Bus Specification Rev 2.0
- Interface compliant with the ULPI Specification revision 1.1 in 8-bit mode
- Industry standard UTMI+ Low Pin Interface (ULPI) Converts 54 UTMI+ signals into a standard 12 pin Link controller interface
- 54.7mA Unconfigured Current (typical) - ideal for bus powered applications
- 83uA suspend current (typical) - ideal for battery powered applications
- Latch-Up performance exceeds 150 mA per EIA/JESD 78, Class II
- ESD protection levels of ±8kV HBM without external protection devices
- Integrated protection to withstand IEC61000-4-2 ESD tests (±8kV contact and ±15kV air) per 3rd party test facility
- Supports FS pre-amble for FS hubs with a LS device attached (UTMI+ Level 3)
- Supports HS SOF and LS keep-alive pulse
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 1.0a specification
- Supports the OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Allows host to turn VBUS off to conserve battery power in OTG applications
- Supports OTG monitoring of VBUS levels with internal comparators. Includes support for an external VBUS or fault monitor.
- Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max) allows use of legacy UTMI Links with a ULPI wrapper
- Integrated Pull-up resistor on STP for interface protection allows a reliable Link/PHY start-up with slow Links (software configured for low power)
- Internal 1.8 volt regulators allow operation from a single 3.3 volt supply
- Internal short circuit protection of ID, DP and DM lines to VBUS or ground
- Integrated 24MHz Crystal Oscillator supports either crystal operation or 24MHz external clock input
- Internal PLL for 480MHz Hi-Speed USB operation
- Industrial Operating Temperature -40°C to +85°C
- 32 pin, QFN RoHS Compliant package (5 x 5 x 0.90 mm height)

### Applications

The USB3300 is the ideal companion to any ASIC, SoC or FPGA solution designed with a ULPI Hi-Speed USB host, peripheral or OTG core.

The USB3300 is well suited for:

- Cell Phones
- PDAs
- MP3 Players
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Printers

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## Table of Contents

# 1.0 INTRODUCTION

## 1.1 General Description

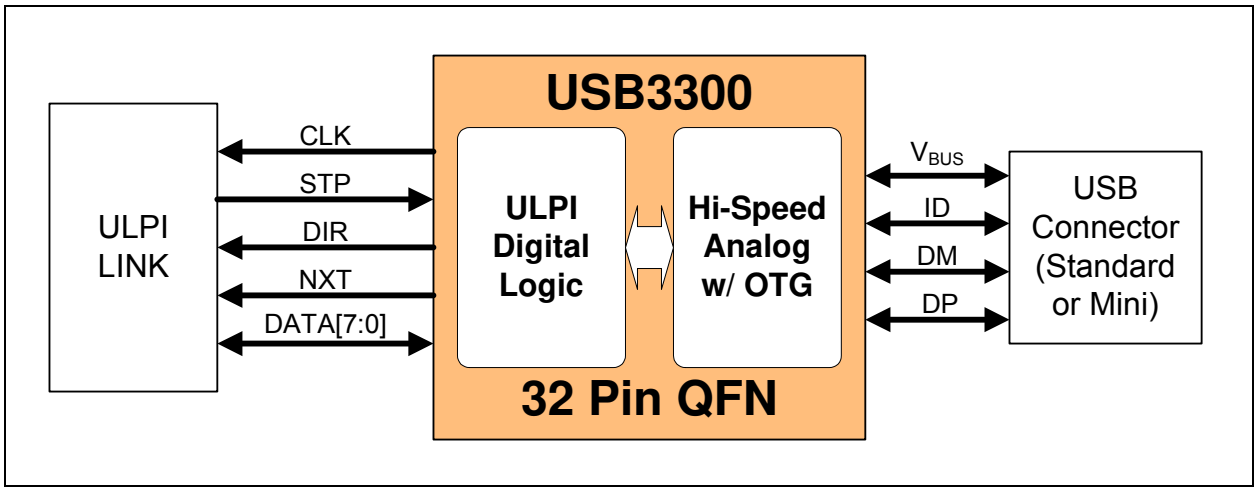
The USB3300 is an industrial temperature Hi-Speed USB Physical Layer Transceiver (PHY). The USB3300 uses a low pin count interface (ULPI) to connect to a ULPI compliant Link layer. The ULPI interface reduces the UTMI+ interface from 54 pins to 12 pins using a method of in-band signaling and status byte transfers between the Link and PHY.

This PHY was designed from the start with the ULPI interface. No UTMI to ULPI wrappers are used in this design which provides a seamless ULPI to Link interface. The result is a PHY with a low latency transmit and receive time. Microchip's low latency high speed and full speed receiver provide the option of re-using existing UTMI Links with a simple wrapper to convert UTMI to ULPI.

The ULPI interface allows the USB3300 PHY to operate as a device, host, or an On-The-Go (OTG) device. Designs using the USB3300 PHY as a device, can add host and OTG capability at a later date with no additional pins.

The ULPI interface, combined with Microchip's proprietary technology, makes the USB3300 the ideal method of adding Hi-Speed USB to new designs. The USB3300 features an industry leading small footprint package (5mm by 5mm) with sub 1mm height. In addition the USB3300 integrates all DP and DM termination resistances and requires a minimal number of external components.

**FIGURE 1-1: BASIC ULPI USB DEVICE BLOCK DIAGRAM**



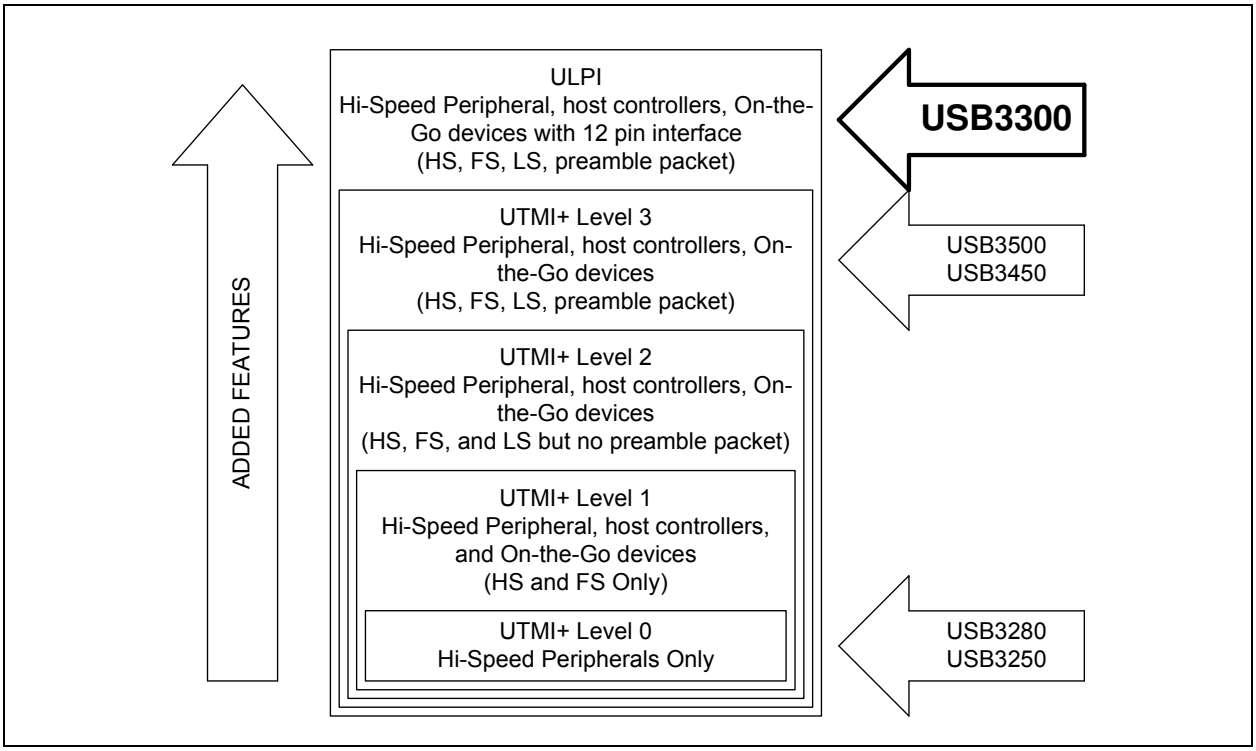

The ULPI interface consists of 12 interface pins; 8 bi-directional data pins, 3 control pins, and a 60 MHz clock. By using the 12 pin ULPI interface the USB3300 is able to provide support for the full range of UTMI+ Level 3 through Level 0, as shown in Figure 1-2. This allows USB3300 to work as a HS and FS peripheral and as a HS, FS, and LS Host.

The USB3300 can also, as an option, fully support the On-the-Go (OTG) protocol defined in the On-The-Go Supplement to the USB 2.0 Specification. On-the-Go allows the USB3300 to function like a host, or peripheral configured dynamically by software. For example, a cell phone may connect to a computer as a peripheral to exchange address information or connect to a printer as a host to print pictures. Finally the OTG enabled device can connect to another OTG enabled device to exchange information. All this is supported using a single low profile Mini-AB USB connector.

Designs not needing OTG can ignore the OTG feature set.

In addition to the advantages of the leading edge ULPI interface, the use of Microchip's advanced analog technology enables the USB3300 to consume a minimum amount of power which results in maximized battery life for portable applications.

**FIGURE 1-2: ULPI INTERFACE FEATURES AS RELATED TO UTMI+**



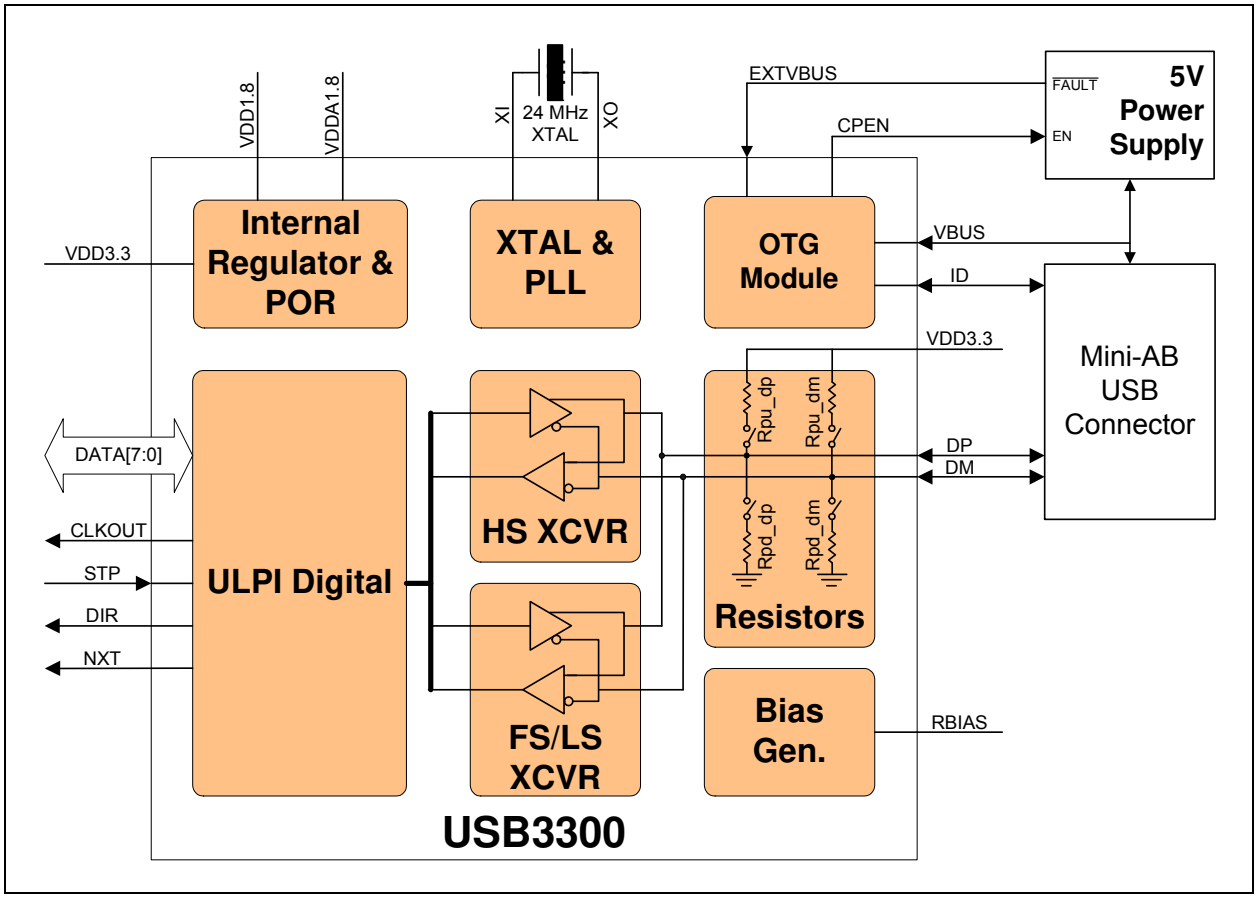

## 1.2 Reference Documents

- Universal Serial Bus Specification, Revision 2.0, April 27, 2000
- On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a, June 24, 2003
- USB 2.0 Transceiver Macrocell Interface (UTMI) Specification, Version 1.02, May 27, 2000
- UTMI+ Specification, Revision 1.0, February 2, 2004
- UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1

## 2.0 FUNCTIONAL OVERVIEW

The USB3300 is a highly integrated USB PHY. It contains a complete Hi-Speed USB 2.0 PHY with the ULPI industry standard interface to support fast time to market for a USB product. The USB3300 is composed of the functional blocks shown in Figure 2-1 below. Details of these individual blocks are described in Architecture Overview on page 16.

**FIGURE 2-1: USB3300 BLOCK DIAGRAM**

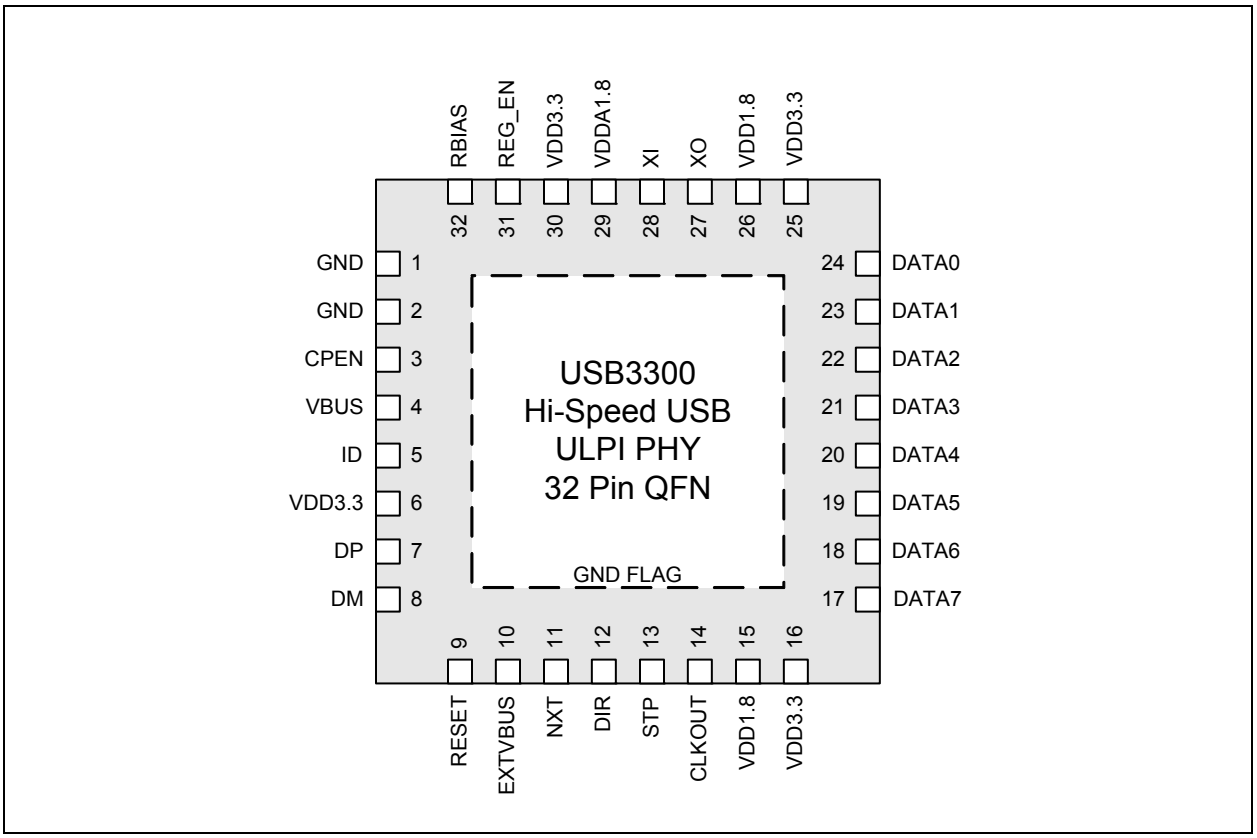


## 3.0 PIN LAYOUT

The USB3300 is offered in a 32 pin QFN package (5 x 5 x 0.9mm). The pin definitions and locations are documented below.

### 3.1 USB3300 Pin Diagram

**FIGURE 3-1: USB3300 PIN DIAGRAM - TOP VIEW**




The exposed flag of the QFN package must be connected to ground with a via array to the ground plane. This is the main ground connection for the USB3300.

### 3.2 Pin Function

**TABLE 3-1: USB3300 PIN DEFINITIONS 32-PIN QFN PACKAGE**

| Pin | Name | Direction, Type | Active Level | Description |
|---|---|---|---|---|
| **1** | **GND** | Ground | N/A | Ground |
| **2** | **GND** | Ground | N/A | Ground |
| **3** | **CPEN** | Output, CMOS | High | External 5 volt supply enable. This pin is used to enable the external Vbus power supply. The CPEN pin is low on POR. |
| **4** | **VBUS** | I/O, Analog | N/A | VBUS pin of the USB cable. The USB3300 uses this pin for the Vbus comparator inputs and for Vbus pulsing during session request protocol. |
| **5** | **ID** | Input, Analog | N/A | ID pin of the USB cable. For non-OTG applications this pin can be floated. For an A-Device ID = 0. For a B-Device ID = 1. |

**TABLE 3-1: USB3300 PIN DEFINITIONS 32-PIN QFN PACKAGE (CONTINUED)**

| Pin | Name | Direction, Type | Active Level | Description |
|---|---|---|---|---|
| 6 | **VDD3.3** | Power | N/A | 3.3V Supply. A 0.1uF bypass capacitor should be connected between this pin and the ground plane on the PCB. |
| 7 | **DP** | I/O, Analog | N/A | D+ pin of the USB cable. |
| 8 | **DM** | I/O, Analog | N/A | D- pin of the USB cable. |
| 9 | **RESET** | Input, CMOS | High | Optional active high transceiver reset. This is the same as a write to the ULPI *Reset*, address 04h, bit 5. This does not reset the ULPI register set. This pin includes an integrated pull-down resistor to ground. If not used, this pin can be floated or connected to ground (recommended).<br><br>See Section 6.1.11, "Reset Pin" for details. |
| 10 | **EXTVBUS** | Input, CMOS | High | External Vbus Detect. Connect to fault output of an external USB power switch or an external Vbus Valid comparator. See Section 6.5.4, "External Vbus Indicator," on page 38 for details. This pin has a pull down resistor to prevent it from floating when the ULPI bit *UseExternalVbusIndicator* is set to 0. |
| 11 | **NXT** | Output, CMOS | High | The PHY asserts NXT to throttle the data. When the Link is sending data to the PHY, NXT indicates when the current byte has been accepted by the PHY. The Link places the next byte on the data bus in the following clock cycle. |
| 12 | **DIR** | Output, CMOS | N/A | Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives DIR high to take ownership of the bus. When the PHY has no data to transfer it drives DIR low and monitors the bus for commands from the Link. The PHY will pull DIR high whenever the interface cannot accept data from the Link, such as during PLL start-up. |
| 13 | **STP** | Input, CMOS | High | The Link asserts STP for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, STP indicates the last byte of data was on the bus in the previous cycle. The STP pin also includes the interface protection detailed in Section 6.1.9.3, "Interface Protection," on page 31**.** |
| 14 | **CLKOUT** | Output, CMOS | N/A | 60MHz reference clock output. All ULPI signals are driven synchronous to the rising edge of this clock. |
| 15 | **VDD1.8** | Power | N/A | 1.8V for digital circuitry on chip. Supplied by On-Chip Regulator when REG_EN is active. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. Connect pin 15 to pin 26. |
| 16 | **VDD3.3** | Power | N/A | A 0.1uF bypass capacitor should be connected between this pin and the ground plane on the PCB. |

**TABLE 3-1: USB3300 PIN DEFINITIONS 32-PIN QFN PACKAGE (CONTINUED)**

| Pin | Name | Direction, Type | Active Level | Description |
|---|---|---|---|---|
| 17 | **DATA[7]** | I/O, CMOS, Pull-low | N/A | 8-bit bi-directional data bus. Bus ownership is determined by DIR. The Link and PHY initiate data transfers by driving a non-zero pattern onto the data bus. ULPI defines interface timing for a single-edge data transfers with respect to rising edge of CLKOUT. DATA[7] is the MSB and DATA[0] is the LSB. |
| 18 | **DATA[6]** | I/O, CMOS, Pull-low | N/A | |
| 19 | **DATA[5]** | I/O, CMOS, Pull-low | N/A | |
| 20 | **DATA[4]** | I/O, CMOS, Pull-low | N/A | |
| 21 | **DATA[3]** | I/O, CMOS, Pull-low | N/A | |
| 22 | **DATA[2]** | I/O, CMOS, Pull-low | N/A | |
| 23 | **DATA[1]** | I/O, CMOS, Pull-low | N/A | |
| 24 | **DATA[0]** | I/O, CMOS, Pull-low | N/A | |
| 25 | **VDD3.3** | Power | N/A | A 0.1uF bypass capacitor should be connected between this pin and the ground plane on the PCB. |
| 26 | **VDD1.8** | Power | N/A | 1.8V for digital circuitry on chip. Supplied by On-Chip Regulator when REG_EN is active. When using the internal regulators, place a 4.7uF low-ESR capacitor near this pin and connect the capacitor from this pin to ground. Connect pin 26 to pin 15. Do not connect VDD1.8 to VDDA1.8 when using internal regulators. When the regulators are disabled, pin 29 may be connected to pins 26 and 15. |
| 27 | **XO** | Output, Analog | N/A | Crystal pin. If using an external clock on XI this pin should be floated. |
| 28 | **XI** | Input, Analog | N/A | Crystal pin. A 24MHz crystal is supported. The crystal is placed across XI and XO. An external 24MHz clock source may be driven into XI in place of a crystal. |
| 29 | **VDDA1.8** | Power | N/A | 1.8V for analog circuitry on chip. Supplied by On-Chip Regulator when REG_EN is active. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. When using the internal regulators, place a 4.7uF low-ESR capacitor near this pin in parallel with the 0.1uF capacitor. Do not connect VDD1.8A to VDD1.8 when using internal regulators. When the regulators are disabled, pin 29 may be connected to pins 26 and 15. |
| 30 | **VDD3.3** | Power | N/A | Analog 3.3 volt supply. A 0.1uF low ESR bypass capacitor connected to the ground plane of the PCB is recommended. |

**TABLE 3-1: USB3300 PIN DEFINITIONS 32-PIN QFN PACKAGE (CONTINUED)**

| Pin | Name | Direction, Type | Active Level | Description |
|---|---|---|---|---|
| 31 | **REG_EN** | I/O, CMOS, Pull-low | N/A | On-Chip 1.8V regulator enable. Connect to ground to disable both of the on chip (VDDA1.8 and VDD1.8) regulators. When regulators are disabled:<br>• External 1.8V must be supplied to VDDA1.8 and VDD1.8 pins. When the regulators are disabled, VDDA1.8 may be connected to VDD1.8 and a bypass capacitor (0.1uF recommended) should be connected to each pin.<br>• The voltage at VDD3.3 must be at least 2.64V (0.8 * 3.3V) before voltage is applied to VDDA1.8 and VDD1.8. |
| 32 | **RBIAS** | Analog, CMOS | N/A | External 12KΩ +/- 1% bias resistor to ground. |
| | **GND FLAG** | Ground | N/A | Ground. The flag must be connected to the ground plane with a via array under the exposed flag. This is the main ground for the IC. |

## 4.0 OPERATIONAL DESCRIPTION

**TABLE 4-1: MAXIMUM GUARANTEED RATINGS**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| Maximum VBUS, ID, EXTVBUS, DP, and DM voltage to GND | $V_{MAX\_5V}$ | | -0.5 | | +5.5 | V |
| Maximum VDD1.8 and VDDA1.8 voltage to Ground | $V_{MAX\_1.8V}$ | | -0.5 | | 2.5 | V |
| Maximum 3.3V supply voltage to Ground | $V_{MAX\_3.3V}$ | | -0.5 | | 4.0 | V |
| Maximum I/O voltage to Ground | $V_{MAX\_IN}$ | | -0.5 | | 4.0 | V |
| Operating Temperature | $T_{MAX\_OP}$ | | -40 | | 85 | °C |
| Storage Temperature | $T_{MAX\_STG}$ | | -55 | | 150 | °C |
| **ESD PERFORMANCE** | | | | | | |
| All Pins | $V_{HBM}$ | Human Body Model | ±8 | | | kV |
| **LATCH-UP PERFORMANCE** | | | | | | |
| All Pins | $I_{LTCH\_UP}$ | EIA/JESD 78, Class II | 150 | | | mA |

**Note:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TABLE 4-2: RECOMMENDED OPERATING CONDITIONS**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| VDD3.3 to GND | $V_{DD3.3}$ | | 3.0 | 3.3 | 3.6 | V |
| Input Voltage on Digital Pins | $V_I$ | | 0.0 | | $V_{DD3.3}$ | V |
| Voltage on Analog I/O Pins (DP, DM, ID) | $V_{I(I/O)}$ | | 0.0 | | $V_{DD3.3}$ | V |
| VBUS to GND | $V_{VBUS}$ | | 0.0 | | 5.25 | |
| Ambient Temperature | $T_A$ | | -40 | | 85 | C |

## 5.0 ELECTRICAL CHARACTERISTICS

**TABLE 5-1: ELECTRICAL CHARACTERISTICS: SUPPLY PINS**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| **Unconfigured Current** | | $I_{AVG(UCFG)}$ | Device Unconfigured | Same as Idle | | mA |
| **FS Idle 3.3V Current** | | $I_{AVG(FS33)}$ | FS idle not data transfer | 18.8 | 21.9 | mA |
| **FS Idle 1.8V Current** | | $I_{AVG(FS18)}$ | FS idle not data transfer | 36.4 | 43.2 | mA |
| **FS Transmit 3.3V Current** | | $I_{AVG(FSTX33)}$ | FS current during data transmit | 36.0 | 41.6 | mA |
| **FS Transmit 1.8V Current** | | $I_{AVG(FSTX18)}$ | FS current during data transmit | 36.8 | 43.2 | mA |
| **FS Receive 3.3V Current** | | $I_{AVG(FSRX33)}$ | FS current during data receive | 22.5 | 27.0 | mA |
| **FS Receive 1.8V Current** | | $I_{AVG(FSRX18)}$ | FS current during data receive | 36.7 | 43.4 | mA |
| **HS Idle 3.3V Current** | | $I_{AVG(HS33)}$ | HS idle not data transfer | 22.1 | 25.4 | mA |
| **HS Idle 1.8V Current** | | $I_{AVG(HS18)}$ | HS idle not data transfer | 38.7 | 45.6 | mA |
| **HS Transmit 3.3V Current** | | $I_{AVG(HSTX33)}$ | HS current during data transmit | 25.4 | 29.0 | mA |
| **HS Transmit 1.8V Current** | | $I_{AVG(HSTX18)}$ | HS current during data transmit | 39.1 | 46.2 | mA |
| **HS Receive 3.3V Current** | | $I_{AVG(HSRX33)}$ | HS current during data receive | 23.0 | 26.6 | mA |
| **HS Receive 1.8V Current** | | $I_{AVG(HSRX18)}$ | HS current during data receive | 39.6 | 46.8 | mA |
| **Low Power Mode 3.3V Current** | | $I_{DD(LPM33)}$ | VBUS 15kΩ pull-down and 1.5kΩ pull-up resistor currents not included. | 59.4 | | uA |
| **Low Power Mode 1.8V Current** | | $I_{DD(LPM18)}$ | VBUS 15kΩ pull-down and 1.5kΩ pull-up resistor currents not included. | 25.5 | | uA |

**Note:**

- $V_{DD3.3}$ = 3.0 to 3.6V; $V_{SS}$ = 0V; $T_A$ = -40C to +85C; unless otherwise specified.
- SessEnd and VbusVld comparators disabled. Interface protection disabled.
- Maximum current numbers are worst case over supply voltage, temperature and process.

**TABLE 5-2: ELECTRICAL CHARACTERISTICS: CLKOUT START-UP**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| Suspend Recovery Time | $T_{START}$ | | | 2.25 | 3.5 | ms |

**Note:** The USB330 uses the *AutoResume* feature, Section 6.3, for host start-up of less than 1ms.

**TABLE 5-3: DC ELECTRICAL CHARACTERISTICS: LOGIC PINS**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| Low-Level Input Voltage | $V_{IL}$ | | $V_{SS}$ | | 0.8 | V |
| High-Level Input Voltage | $V_{IH}$ | | 2.0 | | $V_{DD3.3}$ | V |
| Low-Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 8mA | | | 0.4 | V |
| High-Level Output Voltage | $V_{OH}$ | $I_{OH}$ = -8mA | $V_{DD3.3}$ - 0.4 | | | V |
| Input Leakage Current | $I_{LI}$ | | | | ±10 | uA |
| Pin Capacitance | Cpin | | | | 4 | pF |

**Note:** $V_{DD3.3}$ = 3.0 to 3.6V; $V_{SS}$ = 0V; $T_A$ = -40C to +85C; unless otherwise specified.

**TABLE 5-4: DC ELECTRICAL CHARACTERISTICS: ANALOG I/O PINS (DP/DM)**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| **FS FUNCTIONALITY** | | | | | | |
| **Input levels** | | | | | | |
| Differential Receiver Input Sensitivity | $V_{DIFS}$ | \| V(DP) - V(DM) \| | 0.2 | | | V |
| Differential Receiver Common-Mode Voltage | $V_{CMFS}$ | | 0.8 | | 2.5 | V |
| Single-Ended Receiver Low Level Input Voltage | $V_{ILSE}$ | | | | 0.8 | V |
| Single-Ended Receiver High Level Input Voltage | $V_{IHSE}$ | | 2.0 | | | V |
| Single-Ended Receiver Hysteresis | $V_{HYSSE}$ | | 0.050 | | 0.150 | V |
| **Output Levels** | | | | | | |
| Low Level Output Voltage | $V_{FSOL}$ | Pull-up resistor on DP; $R_L$ = 1.5kΩ to $V_{DD3.3}$ | | | 0.3 | V |
| High Level Output Voltage | $V_{FSOH}$ | Pull-down resistor on DP, DM; $R_L$ = 15kΩ to GND | 2.8 | | 3.6 | V |
| **Termination** | | | | | | |
| Driver Output Impedance for HS and FS | $Z_{HSDRV}$ | Steady state drive | 40.5 | 45 | 49.5 | Ù |
| Input Impedance | $Z_{INP}$ | TX, RPU disabled | 1.0 | | | MΩ |
| Pull-up Resistor Impedance | $Z_{PU}$ | Bus Idle | 0.900 | 1.24 | 1.575 | kΩ |
| Pull-up Resistor Impedance | $Z_{PURX}$ | Device Receiving | 1.425 | 2.26 | 3.09 | kΩ |
| Pull-dn Resistor Impedance | $Z_{PD}$ | | 14.25 | 15.0 | 15.75 | kΩ |
| **HS FUNCTIONALITY** | | | | | | |
| **Input levels** | | | | | | |
| HS Differential Input Sensitivity | $V_{DIHS}$ | \| V(DP) - V(DM) \| | 100 | | | mV |
| HS Data Signaling Common Mode Voltage Range | $V_{CMHS}$ | | -50 | | 500 | mV |
| HS Squelch Detection Threshold (Differential) | $V_{HSSQ}$ | Squelch Threshold | | | 100 | mV |
| | | Un-squelch Threshold | 150 | | | mV |
| **Output Levels** | | | | | | |
| Hi-Speed Low Level Output Voltage (DP/DM referenced to GND) | $V_{HSOL}$ | 45Ω load | -10 | | 10 | mV |
| Hi-Speed High Level Output Voltage (DP/DM referenced to GND) | $V_{HSOH}$ | 45Ω load | 360 | | 440 | mV |
| Hi-Speed IDLE Level Output Voltage (DP/DM referenced to GND) | $V_{OLHS}$ | 45Ω load | -10 | | 10 | mV |
| Chirp-J Output Voltage (Differential) | $V_{CHIRPJ}$ | HS termination resistor disabled, pull-up resistor connected. 45Ω load. | 700 | | 1100 | mV |
| Chirp-K Output Voltage (Differential) | $V_{CHIRPK}$ | HS termination resistor disabled, pull-up resistor connected. 45Ω load. | -900 | | -500 | mV |

**TABLE 5-4: DC ELECTRICAL CHARACTERISTICS: ANALOG I/O PINS (DP/DM) (CONTINUED)**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| **Leakage Current** | | | | | | |
| OFF-State Leakage Current | $I_{LZ}$ | | | | ±10 | uA |
| **Port Capacitance** | | | | | | |
| Transceiver Input Capacitance | $C_{IN}$ | Pin to GND | | 5 | 10 | pF |

**Note:** $V_{DD3.3}$ = 3.0 to 3.6V; $V_{SS}$ = 0V; $T_A$ = -40C to +85C; unless otherwise specified.

**TABLE 5-5: DYNAMIC CHARACTERISTICS: ANALOG I/O PINS (DP/DM)**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| **FS Output Driver Timing** | | | | | | |
| Rise Time | $T_{FSR}$ | $C_L$ = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$ | 4 | | 20 | ns |
| Fall Time | $T_{FFF}$ | $C_L$ = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$ | 4 | | 20 | ns |
| Output Signal Crossover Voltage | $V_{CRS}$ | Excluding the first transition from IDLE state | 1.3 | | 2.0 | V |
| Differential Rise/Fall Time Matching | FRFM | Excluding the first transition from IDLE state | 90 | | 111.1 | % |
| **HS Output Driver Timing** | | | | | | |
| Differential Rise Time | $T_{HSR}$ | | 500 | | | ps |
| Differential Fall Time | $T_{HSF}$ | | 500 | | | ps |
| Driver Waveform Requirements | | Eye pattern of Template 1 in USB 2.0 specification | | | | |
| **Hi-Speed Mode Timing** | | | | | | |
| Receiver Waveform Requirements | | Eye pattern of Template 4 in USB 2.0 specification | | | | |
| Data Source Jitter and Receiver Jitter Tolerance | | Eye pattern of Template 4 in USB 2.0 specification | | | | |

**Note:** $V_{DD3.3}$ = 3.0 to 3.6V; $V_{SS}$ = 0V; $T_A$ = -40C to +85C; unless otherwise specified.

**TABLE 5-6: OTG ELECTRICAL CHARACTERISTICS**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| SessEnd trip point | $V_{SessEnd}$ | | 0.2 | 0.5 | 0.8 | V |
| SessVld trip point | $V_{SessVld}$ | | 0.8 | 1.4 | 2.0 | V |
| VBUSVld trip point | $V_{VbusVld}$ | | 4.4 | 4.58 | 4.75 | V |
| Vbus Pull-Up | $R_{VbusPu}$ | Vbus to VDD3.3 (*ChargeVbus* = 1) | 281 | 340 | | Ù |
| Vbus Pull-down | $R_{VbusPd}$ | Vbus to GND (*DisChargeVbus* = 1) | 656 | 850 | | Ù |
| Vbus Impedance | $R_{Vbus}$ | Vbus to GND | 40 | 75 | 100 | kΩ |
| ID pull-up resistance | $R_{IdPullUp}$ | *IdPullup* = 1 | 80 | 100 | 120 | kΩ |
| ID pull-up resistance | $R_{Id}$ | *IdPullup* = 0 | 1 | | | MΩ |
| STP pull-up resistance | $R_{STP}$ | *InterfaceProtectDisable* = 0 | 240 | 330 | 600 | kΩ |

**Note:** $V_{DD3.3}$ = 3.0 to 3.6V; $V_{SS}$ = 0V; $T_A$ = -40C to +85C; unless otherwise specified.

**TABLE 5-7: REGULATOR OUTPUT VOLTAGES**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| $V_{DDA1.8}$ | $V_{DDA1.8}$ | Normal Operation (*SuspendM* = 1) | 1.6 | 1.8 | 2.0 | V |
| $V_{DDA1.8}$ | $V_{DDA1.8}$ | Low Power Mode (*SuspendM* = 0) | | 0 | | V |
| $V_{DD1.8}$ | $V_{DD1.8}$ | | 1.6 | 1.8 | 2.0 | V |

**Note:** $V_{DD3.3}$ = 3.0 to 3.6V; $V_{SS}$ = 0V; $T_A$ = -040C to +85C; unless otherwise specified.

## 5.1 Piezoelectric Resonator for Internal Oscillator

The internal oscillator may be used with an external quartz crystal or ceramic resonator as described in Section 6.3. See Table 5-8 for the recommended crystal specifications. See Table 5-9 for the ceramic resonator part number for commercial temperature applications. At this time, the ceramic resonator does not offer sufficient temperature stability to operate over the industrial temperature range.

**TABLE 5-8: USB3300 QUARTZ CRYSTAL SPECIFICATIONS**

| Parameter | Symbol | MIN | TYP | MAX | Units | Notes |
|---|---|---|---|---|---|---|
| Crystal Cut | AT, typ | | | | | |
| Crystal Oscillation Mode | Fundamental Mode | | | | | |
| Crystal Calibration Mode | Parallel Resonant Mode | | | | | |
| Frequency | $F_{fund}$ | - | 24 | - | MHz | |
| Total Allowable PPM Budget | | - | - | ±500 | PPM | Note 5-1 |
| Shunt Capacitance | $C_O$ | - | 7 typ | - | pF | |
| Load Capacitance | $C_L$ | - | 20 typ | - | pF | |
| Drive Level | $P_W$ | 0.5 | - | - | mW | |
| Equivalent Series Resistance | $R_1$ | - | - | 30 | Ohm | |
| Operating Temperature Range | | Note 5-2 | - | Note 5-3 | $^oC$ | |
| USB3300 **XI** Pin Capacitance | | - | 3 typ | - | pF | Note 5-4 |
| USB3300 **XO** Pin Capacitance | | - | 3 typ | - | pF | Note 5-4 |

**Note 5-1** The required bit rate accuracy for Hi-Speed USB applications is ±500 ppm as provided in the USB 2.0 Specification. This takes into account the effect of voltage, temperature, aging, etc.

**Note 5-2** $0^oC$ for commercial applications, $-40^oC$ for industrial applications.

**Note 5-3** $+70^oC$ for commercial applications, $+85^oC$ for industrial applications.

**Note 5-4** This number includes the pad, the bond wire and the lead frame. Printed Circuit Board (PCB) capacitance is not included in this value. The PCB capacitance value and the capacitance value of the **XO** and **XI** pins are required to accurately calculate the value of the two external load capacitors.

**TABLE 5-9: USB3300 CERAMIC RESONATOR PART NUMBER**

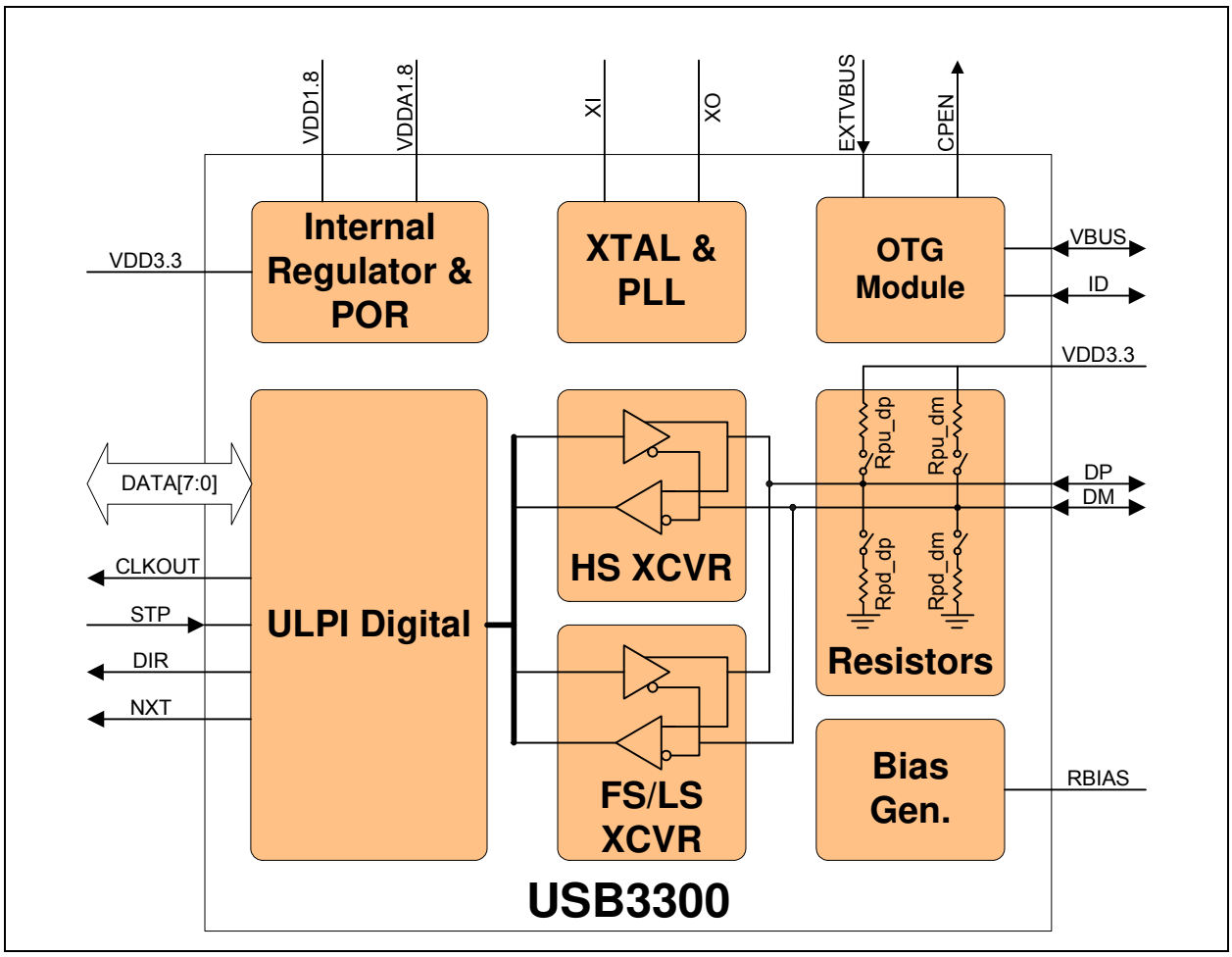
| Frequency | Murata Part Number | Notes |
|---|---|---|
| 24 MHz | CSTCE24M0XK1***-R0 | Commercial Temp Only, Note 5-5 |

**Note 5-5** This is a generic part number assigned by Murata. The oscillating frequency is affected by stray capacitance on the Printed Circuit Board (PCB). Murata will assign the final part number for each customer's PCB after characterizing the customer's PCB design.

## 6.0 ARCHITECTURE OVERVIEW

The USB3300 architecture can be broken down into the following blocks shown in Figure 6-1, "Simplified USB3300 Architecture" below.

**FIGURE 6-1: SIMPLIFIED USB3300 ARCHITECTURE**




### 6.1 ULPI Digital

The USB3300 uses the industry standard ULPI digital interface to facilitate communication between the PHY and Link (device controller). The ULPI interface is designed to reduce the number of pins required to connect a discrete USB PHY to an ASIC or digital controller. For example, a full UTMI+ Level 3 OTG interface requires 54 signals while a ULPI interface requires only 12 signals.

**The ULPI interface is documented completely in the "UTMI+ Low Pin Interface (ULPI) Specification" document (www.ulpi.org).** The following sections highlight the key operating modes of the USB3300 digital interface.

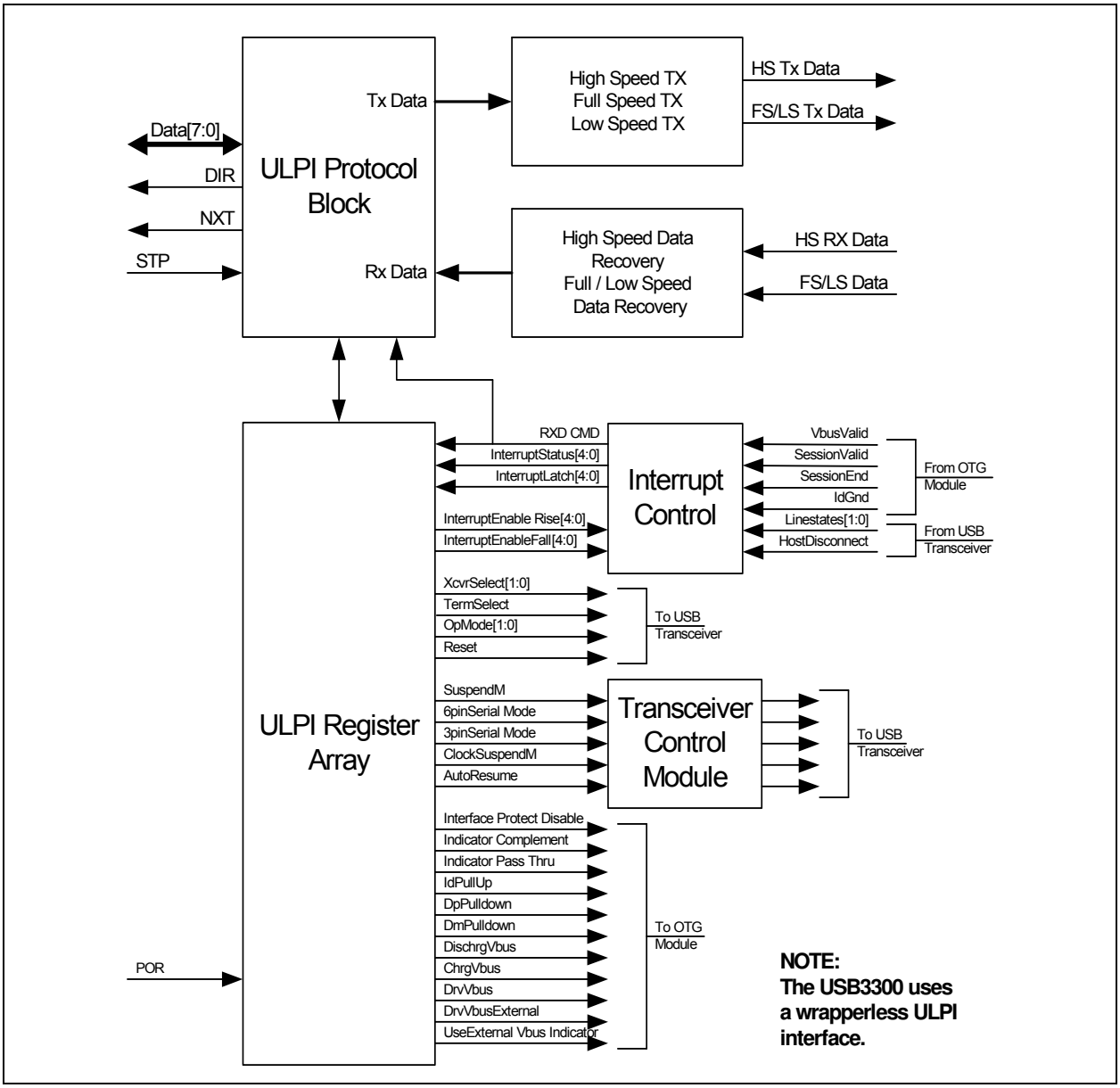
#### 6.1.1 OVERVIEW

Figure 6-2 illustrates the block diagram of the ULPI digital functions. It should be noted that this PHY does not use a "ULPI wrapper" around a UTMI+ PHY core as the ULPI specification implies.

The advantage of a "wrapper less" architecture is that the PHY has a lower USB latency than a design which must first register signals into the PHY's wrapper before the transfer to the PHY core. A low latency PHY allows a Link to use a wrapper around a UTMI Link and still make the required USB turn-around timing given in the USB 2.0 specification.

RxEndDelay maximum allowed by the UTMI+/ULPI for 8-bit data is 63 high speed clocks. USB3300 uses a low latency high speed receiver path to lower the RxEndDelay to 43 high speed clocks. This low latency design gives the Link more cycles to make decisions and reduces the Link complexity. This is the result of the “wrapper less” architecture of the USB3300. This low RxEndDelay should allow legacy UTMI Links to use a “wrapper” to convert the UTMI+ interface to a ULPI interface.

**FIGURE 6-2: ULPI DIGITAL BLOCK DIAGRAM**




In Figure 6-2, "ULPI Digital Block Diagram", a single ULPI Protocol Block decodes the ULPI 8-bit bi-directional bus when the Link addresses the PHY. The Link must use the DIR output to determine direction of the ULPI data bus. The USB3300 is the “bus arbitrator”. The ULPI Protocol Block will route data/commands to the transmitter or the ULPI register array.

### 6.1.2 ULPI INTERFACE SIGNALS

UTMI+ Low Pin Interface (ULPI) uses 12-pins to connect a full OTG Host / Device PHY to an SOC. A reduction of external pins on the PHY is accomplished by realizing that many of the relatively static configuration pins (xcvrselect[1:0], termselect, opmode[1:0], and DpPullDown DmPulldown to list a few,) can be implemented by having a internal static register array.

An 8-bit bi-directional data bus clocked at 60Mhz allows the Link to access this internal register array and transfer USB packets to and from the PHY. The remaining 3 pins function to control the data flow and arbitrate the data bus.

Direction of the 8-bit data bus is control by the DIR output from the PHY. Another output NXT is used to control data flow into and out of the device. Finally, STP, which is in input to the PHY, terminates transfers and is used to start up and resume from a suspend state.

The 12 signals are described below in Table 6-1, "ULPI Interface Signals".

**TABLE 6-1: ULPI INTERFACE SIGNALS**

| Signal | Direction | Description |
|---|---|---|
| CLKOUT | OUT | 60MHz reference clock output. All ULPI signals are driven synchronous to the rising edge of this clock. |
| DATA[7:0] | I/O | 8-bit bi-directional data bus. Bus ownership is determined by DIR. The Link and PHY initiate data transfers by driving a non-zero pattern onto the data bus. ULPI defines interface timing for a single-edge data transfers with respect to rising edge of CLKOUT. |
| DIR | OUT | Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives DIR high to take ownership of the bus. When the PHY has no data to transfer it drives DIR low and monitors the bus for commands from the Link. The PHY will pull DIR high whenever the interface cannot accept data from the Link, such as during PLL start-up. |
| STP | IN | The Link asserts STP for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, STP indicates the last byte of data was on the bus in the previous cycle. |
| NXT | OUT | The PHY asserts NXT to throttle the data. When the Link is sending data to the PHY, NXT indicates when the current byte has been accepted by the PHY. The Link places the next byte on the data bus in the following clock cycle. |

USB3300 implements a Single Data Rate (SDR) ULPI interface with all data transfers happening on the rising edge of the CLKOUT. CLKOUT is supplied by the PHY.

The ULPI interface supports the two basic modes of operation, Synchronous Mode and Low Power Mode. Synchronous Mode with the signals all changing relative to the 60MHz clockout. Low Power Mode where the clock is off in a suspended state and the lower two bits of the data bus contain the linestate[1:0] signals. ULPI adds to Low Power Mode, an interrupt output which permits the Link to receive an asynchronous interrupt when the OTG comparators, or ID pin change state.

In Synchronous Mode operation, data is transferred on the rising edge of CLKOUT. Direction of the data bus is determined by the state of DIR. When DIR is high, the PHY is driving DATA[7:0]. When DIR is low, the Link is driving DATA[7:0].

Each time DIR changes, a “turn-around” cycle occurs where neither the Link nor PHY drive the data bus for one clock cycle. During the “turn–around“ cycle, the state of DATA[7:0] is unknown and the PHY will not read the data bus.

Because USB uses a bit-stuffing encoding, some means of allowing the PHY to throttle the USB transmit data is needed. The ULPI signal NXT is used to request the next byte to be placed on the databus by the Link layer.

### 6.1.3 ULPI INTERFACE TIMING

The control and data timing relationships are given in Figure 6-3, "ULPI Timing Diagram" and Table 6-2, "ULPI Interface Timing". The USB300 PHY provides CLKOUT and all timing is relative to the rising clock edge. The timing relationships detailed below apply to Synchronous Mode only.

**FIGURE 6-3: ULPI TIMING DIAGRAM**

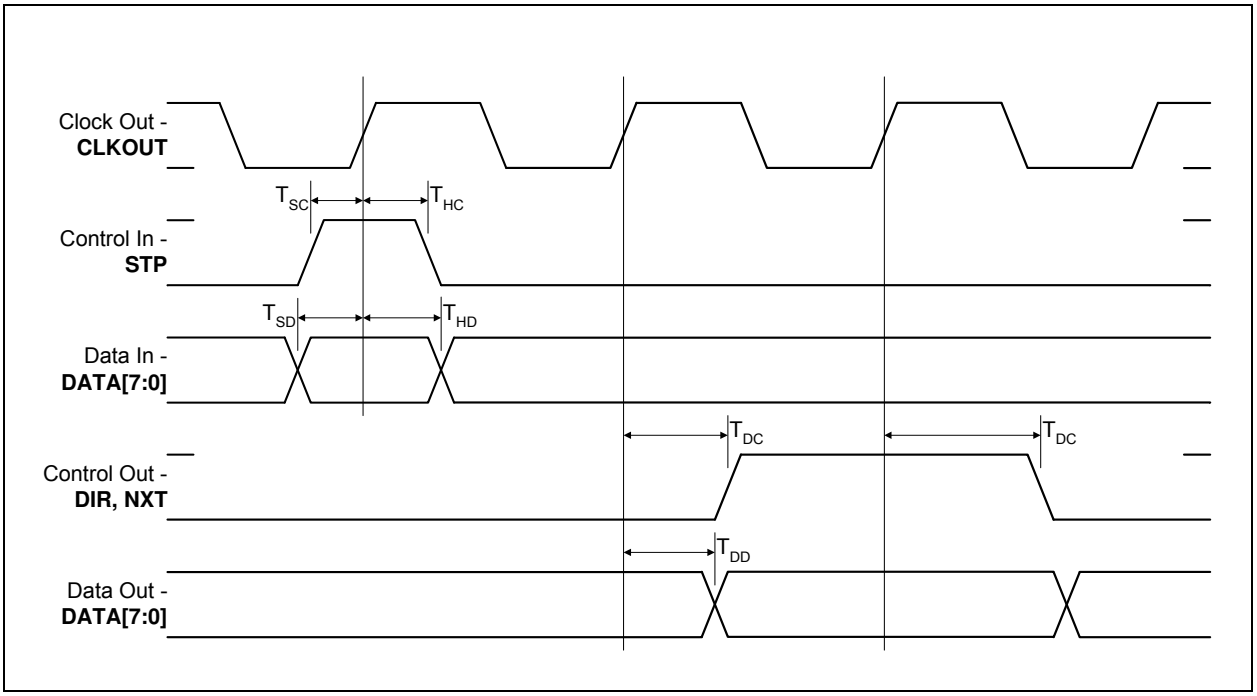



**TABLE 6-2: ULPI INTERFACE TIMING**

| Parameter | Symbol | MIN | MAX | Units |
|---|---|---|---|---|
| Setup time (control in, 8-bit data in) | $T_{SC}$,$T_{SD}$ | 5.0 | | ns |
| Hold time (control in, 8-bit data in) | $T_{HC}$, $T_{HD}$ | 0 | | ns |
| Output delay (control out, 8-bit data out) | $T_{DC}$, $T_{DD}$ | 2.0 | 5.0 | ns |

**Note:** $V_{DD3.3}$ = 3.0 to 3.6V; $V_{SS}$ = 0V; $T_A$ = -40C to 85C; unless otherwise specified.

### 6.1.4 ULPI REGISTER ARRAY

The USB3300 PHY implements all of the ULPI registers detailed in the ULPI revision 1.1 specification. The complete USB3300 ULPI register set is shown in Table 6-3, "ULPI Register Map". All registers are 8 bits. This table also includes the default states of the register upon POR. The RESET bit in the Function Control Register does not reset the bits of the ULPI register array. The Link should not read or write to any registers not listed in this table.

**TABLE 6-3: ULPI REGISTER MAP**

| Register Name | Default State | Address (6bit) | | | |
|---|---|---|---|---|---|
| | | Read | Write | Set | Clear |
| Vendor ID Low | 24h | 00h | - | - | - |
| Vendor ID High | 04h | 01h | - | - | - |
| Product ID Low | 04h | 02h | - | - | - |
| Product ID High | 00h | 03h | - | - | - |
| Function Control | 41h | 04-06h | 04h | 05h | 06h |
| Interface Control | 00h | 07-09h | 07h | 08h | 09h |
| OTG Control | 06h | 0A-0Ch | 0Ah | 0Bh | 0Ch |
| USB Interrupt Enable Rising | 1Fh | 0D-0Fh | 0Dh | 0Eh | 0Fh |
| USB Interrupt Enable Falling | 1Fh | 10-12h | 10h | 11h | 12h |
| USB Interrupt Status | 00h | 13h | - | - | - |
| USB Interrupt Latch | 00h | 14h | - | - | - |
| Debug | 00h | 15h | - | - | - |
| Scratch Register | 00h | 16-18h | 16h | 17h | 18h |

#### 6.1.4.1 Vendor ID Low: Address = 00h (read only)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| Vendor ID Low | 7:0 | 24h | Microchip Vendor ID |

#### 6.1.4.2 Vendor ID High: Address = 01h (read only)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| Vendor ID High | 7:0 | 04h | Microchip Vendor ID |

#### 6.1.4.3 Product ID Low: Address = 02h (read only)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| Product ID Low | 7:0 | 04h | Microchip Product ID revision A0 |

#### 6.1.4.4 Vendor ID Low: Address = 03h (read only)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| Product ID High | 7:0 | 00h | Microchip Product ID revision A0 |

#### 6.1.4.5 Function Control: Address = 04-06h (read), 04h (write), 05h (set), 06h (clear)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| XcvrSelect[1:0] | 1:0 | 01b | Selects the required transceiver speed.<br>00b: Enables HS transceiver<br>01b: Enables FS transceiver<br>10b: Enables LS transceiver<br>11b: Enables FS transceiver for LS packets (FS preamble automatically pre-pended) |
| TermSelect | 2 | 0b | Controls the DP and DM termination depending on XcvrSelect, OpMode, DpPulldown, and DmPulldown. The Dp and DM termination is detailed in Table 6-8, "DP/DM Termination vs. Signaling Mode". |
| OpMode | 4:3 | 00b | Selects the required bit encoding style during transmit.<br>00b: Normal Operation<br>01b: Non-Driving<br>10b: Disable bit-stuff and NRZI encoding<br>11b: Reserved |
| Reset | 5 | 0b | Active high transceiver reset. This reset does not reset the ULPI interface or register set. Automatically clears after reset is complete. |
| SuspendM | 6 | 1b | Active low PHY suspend. When cleared the PHY will enter Low Power Mode as detailed in Section 6.1.9, "Low Power Mode". Automatically set when exiting Low Power Mode. |
| Reserved | 7 | 0b | Driven low. |

#### 6.1.4.6 Interface Control: Address = 07-09h (read), 07h (write), 08h (set), 09h (clear)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| 6-pin FsLsSerialMode | 0 | 0b | Changes the ULPI interface to a 6-pin Serial Mode. The PHY will automatically clear this bit when exiting serial mode. |
| 3-pin FsLsSerialMode | 1 | 0b | Changes the ULPI interface to a 3-pin Serial Mode. The PHY will automatically clear this bit when exiting serial mode. |
| Reserved | 2 | 0b | Driven low. |
| ClockSuspendM | 3 | 0b | Enables Link to turn on 60MHz CLKOUT in serial mode.<br>0b: Disable clock in serial mode.<br>1b: Enable clock in serial mode. |
| AutoResume | 4 | 0b | Only applicable in Host mode. Enables the PHY to automatically transmit resume signaling. This function is detailed in Section 6.1.7.4, "Host Resume K". |
| IndicatorComplement | 5 | 0b | Inverts the EXTVBUS signal. This function is detailed in Section 6.5.4, "External Vbus Indicator". |
| IndicatorPassThru | 6 | 0b | Disables anding the internal VBUS comparator with the EXTVBUS input when asserted. This function is detailed in Section 6.5.4. |
| InterfaceProtectDisable | 7 | 0b | Used to disable the integrated STP pull-up resistor used for interface protection. This function is detailed in Section 6.1.9.3, "Interface Protection". |

### 6.1.4.7 OTG Control: Address = 0A-0Ch (read), 0Ah (write), 0Bh (set), 0Ch (clear)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| IdPullup | 0 | 0b | Connects a pull-up resistor from the ID pin to VDD3.3<br>0b: Disables the pull-up resistor<br>1b: Enables the pull-up resistor |
| DpPulldown | 1 | 1b | Enables the 15k Ohm pull-down resistor on DP.<br>0b: Pull-down resistor not connected to DP<br>1b: Pull-down resistor connected to DP |
| DmPulldown | 2 | 1b | Enables the 15k Ohm pull-down resistor on DM.<br>0b: Pull-down resistor not connected to DM<br>1b: Pull-down resistor connected to DM |
| DischrgVbus | 3 | 0b | This bit is only used during SRP. Connects a resistor from VBUS to ground to discharge VBUS.<br>0b: disconnect resistor from VBUS to ground<br>1b: connect resistor from VBUS to ground |
| ChrgVbus | 4 | 0b | This bit is only used during SRP. Connects a resistor from VBUS to VDD3.3 to charge VBUS above the SessValid threshold.<br>0b: disconnect resistor from VBUS to VDD3.3<br>1b: connect resistor from VBUS to VDD3.3 |
| DrvVbus | 5 | 0b | Used to enable external 5 volt supply to drive 5 volts on VBUS. This signal is or'ed with DrvVbusExternal.<br>0b: do not drive VBUS<br>1b: drive VBUS |
| DrvVbusExternal | 6 | 0b | Used to enable external 5 volt supply to drive 5 volts on VBUS. This signal is or'ed with DrvVbus.<br>0b: do not drive VBUS<br>1b: drive VBUS |
| UseExternalVbus Indicator | 7 | 0b | Tells the PHY to use an external VBUS over-current or voltage indicator. This function is detailed in Section 6.5.4, "External Vbus Indicator".<br>0b: Use the internal VbusValid comparator<br>1b: Use the EXTVBUS input as for VbusValid signal. |

### 6.1.4.8 USB Interrupt Enable Rising: Address = 0D-0Fh (read), 0Dh (write), 0Eh (set), 0Fh (clear)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| HostDisconnect Rise | 0 | 1b | Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode. |
| VbusValid Rise | 1 | 1b | Generate an interrupt event notification when Vbusvalid changes from low to high. |
| SessValid Rise | 2 | 1b | Generate an interrupt event notification when SessValid changes from low to high. |
| SessEnd Rise | 3 | 1b | Generate an interrupt event notification when SessEnd changes from low to high. |
| IdGnd Rise | 4 | 1b | Generate an interrupt event notification when IdGnd changes from low to high. |
| Reserved | 7:5 | 0h | Driven low. |

#### 6.1.4.9 USB Interrupt Enable Falling: Address = 10-12h (read), 10h (write), 11h (set), 12h (clear)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| HostDisconnect Fall | 0 | 1b | Generate an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode. |
| VbusValid Fall | 1 | 1b | Generate an interrupt event notification when Vbusvalid changes from high to low. |
| SessValid Fall | 2 | 1b | Generate an interrupt event notification when SessValid changes from high to low. |
| SessEnd Fall | 3 | 1b | Generate an interrupt event notification when SessEnd changes from high to low. |
| IdGnd Fall | 4 | 1b | Generate an interrupt event notification when IdGnd changes from high to low. |
| Reserved | 7:5 | 0h | Driven low. |

#### 6.1.4.10 USB Interrupt Status Register: Address = 13h (read only with auto clear)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| HostDisconnect | 0 | 0b | Current value of the UTMI+ Hostdisconnect output. Applicable only in host mode. |
| VbusValid | 1 | 0b | Current value of the UTMI+ Vbusvalid output. |
| SessValid | 2 | 0b | Current value of the UTMI+ SessValid output. |
| SessEnd | 3 | 0b | Current value of the UTMI+ SessEnd output. |
| IdGnd | 4 | 0b | Current value of the UTMI+ IdGnd output. |
| Reserved | 7:5 | 0h | Driven low. |

#### 6.1.4.11 USB Interrupt Status: Address = 14h (read only with auto clear)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| HostDisconnect Latch | 0 | 0b | Set to 1b by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode. |
| VbusValid Latch | 1 | 0b | Set to 1b by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read. |
| SessValid Latch | 2 | 0b | Set to 1b by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read. |
| SessEnd Latch | 3 | 0b | Set to 1b by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read. |
| IdGnd Latch | 4 | 0b | Set to 1b by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read. |
| Reserved | 7:5 | 0h | Driven low. |

#### 6.1.4.12 Debug Register: Address = 15h (read only)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| Linestate0 | 0 | 0b | Contains the current value of Linestate[0]. |
| Linestate1 | 1 | 0b | Contains the current value of Linestate[1]. |
| Reserved | 7:2 | 000000b | Driven low. |

#### 6.1.4.13 Scratch Register: Address = 16-18h (read), 16h (write), 17h (set), 18h (clear)

| Field Name | Bit | Default | Description |
|---|---|---|---|
| Scratch | 7:0 | 00h | Empty register byte for testing purposes. Software can read, write, set, and clear this register and the PHY functionality will not be affected. |

#### 6.1.4.14 Carkit Register Access

The Carkit registers are reserved for Microchip testing and should not be written to or read by the Link.

#### 6.1.4.15 Extended Register Access

The extended registers are reserved for Microchip testing and should not be written to or read by the Link.

#### 6.1.4.16 Vendor Register Access

The vendor specific registers are reserved for Microchip testing and should not be written to or read by the Link. The vendor specific registers include the range from 30h to 3Fh.

### 6.1.5 ULPI REGISTER ACCESS

A command from the Link begins a ULPI transfer from the Link to the USB3300. Anytime the Link wants to write or read a ULPI register, the Link will need to wait until DIR is low, and then send a Transmit Command Byte (TXD CMD) to the PHY. The TXD CMD byte informs the PHY of the type of data being sent. The TXD CMD is followed by the a data transfer to or from the PHY. Table 6-4, "ULPI TXD CMD Byte Encoding" gives the TXD command byte (TXD CMD) encoding for the USB3300. The upper two bits of the TX CMD instruct the PHY as to what type of packet the Link is transmitting.

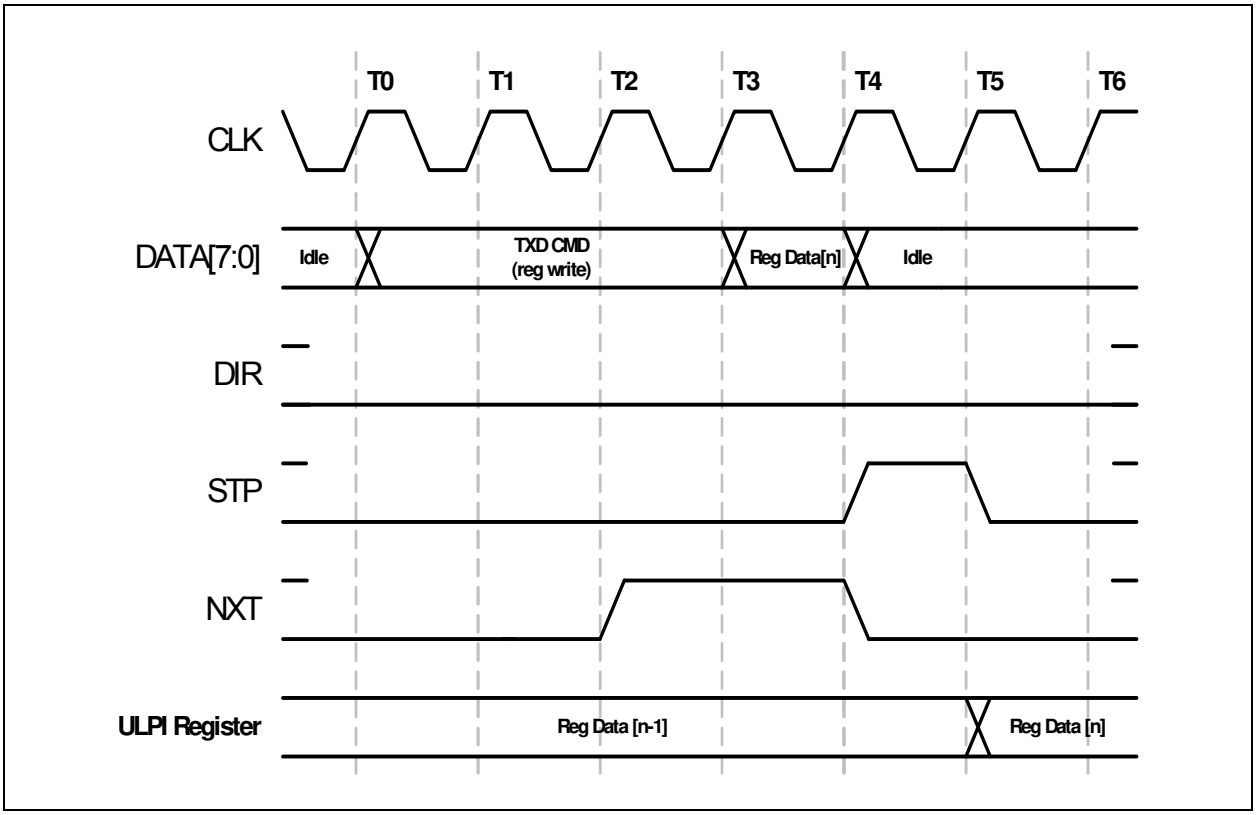
**TABLE 6-4: ULPI TXD CMD BYTE ENCODING**

| Command Name | CMD Bits[7:6] | CMD Bits[5:0] | Command Description |
|---|---|---|---|
| Idle | 00b | 000000b | ULPI Idle |
| Transmit | 01b | 000000b | USB Transmit Packet with No Packet Identifier (NOPID) |
| | | 00XXXXb | USB Transmit Packet Identifier (PID) where DATA[3:0] is equal to the 4-bit PID. $P_3P_2P_1P_0$ where $P_3$ is the MSB. |
| Register Write | 10b | XXXXXXb | Immediate Register Write Command where DATA[5:0] = 6-bit register address |
| Register Read | 11b | XXXXXXb | Immediate Register Read Command where DATA[5:0] = 6-bit register address |

#### 6.1.5.1 ULPI Register Write

A ULPI register write operation is given in Figure 6-4. The TXD command with a register write DATA[7:6] = 10b is driven by the Link at T0. The register address is encoded into DATA[5:0] of the TXD CMD byte.

**FIGURE 6-4: ULPI REGISTER WRITE**




To write to a register, the Link will wait until DIR is low, and at T0, drive the TXD CMD on the databus. At T2 the PHY will drive NXT high. On the next rising clock edge, T3, the Link will write the register data. At T4 the PHY will accept the register data and the Link will drive an Idle on the bus and drive STP high to signal the end of the data packet. Finally, at T5, the PHY will latch the data into the register and drive NXT low. The Link will pull STP low.

NXT is used to control when the Link drives the register data on the bus. DIR is low throughout this transaction since the PHY is receiving data from the Link. STP is used to end the transaction and data is registered after the de-assertion of STP. After the write operation completes, the Link must drive a ULPI Idle (00h) on the data bus or the USB3300 may decode the bus value as a ULPI command.