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USB3318

Hi-Speed USB Transceiver with 1.8V-3.3V ULPI Interface - 13MHz Reference Clock

PRODUCT FEATURES

Datasheet

- USB-IF “Hi-Speed” compliant to the Universal Serial Bus Specification Rev 2.0
- Interface compliant with the ULPI Specification revision 1.1 as a Single Data Rate (SDR) PHY
- 1.8V to 3.3V IO Voltage (±10%)
- flexPWR® Technology
  - Low current design ideal for battery powered applications
  - “Sleep” mode tri-states all ULPI pins and places the part in a low current state
- Supports FS pre-amble for FS hubs with a LS device attached (UTMI+ Level 3)
- Supports HS SOF and LS keep-alive pulse
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 2.0 specification
- Supports the OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Allows host to turn VBUS off to conserve battery power in OTG applications
- Support OTG monitoring of VBUS levels with internal comparators
- “Wrapper-less” design for optimal timing performance and design ease
  - Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max) allows use of legacy UTMI Links with a ULPI bridge
- Internal 5V cable short-circuit protection of ID, DP and DM lines to VBUS or ground
- 13MHz Reference Clock Operation
  - 0 to 3.6V input drive tolerant
  - Able to accept “noisy” clock sources
- Internal low jitter PLL for 480MHz Hi-Speed USB operation
- Internal detection of the value of resistance to ground on the ID pin
- Integrated battery to 3.3V LDO regulator
  - 2.2uF bypass capacitor
  - 100mV dropout voltage
- Integrated ESD protection circuits
  - Up to ±15kV without any external devices
- Carkit UART mode for non-USB serial data transfers
- Industrial Operating Temperature -40°C to +85°C
- Packaging Options
  - 24 pin QFN lead-free RoHS compliant package (4 x 4 x 0.90 mm height)

Applications

The USB3318 is targeted for any application where a Hi-Speed USB connection is desired and when board space, power, and interface pins must be minimized.

The USB3318 is well suited for:

- Cell Phones
- PDAs
- MP3 Players
- GPS Personal Navigation
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Entertainment Devices
- Printers
- Set Top Boxes
- Video Record/Playback Systems
- IP and Video Phones
- Gaming Consoles
- POS Terminals

Order Number(s):

USB3318C-CP-TR FOR 24 PIN, QFN LEAD-FREE ROHS COMPLIANT PACKAGE (TAPE AND REEL)

REEL SIZE IS 4000 PIECES.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

0.1 Reference Documents

- Universal Serial Bus Specification, Revision 2.0, April 27, 2000
- On-The-Go Supplement to the USB 2.0 Specification, Revision 2.0, May 8, 2009
- 27% Resistor ECN
- USB 2.0 Transceiver Macrocell Interface (UTMI) Specification, Version 1.02, May 27, 2000
- UTMI+ Specification, Revision 1.0, February 2, 2004
- UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1, October 20, 2004
- Technical Requirements and Test Methods of Charger and Interface for Mobile Telecommunication Terminal Equipment (Chinese Charger Specification Approval Draft 11/29/2006)

Table of Contents

List of Figures

List of Tables

Chapter 1 General Description

The USB3318 is a highly integrated Hi-Speed USB 2.0 Transceiver (PHY) that supports systems architectures based on a 13MHz reference clock. It is designed to be used in both commercial and industrial temperature applications.

The USB3318 meets all of the electrical requirements to be used as a Hi-Speed USB Host, Device, or an On-the-Go (OTG) device. In addition to the supporting USB signaling the USB3318 also provides USB UART mode

USB3318 uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB PHY to the Link. The industry standard ULPI interface uses a method of in-band signaling and status byte transfers between the Link and PHY, to facilitate a USB session. By using in-band signaling and status byte transfers the ULPI interface requires only 12 pins.

The USB3318 uses SMSC's "wrapper-less" technology to implement the ULPI interface. This "wrapper-less" technology allows the PHY to achieve a low latency transmit and receive time. SMSC's low latency transceiver allows an existing UTMI Link to be reused by adding a UTMI to ULPI bridge. By adding a bridge to the ASIC the existing and proven UTMI Link IP can be reused.

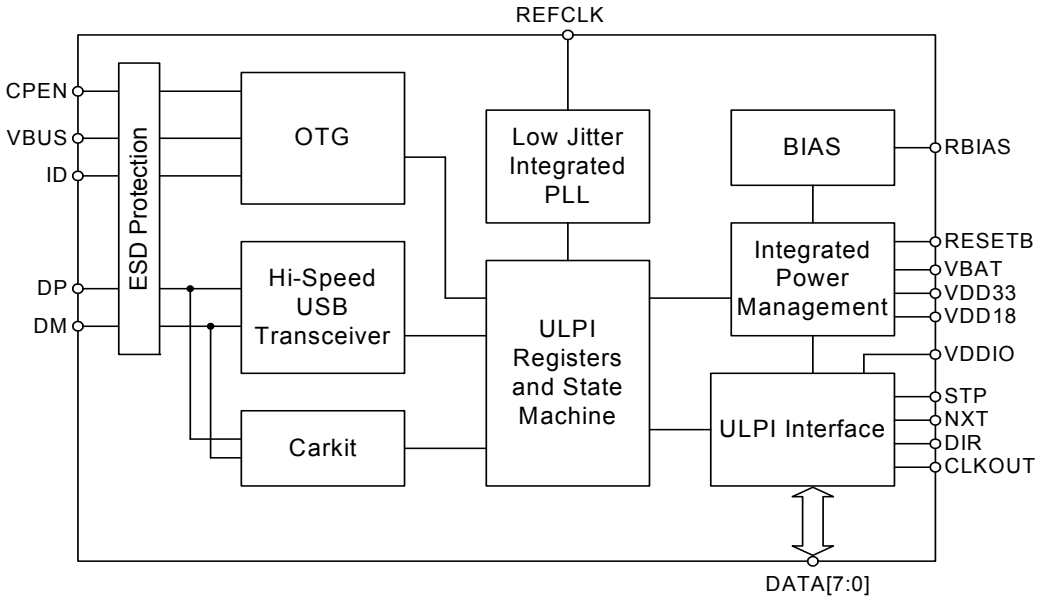

Figure 1.1 USB3318 Block Diagram

The USB3318 is designed to run with a 13MHz reference clock. By using a reference clock from the Link the USB3318 is able to remove the cost of a crystal reference from the design.

The USB3318 includes a integrated 3.3V LDO regulator to generate its own supply from power applied at the **VBAT** pin. The voltage on the **VBAT** pin can range from 3.1 to 5.5V. The regulator dropout voltage is less than 100mV which allows the PHY to continue USB signaling when the voltage on **VBAT** drops to 3.1V. The USB transceiver will continue to operate at lower voltages, although some parameters may be outside the limits of the USB specifications. If the user would like to provide a 3.3V supply to the USB3318, the **VBAT** and **VDD33** pins should be connected together as described in Section 5.5.1.

The USB3318 also includes integrated pull-up resistors that can be used for detecting the attachment of a USB Charger. By sensing the attachment to a USB Charger, a product using the USB3318 can charge its battery at more than the 500mA allowed when charging from a USB Host as described in Section 8.2.

Chapter 2 USB3318 Pin Locations and Definitions

2.1 USB3318 Pin Locations and Descriptions

2.1.1 Package Diagram with Pin Locations

The pinout below is viewed from the top of the package.

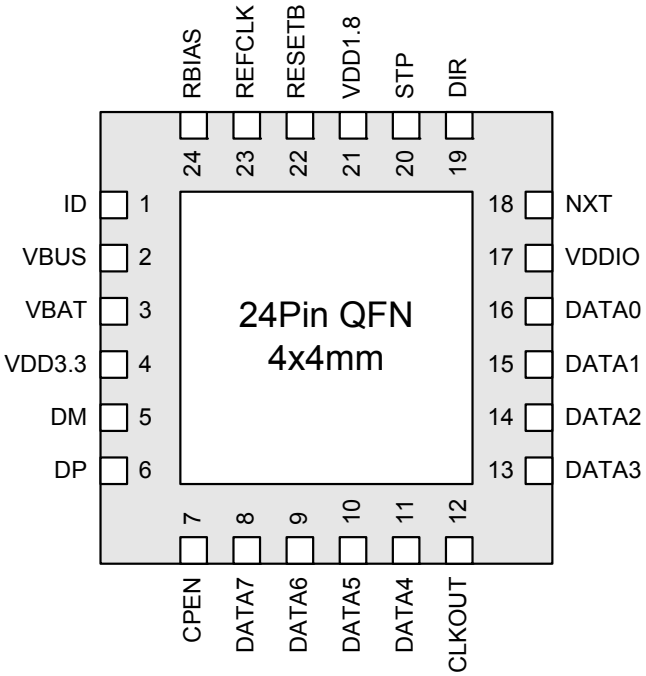

Figure 2.1 USB3318 QFN Pinout - Top View

2.1.2 Pin Definitions

The following table details the pin definitions for the figure above.

Table 2.1 USB3318 Pin Description

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
1	**ID**	Input, Analog	N/A	**ID** pin of the USB cable. For non-OTG applications this pin can be floated. For an A-Device **ID** is grounded. For a B-Device **ID** is floated.
2	**VBUS**	I/O, Analog	N/A	**VBUS** pin of the USB cable. This pin is used for the Vbus comparator inputs and for Vbus pulsing during session request protocol.
3	**VBAT**	Power	N/A	Regulator input. The regulator supply can be from 5.5V to 3.1V.

Table 2.1 USB3318 Pin Description (continued)

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
4	**VDD3.3**	Power	N/A	3.3V Regulator Output. A 2.2uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3318.
5	**DM**	I/O, Analog	N/A	D- pin of the USB cable.
6	**DP**	I/O, Analog	N/A	D+ pin of the USB cable.
7	**CPEN**	Output, CMOS	High	External 5 volt supply enable. This pin is used to enable the external Vbus power supply. The **CPEN** pin is low on POR. This pad uses VDD3.3 logic level.
8	**DATA[7]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[7]** is the MSB.
9	**DATA[6]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
10	**DATA[5**	I/O, CMOS	N/A	ULPI bi-directional data bus.
11	**DATA[4]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
12	**CLKOUT**	Output, CMOS	N/A	60MHz reference clock output. All ULPI signals are driven synchronous to the rising edge of this clock. Following POR or hardware reset, the voltage at **CLKOUT** must not exceed V_{IH_ED} as provided in Table 4.4.
13	**DATA[3]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
14	**DATA[2]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
15	**DATA[1]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
16	**DATA[0]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[0]** is the LSB.
17	**VDDIO**	Power	N/A	1.8V to 3.3V ULPI interface supply voltage. This voltage sets the value of V_{OH} for the ULPI interface.
18	**NXT**	Output, CMOS	High	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY. The Link places the next byte on the data bus in the following clock cycle.

Table 2.1 USB3318 Pin Description (continued)

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
19	**DIR**	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.
20	**STP**	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
21	**VDD1.8**	Power	N/A	External 1.8V Supply input pin. This pad needs to be bypassed with a 0.1uF capacitor to ground, placed as close as possible to the USB3318.
22	**RESETB**	Input, CMOS,	N/A	When low, the part is suspended with all of the I/O tri-stated. When high the USB3318 will operate as a normal ULPI device.
23	**REFCLK**	Input, CMOS	N/A	13MHz Reference Clock input.
24	**RBIAS**	Analog, CMOS	N/A	Rbias pin. This pin requires an 8.06kΩ (±1%) resistor to ground, placed as close as possible to the USB3318.
FLAG	**GND**	Ground	N/A	Ground. QFN only: The flag should be connected to the ground plane with a via array under the exposed flag. This is the main ground for the IC.

Chapter 3 Limiting Values

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum **VBUS**, **VBAT**, **ID**, **DP**, **DM**, and **CPEN** voltage to **GND**	V_{MAX_5V}		-0.5		+6.0	V
Maximum **VDD18** voltage to Ground	$V_{MAX\_1.8V}$		-0.5		2.5	V
Maximum **VDDIO** voltage to Ground	V_{MAX_IOV}	**VDD18** = V_{DD18}	-0.5		4.0	V
Maximum **VDDIO** voltage to Ground	V_{MAX_IOV}	**VDD18** = 0V	-0.5		0.7	V
Maximum **VDD33** voltage to Ground	$V_{MAX\_3.3V}$		-0.5		4.0	V
Maximum I/O voltage to Ground	V_{MAX_IN}		-0.5		V_{DDIO} + 0.7	V
QFN Package Junction to Ambient (θ_{JA})		Thermal vias per Layout Guidelines.		58		°C/W
QFN Package Junction to Case (θ_{JC})				11		°C/W
Operating Temperature	T_{MAX_OP}		-40		85	C
Storage Temperature	T_{MAX_STG}		-55		150	C

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

Table 3.2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBAT to **GND**	V_{VBAT}		3.1		5.5	V
VDD33 to **GND**	V_{DD33}		3.0	3.3	3.6	V
VDDIO to **GND**	V_{DDIO}	**VDDIO** ≥ **VDD18**(min)	1.6	1.8-3.3	3.6	V
VDD18 to **GND**	V_{DD18}		1.6	1.8	2.0	V
Input Voltage on Digital Pins (**RESETB**, **STP**, **DIR**, **NXT**, **DATA[7:0]**)	V_I		0.0		V_{DDIO}	V
Voltage on Analog I/O Pins (**DP**, **DM**, **ID**, **CPEN**) **CPEN**,	$V_{I(I/O)}$		0.0		V_{DD33}	V
VBUS to **GND**	V_{VMAX}		0.0		5.5	V
Ambient Temperature	T_A		-40		85	C

Chapter 4 Electrical Characteristics

The following conditions are assumed unless otherwise specified:

V_{VBAT} = 3.1 to 5.5V; V_{DD18} = 1.6 to 2.0V; V_{DDIO} = 1.6 to 2.0V; V_{SS} = 0V; T_A = -40C to +85C

The current for 3.3V circuits is sourced at the VBAT pin, except when using an external 3.3V supply as shown in Figure 5.4.

4.1 Operating Current

Table 4.1 Electrical Characteristics: Operating Current

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Synchronous Mode Current (Default Configuration)	$I_{33AVG(SYNC)}$	Start-up sequence defined in Section 5.5.4 has completed.	5.0	5.5	8.0	mA
	$I_{18AVG(SYNC)}$		17.5	22.0	27.0	mA
	$I_{IOAVG(SYNC)}$		2.5	3.0	4.0	mA
Synchronous Mode Current (HS USB operation)	$I_{33AVG(HS)}$	Active USB Transfer	7.0	10.0	14.0	mA
	$I_{18AVG(HS)}$		23.0	28.0	34.0	mA
	$I_{IOAVG(HS)}$		2.5	3.0	4.0	mA
Synchronous Mode Current (FS/LS USB operation)	$I_{33AVG(FS)}$	Active USB Transfer	5.0	8.5	13.0	mA
	$I_{18AVG(FS)}$		19.0	22.0	27.0	mA
	$I_{IOAVG(FS)}$		2.5	3.0	4.0	mA
Serial Mode Current (FS/LS USB) Note 4.1	$I_{33AVG(FS\_S)}$		5.0	5.5	7.0	mA
	$I_{18AVG(FS\_S)}$		1.5	2.2	3.5	mA
	$I_{IOAVG(FS\_S)}$				0.1	mA
USB UART Current Note 4.1	$I_{33AVG(UART)}$		5.0	5.5	7.0	mA
	$I_{18AVG(UART)}$		1.4	2.1	3.5	mA
	$I_{IOAVG(UART)}$				0.1	mA
Low Power Mode Note 4.2	$I_{DD33(LPM)}$	V_{VBAT} = 4.2V V_{DD18} = 1.8V V_{DDIO} = 1.8V	14.0	20.0	25.0	uA
	$I_{DD18(LPM)}$			0.3	10.0	uA
	$I_{DDIO(LPM)}$				1.5	uA
Standby Mode	$I_{DD33(RSTB)}$	RESETB = 0 V_{VBAT} = 4.2V V_{DD18} = 1.8V V_{DDIO} = 1.8V	14.0	20.0	25.0	uA
	$I_{DD18(RSTB)}$			0.3	10.0	uA
	$I_{DDIO(RSTB)}$				1.5	uA

Note 4.1 *ClockSuspendM* bit = 0.

Note 4.2 SessEnd, VbusVld, and IdFloat comparators disabled. STP Interface protection disabled.

4.2 CLKOUT Specifications

Table 4.2 Electrical Characteristics: CLKOUT Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Suspend Recovery Time Note 4.3	T_{START}			2.07	3.32	ms
CLKOUT Duty Cycle	DC_{CLKOUT}		45		55	%
REFCLK Duty Cycle	DC_{REFCLK}		20		80	%
REFCLK Frequency Accuracy	F_{REFCLK}		-500		+500	PPM

Note 4.3 The USB3318 uses the *AutoResume* feature, Section 5.4, to allow a host start-up time of less than 1ms

4.3 ULPI Interface Timing

Table 4.3 ULPI Interface Timing

PARAMETER	SYMBOL	MIN	MAX	UNITS
Setup time (STP, data in)	T_{SC}, T_{SD}	5.0		nS
Hold time (STP, data in)	T_{HC}, T_{HD}	0.0		nS
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	1.5	3.5	nS

Note: V_{DDIO} = 1.6 to 3.6V; V_{SS} = 0V; T_A = -40C to 85C; C_{Load} = 10pF

4.4 Digital IO Pins

Table 4.4 Digital IO Characteristics: RESETB, CLKOUT, STP, DIR, NXT, DATA[7:0] and XI Pins

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}		V_{SS}		0.4 * V_{DDIO}	V
High-Level Input Voltage	V_{IH}		0.68 * V_{DDIO}		V_{DDIO}	V
High-Level Input Voltage REFCLK only	V_{IH}		0.68 * V_{DD18}		V_{DD33}	V
Clock High REFCLK only	T_{HIGH}		0.3 * T_P	0.5 * T_P	0.7 * T_P	
Clock Low REFCLK only	T_{LOW}		0.3 * T_P	0.5 * T_P	0.7 * T_P	
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	V_{DDIO}- 0.4			V
High-Level Output Voltage **CPEN** Only	V_{OH}	I_{OH} = -8mA	V_{DD33} - 0.4			V
Input Leakage Current	I_{LI}				±10	uA
Pin Capacitance	Cpin				4	pF

Table 4.4 Digital IO Characteristics: RESETB, CLKOUT, STP, DIR, NXT, DATA[7:0] and XI Pins (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STP pull-up resistance	R_{STP}	InterfaceProtectDisable = 0	51	60	65	kΩ
DATA[7:0] pull-dn resistance	R_{DATA_PD}	ULPI Synchronous Mode	55	67	79	kΩ
CLKOUT External Drive	V_{IH_ED}	At start-up or following reset			0.4 * V_{DDIO}	V

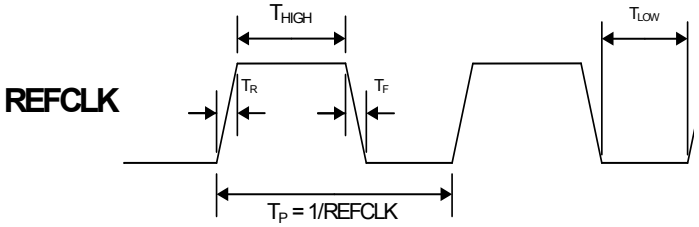

Figure 4.1 External Reference Clock

4.5 DC Characteristics: Analog I/O Pins

Table 4.5 DC Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LS/FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}	Note 4.5			0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}	Note 4.5	2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to V_{DD33}			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; Note 4.5 R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS and FS	Z_{HSDRV}	Steady state drive	40.5	45	49.5	Ω
Input Impedance	Z_{INP}	RX, RPU, RPD disabled	1.0			MΩ
Pull-up Resistor Impedance	R_{PU}	Bus Idle, Note 4.4	0.900	1.24	1.575	kΩ

Table 4.5 DC Characteristics: Analog I/O Pins (DP/DM) (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pull-up Resistor Impedance	R_{PU}	Device Receiving, Note 4.4	1.425	2.26	3.09	kΩ
Pull-dn Resistor Impedance	R_{PD}	Note 4.4	14.25	16.9	20	kΩ
Weak Pull-up Resistor Impedance	R_{CD}	Configured by bits 4 and 5 in USB IO & Power Management register.	128	170	212	kΩ
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
High-Speed Squelch Detection Threshold (Differential Signal Amplitude)	V_{HSSQ}	Note 4.6	100		150	mV
Output Levels						
Hi-Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV
Hi-Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
Hi-Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV
Leakage Current						
OFF-State Leakage Current	I_{LZ}				±10	uA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

Note 4.4 The resistor value follows the 27% Resistor ECN published by the USB-IF.

Note 4.5 The values shown are valid when the *USB RegOutput* bits in the USB IO & Power Management register are set to the default value.

Note 4.6 An automatic waiver up to 200mV is granted to accommodate system-level elements such as measurement/test fixtures, captive cables, EMI components, and ESD suppression.

4.6 Dynamic Characteristics: Analog I/O Pins

Table 4.6 Dynamic Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS Output Driver Timing						
FS Rise Time	T_{FR}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
FS Fall Time	T_{FF}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	T_{FRFM}	Excluding the first transition from IDLE state	90		111.1	%
LS Output Driver Timing						
LS Rise Time	T_{LR}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
LS Fall Time	T_{LF}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
Differential Rise/Fall Time Matching	T_{LRFM}	Excluding the first transition from IDLE state	80		125	%
HS Output Driver Timing						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification				
Hi-Speed Mode Timing						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification				
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification				

4.7 OTG Electrical Characteristics

Table 4.7 OTG Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SessEnd trip point	$V_{SessEnd}$		0.2	0.5	0.8	V
SessVld trip point	$V_{SessVld}$		0.8	1.4	2.0	V
VbusVld trip point	$V_{VbusVld}$		4.4	4.58	4.75	V
A-Device Impedance	R_{IdGnd}	Maximum A device Impedance to ground on **ID** pin			100	kΩ
ID Float trip point	$V_{IdFloat}$		1.9	2.2	2.5	V
Vbus Pull-Up	R_{VPU}	**VBUS** to **VDD33** (*ChargeVbus* = 1)	281	340	450	Ω

Table 4.7 OTG Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Vbus Pull-down	R_{VPD}	**VBUS** to **GND** (*DisChargeVbus* = 1)	656	850	1100	Ω
Vbus Impedance	R_{VB}	**VBUS** to **GND**	40	75	100	kΩ
ID pull-up resistance	R_{ID}	*IdPullup* = 1	80	100	120	kΩ
ID weak pull-up resistance	R_{IDW}	*IdPullup* = 0	1			MΩ
ID pull-dn resistance	R_{IDPD}	*IdGndDrv* = 1			1000	Ω

4.8 Regulator Output Voltages and Capacitor Requirement

Table 4.8 Regulator Output Voltages and Capacitor Requirement

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Output Voltage	V_{DD33}	6V > VBAT > 3.1V	3.0	3.3	3.6	V
Regulator Output Voltage	V_{DD33}	USB UART Mode & *UART RegOutput[1:0]* = 01 6V > VBAT > 3.1V	2.7	3.0	3.3	V
Regulator Output Voltage	V_{DD33}	USB UART Mode & *UART RegOutput[1:0]* = 10 6V > VBAT > 3.1V	2.47	2.75	3.03	V
Regulator Output Voltage	V_{DD33}	USB UART Mode & *UART RegOutput[1:0]* = 11 6V > VBAT > 3.1V	2.25	2.5	2.75	V
Regulator Bypass Capacitor	C_{BYP}		2.2			uF
Bypass Capacitor ESR	C_{ESR}				1	Ω

Table 4.9 ESD and LATCH-UP Performance

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	COMMENTS
ESD PERFORMANCE						
Note 4.7	Human Body Model			±8	kV	Device
System	EN/IEC 61000-4-2 Contact Discharge			±8	kV	3rd party system test
System	EN/IEC 61000-4-2 Air-gap Discharge			±15	kV	3rd party system test
LATCH-UP PERFORMANCE						
All Pins	EIA/JESD 78, Class II		150		mA	

Note 4.7 **REFCLK** pin ±5kV Human Body Model.

Chapter 5 Architecture Overview

The USB3318 consists of the blocks shown in the diagram below. All pull-up resistors shown in Figure 5.1 are connected to VDD33.

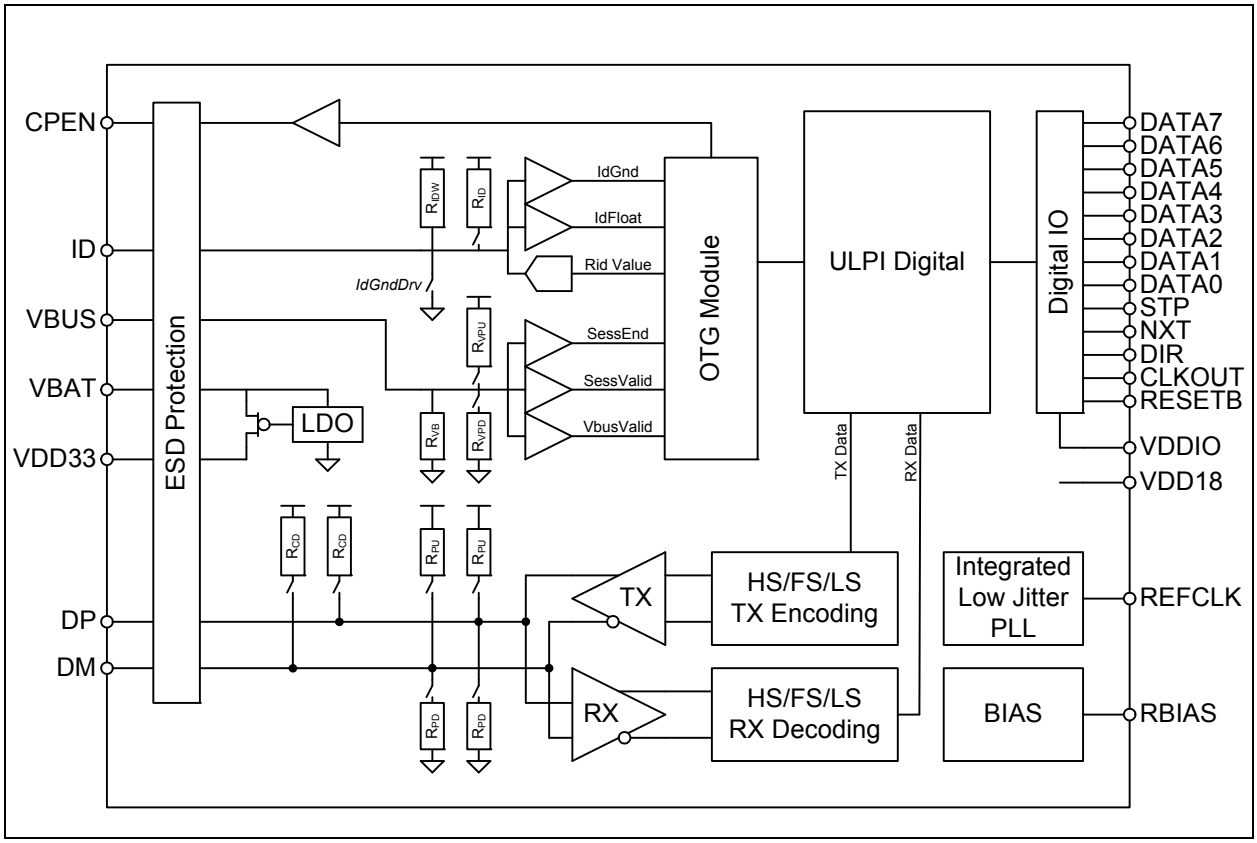

Figure 5.1 USB3318 System Diagram

5.1 ULPI Digital Operation and Interface

This section of the USB3318 is covered in detail in Chapter 6, ULPI Operation Overview.

5.2 Interface to DP/DM

The blocks in the lower left-hand corner of Figure 5.1 interface to the DP/DM pins.

5.2.1 USB Transceiver

The USB3318 transceiver includes the receivers and transmitters required to be compliant to the Universal Serial Bus Specification Rev 2.0. The DP/DM signals in the USB cable connect directly to the receivers and transmitters.

The RX block consists of separate differential receivers for HS and FS/LS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX Logic block. For HS mode support, the HS RX block contains a squelch circuit to insure that noise is not interpreted as data. The RX block also includes a single-ended receiver on each of the data lines to determine the correct FS linestate.

Data from the TX Logic block is encoded, bit stuffed, serialized and transmitted onto the USB cable by the TX block. Separate differential FS/LS and HS transmitters are included to support all modes.

The USB3318 TX block meets the HS signalling level requirements in the USB 2.0 Specification when the PCB traces from the **DP** and **DM** pins to the USB connector have very little loss. In some systems, it may be desirable to compensate for loss by adjusting the HS transmitter amplitude. The *Boost* bits in the HS TX Boost register may be configured to adjust the HS transmitter amplitude at the **DP** and **DM** pins.

5.2.2 Termination Resistors

The USB3318 transceiver fully integrates all of the USB termination resistors on both **DP** and **DM**. This includes 1.5kΩ pull-up resistors, 15kΩ pull-down resistors and the 45Ω high speed termination resistors. These resistors require no tuning or trimming by the Link. The state of the resistors is determined by the operating mode of the PHY when operating in synchronous mode.

The *XcvrSelect[1:0]*, *TermSelect* and *OpMode[1:0]* bits in the Function Control register, and the *DpPulldown* and *DmPulldown* bits in the OTG Control register control the configuration. The possible valid resistor combinations are shown in Table 5.1, and operation is guaranteed in only the configurations shown. If a ULPI Register Setting is configured that does not match a setting in the table, the transceiver operation is not guaranteed and the settings in the last row of Table 5.1 will be used.

- RPU_DP_EN activates the 1.5kΩ DP pull-up resistor
- RPU_DM_EN activates the 1.5kΩ DM pull-up resistor
- RPD_DP_EN activates the 15kΩ DP pull-down resistor
- RPD_DM_EN activates the 15kΩ DM pull-down resistor
- HSTERM_EN activates the 45Ω DP and DM high speed termination resistors

The USB3318 also includes two 125kΩ **DP** and **DM** pull-up resistors described in Section 5.8.

Table 5.1 DP/DM Termination vs. Signaling Mode

SIGNALING MODE	ULPI REGISTER SETTINGS					USB3318 TERMINATION RESISTOR SETTINGS				
	XCVRSELECT[1:0]	TERMSELECT	OPMODE[1:0]	DPPULLDOWN	DMPULLDOWN	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
General Settings										
Tri-State Drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or Vbus < $V_{SESSEND}$	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
Host Settings										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host Hi-Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b

Table 5.1 DP/DM Termination vs. Signaling Mode (continued)

SIGNALING MODE	ULPI REGISTER SETTINGS					USB3318 TERMINATION RESISTOR SETTINGS				
	XCVRSELECT[1:0]	TERMSELECT	OPMODE[1:0]	DPPULLDOWN	DMPULLDOWN	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
Host low Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Resume	10b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Test J/Test_K	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Peripheral Settings										
Peripheral Chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS	00b	0b	00b	0b	0b	0b	0b	0b	0b	1b
Peripheral FS	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral LS	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Suspend	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Resume	10b	1b	10b	0b	0b	0b	1b	0b	0b	0b
Peripheral Test J/Test K	00b	0b	10b	0b	0b	0b	0b	0b	0b	1b
OTG device, Peripheral Chirp	00b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS	00b	0b	00b	0b	1b	0b	0b	0b	1b	1b
OTG device, Peripheral FS	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Resume	01b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral Test J/Test K	00b	0b	10b	0b	1b	0b	0b	0b	1b	1b
Any combination not defined above Note 5.1						0b	0b	0b	0b	0b

Note: This is the same as Table 40, Section 4.4 of the ULPI 1.1 specification.

Note: USB3318 does not support operation as an upstream hub port. See Section 6.2.4.3.

Note 5.1 The transceiver operation is not guaranteed in a combination that is not defined.

The USB3318 uses the 27% resistor ECN resistor tolerances. The resistor values are shown in Table 4.5.

5.3 Bias Generator

This block consists of an internal bandgap reference circuit used for generating the driver current and the biasing of the analog circuits. This block requires an external 8.06KΩ, 1% tolerance, reference resistor connected from **RBIAS** to ground. This resistor should be placed as close as possible to the USB3318 to minimize the trace length. The nominal voltage at **RBIAS** is 0.8V and therefore the resistor will dissipate approximately 80μW of power.

5.4 Integrated Low Jitter PLL

The USB3318 uses an integrated low jitter phase locked loop (PLL) to provide a clean 480MHz clock. This clock is used by the PHY during both transmit and receive. The USB3318 requires a 13MHz reference clock to be driven on the **REFCLK** pin.

After the PLL has locked to the correct frequency, the USB3318 will de-assert **DIR** and the Link can begin using the ULPI interface. The USB3318 is guaranteed to start the clock within the time specified in Table 4.2. For Host applications, the ULPI *AutoResume* bit should be enabled. This is described in Section 6.2.4.4.

The system must not drive voltage on the CLKOUT pin following POR or hardware reset that exceeds the value of V_{IH_ED} provided in Table 4.4.

5.4.1 Reference Clock Requirements

The reference clock is connected to the REFCLK pins as shown in the application diagram, Figure 8.1. The REFCLK pin is designed to be driven with a square wave from 0V to V_{DDIO}, but can be driven with a square wave from 0V to as high as 3.6V.

When using an external reference clock, the USB3318 only uses the positive edge of the clock. The signal must comply with the V_{IH} and V_{IL} parameters provided in Table 4.4. It may be possible to AC couple the reference clock to change the common-mode voltage level when it is sourced by a device that does not comply with the V_{IH} and V_{IL} parameters. A DC bias network must be provided at the REFCLK pin when the reference clock is AC coupled. The component values provided in Figure 5.2 are for example only. The actual values should be selected to satisfy system requirements.

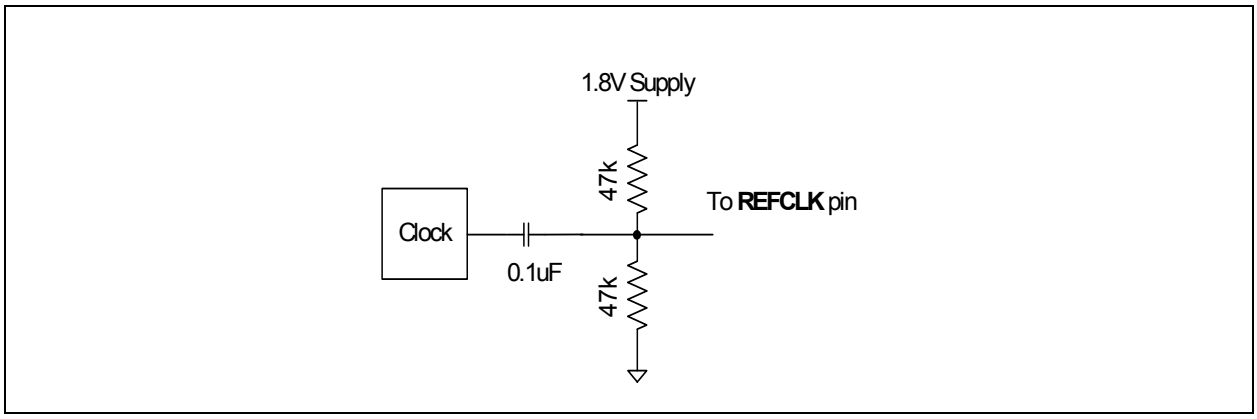

Figure 5.2 Example of circuit used to shift a reference clock common-mode voltage level.

The USB3318 is tolerant to jitter on the reference clock. The REFCLK jitter should be limited to a peak to peak jitter of less than 1nS over a 10uS time interval. If this level of jitter is exceeded the USB3318 high speed eye diagram may be degraded.

The edges of the reference clock do not need to be aligned in any way to the ULPI interface signals. The reference clock is used by a PLL to generate the 60MHz CLKOUT for the ULPI digital. There is no need to align the phase of the REFCLK and the 60MHz CLKOUT.

The REFCLK should be enabled when the RESETB pin is brought high. The ULPI interface will start running after the time specified in Table 4.2. If the REFCLK enable is delayed relative to the RESETB pin, the ULPI interface will start operation delayed by the same amount. The REFCLK can be run at anytime the RESETB pin is low without causing the USB3318 to start-up or draw current.

When the USB3318 is placed in Low Power Mode or carkit mode the REFCLK can be stopped after the final ULPI register write is complete. The STP pin is asserted to bring the USB3318 out of Low Power Mode. The REFCLK should be started at the same time STP is asserted to minimize the USB3318 start-up time.

If the REFCLK is stopped while CLKOUT is running the PLL will come out of lock and the frequency of the CLKOUT signal will decrease to the minimum allowed by the PLL design. If the REFCLK is stopped during a USB session the session may drop.

5.5 Internal Regulators and POR

The USB3318 includes integrated power management functions, including a Low-Dropout regulator that can be used to generate the 3.3V USB supply, and a POR generator.

5.5.1 Integrated Low Dropout Regulator

The USB3318 has an integrated linear regulator. Power sourced at the **VBAT** pin is regulated to 3.3V and the regulator output is on the **VDD33** pin. To ensure stability, the regulator requires an external bypass capacitor as specified in Table 4.8 placed as close to the pin as possible.

The USB3318 regulator is designed to generate a 3.3 volt supply for the USB3318 only. Using the regulator to provide current for other circuits is not recommended and SMSC does not guarantee USB performance or regulator stability.

During USB UART mode the regulator output voltage can be changed to allow the USB3318 to work with UARTs operating at different operating voltages. The regulator output voltage is controlled by the *UART RegOutput[1:0]* bits described in Section 7.1.4.4 and Table 4.8.

The USB3318 regulator can be powered in the three methods as shown below.

For USB Peripheral, Host, and OTG operations the regulator can be connected as shown in Figure 5.3 or Figure 5.4 below. For OTG operation, the **VDD33** supply on the USB3318 must be powered to detect devices attaching to the USB connector and detect a SRP during an OTG session. When using a battery to supply the USB3318 the battery voltage must be within the range of 3.1V to 5.5V

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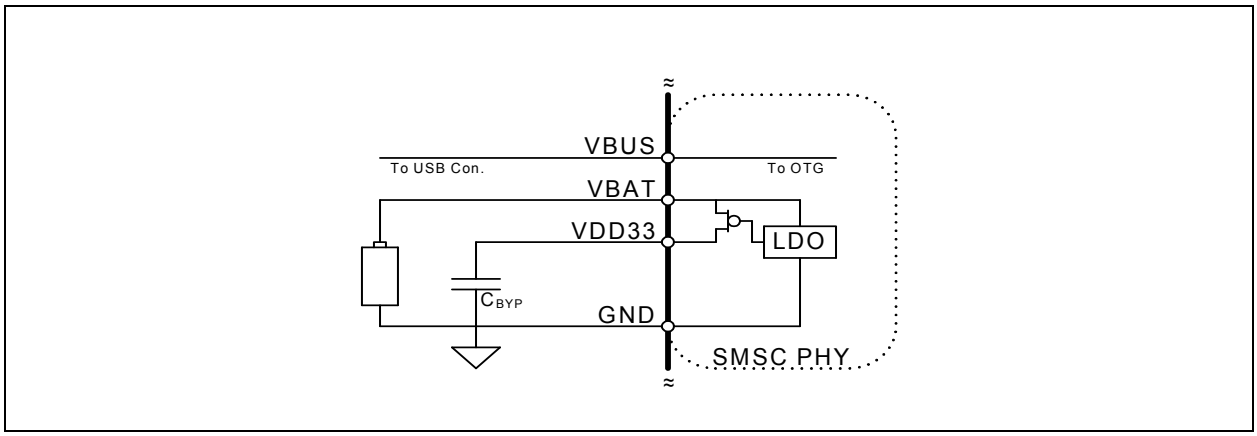

Figure 5.3 Powering the USB3318 from a Battery

The USB3318 can be powered from an external 3.3V supply as shown in Figure 5.4. When using the external supply both the **VBAT** and **VDD33** pins are connected together. The bypass capacitor should be included when using the external supply.

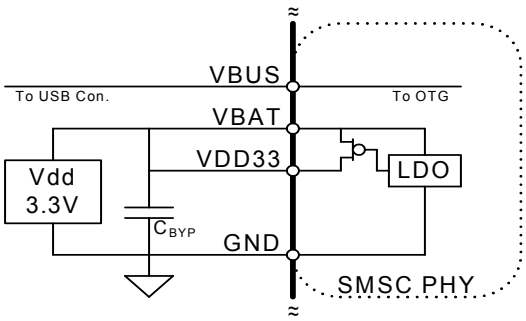

Figure 5.4 Powering the USB3318 from a 3.3V Supply

For peripheral only or host only operation the regulator can be connected as shown in Figure 5.5. This connection of the regulator requires the Vbus supply to be present any time the USB operation is desired. When a Vbus voltage is not present, the USB3318 cannot detect OTG or Carkit signaling.

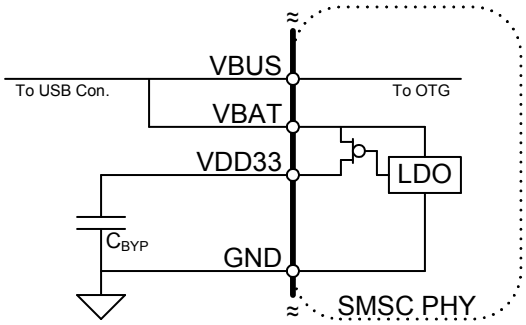

Figure 5.5 Powering the USB3318 from the USB Cable Vbus

When using the USB3318 connected as shown in Figure 5.5, the ULPI interface will operate when Vbus is removed. When Vbus is removed the USB3318 should be placed into Low Power Mode until Vbus is detected through an interrupt. While the USB3318 is in Low Power Mode the status of **VBUS**, **ID**, **DP**, and **DM** can be monitored while drawing a minimum amount of current from the **VDD18** supply as described in Section 6.2.6.4.

5.5.2 Power On Reset (POR)

The USB3318 provides an internal POR circuit that generates a reset pulse after the **VDD18** supply is stable. After the internal POR goes high and the **RESETB** pin is high, the USB3318 will release from reset and begin normal ULPI operation. Provided that REFCLK is present when the **RESETB** pin is brought high, the ULPI bus will be available in the time defined as T_{START} as given in Table 4.2.

The ULPI registers will power up in their default state summarized in Table 7.1 when the 1.8V supply is brought up. Cycling the 1.8 volt power supply will reset the ULPI registers to their default states. The **RESETB** pin can also be used to reset the ULPI registers to their default state (and reset all internal state machines) by bringing the pin low for a minimum of 1 microsecond and then high.