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USB3320

Highly Integrated Full Featured Hi-Speed USB 2.0 ULPI Transceiver

Features

- Integrated ESD protection circuits
  - Up to ±15kV IEC Air Discharge without external devices
- Over-Voltage Protection circuit (OVP) protects the VBUS pin from continuous DC voltages up to 30V
- Integrated USB Switch
  - No degradation of Hi-Speed electrical characteristics
  - Allows single USB port of connection by providing switching function for:
    - –Battery charging
    - –Stereo and mono/mic audio
    - –USB Full-Speed/Low-Speed data
- flexPWR® Technology
  - Low current design ideal for battery powered applications
  - “Sleep” mode tri-states all ULPI pins and places the part in a low current state
  - 1.8V to 3.3V IO Voltage (±10%)
- Integrated battery to 3.3V regulator
  - 2.2uF bypass capacitor
  - 100mV dropout voltage
- “Wrapper-less” design for optimal timing performance and design ease
  - Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max) allows use of legacy UTMI Links with a ULPI bridge
- Selectable Reference Clock Frequency
  - Frequencies: 12, 13, 19.2, 24, 26, 27, 38.4, 52 or 60MHz - pin selectable
- External Reference Clock operation available
  - ULPI Input Clock Mode (60MHz sourced by Link)
  - 0 to 3.6V input drive tolerant
  - Able to accept “noisy” clock sources as reference to internal, low-jitter PLL
- Internal Oscillator operation available
- This mode requires external Quartz Crystal or Ceramic Resonator
- Smart detection circuits allow identification of USB charger, headset, or data cable insertion
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 2.0 specification
- Supports Headset Audio Mode
- Supports the OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- UART mode for non-USB serial data transfers
- Internal 5V cable short-circuit protection of ID, DP and DM lines to VBUS or ground
- Industrial Operating Temperature -40°C to +85°C
- 32-pin, QFN RoHS Compliant Package (5 x 5 x 0.90 mm height)

Applications

The USB3320 is targeted for any application where a Hi-Speed USB connection is desired and when board space, power, and interface pins must be minimized.

The USB3320 is well suited for:

- Networking
- Audio Video
- Medical
- Industrial Computers
- Printers
- Repeaters
- Communication

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Table of Contents

1.0 INTRODUCTION

1.1 General Description

The Microchip USB3320 is a Hi-Speed USB 2.0 Transceiver that provides a configurable physical layer (PHY) solution and is an excellent match for a wide variety of products.

The frequency of the reference clock is user selectable. The USB3320 includes an internal oscillator that may be used with either a quartz crystal or a ceramic resonator. Alternatively, the crystal input can be driven by an external clock oscillator. Another option is the use of a 60MHz external clock when using the ULPI Input Clock mode.

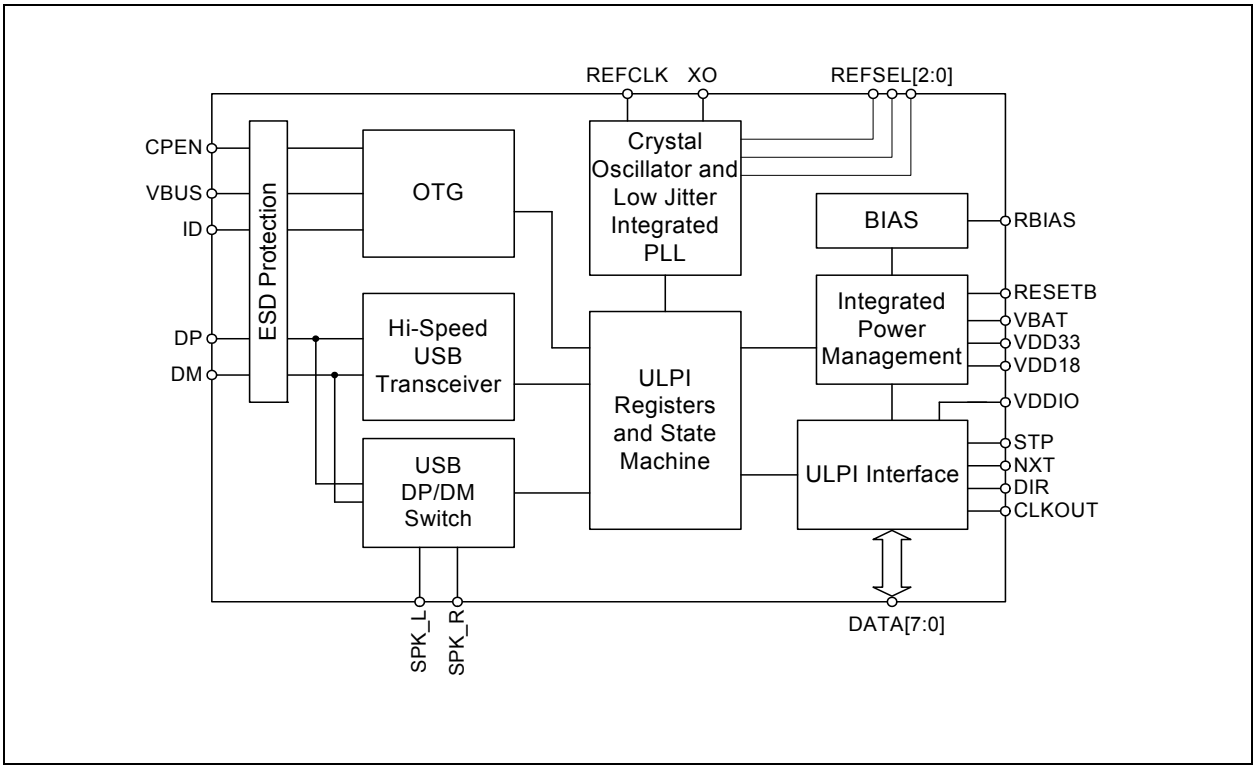
Several advanced features make the USB3320 the transceiver of choice by reducing both electrical bill of material (eBOM) part count and printed circuit board (PCB) area. Outstanding ESD robustness eliminates the need for external ESD protection devices in typical applications. The internal Over-Voltage Protection circuit (OVP) protects the USB3320 from voltages up to 30V. By using a reference clock from the Link, the USB3320 removes the cost of a dedicated crystal reference from the design. And the integrated USB switch enables unique product features with a single USB port of connection.

The USB3320 meets all of the electrical requirements to be used as a Hi-Speed USB Host, Device, or an On-the-Go (OTG) transceiver. In addition to the supporting USB signaling, the USB3320 also provides USB UART mode and USB Audio mode.

USB3320 uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB Transceiver to the Link. ULPI uses a method of in-band signaling and status byte transfers between the Link and transceiver to facilitate a USB session with only 12 pins.

The USB3320 uses Microchip's "wrapper-less" technology to implement the ULPI interface. This "wrapper-less" technology allows the transceiver to achieve a low latency transmit and receive time. Microchip's low latency transceiver allows an existing UTMI Link to be reused by adding a UTMI to ULPI bridge. By adding a bridge to the ASIC the existing and proven UTMI Link IP can be reused.

FIGURE 1-1: USB3320 BLOCK DIAGRAM



The USB3320 includes an integrated 3.3V Low Drop Out (LDO) regulator that may optionally be used to generate 3.3V from power applied at the **VBAT** pin. The voltage on the **VBAT** pin can range from 3.1 to 5.5V. The regulator dropout voltage is less than 100mV which allows the transceiver to continue USB signaling when the voltage on **VBAT** drops to 3.1V. The USB transceiver will continue to operate at lower voltages, although some parameters may be outside the limits of the USB specifications. If the user would like to provide a 3.3V supply to the USB3320, the **VBAT** and **VDD33** pins should be connected together as described in Section 5.5.1.

The USB3320 also includes integrated pull-up resistors that can be used for detecting the attachment of a USB Charger. By sensing the attachment to a USB Charger, a product using the USB3320 can charge its battery at more than the 500mA allowed when charging from a USB Host. Please see Microchip Application Note AN 19.7 - Battery Charging Using Microchip USB Transceivers for more information on battery charging.

In USB UART mode, the USB3320 **DP** and **DM** pins are redefined to enable pass-through of asynchronous serial data. The USB3320 can only enter UART mode when the user programs the part into this mode, as described in Section 6.5.1.

In USB audio mode, a switch connects the **DP** pin to the **SPK_R** pin, and another switch connects he **DM** pin to the **SPK_L** pin. These switches are shown in the lower left-hand corner of Figure 5.1. The USB3320 can be configured to enter USB audio mode as described in Section 6.5.2. In addition, these switches are on when the **RESETB** pin of the USB3320 is asserted. The USB audio mode enables audio signaling from a single USB port of connection, and the switches may also be used to connect Full Speed USB from another transceiver onto the USB cable.

1.2 Reference Documents

- Universal Serial Bus Specification, Revision 2.0, April 27, 2000
- On-The-Go Supplement to the USB 2.0 Specification, Revision 2.0, May 8, 2009
- USB Specification Revision 2.0 "Pull-up/pull-down resistors" ECN (27% Resistor ECN)
- USB 2.0 Transceiver Macrocell Interface (UTMI) Specification, Version 1.02, May 27, 2000
- UTMI+ Specification, Revision 1.0, February 25, 2004
- UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1, October 20th, 2004
- Technical Requirements and Test Methods of Charger and Interface for Mobile Telecommunication Terminal Equipment (Chinese Charger Specification Approval Draft 11/29/2006)

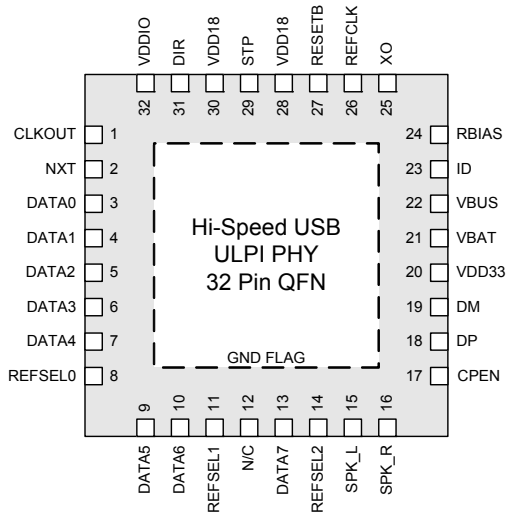
2.0 USB3320 PIN LOCATIONS AND DEFINITIONS

2.1 USB3320 Pin Locations and Descriptions

2.1.1 PACKAGE DIAGRAM WITH PIN LOCATIONS

The illustration below is viewed from the top of the package.

FIGURE 2-1: USB3320 PIN LOCATIONS - TOP VIEW



2.1.2 PIN DEFINITIONS

The following table details the pin definitions for the figure above.

TABLE 2-1: USB3320 PIN DESCRIPTION

Pin	Name	Direction/ Type	Active Level	Description
1	**CLKOUT**	Output, CMOS	N/A	**ULPI Output Clock Mode:** 60MHz ULPI clock output. All ULPI signals are driven synchronous to the rising edge of this clock. **ULPI Input Clock Mode:** This pin is connected to VDDIO to configure 60MHz ULPI Input Clock mode as described in Section 5.4.1. Following POR or hardware reset, the voltage at **CLKOUT** must not exceed V_{IH_ED} as provided inTable 4-4.
2	**NXT**	Output, CMOS	High	The transceiver asserts **NXT** to throttle the data. When the Link is sending data to the transceiver, **NXT** indicates when the current byte has been accepted by the transceiver. The Link places the next byte on the data bus in the following clock cycle.
3	**DATA[0]**	I/O, CMOS	N/A	ULPI bi-directional data bus.

TABLE 2-1: USB3320 PIN DESCRIPTION (CONTINUED)

Pin	Name	Direction/ Type	Active Level	Description
4	**DATA[1]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
5	**DATA[2]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
6	**DATA[3]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
7	**DATA[4]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
8	**REFSEL[0]**	Input, CMOS	N/A	This signal, along with **REFSEL[1]** and **REFSEL[2]** selects one of the available reference frequencies as defined in Table 5-10. Note: This signal must be tied to VDDIO when in ULPI 60MHz REFCLK IN mode.
9	**DATA[5]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
10	**DATA[6]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
11	**REFSEL[1]**	Input, CMOS	N/A	This signal, along with **REFSEL[0]** and **REFSEL[2]** selects one of the available reference frequencies as defined in Table 5-10. Note: This signal must be tied to VDDIO when in ULPI 60MHz REFCLK IN mode.
12	**N/C**		N/A	This pin must not be connected.
13	**DATA[7]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
14	**REFSEL[2]**	Input, CMOS	N/A	This signal, along with **REFSEL[0]** and **REFSEL[1]** selects one of the available reference frequencies as defined in Table 5-10. Note: This signal must be tied to VDDIO when in ULPI 60MHz REFCLK IN mode.
15	**SPK_L**	I/O, Analog	N/A	USB switch in/out for DM signals
16	**SPK_R**	I/O, Analog	N/A	USB switch in/out for DP signals
17	**CPEN**	Output, CMOS	N/A	External 5V supply enable. Controls the external V_{BUS} power switch. **CPEN** is low on POR.
18	**DP**	I/O, Analog	N/A	D+ pin of the USB cable.
19	**DM**	I/O, Analog	N/A	D- pin of the USB cable.
20	**VDD33**	Power	N/A	3.3V Regulator Output. A 2.2uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3320.
21	**VBAT**	Power	N/A	Regulator input.

TABLE 2-1: USB3320 PIN DESCRIPTION (CONTINUED)

Pin	Name	Direction/ Type	Active Level	Description
22	**VBUS**	I/O, Analog	N/A	This pin connects to an external resistor (R_{VBUS}) connected to the VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs and for VBUS pulsing during session request protocol. See Table 5-7, "Required RVBUS Resistor Value".
23	**ID**	Input, Analog	N/A	**ID** pin of the USB cable. For applications not using ID this pin can be connected to **VDD33**. For an A-Device **ID** is grounded. For a B-Device **ID** is floated.
24	**RBIAS**	Analog, CMOS	N/A	Bias Resistor pin. This pin requires an 8.06kΩ (±1%) resistor to ground, placed as close as possible to the USB3320. Nominal voltage during ULPI operation is 0.8V.
25	**XO**	Output, CMOS	N/A	External resonator pin. When using an external clock on **REFCLK**, this pin should be floated.
26	**REFCLK**	Input, CMOS	N/A	**ULPI Output Clock Mode:** Reference frequency as defined in Table 5-10. **ULPI Input Clock Mode:** 60MHz ULPI clock input.
27	**RESETB**	Input, CMOS,	Low	When low, the part is suspended with all ULPI outputs tri-stated. When high, the USB3320 will operate as a normal ULPI device, as described in Section 5.5.2. The state of this pin may be changed asynchronously to the clock signals. When asserted for a minimum of 1 microsecond and then de-asserted, the ULPI registers are reset to their default state and all internal state machines are reset.
28	**VDD18**	Power	N/A	External 1.8V Supply input pin. This pad needs to be bypassed with a 0.1uF capacitor to ground, placed as close as possible to the USB3320.
29	**STP**	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the transceiver, **STP** indicates the last byte of data was on the bus in the previous cycle.
30	**VDD18**	Power	N/A	External 1.8V Supply input pin. This pad needs to be bypassed with a 0.1uF capacitor to ground, placed as close as possible to the USB3320.
31	**DIR**	Output, CMOS	N/A	Controls the direction of the data bus. When the transceiver has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the transceiver has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.
32	**VDDIO**	Power	N/A	External 1.8V to 3.3V ULPI supply input pin. This voltage sets the value of V_{OH} for the ULPI signals. This pad needs to be bypassed with a 0.1uF capacitor to ground, placed as close as possible to the USB3320.
FLAG	**GND**	Ground	N/A	Ground.

3.0 LIMITING VALUES

3.1 Absolute Maximum Ratings

TABLE 3-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
VBUS, **VBAT**, **ID**, **CPEN**, **DP**, **DM**, **SPK_L**, and **SPK_R** voltage to **GND**	V_{MAX_5V}	Voltage measured at pin. **VBUS** tolerant to 30V with external R_{VBUS}.	-0.5		+6.0	V
Maximum **VDD18** voltage to Ground	V_{MAX_18V}		-0.5		2.5	V
Maximum **VDDIO** voltage to Ground	V_{MAX_IOV}	**VDD18** = V_{DD18}	-0.5		4.0	V
Maximum **VDDIO** voltage to Ground	V_{MAX_IOV}	**VDD18** = 0V	-0.5		0.7	V
Maximum **VDD33** voltage to Ground	V_{MAX_33V}		-0.5		4.0	V
Maximum I/O voltage to Ground	V_{MAX_IN}		-0.5		V_{DDIO} + 0.7	V
Operating Temperature	T_{MAX_OP}		-40		85	°C
Storage Temperature	T_{MAX_STG}		-55		150	°C

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

TABLE 3-2: RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
VBAT to **GND**	V_{VBAT}		3.1		5.5	V
VDD33 to **GND**	V_{DD33}		3.0	3.3	3.6	V
VDDIO to **GND**	V_{DDIO}	$\boldsymbol{VDDIO} \geq \boldsymbol{VDD18}(min)$	1.6	1.8-3.3	3.6	V
VDD18 to **GND**	V_{DD18}		1.6	1.8	2.0	V
Input Voltage on Digital Pins (**RESETB**, **STP**, **DIR**, **NXT**, **DATA[7:0]**)	V_I		0.0		V_{DDIO}	V
Voltage on Analog I/O Pins (**DP**, **DM**, **ID**, **CPEN**, **SPK_L**, **SPK_R**)	$V_{I(I/O)}$		0.0		V_{DD33}	V
VBUS to **GND**	V_{VMAX}		0.0		5.5	V
Ambient Temperature	T_A		-40		85	°C

4.0 ELECTRICAL CHARACTERISTICS

The following conditions are assumed unless otherwise specified:

V_{VBAT} = 3.1 to 5.5V; V_{DD18} = 1.6 to 2.0V; V_{DDIO} = 1.6 to 2.0V; V_{SS} = 0V; T_A = -40°C to +85°C

The current for 3.3V circuits is sourced at the VBAT pin, except when using an external 3.3V supply as shown in Figure 5-7.

4.1 Operating Current

TABLE 4-1: ELECTRICAL CHARACTERISTICS: OPERATING CURRENT

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
Synchronous Mode Current (Default Configuration)	$I_{33AVG(SYNC)}$	Start-up sequence defined in Section 5.5.4 has completed.		7.5		mA
	$I_{18AVG(SYNC)}$			28.0		mA
	$I_{IOAVG(SYNC)}$			4.1		mA
Synchronous Mode Current (HS USB operation)	$I_{33AVG(HS)}$	Active USB Transfer		11.1		mA
	$I_{18AVG(HS)}$			29.4		mA
	$I_{IOAVG(HS)}$			5.9		mA
Synchronous Mode Current (FS/LS USB operation)	$I_{33AVG(FS)}$	Active USB Transfer		6.3		mA
	$I_{18AVG(FS)}$			22.5		mA
	$I_{IOAVG(FS)}$			5.0		mA
Serial Mode Current (FS/LS USB) Note 4-1	$I_{33AVG(FS\_S)}$			5.6		mA
	$I_{18AVG(FS\_S)}$			2.4		mA
	$I_{IOAVG(FS\_S)}$			86		uA
USB UART Current Note 4-1	$I_{33AVG(UART)}$			5.6		mA
	$I_{18AVG(UART)}$			2.4		mA
	$I_{IOAVG(UART)}$			58		uA
Low Power Mode Note 4-2	$I_{DD33(LPM)}$	V_{VBAT} = 4.2V V_{DD18} = 1.8V V_{DDIO} = 1.8V		18.8		uA
	$I_{DD18(LPM)}$			0.7		uA
	$I_{DDIO(LPM)}$			30		uA
Standby Mode	$I_{DD33(RSTB)}$	RESETB = 0 V_{VBAT} = 4.2V V_{DD18} = 1.8V V_{DDIO} = 1.8V		18		uA
	$I_{DD18(RSTB)}$			0.6		uA
	$I_{DDIO(RSTB)}$			0.1		uA

Note 4-1 *ClockSuspendM* bit = 0.

Note 4-2 SessEnd, VbusVld, and IdFloat comparators disabled. STP Interface protection disabled.

4.2 Clock Specifications

TABLE 4-2: ULPI CLOCK SPECIFICATIONS

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
Suspend Recovery Time Note 4-3	T_{START}	26MHz **REFCLK**		1.03	2.28	ms
		12MHz **REFCLK**		2.24	3.49	ms
		52MHz **REFCLK**		0.52	1.77	ms
		24MHz **REFCLK**		1.12	2.37	ms
		19.2MHz **REFCLK**		1.40	2.65	ms
		27MHz **REFCLK**		1.00	2.25	ms
		38.4MHz **REFCLK**		0.70	1.95	ms
		13MHz **REFCLK**		2.07	3.32	ms
PHY Preparation Time	T_{PREP}	60MHz **REFCLK** **ULPI Input Clock Mode**	0.4	0.45	0.5	ms
CLKOUT Duty Cycle	DC_{CLKOUT}	**ULPI Input Clock Mode**	45		55	%
REFCLK Duty Cycle	DC_{REFCLK}		20		80	%
REFCLK Frequency Accuracy	F_{REFCLK}		-500		+500	PPM

Note 4-3 The Suspend Recovery Time is measured from the start of the REFCLK to when the USB3320 de-asserts **DIR**.

Note: The USB3320 uses the *AutoResume* feature, Section 6.2.4.4, to allow a host start-up time of less than 1ms.

4.3 ULPI Interface Timing

TABLE 4-3: ULPI INTERFACE TIMING

Parameter	Symbol	Condition	MIN	MAX	Units
60MHz ULPI Output Clock Note 4-4					
Setup time (STP, data in)	T_{SC}, T_{SD}	Model-specific **REFCLK**	5.0		ns
Hold time (STP, data in)	T_{HC}, T_{HD}	Model-specific **REFCLK**	0.0		ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	Model-specific **REFCLK**	1.0	3.5	ns
60MHz ULPI Input Clock					
Setup time (STP, data in)	T_{SC}, T_{SD}	60MHz **REFCLK**	1.5		ns
Hold time (STP, data in)	T_{HC}, T_{HD}	60MHz **REFCLK**	-0.5		ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	60Mhz **REFCLK**	1.5	6.0	ns

Note: V_{DD18} = 1.6 to 2.0V; V_{SS} = 0V; T_A = -40°C to +85°C.

Note 4-4 **REFCLK** does not need to be aligned in any way to the ULPI signals.

4.4 Digital IO Pins

TABLE 4-4: DIGITAL IO CHARACTERISTICS: RESETB, CLKOUT, STP, DIR, NXT, DATA[7:0] & REFCLK PINS

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
Low-Level Input Voltage	V_{IL}		V_{SS}		0.4 * V_{DDIO}	V
High-Level Input Voltage	V_{IH}		0.68 * V_{DDIO}		V_{DDIO}	V
High-Level Input Voltage **REFCLK** only	V_{IH}		0.68 * V_{DD18}		V_{DD33}	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	V_{DDIO} - 0.4			V
High-Level Output Voltage **CPEN** Only	V_{OH}	I_{OH} = -8mA	V_{DD33} - 0.4			V
Input Leakage Current	I_{LI}		V_{DD33} - 0.4		±10	uA
Pin Capacitance	Cpin				4	pF
STP pull-up resistance	R_{STP}	*InterfaceProtectDisable* = 0	55	67	77	kΩ
DATA[7:0] pull-dn resistance	R_{DATA_PD}	*ULPI Synchronous Mode*	55	67	77	kΩ
CLKOUT External Drive	V_{IH_ED}	At start-up or following reset			0.4 * V_{DDIO}	V

4.5 DC Characteristics: Analog I/O Pins

TABLE 4-5: DC CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
LS/FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}	Note 4-6			0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}	Note 4-6	2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to V_{DD33}			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; Note 4-6 R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS and FS	Z_{HSDRV}	Steady state drive	40.5	45	49.5	Ω
Input Impedance	Z_{INP}	RX, RPU, RPD disabled	1.0			MΩ
Pull-up Resistor Impedance	R_{PU}	Bus Idle, Note 4-5	0.900	1.24	1.575	kΩ
Pull-up Resistor Impedance	R_{PU}	Device Receiving, Note 4-5	1.425	2.26	3.09	kΩ

TABLE 4-5: DC CHARACTERISTICS: ANALOG I/O PINS (DP/DM) (CONTINUED)

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
Pull-dn Resistor Impedance	R_{PD}	Note 4-5	14.25	16.9	20	kΩ
Weak Pull-up Resistor Impedance	R_{CD}	Configured by bits 4 and 5 in USB IO & Power Management register.	128	170	212	kΩ
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
High-Speed Squelch Detection Threshold (Differential Signal Amplitude)	V_{HSSQ}	Note 4-7	100		150	mV
Output Levels						
Hi-Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV
Hi-Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
Hi-Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV
Leakage Current						
OFF-State Leakage Current	I_{LZ}				±10	uA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

Note 4-5 The resistor value follows the 27% Resistor ECN published by the USB-IF.

Note 4-6 The values shown are valid when the *USB RegOutput* bits in the USB IO & Power Management register are set to the default value.

Note 4-7 An automatic waiver up to 200mV is granted to accommodate system-level elements such as measurement/test fixtures, captive cables, EMI components, and ESD suppression.

4.6 Dynamic Characteristics: Analog I/O Pins

TABLE 4-6: DYNAMIC CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
FS Output Driver Timing						
FS Rise Time	T_{FR}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
FS Fall Time	T_{FF}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	T_{FRFM}	Excluding the first transition from IDLE state	90		111.1	%
LS Output Driver Timing						
LS Rise Time	T_{LR}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
LS Fall Time	T_{LF}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
Differential Rise/Fall Time Matching	T_{LRFM}	Excluding the first transition from IDLE state	80		125	%
HS Output Driver Timing						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification				
Hi-Speed Mode Timing						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification				
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification				

4.7 OTG Electrical Characteristics

TABLE 4-7: OTG ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
SessEnd trip point	$V_{SessEnd}$		0.2	0.5	0.8	V
SessVld trip point	$V_{SessVld}$		0.8	1.4	2.0	V
VbusVld trip point	$V_{VbusVld}$		4.4	4.58	4.75	V
A-Device Impedance	R_{IdGnd}	Maximum A device Impedance to ground on **ID** pin			100	kΩ
ID Float trip point	$V_{IdFloat}$		1.9	2.2	2.5	V
VBUS Pull-Up	R_{VPU}	**VBUS** to **VDD33** Note 4-8 (*ChargeVbus* = 1)	1.29	1.34	1.45	kΩ
VBUS Pull-down	R_{VPD}	**VBUS** to **GND** Note 4-8 (*DisChargeVbus* = 1)	1.55	1.7	1.85	kΩ
VBUS Impedance	R_{VB}	**VBUS** to **GND**	40	75	100	kΩ
ID pull-up resistance	R_{ID}	*IdPullup* = 1	80	100	120	kΩ
ID weak pull-up resistance	R_{IDW}	*IdPullup* = 0	1			MΩ
ID pull-dn resistance	R_{IDPD}	*IdGndDrv* = 1			1000	Ω

Note 4-8 The R_{VPD} and R_{VPU} values include the required 1kΩ external R_{VBUS} resistor.

4.8 USB Audio Switch Characteristics

TABLE 4-8: USB AUDIO SWITCH CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
Minimum “ON” Resistance	R_{ON_Min}	$0 < V_{switch} < V_{DD33}$	2.7	5	5.8	Ω
Maximum “ON” Resistance	R_{ON_Max}	$0 < V_{switch} < V_{DD33}$	4.5	7	10	Ω
Minimum “OFF” Resistance	R_{OFF_Min}	$0 < V_{switch} < V_{DD33}$	1			MΩ

4.9 Regulator Output Voltages and Capacitor Requirement

TABLE 4-9: REGULATOR OUTPUT VOLTAGES AND CAPACITOR REQUIREMENT

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
Regulator Output Voltage	V_{DD33}	6V > VBAT > 3.1V	3.0	3.3	3.6	V
Regulator Output Voltage	V_{DD33}	USB UART Mode & *UART RegOutput[1:0]* = 01 6V > VBAT > 3.1V	2.7	3.0	3.3	V
Regulator Output Voltage	V_{DD33}	USB UART Mode & *UART RegOutput[1:0]* = 10 6V > VBAT > 3.1V	2.47	2.75	3.03	V
Regulator Output Voltage	V_{DD33}	USB UART Mode & *UART RegOutput[1:0]* = 11 6V > VBAT > 3.1V	2.25	2.5	2.75	V
Regulator Bypass Capacitor	C_{OUT}		2.2			uF
Bypass Capacitor ESR	C_{ESR}				1	Ω

TABLE 4-10: ESD AND LATCH-UP PERFORMANCE

Parameter	Conditions	MIN	TYP	MAX	Units	Comments
ESD PERFORMANCE						
Note 4-9	Human Body Model			±8	kV	Device
System	EN/IEC 61000-4-2 Contact Discharge			±8	kV	3rd party system test
System	EN/IEC 61000-4-2 Air-gap Discharge			±15	kV	3rd party system test
LATCH-UP PERFORMANCE						
All Pins	EIA/JESD 78, Class II		150		mA	

Note 4-9 **REFCLK**, **XO, SPK_L** and **SPK_R** pins: ±5kV Human Body Model.

4.10 Piezoelectric Resonator for Internal Oscillator

The internal oscillator may be used with an external quartz crystal or ceramic resonator as described in Section 5.4.1.2. See Table 4-11 for the recommended crystal specifications.

TABLE 4-11: USB3320 QUARTZ CRYSTAL SPECIFICATIONS

Parameter	Symbol	MIN	TYP	MAX	Units	Notes
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	Table 5-10	-	MHz	
Total Allowable PPM Budget		-	-	±500	PPM	Note 4-10
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	0.5	-	-	mW	
Equivalent Series Resistance	R_1	-	-	30	Ohm	
Operating Temperature Range		-40	-	+85	^oC	
USB3320 **REFCLK** Pin Capacitance		-	3 typ	-	pF	Note 4-11
USB3320 **XO** Pin Capacitance		-	3 typ	-	pF	Note 4-11

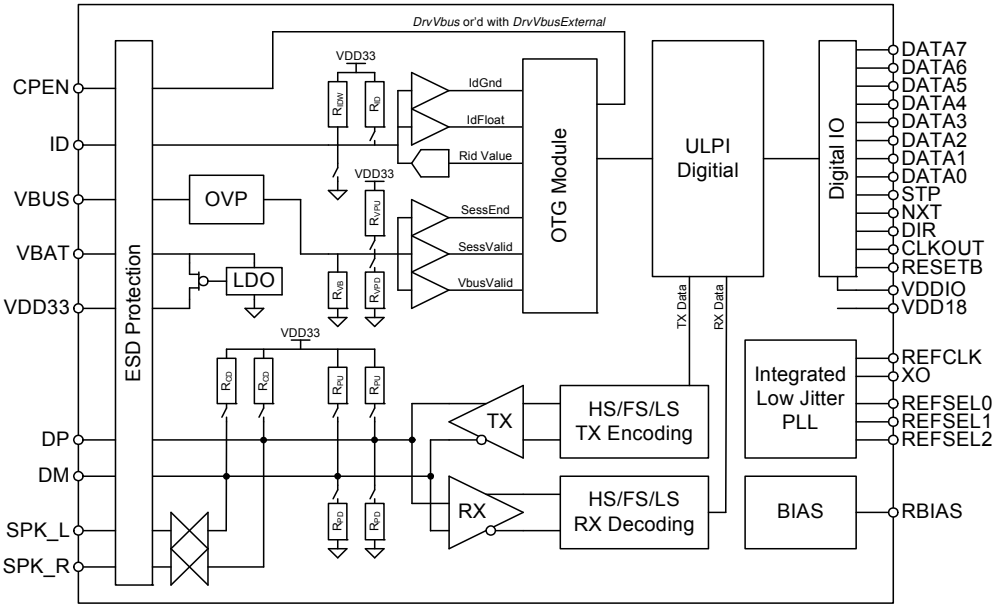
Note 4-10 The required bit rate accuracy for Hi-Speed USB applications is ±500 ppm as provided in the USB 2.0 Specification. This takes into account the effect of voltage, temperature, aging, etc.

Note 4-11 This number includes the pad, the bond wire and the lead frame. Printed Circuit Board (PCB) capacitance is not included in this value. The PCB capacitance value and the capacitance value of the **XO** and **REFCLK** pins are required to accurately calculate the value of the two external load capacitors.

5.0 ARCHITECTURE OVERVIEW

The USB3320 consists of the blocks shown in the diagram below. All pull-up resistors shown in this diagram are connected internally to the **VDD33** pin.

FIGURE 5-1: USB3320 INTERNAL BLOCK DIAGRAM



5.1 ULPI Digital Operation and Interface

This section of the USB3320 is covered in detail in Section 6.0, "ULPI Operation".

5.2 USB 2.0 Hi-Speed Transceiver

The blocks in the lower left-hand corner of Figure 5.1 interface to the DP/DM pins.

5.2.1 USB TRANSCEIVER

The USB3320 includes the receivers and transmitters that are compliant to the Universal Serial Bus Specification Rev 2.0. The DP/DM signals in the USB cable connect directly to the receivers and transmitters.

The RX block consists of a differential receiver for HS and separate receivers for FS/LS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX Logic block. For HS mode support, the HS RX block contains a squelch circuit to insure that noise is not interpreted as data. The RX block also includes a single-ended receiver on each of the data lines to determine the correct FS linestate.

Data from the TX Logic block is encoded, bit stuffed, serialized and transmitted onto the USB cable by the TX block. Separate differential FS/LS and HS transmitters are included to support all modes.

The USB3320 TX block meets the HS signaling level requirements in the USB 2.0 Specification when the PCB traces from the **DP** and **DM** pins to the USB connector have very little loss. In some systems, it may be desirable to compensate for loss by adjusting the HS transmitter amplitude. The *Boost* bits in the HS TX Boost register may be configured to adjust the HS transmitter amplitude at the **DP** and **DM** pins.

5.2.2 TERMINATION RESISTORS

The USB3320 transceiver fully integrates all of the USB termination resistors on both **DP** and **DM**. This includes 1.5kΩ pull-up resistors, 15kΩ pull-down resistors and the 45Ω high speed termination resistors. These resistors require no tuning or trimming by the Link. The state of the resistors is determined by the operating mode of the transceiver when operating in synchronous mode.

The *XcvrSelect[1:0]*, *TermSelect* and *OpMode[1:0]* bits in the Function Control register, and the *DpPulldown* and *DmPulldown* bits in the OTG Control register control the configuration. The possible valid resistor combinations are shown in Table 5-1, and operation is maintained in only the configurations shown. If a ULPI Register Setting is configured that does not match a setting in the table, the transceiver operation is not ensured and the settings in the last row of Table 5-1 will be used.

- RPU_DP_EN activates the 1.5kΩ DP pull-up resistor
- RPU_DM_EN activates the 1.5kΩ DM pull-up resistor
- RPD_DP_EN activates the 15kΩ DP pull-down resistor
- RPD_DM_EN activates the 15kΩ DM pull-down resistor
- HSTERM_EN activates the 45Ω DP and DM high speed termination resistors

The USB3320 also includes two **DP** and **DM** pull-up resistors described in Section 5.8.

TABLE 5-1: DP/DM TERMINATION VS. SIGNALING MODE

Signaling Mode	ULPI Register Settings					USB3320 Termination Resistor Settings				
	XCVRSELECT[1:0]	TERMSELECT	OPMODE[1:0]	DPPULLDOWN	DMPULLDOWN	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
General Settings										
Tri-State Drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or VBUS < $V_{SESSEND}$	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
Host Settings										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host Hi-Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host low Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Resume	10b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Test J/Test_K	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Peripheral Settings										
Peripheral Chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS	00b	0b	00b	0b	0b	0b	0b	0b	0b	1b
Peripheral FS	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral LS	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Suspend	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Resume	10b	1b	10b	0b	0b	0b	1b	0b	0b	0b

TABLE 5-1: DP/DM TERMINATION VS. SIGNALING MODE (CONTINUED)

Signaling Mode	ULPI Register Settings					USB3320 Termination Resistor Settings				
	XCVRSELECT[1:0]	TERMSELECT	OPMODE[1:0]	DPPULLDOWN	DMPULLDOWN	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
Peripheral Test J/Test K	00b	0b	10b	0b	0b	0b	0b	0b	0b	1b
OTG device, Peripheral Chirp	00b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS	00b	0b	00b	0b	1b	0b	0b	0b	1b	1b
OTG device, Peripheral FS	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Resume	01b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral Test J/Test K	00b	0b	10b	0b	1b	0b	0b	0b	1b	1b
Any combination not defined above Note 5-1						0b	0b	0b	0b	0b

Note 1: This is the same as Table 40, Section 4.4 of the ULPI 1.1 specification.

2: USB3320 does not support operation as an upstream hub port. See Section 6.2.4.3, "UTMI+ Level 3".

Note 5-1 The transceiver operation is not ensured in a combination that is not defined.

The USB3320 uses the 27% resistor ECN resistor tolerances. The resistor values are shown in Table 4-5.

5.3 Bias Generator

This block consists of an internal bandgap reference circuit used for generating the driver current and the biasing of the analog circuits. This block requires an external 8.06KΩ, 1% tolerance, reference resistor connected from **RBIAS** to ground. This resistor should be placed as close as possible to the USB3320 to minimize the trace length. The nominal voltage at **RBIAS** is 0.8V +/- 10% and therefore the resistor will dissipate approximately 80μW of power.

5.4 Integrated Low Jitter PLL

The USB3320 uses an integrated low jitter phase locked loop (PLL) to provide a clean 480MHz clock required for HS USB signal quality. This clock is used by the transceiver during both transmit and receive. The USB3320 PLL requires an accurate frequency reference to be driven on the **REFCLK** pin.

5.4.1 REFCLK MODE SELECTION

The USB3320 is designed to operate in one of two available modes as shown in Table 5-2. In the first mode, a 60MHz ULPI clock is driven on the **REFCLK** pin as described in Section 5.4.1.1. In the second mode, the USB3320 generates the ULPI clock as described in Section 5.4.1.2. When using the second mode, the frequency of the reference clock is configured by **REFSEL[2]**, **REFSEL[1]** and **REFSEL[0]** as described in Section 5.10.

TABLE 5-2: REFCLK MODES

Mode	REFCLK Frequency	ULPI Clock Description
ULPI Input Clock Mode	60Mhz	Sourced by Link, driven on the **REFCLK** pin
ULPI Output Clock Mode	Table 5-10	Sourced by **USB3320** at the **CLKOUT** pin

During start-up, the USB3320 monitors the **CLKOUT** pin to determine which mode has been configured as described in Section 5.4.1.1.

The system must not drive voltage on the **CLKOUT** pin following POR or hardware reset that exceeds the value of V_{IH_ED} provided in Table 4-4.

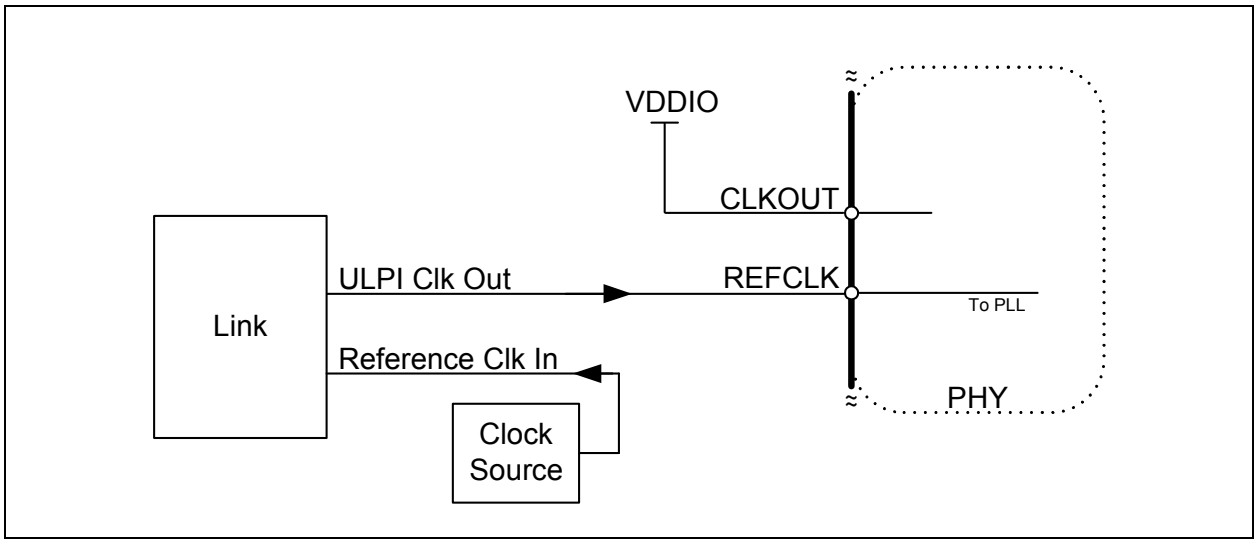
5.4.1.1 ULPI Input Clock Mode (60MHz REFCLK Mode)

When using ULPI Input Clock Mode, the Link must supply the 60MHz ULPI clock to the USB3320. As shown in Figure 5-2, the 60MHz ULPI Clock is connected to the **REFCLK** pin, and the **CLKOUT** pin is tied high to **VDDIO**. A simplified schematic using the ULPI Input Clock Mode is shown in Figure 8-2.

After the PLL has locked to the correct frequency, the USB3320 will de-assert **DIR** and the Link can begin using the ULPI interface. The USB3320 is ensured to start the clock within the time specified in Table 4-2. For Host applications, the ULPI *AutoResume* bit should be enabled. This is described in Section 6.2.4.4.

REFSEL[2], **REFSEL[1]** and **REFSEL[0]** should all be tied to VDDIO for ULPI Input Clock Mode.

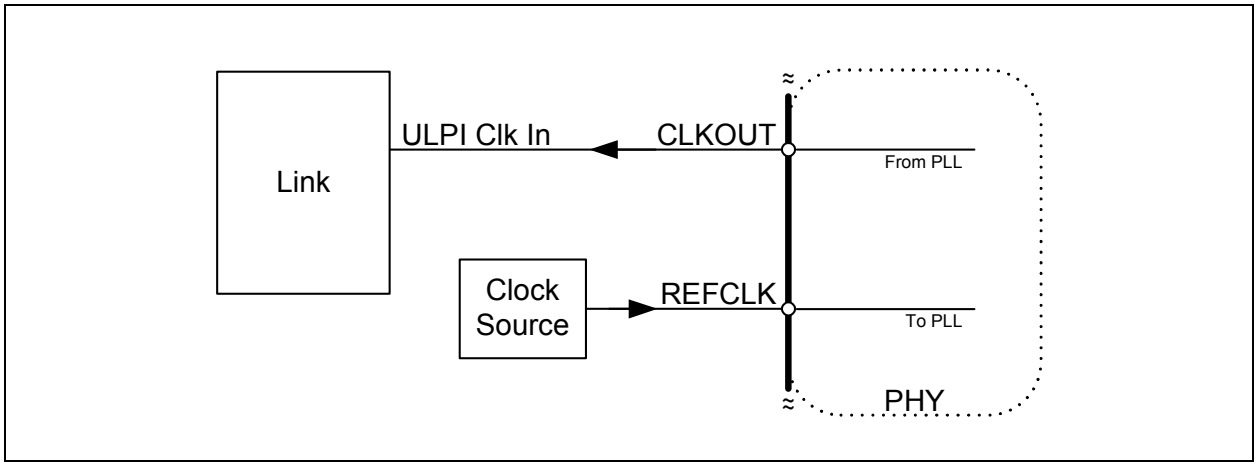
FIGURE 5-2: CONFIGURING THE USB332X FOR ULPI INPUT CLOCK MODE (60 MHZ)



5.4.1.2 ULPI Output Clock

When using ULPI Output Clock Mode, the USB3320 generates the 60MHz ULPI clock used by the Link. The frequency of the reference clock is configured by **REFSEL[2]**, **REFSEL[1]** and **REFSEL[0]** as described in Table 5-10. As shown in Figure 5-3, the **CLKOUT** pin sources the 60MHz ULPI clock to the Link.

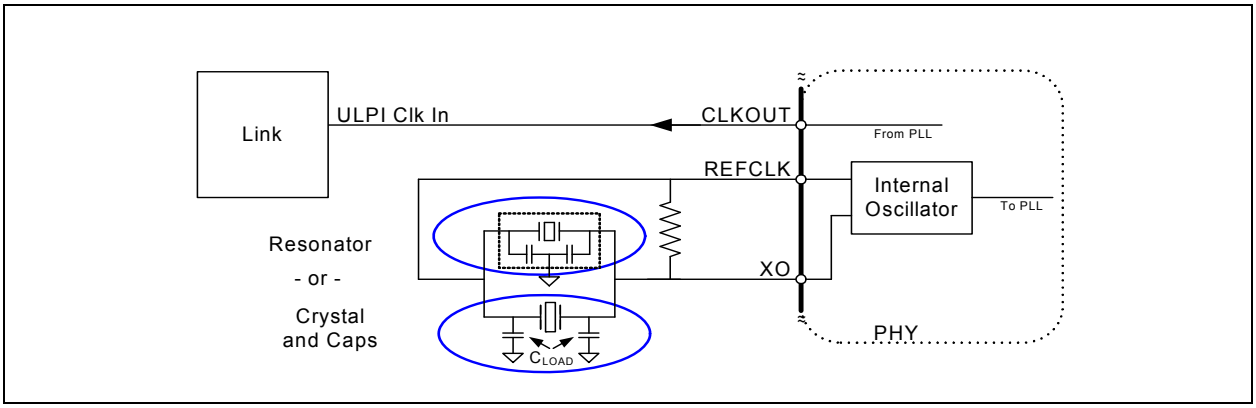
FIGURE 5-3: CONFIGURING THE USB332X FOR ULPI OUTPUT CLOCK MODE



In this mode, the **REFCLK** pin may be driven at the reference clock frequency. Alternatively, the internal oscillator may be used with an external crystal or resonator as shown in Figure 5-4.

An example of ULPI Output Clock Mode is shown in Figure 8-1.

FIGURE 5-4: ULPI OUTPUT CLOCK MODE



After the PLL has locked to the correct frequency, the USB3320 generates the 60MHz ULPI clock on the **CLKOUT** pin, and de-asserts **DIR** to indicate that the PLL is locked. The USB3320 is ensured to start the clock within the time specified in Table 4-2, and it will be accurate to within ±500ppm. For Host applications the ULPI *AutoResume* bit should be enabled. This is described in Section 6.2.4.4.

When using ULPI Output Clock Mode, the edges of the reference clock do not need to be aligned in any way to the ULPI interface signals; in other words, there is no need to align the phase of the **REFCLK** and the **CLKOUT**.

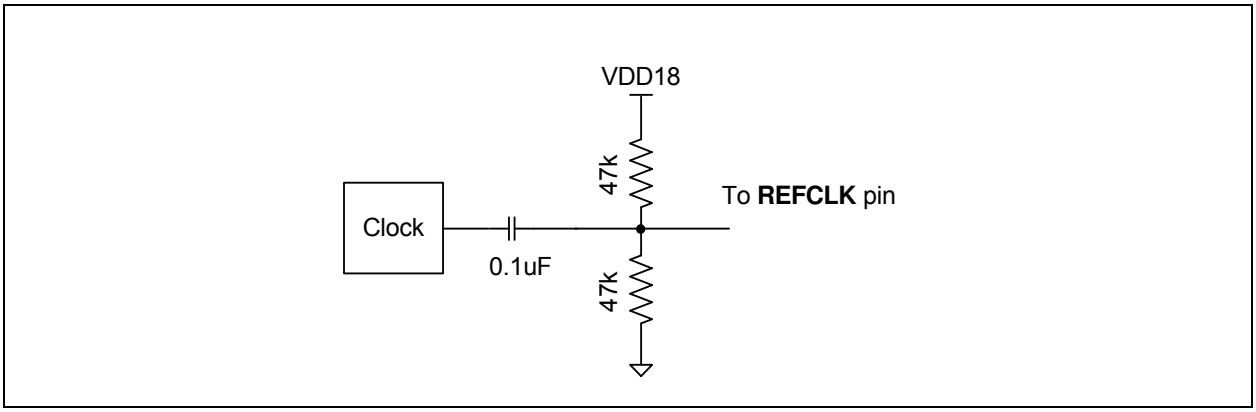
5.4.2 REFCLK AMPLITUDE

The reference clock is connected to the **REFCLK** pin as shown in the application diagrams, Figure 8-1, Figure 8-2 and Figure 8-3. The **REFCLK** pin is designed to be driven with a square wave from 0V to V_{DD18}, but can be driven with a square wave from 0V to as high as 3.6V. The USB3320 uses only the positive edge of the **REFCLK**.

If a digital reference is not available, the **REFCLK** pin can be driven by an analog sine wave that is AC coupled into the **REFCLK** pin. If using an analog clock, the DC bias should be set at the mid-point of the **VDD18** supply using a bias circuit as shown in Figure 5-5. The amplitude must be greater than 300mV peak to peak. The component values provided in Figure 5-5 are for example only. The actual values should be selected to satisfy system requirements.

The **REFCLK** amplitude must comply with the signal amplitudes shown in Table 4-4 and the duty cycle in Table 4-2.

FIGURE 5-5: EXAMPLE OF CIRCUIT USED TO SHIFT A REFERENCE CLOCK COMMON-MODE VOLTAGE LEVEL



5.4.3 REFCLK JITTER

The USB3320 is tolerant to jitter on the reference clock. The REFCLK jitter should be limited to a peak to peak jitter of less than 1nS over a 10uS time interval. If this level of jitter is exceeded when configured for either ULPI Input Clock Mode or ULPI Output Clock Mode, the USB3320 Hi-Speed eye diagram may be degraded.

The frequency accuracy of the REFCLK must meet the +/- 500ppm requirement as shown in Table 4-2.

5.4.4 REFCLK ENABLE/DISABLE

The **REFCLK** should be enabled when the **RESETB** pin is brought high. The ULPI interface will start running after the time specified in Table 4-2. If the REFCLK enable is delayed relative to the RESETB pin, the ULPI interface will start operation delayed by the same amount. The REFCLK can be run at anytime the **RESETB** pin is low without causing the USB3320 to start-up or draw current.

When the USB3320 is placed in Low Power Mode or Carkit Mode, the REFCLK can be stopped after the final ULPI register write is complete. The **STP** pin is asserted to bring the USB3320 out of Low Power Mode. The **REFCLK** should be started at the same time **STP** is asserted to minimize the USB3320 start-up time.

If the **REFCLK** is stopped while **CLKOUT** is running, the PLL will come out of lock and the frequency of the **CLKOUT** signal will decrease to the minimum allowed by the PLL design. If the **REFCLK** is stopped during a USB session, the session may drop.

5.5 Internal Regulators and POR

The USB3320 includes integrated power management functions, including a Low-Dropout regulator that can be used to generate the 3.3V USB supply, and a POR generator described in Section 5.5.2.

5.5.1 INTEGRATED LOW DROPOUT REGULATOR

The USB3320 has an integrated linear regulator. Power sourced at the **VBAT** pin is regulated to 3.3V and the regulator output is on the **VDD33** pin. To ensure stability, the regulator requires an external bypass capacitor ($C_{OUT)}$ as specified in Table 4-9 placed as close to the pin as possible.

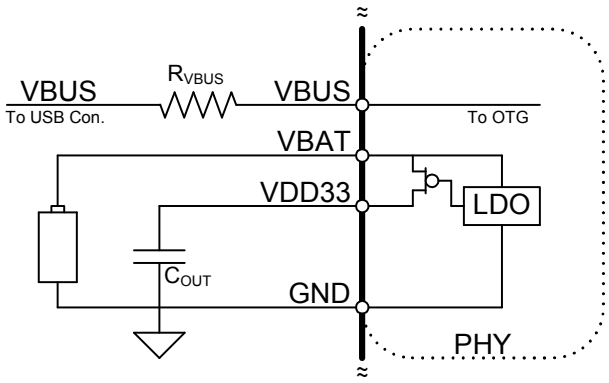
The USB3320 regulator is designed to generate a 3.3 volt supply for the USB3320 only. Using the regulator to provide current for other circuits is not recommended and Microchip does not support USB performance or regulator stability.

During USB UART mode the regulator output voltage can be changed to allow the USB3320 to work with UARTs operating at different operating voltages. The regulator output is configured to the voltages shown in Table 4-9 with the *UART RegOutput[1:0]* bits in the USB IO & Power Management register.

The USB3320 regulator can be powered in the three methods as shown below.

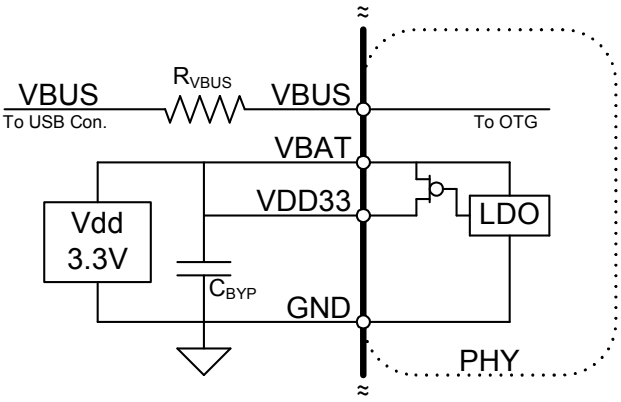
For USB Peripheral, Host, and OTG operations the regulator can be connected as shown in Figure 5-6 or Figure 5-7 below. For OTG operation, the **VDD33** supply on the USB3320 must be powered to detect devices attaching to the USB connector and detect a SRP during an OTG session. When using a battery to supply the USB3320, the battery voltage must be within the range of 3.1V to 5.5V.

FIGURE 5-6: POWERING THE USB3320 FROM A BATTERY



The USB3320 can be powered from an external 3.3V supply as shown below in Figure 5-7. When using the external supply, both the **VBAT** and **VDD33** pins are connected together. The bypass capacitor, C_{BYP}, is recommended when using the external supply.

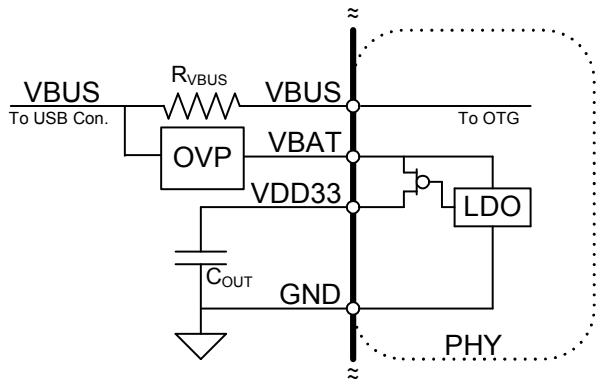
FIGURE 5-7: POWERING THE USB3320 FROM A 3.3V SUPPLY



For peripheral only or host only operation, the **VBAT** supply shown below in Figure 5-8 may be connected to the **VBUS** pin of the USB connector for bus powered applications. In this configuration, external overvoltage protection is required to protect the **VBAT** supply from any transient voltage present at the **VBUS** pin of the USB connector.

The **VBAT** input must never be exposed to a voltage that exceeds V_{VBAT}. (See Table 3-2)

FIGURE 5-8: POWERING THE USB3320 FROM VBUS



5.5.2 POWER ON RESET (POR)

The USB3320 provides a POR circuit that generates an internal reset pulse after the **VDD18** supply is stable. After the internal POR goes high and the **RESETB** pin is high, the USB3320 will release from reset and begin normal ULPI operation as described in Section 5.5.4.

The ULPI registers will power up in their default state summarized in Table 7-1 when the 1.8V supply is brought up. Cycling the 1.8 volt power supply will reset the ULPI registers to their default states. The **RESETB** pin can also be used to reset the ULPI registers to their default state (and reset all internal state machines) by bringing the pin low for a minimum of 1 microsecond and then high.

The Link is not required to assert the **RESETB** pin. A pull-down resistor is not present on the **RESETB** pin and therefore the Link must drive the **RESETB** pin to the desired state at all times (including system start-up) or connect the **RESETB** pin to **VDDIO.**

5.5.3 RECOMMENDED POWER SUPPLY SEQUENCE

For USB operation the USB3320 requires the **VBAT**, **VDD33**, **VDDIO** and **VDD18** supples. **VBAT**, **VDD33**, and **VDD18** can be applied in any order. The **VDD18** supply must be turned on and stable before the **VDDIO** supply is applied. This does not apply in cases where the **VDD18** and **VDDIO** supply pins are tied together.

When the **VBAT** supply is applied, the integrated regulator will automatically start-up and regulate **VBAT** to **VDD33**. If the **VDD33** supply is powered and the **VDD18** supply is not powered, the 3.3V circuits are powered off and the **VDD33** current will be limited as shown in Table 4-1.

The ULPI interface will start operating after the **VDD18** and **VDDIO** supplies are applied and the **RESETB** pin is brought high. The **RESETB** pin must be held low until the **VDD18** and **VDDIO** supplies are stable. If the Link is not ready to interface the USB3320, the Link may choose to hold the **RESETB** pin low until it is ready to control the ULPI interface.

TABLE 5-3: OPERATING MODE VS. POWER SUPPLY CONFIGURATION

VDD33	VDD18	RESETB	Operating Modes Available
0	0	0	Powered Off
0	1	0	RESET Mode.
0	1	1	In this configuration the ULPI interface is available and can be programed into all operating modes described in Section 6.0, "ULPI Operation". All USB signals will read 0.
1	0	X	In this mode the ULPI interface is not active and the circuits powered from the **VDD33** supply are turned off and the current will be limited to the RESET Mode current. (Note 5-2)

TABLE 5-3: OPERATING MODE VS. POWER SUPPLY CONFIGURATION (CONTINUED)

VDD33	VDD18	RESETB	Operating Modes Available
1	1	0	RESET Mode
1	1	1	Full USB operation as described in Section 6.0, "ULPI Operation".

Note: Anytime **VBAT** is powered per Table 3-2, the **VDD33** pin will be powered up.

Note 5-2 **VDDIO** must be powered to tri-state the ULPI interface in this configuration.

5.5.4 START-UP

The power on default state of the USB3320 is ULPI Synchronous mode. The USB3320 requires the following conditions to begin operation: the power supplies must be stable, the **REFCLK** must be present and the **RESETB** pin must be high. After these conditions are met, the USB3320 will begin ULPI operation that is described in Section 6.0, "ULPI Operation".

Figure 5-9 below shows a timing diagram to illustrate the start-up of the USB3320. At T0, the supplies are stable and the USB3320 is held in reset mode. At T1, the Link drives **RESETB** high after the **REFCLK** has started. The **RESETB** pin may be brought high asynchronously to **REFCLK**. At this point the USB3320 will drive idle on the data bus and assert **DIR** until the internal PLL has locked. After the PLL has locked, the USB3320 will check that the Link has de-asserted **STP** and at T2 it will de-assert **DIR** and begin ULPI operation.

The ULPI bus will be available as shown in Figure 5-9 in the time defined as T_{START} given in Table 4-2. If the **REFCLK** signal starts after the **RESETB** pin is brought high, then time T0 will begin when **REFCLK** starts. T_{START} also assumes that the Link has de-asserted **STP**. If the Link has held **STP** high the USB3320 will hold **DIR** high until **STP** is de-asserted. When the LINK de-asserts STP, it must drive a ULPI IDLE one cycle after **DIR** de-asserts.

FIGURE 5-9: ULPI START-UP TIMING